

QL3025 pASIC 3 FPGA Data Sheet



- 25,000 Usable PLD Gate pASIC 3 FPGA Combining High Performance and High Density

Device Highlights

High Performance & High Density

- 25,000 Usable PLD Gates with 204 I/Os
- 300 MHz, 16-bit Counters, 400 MHz Datapaths
- 0.35 μm four-layer metal non-volatile CMOS process for smallest die sizes

Easy to Use / Fast Development Cycles

- 100% routable with 100% utilization and complete pin-out stability
- Variable-grain logic cells provide high performance and 100% utilization
- Comprehensive design tools include high quality Verilog/VHDL synthesis

Advanced I/O Capabilities

- Interfaces with both 3.3 V and 5.0 V devices
- PCI compliant with 3.3 V and 5.0 V buses for -1/-2/-3/-4 speed grades
- Full JTAG boundary scan
- I/O Cells with individually controlled Registered Input Path and Output Enables

Total of 204 I/O Pins

- 196 bidirectional input/output pins, PCI-compliant for 5.0 V and 3.3 V buses for -1/-2/-3/-4 speed grades
- Four High Drive input-only pins
- Four High Drive input-only/distributed network pins

Four Low-Skew Distributed Networks

- Two array clock/control networks available to the logic cell flip-flop clock, set and reset inputs — each driven by an input-only pin
- Two global clock/control networks available to the logic cell; F1, clock set, reset inputs and the input, I/O register clock, reset, and enable inputs as well as the output enable control — each driven by an input-only or I/O pin, or any logic cell output or I/O cell feedback

High Performance

- Input + logic cell + output total delays under 6 ns
- Data path speeds over 400 MHz
- Counter speeds over 300 MHz

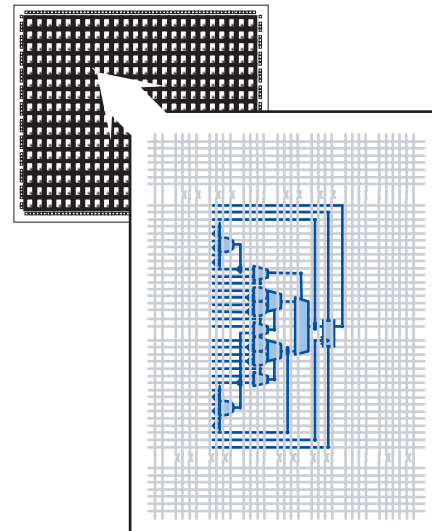


Figure 1: 672 pASIC 3 Logic Cells

Architecture Overview

The QL3025 is a 25,000 usable PLD gate member of the pASIC 3 family of FPGAs. pASIC 3 FPGAs are fabricated on a 0.35 μm four-layer metal process using QuickLogic[®]'s patented ViaLink[®] technology to provide a unique combination of high performance, high density, low cost, and extreme ease-of-use.

The QL3025 contains 672 logic cells. With a maximum of 204 I/Os, the QL3025 is available in 144-pin TQFP, 208-pin PQFP, and 256-pin PBGA packages.

Software support for the complete pASIC 3 family, including the QL3025, is available through three basic packages. The turnkey QuickWorks[®] package provides the most complete FPGA software solution from design entry to logic synthesis, to place and route, to simulation. The QuickTools[™] for Workstations package provides a solution for designers who use Cadence[®], Exemplar[™], Mentor[®], Synopsys[®], Synplicity[®], Viewlogic[™], Aldec[™],

www.DataSheet4U.com or other third-party tools for design entry, synthesis, or simulation.

Electrical Specifications

AC Characteristics at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$ ($K = 1.00$)

To calculate delays, multiply the appropriate K factor from **Table 7** by the numbers provided in **Table 1** through **Table 5**.

Table 1: Logic Cells

Symbol	Parameter	Propagation Delays (ns) Fanout ^a				
		1	2	3	4	8
t_{PD}	Combinatorial Delay ^b	1.4	1.7	1.9	2.2	3.2
t_{SU}	Setup Time ^b	1.7	1.7	1.7	1.7	1.7
t_H	Hold Time	0.0	0.0	0.0	0.0	0.0
t_{CLK}	Clock to Q Delay	0.7	1.0	1.2	1.5	2.5
t_{CWHI}	Clock High Time	1.2	1.2	1.2	1.2	1.2
t_{CWLO}	Clock Low Time	1.2	1.2	1.2	1.2	1.2
t_{SET}	Set Delay	1.0	1.3	1.5	1.8	2.8
t_{RESET}	Reset Delay	0.8	1.1	1.3	1.6	2.6
t_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9
t_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8

- a. Stated timing for worst case Propagation Delay over process variation at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$. Multiply by the appropriate Delay Factor, K, for speed grade, voltage, and temperature settings as specified in **Table 7**.
- b. These limits are derived from a representative selection of the slowest paths through the pASIC 3 logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

Table 2: Input-Only/Clock Cells

Symbol	Parameter	Propagation Delays (ns) Fanout ^a						
		1	2	3	4	8	12	24
t_{IN}	High Drive Input Delay	1.5	1.6	1.8	1.9	2.4	2.9	4.4
t_{INI}	High Drive Input, Inverting Delay	1.6	1.7	1.9	2.0	2.5	3.0	4.5
t_{ISU}	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0
t_{ICLK}	Input Register Clock To Q	0.7	0.8	1.0	1.1	1.6	2.1	3.6
t_{IRST}	Input Register Reset Delay	0.6	0.7	0.9	1.0	1.5	2.0	3.5
t_{ESU}	Input Register clock Enable Set-Up Time	2.3	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0

- a. Stated timing for worst case Propagation Delay over process variation at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$. Multiply by the appropriate Delay Factor, K, for speed grade, voltage, and temperature settings as specified in **Table 7**.

Table 3: Clock Cells

Symbol	Parameter	Propagation Delays (ns) Loads per Half Column ^a						
		1	2	3	4	8	10	11
t _{ACK}	Array Clock Delay	1.2	1.2	1.3	1.3	1.5	1.6	1.7
t _{GCKP}	Global Clock Pin Delay	0.7	0.7	0.7	0.7	0.7	0.7	0.7
t _{GCKB}	Global Clock Buffer Delay	0.8	0.8	0.9	0.9	1.1	1.2	1.3

a. The array distributed networks consist of 40 half columns and the global distributed networks consist of 44 half columns, each driven by an independent buffer. The number of half columns used does not affect clock buffer delay. The array clock has up to eight loads per half column. The global clock has up to 11 loads per half column.

www.DataSheet4U.com

Table 4: Input-Only I/O Cells

Symbol	Parameter	Propagation Delays (ns) Fanout ^a					
		1	2	3	4	8	10
t _{I/O}	Input Delay (bidirectional pad)	1.3	1.6	1.8	2.1	3.1	3.6
t _{ISU}	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1
t _{IH}	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0
t _{IOCLK}	Input Register Clock To Q	0.7	1.0	1.2	1.5	2.5	3.0
t _{IORST}	Input Register Reset Delay	0.6	0.9	1.1	1.4	2.4	2.9
t _{IESU}	Input Register clock Enable Set-Up Time	2.3	2.3	2.3	2.3	2.3	2.3
t _{IEH}	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage, and temperature settings as specified in **Table 7**.

Table 5: Output-Only I/O Cells

Symbol	Parameter	Propagation Delays (ns) Output Load Capacitance (pF)				
		30	50	75	100	150
t_{OUTLH}	Output Delay Low to High	2.1	2.5	3.1	3.6	4.7
t_{OUTHl}	Output Delay High to Low	2.2	2.6	3.2	3.7	4.8
t_{PZH}	Output Delay Tri-state to High	1.2	1.7	2.2	2.8	3.9
t_{PZL}	Output Delay Tri-state to Low	1.6	2.0	2.6	3.1	4.2
t_{PHZ}	Output Delay High to Tri-State ^a	2.0	-	-	-	-
t_{PLZ}	Output Delay Low to Tri-State	1.2	-	-	-	-

www.DataSheet4U.com

a. The following loads presented in **Figure 2** are used for t_{PXZ} :

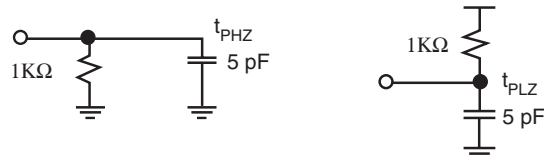


Figure 2: Loads used for t_{PXZ}

DC Characteristics

The DC specifications are provided in **Table 6** through **Table 8**.

Table 6: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
V _{CC} Voltage	-0.5 V to 4.6 V	DC Input Current	±20 mA
V _{CCIO} Voltage	-0.5 V to 7.0 V	ESD Pad Protection	±2000 V
Input Voltage	-0.5 V to V _{CCIO} +0.5 V	Storage Temperature	-65°C to +150°C
Latch-up Immunity	±200 mA	Lead Temperature	300°C

Table 7: Operating Range

www.DataSheet4U.com

Symbol	Parameter	Military		Industrial		Commercial		Unit	
		Min	Max	Min	Max	Min	Max		
V _{CC}	Supply Voltage	3.0	3.6	3.0	3.6	3.0	3.6	V	
V _{CCIO}	I/O Input Tolerance Voltage	3.0	5.5	3.0	5.5	3.0	5.25	V	
TA	Ambient Temperature	-55	-	-40	85	0	70	°C	
TC	Case Temperature	-	125	-	-	-	-	°C	
K	Delay Factor	-0 Speed Grade	-	-	0.43	1.90	0.46	1.85	n/a
		-1 Speed Grade	0.42	1.64	0.43	1.54	0.46	1.50	n/a
		-2 Speed Grade	0.42	1.37	0.43	1.28	0.46	1.25	n/a
		-3 Speed Grade			0.43	0.90	0.46	0.88	n/a
		-4 Speed Grade			0.43	0.82	0.46	0.80	n/a

Table 8: DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	Input HIGH Voltage		$0.5 V_{CC}$	$V_{CCIO} + 0.5$	V
V_{IL}	Input LOW Voltage		-0.5	$0.3 V_{CC}$	V
V_{OH}	Output HIGH Voltage	$I_{OH} = -12 \text{ mA}$	2.4		V
		$I_{OH} = -500 \mu\text{A}$	$0.9 V_{CC}$		V
V_{OL}	Output LOW Voltage	$I_{OL} = 16 \text{ mA}^a$		0.45	V
		$I_{OL} = 1.5 \text{ mA}$		$0.1 V_{CC}$	V
I_I	I or I/O Input Leakage Current	$V_I = V_{CCIO}$ or GND	-10	10	μA
I_{OZ}	3-State Output Leakage Current	$V_I = V_{CCIO}$ or GND	-10	10	μA
C_I	Input Capacitance ^b			10	pF
I_{OS}	Output Short Circuit Current ^c	$V_O = \text{GND}$	-15	-180	mA
		$V_O = V_{CC}$	40	210	mA
I_{CC}	D.C. Supply Current ^d	$V_I, V_{IO} = V_{CCIO}$ or GND	0.50 (typ)	2	mA
I_{CCIO}	D.C. Supply Current on V_{CCIO}		0	100	μA

- a. Applies only to -1/-2/-3/-4 commercial grade devices. These speed grades are also PCI-compliant. All other devices have 8 mA IOL specifications.
- b. Capacitance is sample tested only. Clock pins are 12 pF maximum.
- c. Only one output at a time. Duration should not exceed 30 seconds.
- d. For -1/-2/-3/-4 commercial grade devices only. Maximum I_{CC} is 3 mA for -0 commercial grade and all industrial grade devices, and 5 mA for all military grade devices. For AC conditions, contact QuickLogic customer applications group. (See [Contact Information](#)).

Kv and Kt Graphs

www.DataSheet4U.com

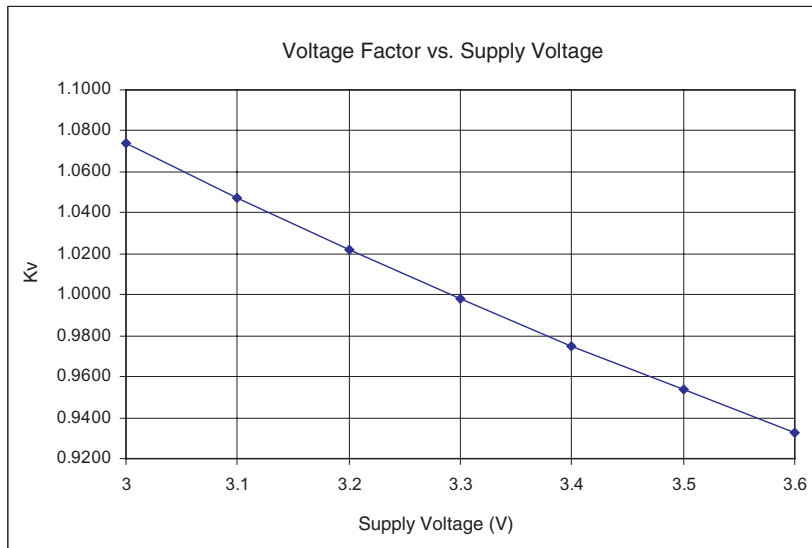


Figure 3: Voltage Factor vs. Supply Voltage

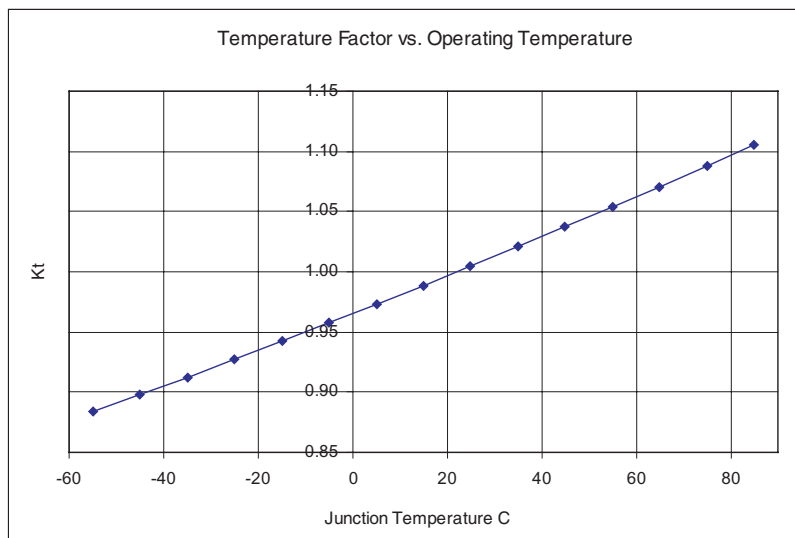
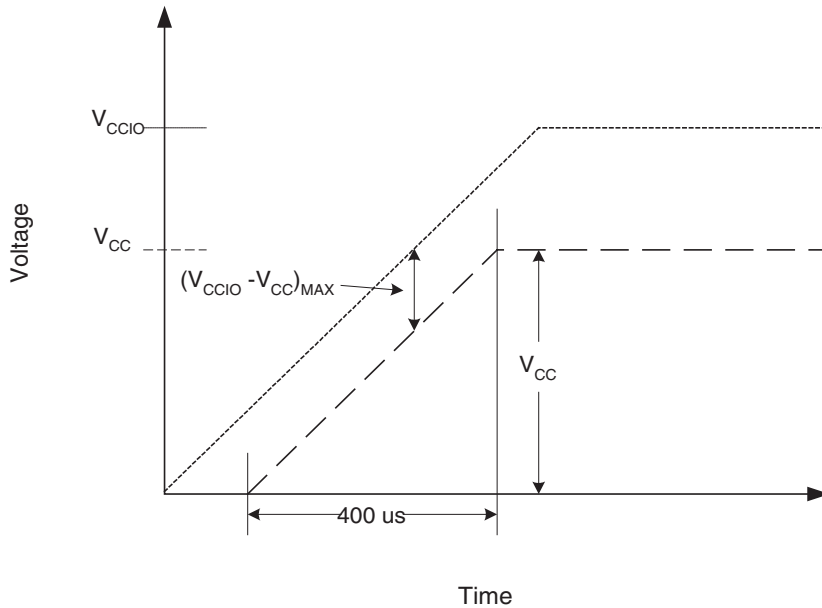


Figure 4: Temperature Factor vs. Operating Temperature

Power-up Sequencing



www.DataSheet4U.com

Figure 5: Power-up Requirements

The following requirements must be met when powering up the device (refer to **Figure 5**):

- When ramping up the power supplies keep $(V_{CCIO} - V_{CC})_{MAX} \leq 500$ mV. Deviation from this recommendation can cause permanent damage to the device.
- V_{CCIO} must lead V_{CC} when ramping the device.
- The power supply must take greater than or equal to 400 μ s to reach V_{CC} . Ramping to V_{CC}/V_{CCIO} earlier than 400 μ s can cause the device to behave improperly.

An internal diode is present in-between V_{CC} and V_{CCIO} , as shown in **Figure 6**.

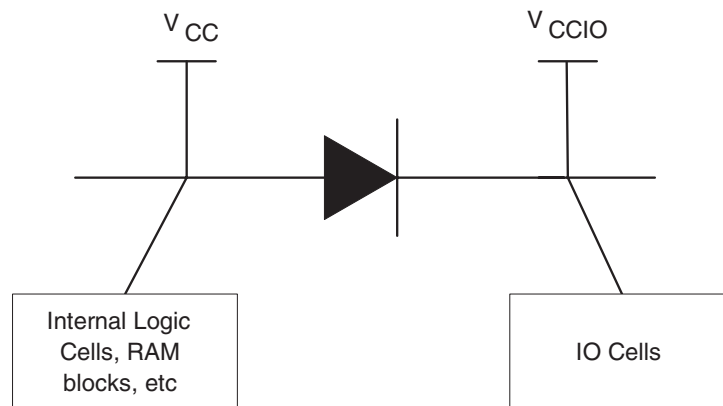
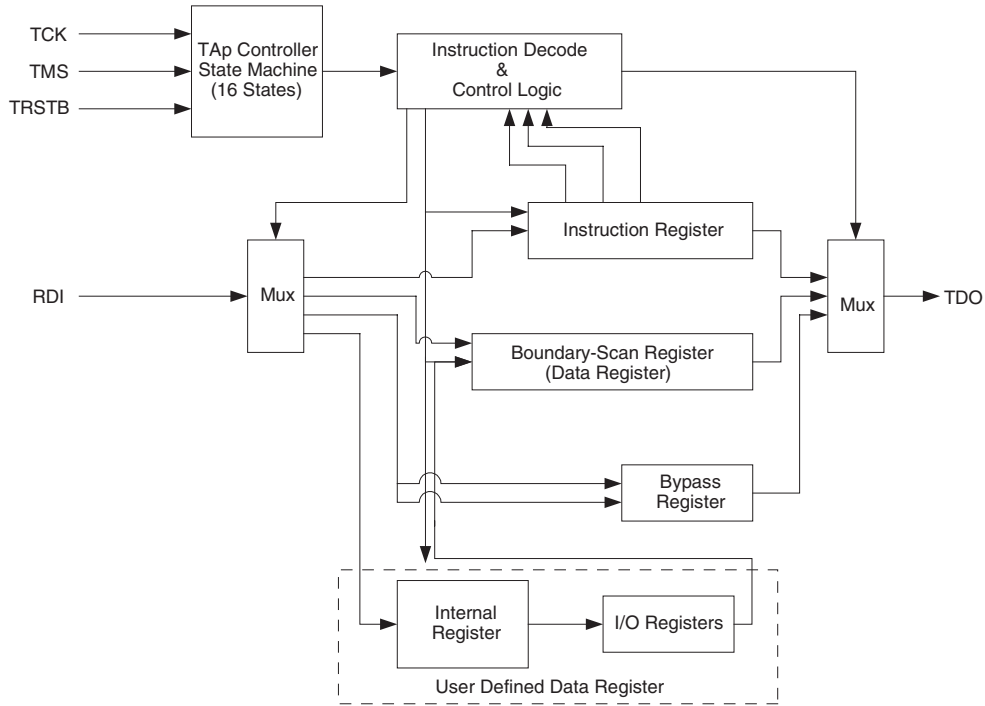


Figure 6: Internal Diode Between V_{CC} and V_{CCIO}

JTAG



www.DataSheet4U.com

Figure 7: JTAG Block Diagram

Microprocessors and Application Specific Integrated Circuits (ASICs) pose many design challenges, not the least of which concerns the accessibility of test points. The Joint Test Access Group (JTAG) formed in response to this challenge, resulting in IEEE standard 1149.1, the Standard Test Access Port and Boundary Scan Architecture.

The JTAG boundary scan test methodology allows complete observation and control of the boundary pins of a JTAG-compatible device through JTAG software. A Test Access Port (TAP) controller works in concert with the Instruction Register (IR); these allow users to run three required tests, along with several user-defined tests.

JTAG tests allow users to reduce system debug time, reuse test platforms and tools, and reuse subsystem tests for fuller verification of higher level system elements.

The 1149.1 standard requires the following three tests:

- **Extest Instruction.** The Extest instruction performs a PCB interconnect test. This test places a device into an external boundary test mode, selecting the boundary scan register to be connected between the TAP's Test Data In (TDI) and Test Data Out (TDO) pins. Boundary scan cells are preloaded with test patterns (via the Sample/Preload Instruction), and input boundary cells capture the input data for analysis.
- **Sample/Preload Instruction.** This instruction allows a device to remain in its functional mode, while selecting the boundary scan register to be connected between the TDI and TDO pins. For this test, the boundary scan register can be accessed via a data scan operation, allowing users to sample the functional data entering and leaving the device.
- **Bypass Instruction.** The Bypass instruction allows data to skip a device's boundary scan entirely, so the data passes through the bypass register. The Bypass instruction allows users to test a device without passing through other devices. The bypass register is connected between the TDI and TDO pins, allowing serial data to be transferred through a device without affecting the operation of the device.

www.DataSheet4U.com

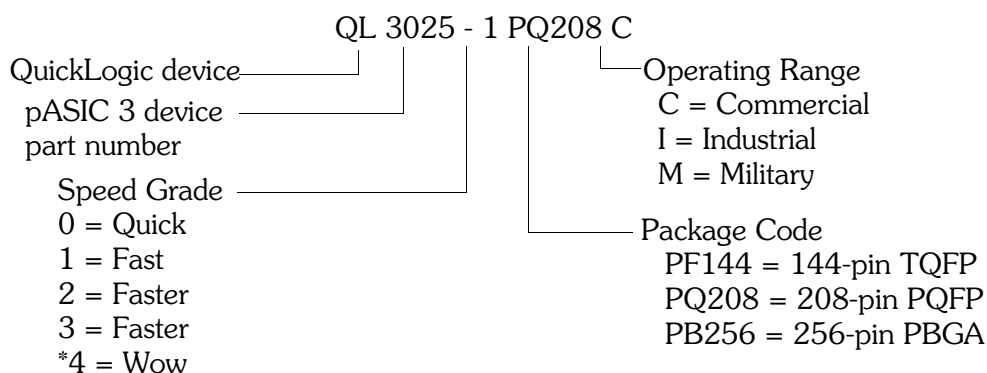
Pin Descriptions

Table 9: Pin Descriptions

Pin	Function	Description
TDI	Test Data In for JTAG	Hold HIGH during normal operation. Connect to V _{CC} if not used for JTAG.
TRSTB	Active low Reset for JTAG	Hold LOW during normal operation. Connect to ground if not used for JTAG.
TMS	Test Mode Select for JTAG	Hold HIGH during normal operation. Connect to V _{CC} if not used for JTAG.
TCK	Test Clock for JTAG	Hold HIGH or LOW during normal operation. Connect to V _{CC} or ground if not used for JTAG.
TDO	Test data out for JTAG	Output that must be left unconnected if not used for JTAG.
STM	Special Test Mode	Must be grounded during normal operation.
I/ACLK	High-drive input and/or array network driver	Can be configured as either or both.
I/GCLK	High-drive input and/or global network driver	Can be configured as either or both.
I	High-drive input	Use for input signals with high fanout.
I/O	Input/Output pin	Can be configured as an input and/or output.
V _{CC}	Power supply pin	Connect to 3.3 V supply.
V _{CCIO}	Input voltage tolerance pin	Connect to 5.0 V supply if 5 V input tolerance is required, otherwise connect to 3.3 V supply.
GND	Ground pin	Connect to ground.

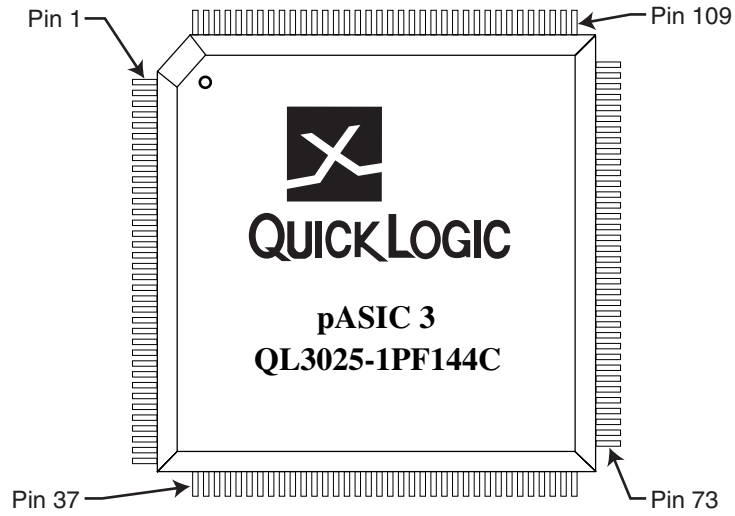
www.DataSheet4U.com

Ordering Information



* Contact QuickLogic regarding availability. (See [Contact Information](#))

144 TQFP Pinout Diagram



www.DataSheet4U.com

Figure 8: Top View of 144 Pin TQFP

208 PQFP Pinout Diagram

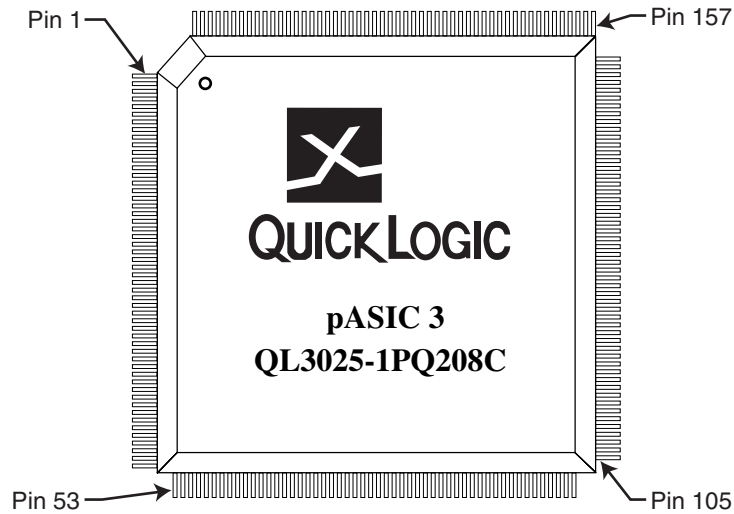


Figure 9: Top View of 208 Pin PQFP

144 TQFP & 208 PQFP Pinout Table

Table 10: 144 TQFP & 208 PQFP Pinout Table

208 PQFP	144 TQFP	Function	208 PQFP	144 TQFP	Function	208 PQFP	144 TQFP	Function	208 PQFP	144 TQFP	Function	208 PQFP	144 TQFP	Function
1	NC	I/O	43	30	GND	85	60	I/O	127	87	GND	169	117	I/O
2	1	I/O	44	31	I/O	86	61	I/O	128	88	I/O	170	118	I/O
3	2	I/O	45	NC	I/O	87	NC	I/O	129	89	I	171	119	I/O
4	3	I/O	46	32	I/O	88	62	I/O	130	90	ACLK / I	172	120	I/O
5	NC	I/O	47	NC	I/O	89	63	I/O	131	91	V _{CC}	173	NC	I/O
6	4	I/O	48	33	I/O	90	NC	I/O	132	92	I	174	NC	I/O
7	5	I/O	49	NC	I/O	91	NC	I/O	133	93	GCLK / I	175	121	I/O
8	NC	I/O	50	34	I/O	92	64	I/O	134	94	V _{CC}	176	NC	I/O
9	6	I/O	51	35	I/O	93	NC	I/O	135	95	I/O	177	122	GND
10	7	V _{CC}	52	36	I/O	94	65	I/O	136	NC	I/O	178	123	I/O
11	NC	I/O	53	37	I/O	95	66	GND	137	96	I/O	179	124	I/O
12	NC	GND	54	38	TDI	96	67	I/O	138	NC	I/O	180	NC	I/O
13	8	I/O	55	39	I/O	97	NC	V _{CC}	139	97	I/O	181	125	I/O
14	NC	I/O	56	NC	I/O	98	NC	I/O	140	98	I/O	182	126	GND
15	9	I/O	57	40	I/O	99	68	I/O	141	NC	I/O	183	127	I/O
16	NC	I/O	58	NC	I/O	100	69	I/O	142	99	I/O	184	128	I/O
17	10	I/O	59	NC	GND	101	NC	I/O	143	NC	I/O	185	129	I/O
18	11	I/O	60	41	I/O	102	70	I/O	144	100	I/O	186	NC	I/O
19	12	I/O	61	42	V _{CC}	103	71	TRSTB	145	NC	V _{CC}	187	130	V _{CCIO}
20	13	I/O	62	43	I/O	104	72	TMS	146	101	I/O	188	131	I/O
21	NC	I/O	63	NC	I/O	105	NC	I/O	147	102	GND	189	132	I/O
22	14	I/O	64	44	I/O	106	73	I/O	148	103	I/O	190	NC	I/O
23	15	GND	65	45	I/O	107	NC	I/O	149	104	I/O	191	133	I/O
24	16	I/O	66	NC	I/O	108	74	I/O	150	NC	I/O	192	134	I/O
25	17	I	67	46	I/O	109	75	I/O	151	105	I/O	193	NC	I/O
26	18	ACLK / I	68	47	I/O	110	76	I/O	152	106	I/O	194	135	I/O
27	19	V _{CC}	69	48	I/O	111	77	I/O	153	NC	I/O	195	136	I/O
28	20	I	70	NC	I/O	112	NC	I/O	154	107	I/O	196	NC	I/O
29	21	GCLK / I	71	49	I/O	113	78	I/O	155	NC	I/O	197	137	I/O
30	22	V _{CC}	72	NC	I/O	114	79	V _{CC}	156	108	I/O	198	NC	I/O
31	23	I/O	73	50	GND	115	80	I/O	157	109	TCK	199	138	GND
32	NC	I/O	74	51	I/O	116	NC	GND	158	110	STM	200	139	I/O
33	24	I/O	75	52	I/O	117	81	I/O	159	111	I/O	201	NC	V _{CC}
34	NC	I/O	76	NC	I/O	118	82	I/O	160	NC	I/O	202	140	I/O
35	25	I/O	77	53	I/O	119	NC	I/O	161	112	I/O	203	NC	I/O
36	NC	I/O	78	54	GND	120	83	I/O	162	113	I/O	204	141	I/O
37	26	I/O	79	55	I/O	121	NC	I/O	163	NC	GND	205	142	I/O
38	27	I/O	80	56	I/O	122	84	I/O	164	NC	I/O	206	NC	I/O
39	28	I/O	81	NC	I/O	123	85	I/O	165	114	V _{CC}	207	143	TDO
40	NC	I/O	82	57	I/O	124	NC	I/O	166	115	I/O	208	144	I/O
41	NC	V _{CC}	83	58	V _{CCIO}	125	86	I/O	167	116	I/O			
42	29	I/O	84	59	I/O	126	NC	I/O	168	NC	I/O			

256 PBGA Pinout Diagram

www.DataSheet4U.com

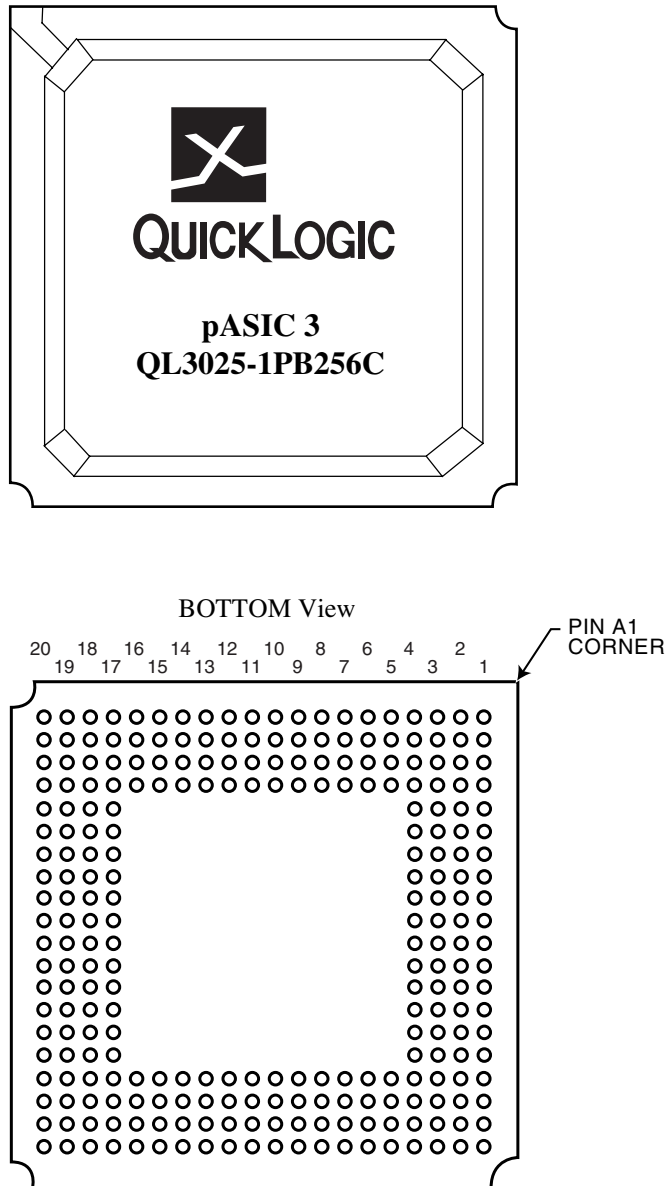


Figure 10: 256-Pin PBGA Pinout Diagram

256 PBGA Pinout Table

Table 11: 256 PBGA Pinout Table

256 PBGA	Function	256	Function	256	Function	256	Function	256	Function	256	Function
A1	VSS	C4	I/O	E19	I/O	L2	ACLK / I	T17	I/O	V20	I/O
A2	I/O	C5	I/O	E20	I/O	L3	I	T18	I/O	W1	I/O
A3	I/O	C6	I/O	F1	I/O	L4	GCLK / I	T19	NC	W2	I/O
A4	I/O	C7	I/O	F2	I/O	L17	V _{CC}	T20	I/O	W3	TDI
A5	I/O	C8	I/O	F3	I/O	L18	I/O	U1	I/O	W4	I/O
A6	I/O	C9	V _{CCIO}	F4	V _{CC}	L19	I/O	U2	I/O	W5	I/O
A7	I/O	C10	I/O	F17	V _{CC}	L20	I/O	U3	I/O	W6	I/O
A8	I/O	C11	I/O	F18	NC	M1	I/O	U4	VSS	W7	I/O
A9	I/O	C12	I/O	F19	I/O	M2	I/O	U5	I/O	W8	I/O
A10	I/O	C13	I/O	F20	I/O	M3	I/O	U6	V _{CC}	W9	I/O
A11	I/O	C14	I/O	G1	I/O	M4	NC	U7	I/O	W10	I/O
A12	I/O	C15	I/O	G2	NC	M17	NC	U8	VSS	W11	I/O
A13	I/O	C16	I/O	G3	I/O	M18	I/O	U9	I/O	W12	I/O
A14	I/O	C17	I/O	G4	I/O	M19	I/O	U10	V _{CC}	W13	I/O
A15	I/O	C18	I/O	G17	I/O	M20	I/O	U11	I/O	W14	I/O
A16	I/O	C19	I/O	G18	I/O	N1	I/O	U12	I/O	W15	I/O
A17	I/O	C20	I/O	G19	NC	N2	I/O	U13	VSS	W16	I/O
A18	I/O	D1	I/O	G20	I/O	N3	I/O	U14	I/O	W17	I/O
A19	TCK	D2	I/O	H1	I/O	N4	VSS	U15	V _{CC}	W18	I/O
A20	I/O	D3	I/O	H2	I/O	N17	VSS	U16	I/O	W19	I/O
B1	TDO	D4	VSS	H3	I/O	N18	I/O	U17	VSS	W20	TRSTB
B2	I/O	D5	I/O	H4	VSS	N19	I/O	U18	I/O	Y1	I/O
B3	I/O	D6	V _{CC}	H17	VSS	N20	I/O	U19	I/O	Y2	NC
B4	I/O	D7	I/O	H18	I/O	P1	I/O	U20	I/O	Y3	I/O
B5	I/O	D8	VSS	H19	I/O	P2	I/O	V1	I/O	Y4	I/O
B6	I/O	D9	I/O	H20	I/O	P3	I/O	V2	NC	Y5	I/O
B7	I/O	D10	I/O	J1	I/O	P4	I/O	V3	I/O	Y6	I/O
B8	I/O	D11	V _{CC}	J2	I/O	P17	I/O	V4	I/O	Y7	I/O
B9	I/O	D12	I/O	J3	NC	P18	I/O	V5	I/O	Y8	I/O
B10	I/O	D13	VSS	J4	I/O	P19	NC	V6	I/O	Y9	I/O
B11	I/O	D14	I/O	J17	NC	P20	I/O	V7	I/O	Y10	I/O
B12	I/O	D15	V _{CC}	J18	I/O	R1	NC	V8	I/O	Y11	I/O
B13	I/O	D16	I/O	J19	I/O	R2	I/O	V9	I/O	Y12	I/O
B14	I/O	D17	VSS	J20	GCLK / I	R3	I/O	V10	I/O	Y13	I/O
B15	I/O	D18	I/O	K1	I/O	R4	V _{CC}	V11	I/O	Y14	I/O
B16	I/O	D19	I/O	K2	I/O	R17	V _{CC}	V12	V _{CCIO}	Y15	I/O
B17	NC	D20	I/O	K3	I/O	R18	I/O	V13	I/O	Y16	I/O
B18	STM	E1	NC	K4	V _{CC}	R19	I/O	V14	I/O	Y17	I/O
B19	NC	E2	I/O	K17	I	R20	I/O	V15	I/O	Y18	I/O
B20	I/O	E3	I/O	K18	ACLK / I	T1	NC	V16	I/O	Y19	I/O
C1	I/O	E4	I/O	K19	I	T2	I/O	V17	I/O	Y20	NC
C2	I/O	E17	I/O	K20	NC	T3	I/O	V18	I/O		
C3	I/O	E18	I/O	L1	I	T4	NC	V19	TMS		

Contact Information

Telephone: 408 990 4000 (US)
 416 497 8884 (Canada)
 44 1932 57 9011 (Europe)
 49 89 930 86 170 (Germany)
 852 8106 9091 (Asia)
 81 45 470 5525 (Japan)

E-mail: info@quicklogic.com

Support: support@quicklogic.com

www.DataSheet4U.com Web site: <http://www.quicklogic.com/>

Revision History

Table 12: Revision History

Revision	Date	Comments
A	not avail.	First release.
B	not avail.	
C	not avail	
D	May 2001	Update of AC/DC Specs and reformat
E	June 2002	Added Kfactor, Power-up, JTAG and mechanical drawing information. Reformatted.

Copyright Information

Copyright © 2002 QuickLogic Corporation.

All Rights Reserved.

The information contained in this product brief, and the accompanying software programs are protected by copyright. All rights are reserved by QuickLogic Corporation. QuickLogic Corporation reserves the right to make periodic modifications of this product without obligation to notify any person or entity of such revision. Copying, duplicating, selling, or otherwise distributing any part of this product without the prior written consent of an authorized representative of QuickLogic is prohibited.

QuickLogic, QuickWorks, pASIC, and ViaLink are registered trademarks of QuickLogic Corporation.

Verilog is a registered trademark of Cadence Design Systems, Inc.

All trademarks and registered trademarks are the property of their respective owners.