M53230400CW0/CB0 & M53230410CW0/CB0 EDO Mode

4M x 32 DRAM SIMM using 4Mx4, 4K/2K Refresh, 5V

GENERAL DESCRIPTION

The Samsung M5323040(1)0C is a 4Mx32bits Dynamic RAM high density memory module. The Samsung M5323040(1)0C consists of eight CMOS 4Mx4bits DRAMs in 24-pin SOJ package mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The M5323040(1)0C is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-50	50ns	13ns	90ns	25ns
-60	60ns	15ns	110ns	30ns

FEATURES

- Part Identification
  - M53230400CW0-C(4096 cycles/64ms Ref, SOJ, Solder)
  - M53230400CB0-C(4096 cycles/64ms Ref, SOJ, Gold)
  - M53230410CW0-C(2048 cycles/32ms Ref, SOJ, Solder)
  - M53230410CB0-C(2048 cycles/32ms Ref, SOJ, Gold)
- Extended Data Out
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- 1st Gen. JEDEC standard PDPin & pinout
- PCB : Height(1000mil), single sided component

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	V_{SS}	37	NC
2	DQ0	38	NC
3	DQ16	39	$\overline{V_{SS}}$
4	DQ1	40	$\overline{CAS0}$
5	DQ17	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ18	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ19	45	Res(RAS1)
10	Vcc	46	NC
11	NC	47	W
12	A0	48	NC
13	A1	49	DQ8
14	A2	50	DQ24
15	A3	51	DQ9
16	A4	52	DQ25
17	A5	53	DQ10
18	A6	54	DQ26
19	A10	55	DQ11
20	DQ4	56	DQ27
21	DQ20	57	DQ12
22	DQ5	58	DQ28
23	DQ21	59	V_{CC}
24	DQ6	60	DQ29
25	DQ22	61	DQ13
26	DQ7	62	DQ30
27	DQ23	63	DQ14
28	A7	64	DQ31
29	A11	65	DQ15
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	Res(RAS1)	69	PD3
34	RAS0	70	PD4
35	NC	71	NC
36	NC	72	Vss

PIN NAMES

Pin Name	Function
A0 - A11	Address Inputs(4K Ref)
A0 - A10	Address Inputs(2K Ref)
DQ0 - DQ31	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	Vss	Vss
PD2	NC	NC
PD3	Vss	NC
PD4	Vss	NC

* Pin connection changing available

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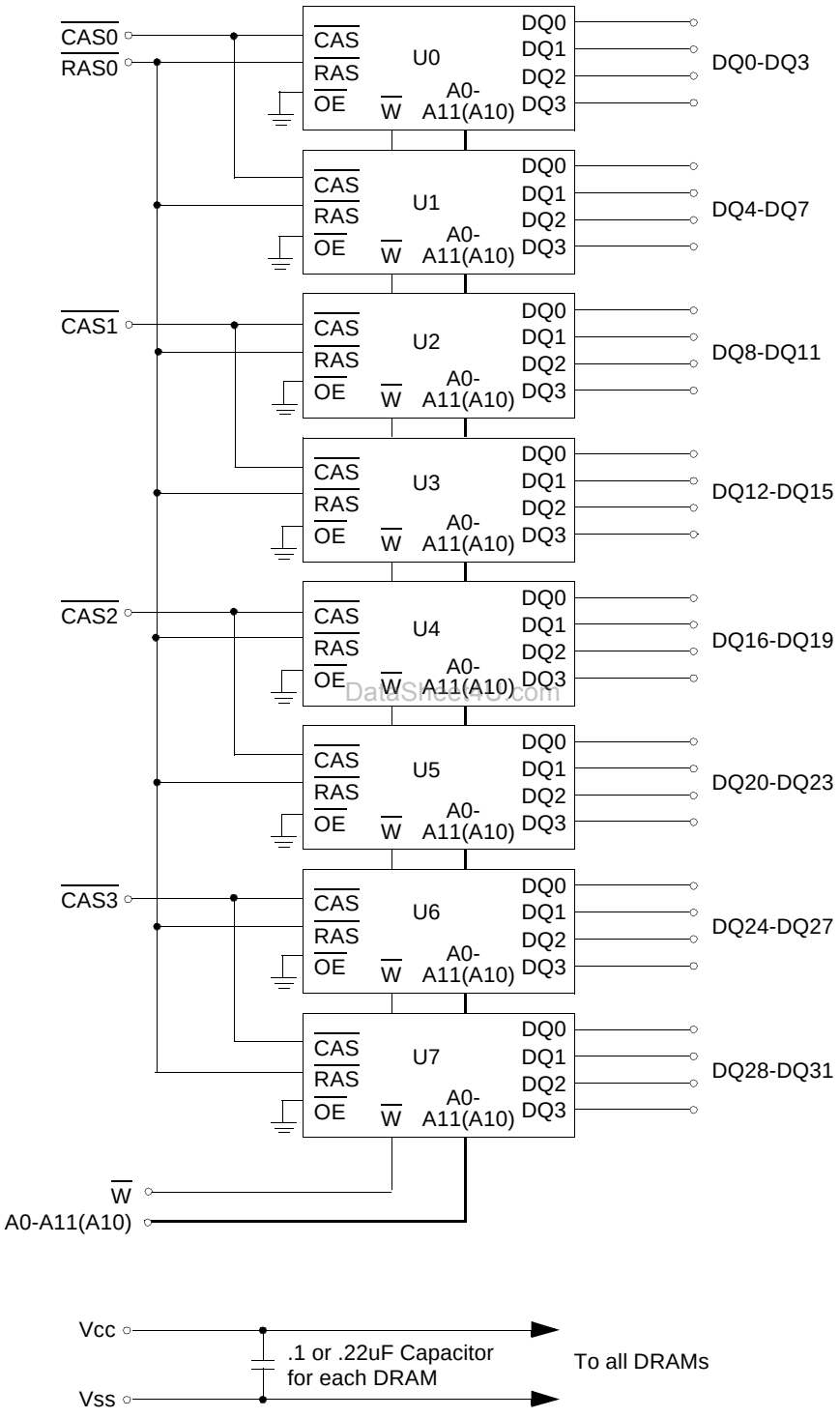
* NOTE : A11 is used for only M53230400CW0/CB0 (**4K ref**.)

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_d	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1[*1]	V
Input Low Voltage	V_{IL}	-1.0[*2]	-	0.8	V

*1 : V_{CC}+2.0V/20ns, Pulse width is measured at V_{CC}.

*2 : -2.0V/20ns, Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	M53230400CW0/CB0		M53230410CW0/CB0		Unit
		Min	Max	Min	Max	
I_{CC1}	-50 -60	- -	720 640	- -	880 800	mA mA
I_{CC2}	Don't care	-	16	-	16	mA
I_{CC3}	-50 -60	- -	720 640	- -	880 800	mA mA
I_{CC4}	-50 -60	- -	640 560	- -	720 640	mA mA
I_{CC5}	Don't care	-	8	-	8	mA
I_{CC6}	-50 -60	- -	720 640	- -	880 800	mA mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-40 -5	40 5	-40 -5	40 5	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	2.4 -	- 0.4	V V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : EDO Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Address cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{I(L)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{O(L)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

*** NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11(A10)]	C_{IN1}	-	55	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	70	pF
Input capacitance[$\overline{RAS0}$]	C_{IN3}	-	70	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	30	pF
Input/Output capacitance[DQ0-31]	C_{DQ1}	-	20	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	15	ns	6,11,12
Transition time(rise and fall)	t_T	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		45		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	13
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data-in set-up time	t_{DS}	0		0		ns	9
Data-in hold time	t_{DH}	8		10		ns	9
Refresh period (4K Ref)	t_{REF}		64		64	ms	
Refresh period (2K Ref)	t_{REF}		32		32	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	

AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=5.0V±10%. See notes 1,2.)

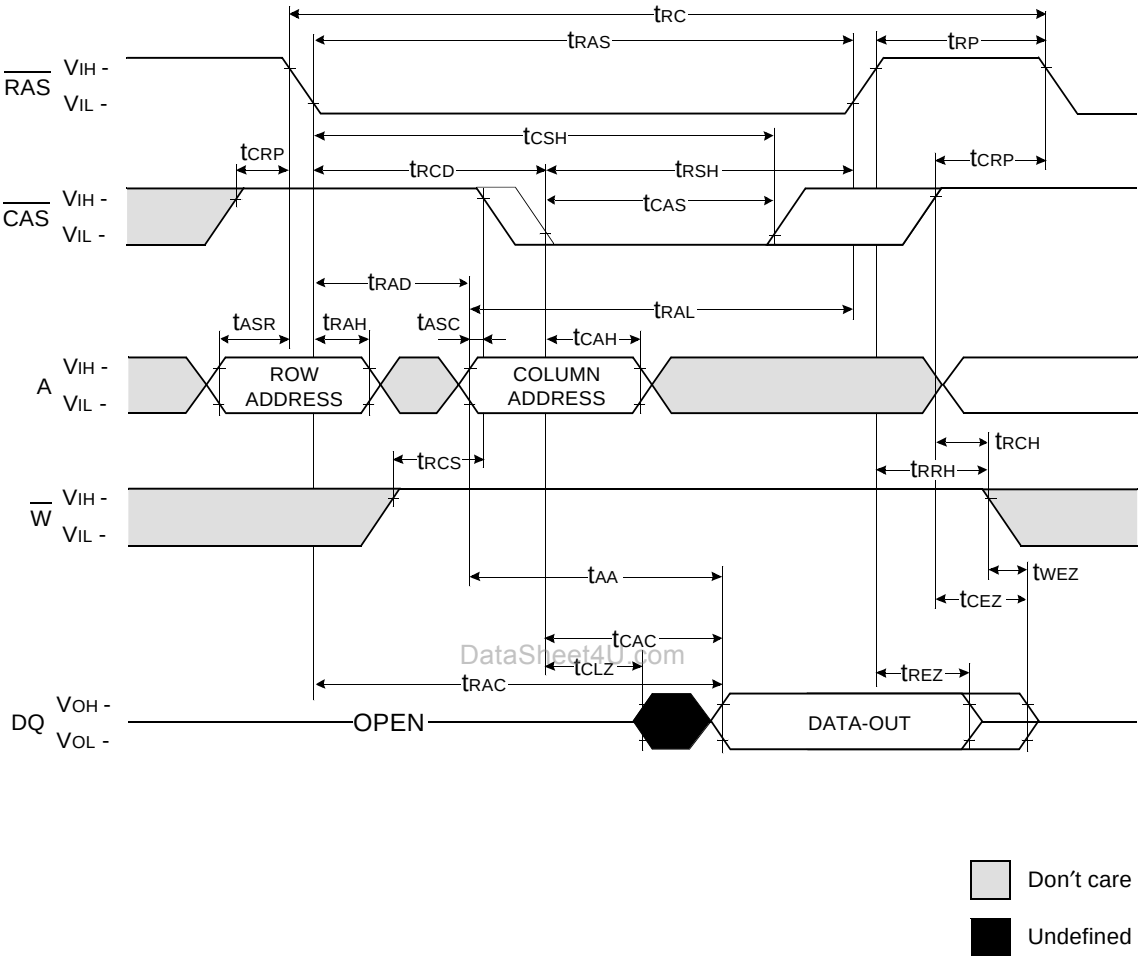
Test condition : Vih/Vil=2.4/0.8V, Voh/Vol=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	20		20		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		30		35	ns	3
Hyper page mode cycle time	t_{HPC}	25		30		ns	13
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width(Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	7,11,12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	7,11
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	t_{WPE}	5		5		ns	

NOTES

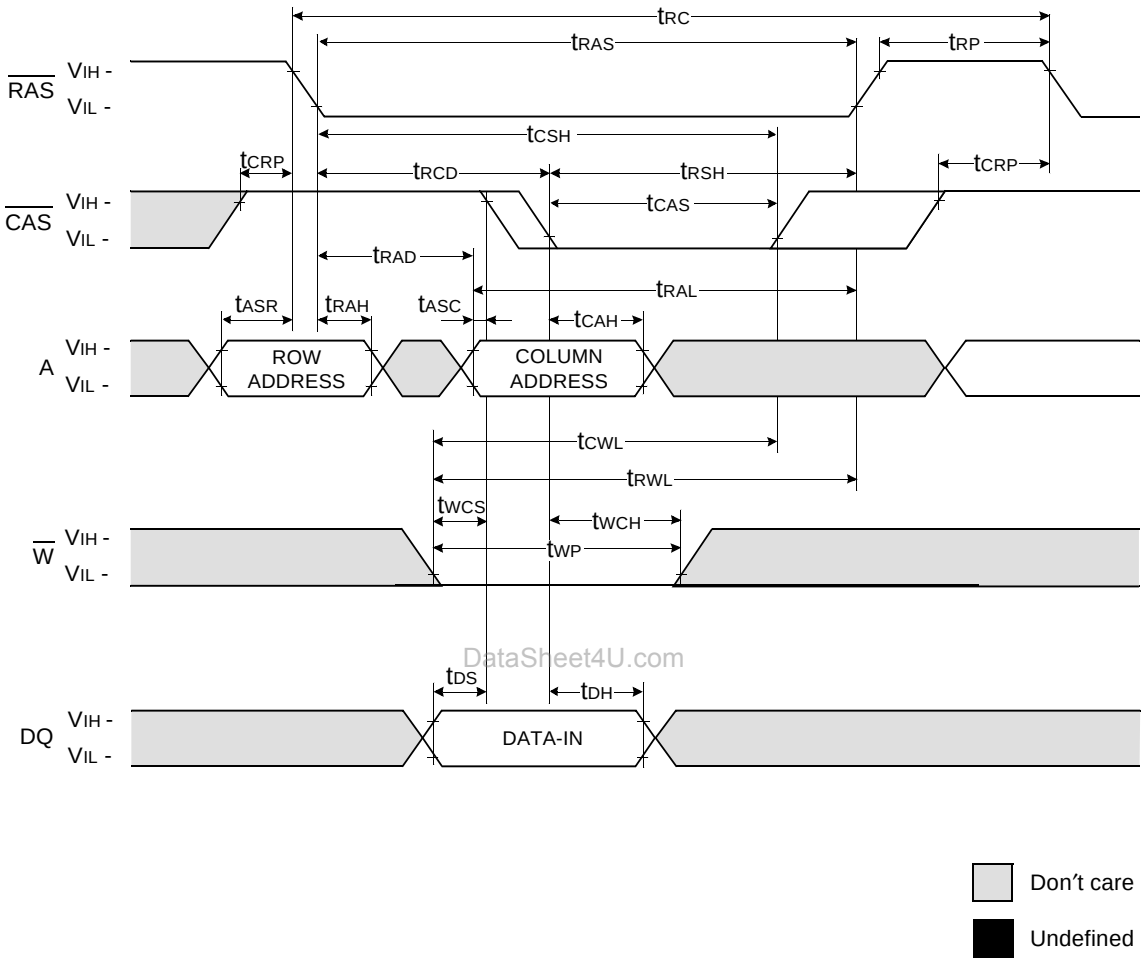
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameter are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
11. t_{CEZ}(max), t_{REZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condtion of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condtion of the output is achieved by $\overline{RAS}$ high going.
13. $t_{ASC} \geq t_{CP}$ min

READ CYCLE

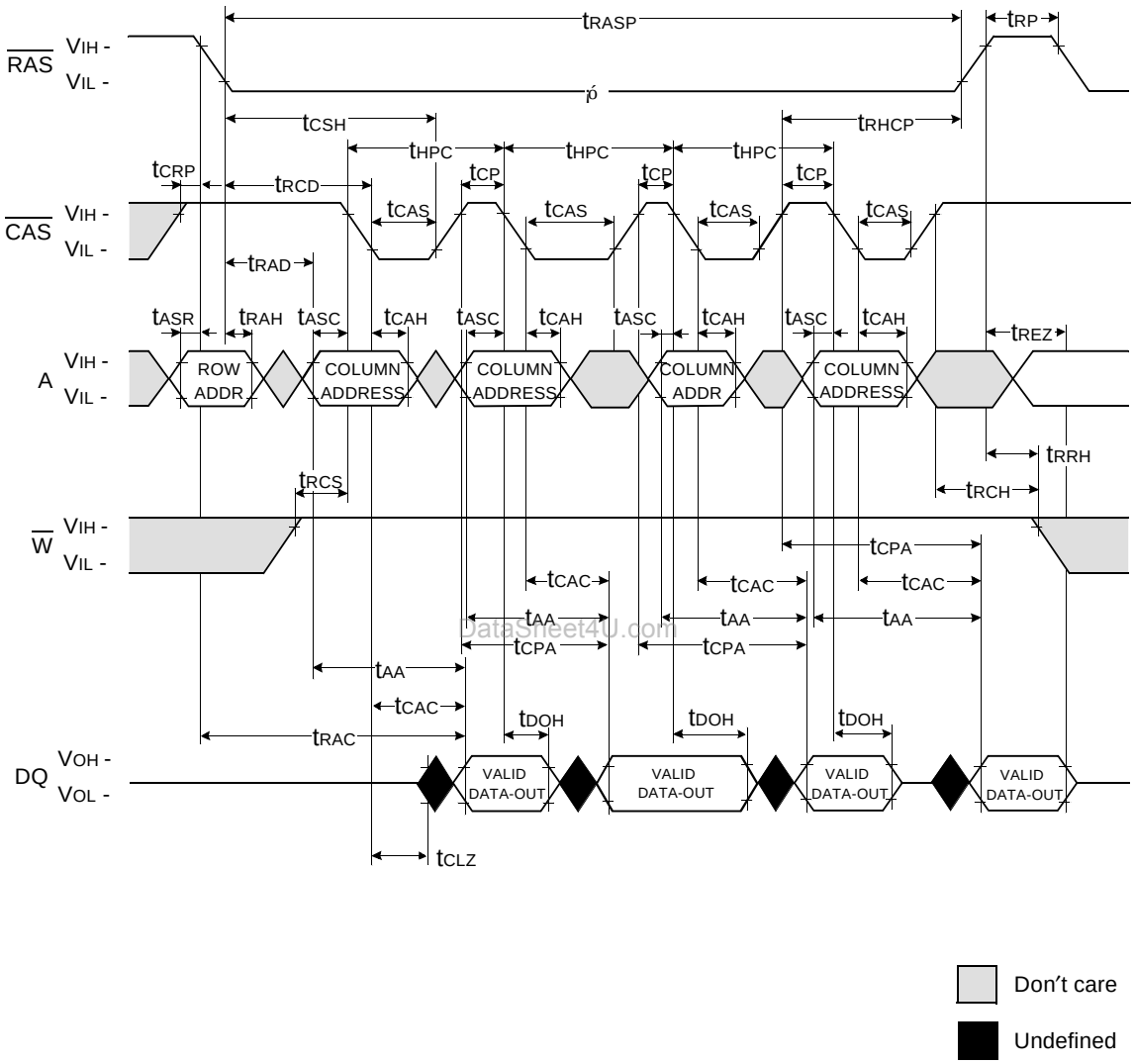


WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

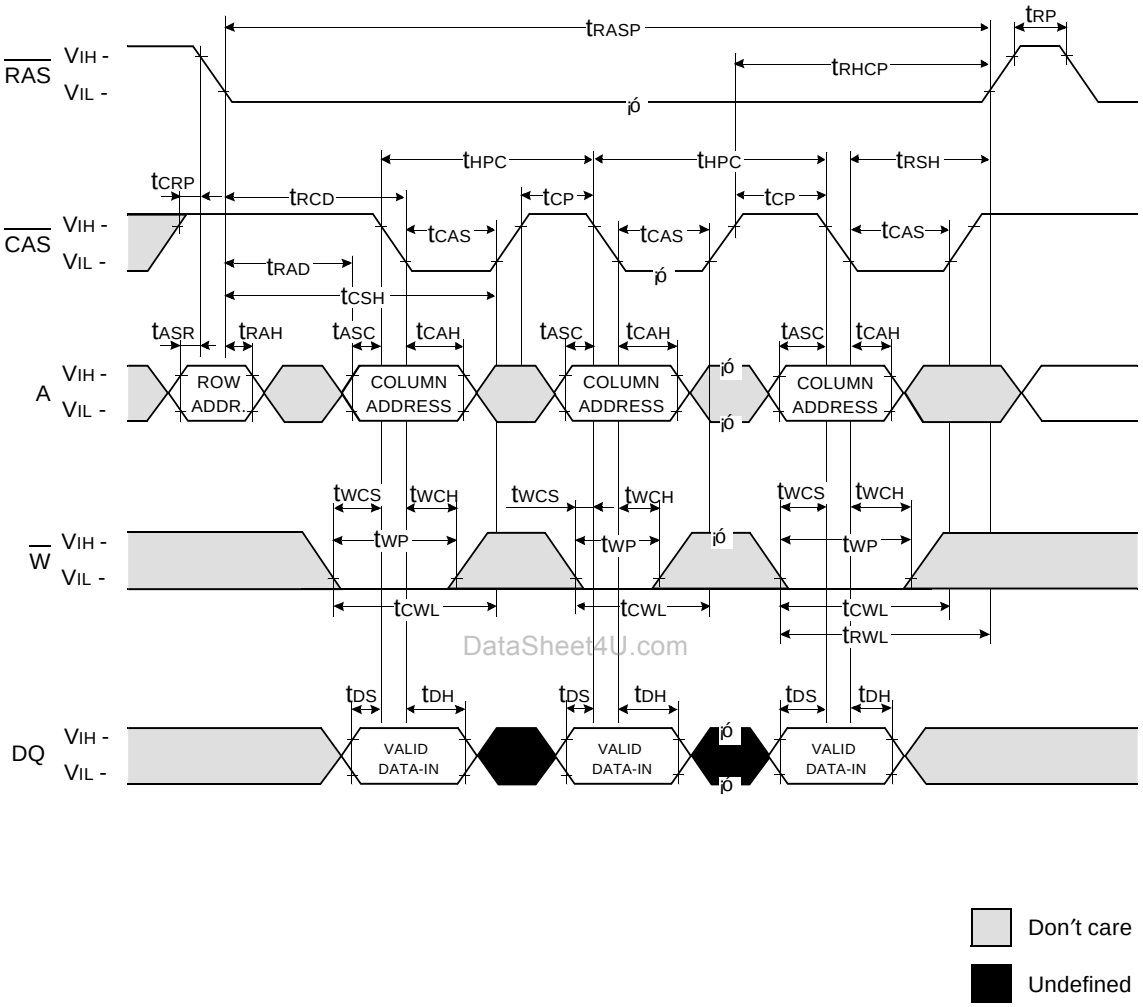


HYPER PAGE READ CYCLE



HYPER PAGE WRITE CYCLE (EARLY WRITE)

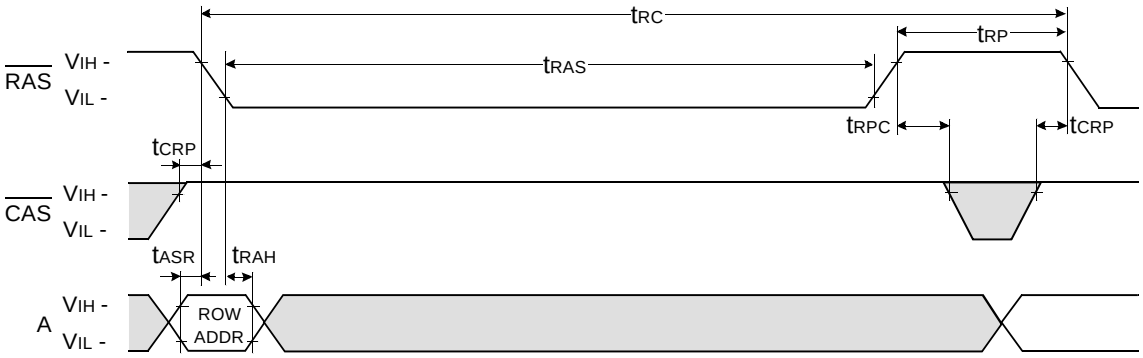
NOTE : DOUT = OPEN



$\overline{RAS}$ - ONLY REFRESH CYCLE*

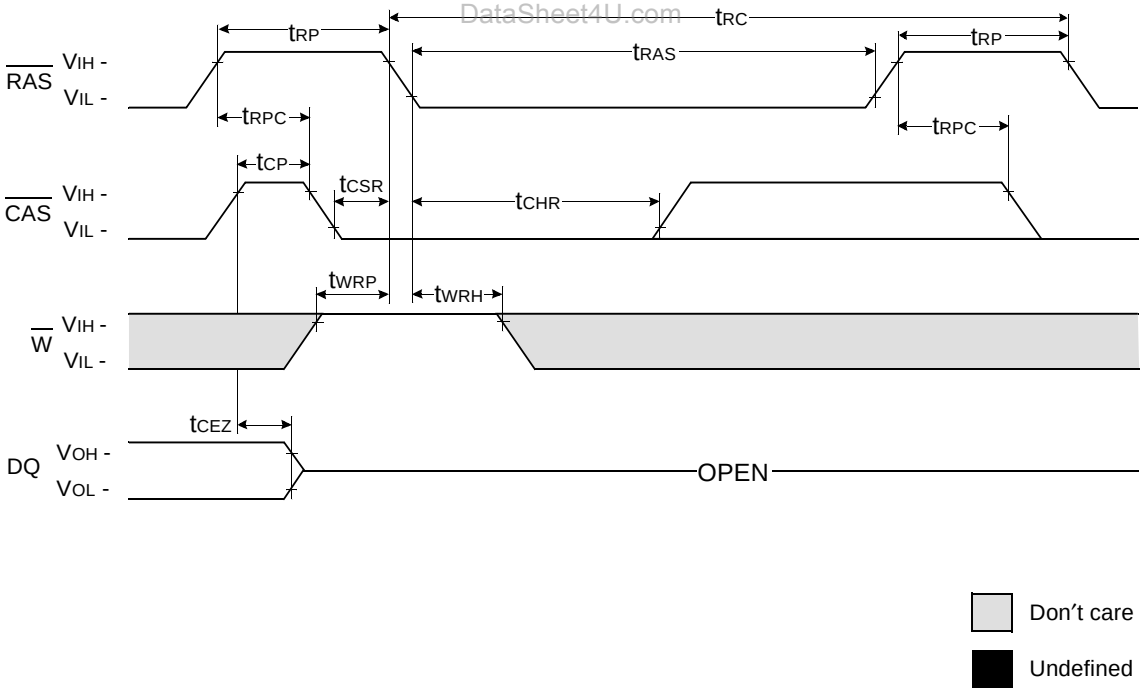
NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care

D_{OUT} = OPEN



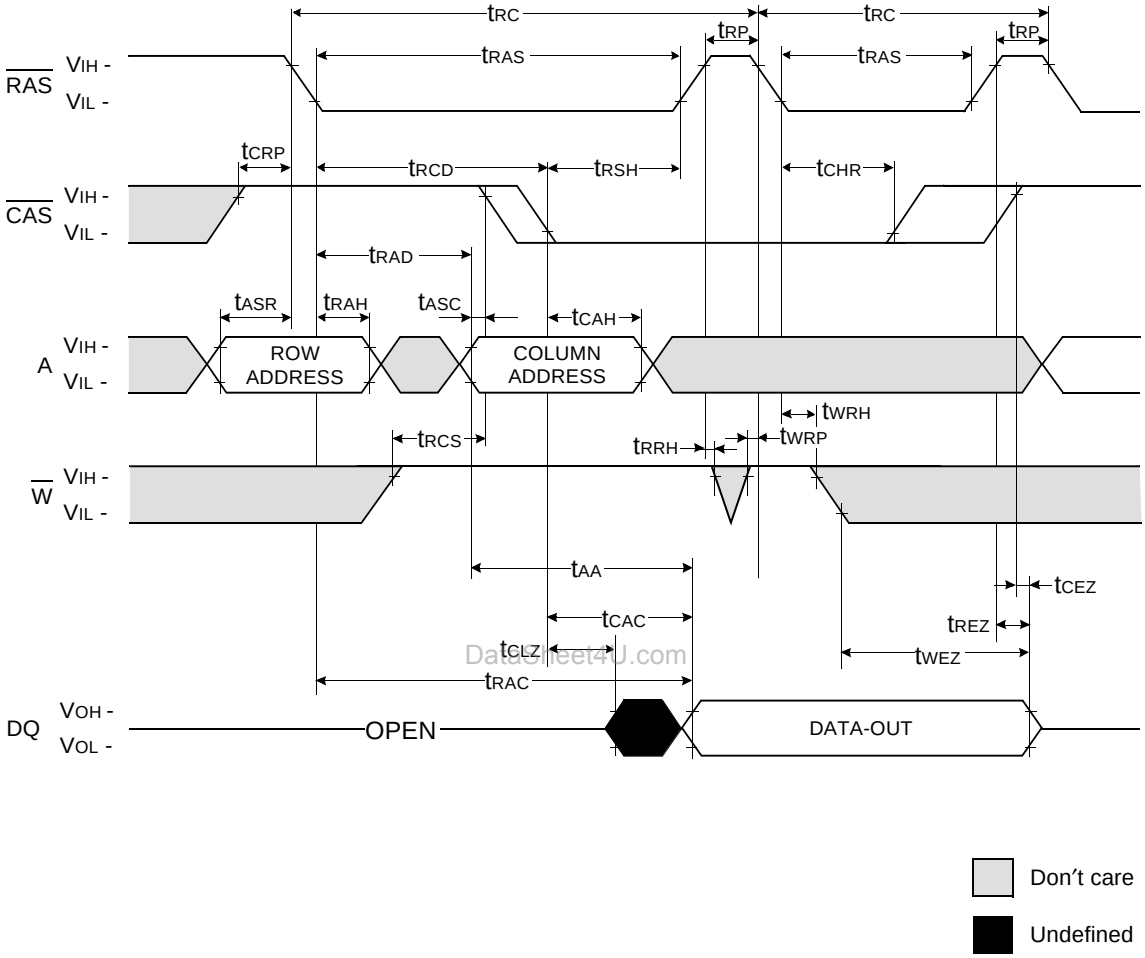
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



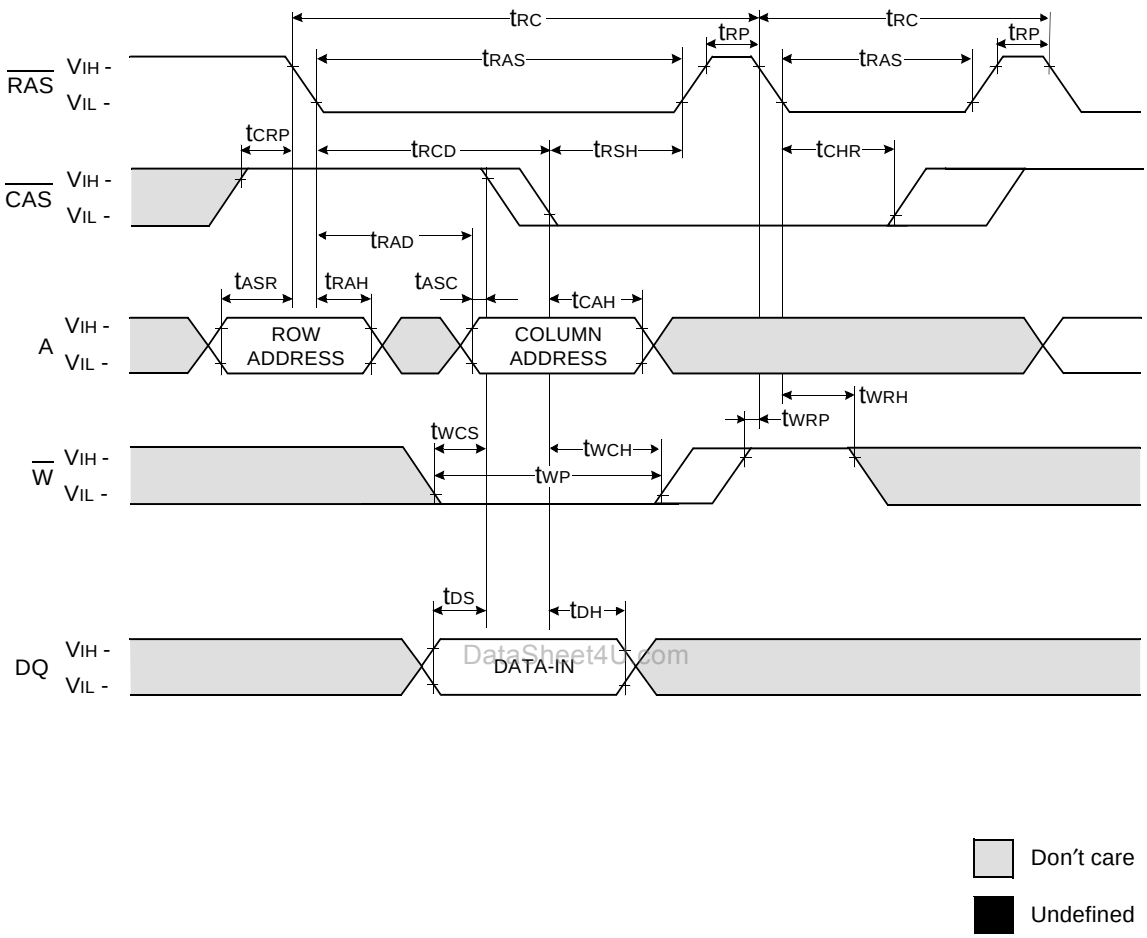
* In $\overline{RAS}$-only refresh cycle of 64Mb A-dile & B-die, when $\overline{CAS}$ signal transits from Low to High, the valid data may be cut off.

HIDDEN REFRESH CYCLE (READ)

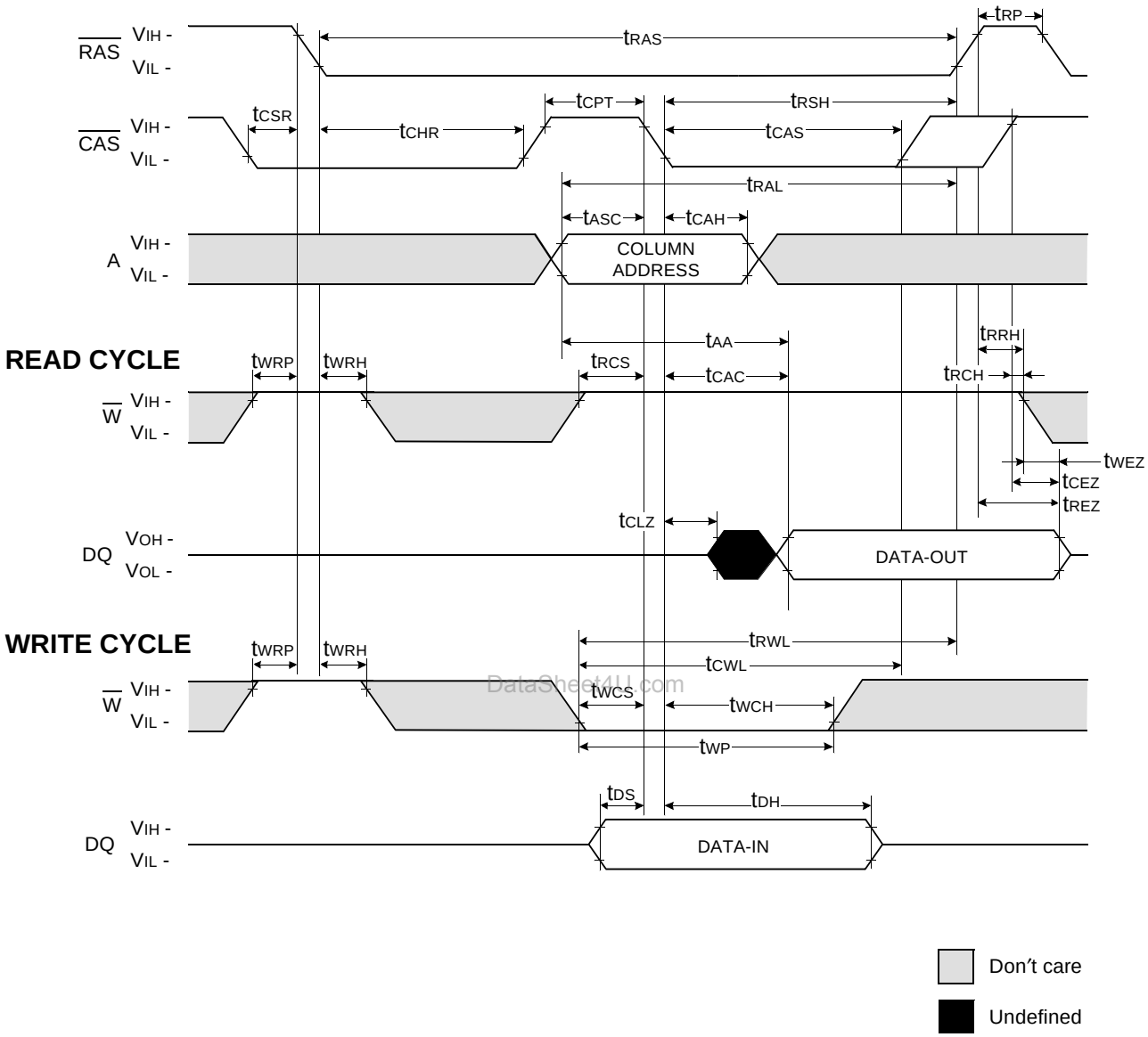


HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



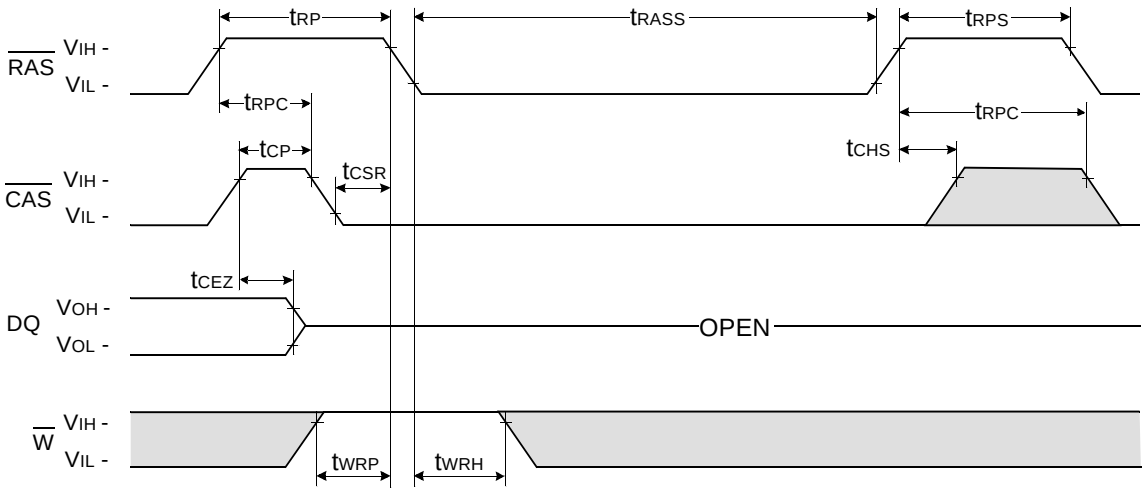
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

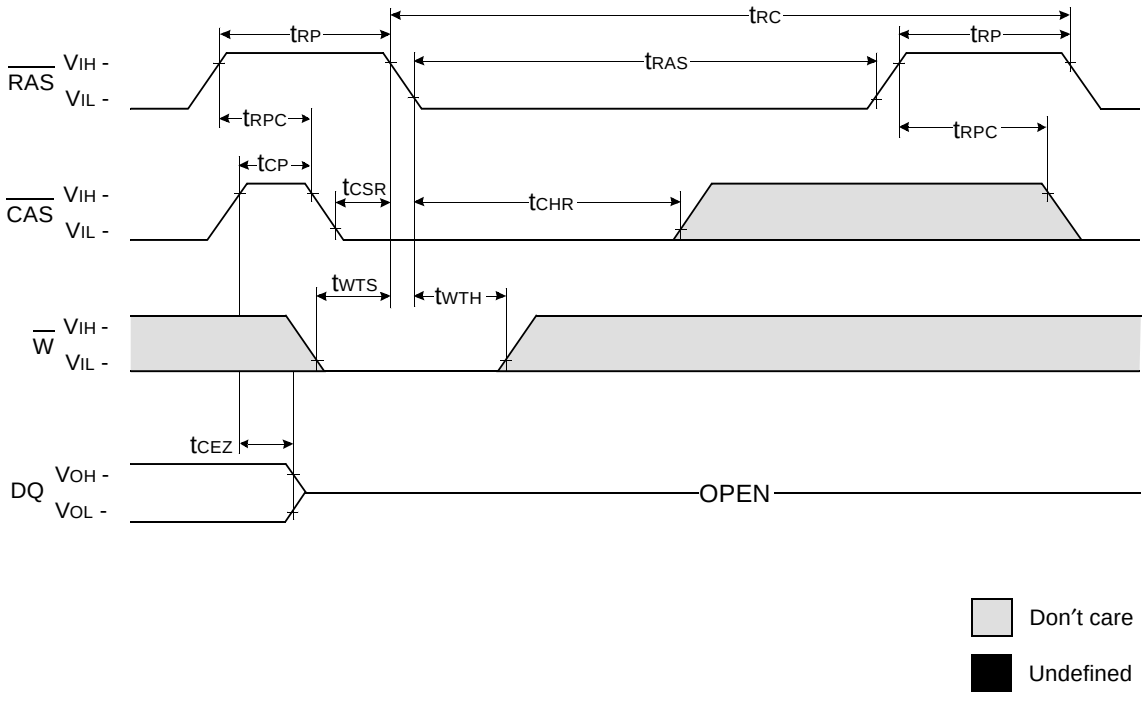
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



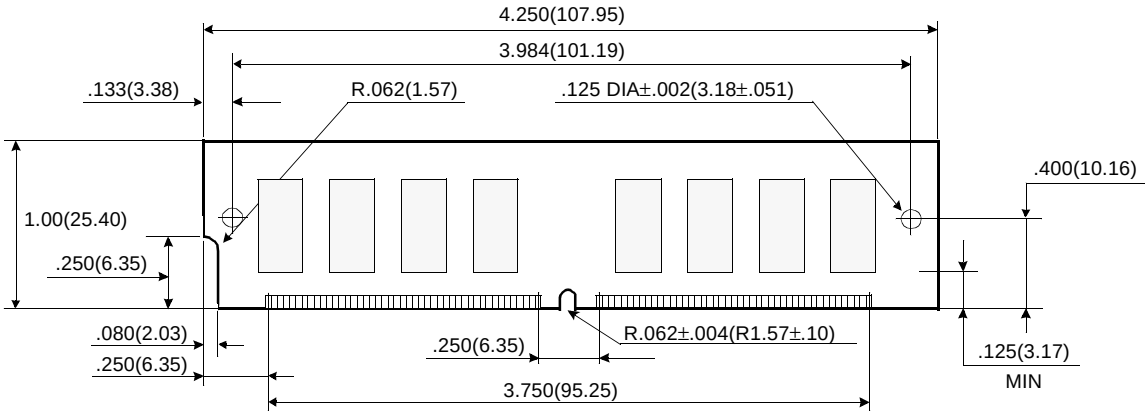
TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't care

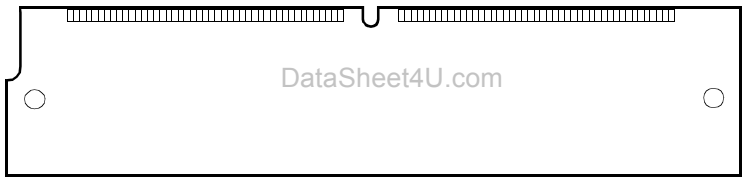


PACKAGE DIMENSIONS

Units : Inches (millimeters)

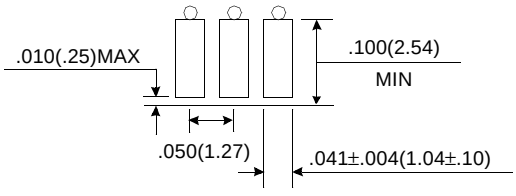


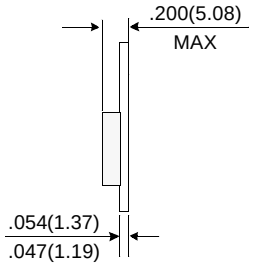
(Front view)



(Back view)

Gold & Solder Plating Lead





Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device are 4Mx4 EDO DRAM (SOJ & 300mil)

DRAM Part No. : M53230400CW0/CB0 -- K4E170411C-B(300 mil)
M53230410CW0/CB0 -- K4E160411C-B(300 mil)

Revision History
Rev 0.0 : Oct. 1999