FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12559-1E

*8-bit Proprietary Microcontroller*

**CMOS**

# F²MC-8L MB89480/MB89480L Series

# MB89485/485L/P485/P485L/PV480

## ■ DESCRIPTION

The MB89480 series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit single-chip microcontrollers.

In addition to a compact instruction set, the microcontroller contains a variety of peripheral functions such as 21-bit timebase timer, watch prescaler, PWC timer, PWM timer, 8/16-bit timer/counter, 6-bit PPG, LCD controller/driver, external interrupt 1 (edge), external interrupt 2 (level), 10-bit A/D converter, UART/SIO, buzzer, watchdog timer reset.

The MB89480 series is designed suitable for LCD remote controller as well as in a wide range of applications for consumer product.

*: F²MC stands for FUJITSU Flexible Microcontroller.

## ■ FEATURES

- Package used
  LQFP package and SH-DIP package for MB89P485/P485L, MB89485/485L
  MDIP package and MQFP package for MB89PV480
- High speed operating capability at low voltage
- Minimum execution time: 0.32 µs at 12.5 MHz

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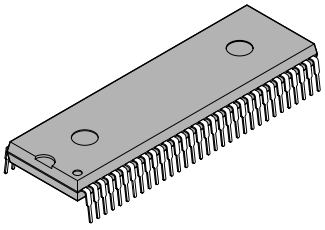
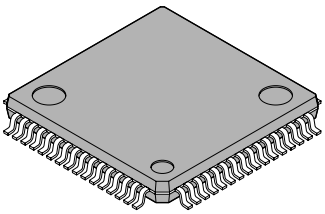
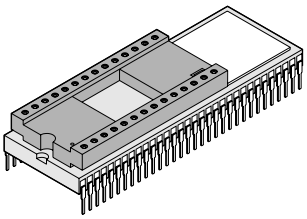
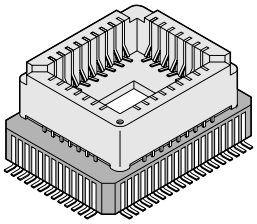
## ■ PACKAGES

| 64-pin Plastic SH-DIP | 64-pin Plastic LQFP | 64-pin Ceramic MDIP | 64-pin Ceramic MQFP |
|---|---|---|---|
|  |  |  |  |
| (DIP-64P-M01) | (FPT-64P-M09) | (MDP-64C-P02) | (MQP-64C-P01) |

FUJITSU

*(Continued)*

- F²MC-8L family CPU core

  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Test and branch instructions
  - Bit manipulation instructions, etc.

- Six timers
  PWC timer (also usable as an interval timer)
  PWM timer
  8/16-bit timer/counter x 2
  21-bit timebase timer
  Watch prescaler
- Programmable pulse generator
  6-bit PPG with program-selectable pulse width and period
- External interrupt
  Edge detection (selectable edge) : 4 channels
  Low level interrupt (wake-up function) : 8 channels
- A/D converter (4 channels)
  10-bit successive approximation type
- UART/SIO
  Synchronous/asynchronous data transfer capability
- LCD controller/driver
  Max 31 segments output x 4 commons
  Booster for LCD driving (selected by mask option)
- Buzzer
  7 frequencies are selectable by software
- Low-power consumption mode
  Stop mode (oscillation stops so as to minimize the current consumption.)
  Sleep mode (CPU stops so as to reduce the current consumption to approx. 1/3 of normal.)
  Watch mode (everything except the watch prescaler stops so as to reduce the power comsumption to an extremely low level.)
  Sub-clock mode
- Watchdog timer reset
- I/O ports: Max 42 channels

## ■ PRODUCT LINEUP

| Parameter \ Part number | MB89485L | MB89485 | MB89P485L | MB89P485 | MB89PV480 |
|---|---|---|---|---|---|
| Classification | Mass production products (mask ROM product) | | OTP | | Piggy-back |
| ROM size | 16K x 8-bit (internal ROM) | | 16K x 8-bit (internal PROM with read protection) *2 | | 32K x 8-bit (external ROM)*1 |
| RAM size | 512 x 8-bit | | | | 1K × 8-bit |
| CPU functions | Number of instructions : 136<br>Instruction bit length : 8 bits<br>Instruction length : 1 to 3 bytes<br>Data bit length : 1, 8, 16 bits<br>Minimum execution time : 0.32 µs at 12.5 MHz<br>Minimum interrupt processing time : 2.88 µs at 12.5 MHz | | | | |
| Ports | I/O ports (CMOS) : 11 pins<br>N-channel open drain I/O ports : 28 pins<br>Output ports (N-channel open drain) : 2 pins<br>Input port : 1 pin<br>Total : 42 pins | | | | |
| 21-bit timebase timer | Interrupt period (0.66 ms, 2.6 ms, 21.0 ms, 335.5 ms) at 12.5 MHz. | | | | |
| Watchdog timer | Reset period (167.8 ms to 335.5 ms) at 12.5 MHz. | | | | |
| Pulse width count timer | 1 channel.<br>8-bit one-shot timer operation (supports underflow output, operating clock period: 1, 4, 32 $t_{inst}$, external).<br>8-bit reload timer operation (supports square wave output, operating clock period: 1, 4, 32 $t_{inst}$, external).<br>8-bit pulse width measurement operation (supports continuous measurement, H width, L width, rising edge to rising edge, falling edge to falling edge measurement and both edge measurement). | | | | |
| PWM timer | 8-bit reload timer operation (supports square wave output, operating clock period: 1, 4, 32 $t_{inst}$, external).<br>8-bit resolution PWM operation. | | | | |
| 6- bit programmable pulse generator | Can generate square pulse with programmable period. | | | | |
| 8/16-bit timer/counter 11, 12 | Can be operated either as a 2-channel 8-bit timer/counter (timer 11 and timer 12, each with its own independent operating clock cycle), or as one 16-bit timer/counter.<br>In timer 11 or 16-bit timer/counter operation, event counter operation (external clock-triggered) and square wave output capability. | | | | |
| 8/16-bit timer/counter 21, 22 | Can be operated either as a 2-channel 8-bit timer/counter (timer 21 and timer 22, each with its own independent operating clock cycle), or as one 16-bit timer/counter.<br>In timer 21 or 16-bit timer/counter operation, event counter operation (external clock-triggered) and square wave output capability. | | | | |
| External interrupt | 4 independent channels (selectable edge, interrupt vector, request flag).<br>8 channels (low level interrupt). | | | | |

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| Parameter \ Part number | MB89485L | MB89485 | MB89P485L | MB89P485 | MB89PV480 |
|---|---|---|---|---|---|
| A/D converter | 10-bit resolution × 4 channels.<br>A/D conversion function (conversion time: 60 $t_{inst}$ ).<br>Supports repeated activation by internal clock. | | | | |
| LCD controller/driver | Common output : 4 (Max)<br>Segment output : 31 (Max) (selected resistor ladder)<br>: 26 (Max) (selected booster)<br>Bias power supply pins : 4<br>LCD display RAM size : 31 × 4 bits<br>Dividing resistor/booster : selected by mask option | | | | |
| UART/SIO | Synchronous/asynchronous data transfer capability.<br>(Max baud rate: 97.656 Kbps at 12.5 MHz).<br>(7 and 8 bits with parity bit; 8 and 9 bits without parity bit). | | | | |
| Buzzer output | 7 frequencies are selectable by software. | | | | |
| Standby mode | Sleep mode, stop mode, watch mode, sub-clock mode. | | | | |
| Process | CMOS | | | | |
| Operating voltage | 2.2 V to 3.6 V | 2.2 V to 5.5 V | 2.7 V to 3.6 V | 3.5 V to 5.5 V | 2.7 V to 5.5 V |

*1 : Use MBM27C256A as the external ROM.

*2 : Read protection feature is selected by part number, detail please refer to MASK OPTIONS.

Note : 1 $t_{inst}$ = one instruction cycle (execution time) which can be selected as 1/4, 1/8, 1/16, or 1/64 of main clock.

## ■ PACKAGE AND CORRESPONDING PRODUCTS

| Package \ Part number | MB89485/485L | MB89P485/P485L | MB89PV480 |
|---|---|---|---|
| DIP-64P-M01 | O | O | X |
| FPT-64P-M09 | O | O | X |
| MDP-64C-P02 | X | X | O |
| MQP-64C-P01 | X | X | O |

O : Availabe
X : Not available

## ■ DIFFERENCES AMONG PRODUCTS

### 1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following point:

- The stack area is set at the upper limit of the RAM.

### 2. Current Consumption

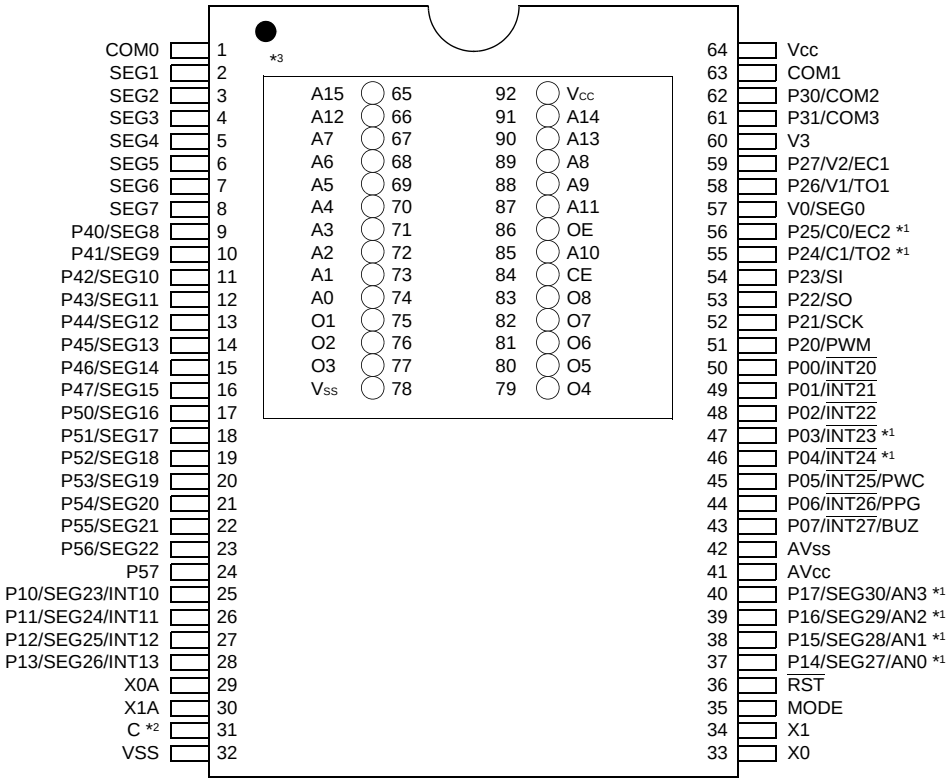
- For the MB89PV480, the current consumed by the EPROM mounted in the piggy-back socket is needed to be included.
- When operating at low speed, the current consumed by the one-time PROM product is greater than that for the mask ROM product. However, the current consumption is roughly the same in sleep and stop mode.
- For more information, see “■ ELECTRICAL CHARACTERISTICS”.

### 3. Oscillation Stabilization Time after Power-on Reset

- For MB89PV480, MB89P485L and MB89485L, there is no power-on stabilization time after power-on reset.
- For MB89P485, there is power-on stabilization time after power-on reset.
- For MB89485, the power-on stabilization time can be selected.
- For more information, please refer to “■ MASK OPTION”.

## ■ PIN ASSIGNMENT

(TOP VIEW)




(DIP-64P-M01)
(MDP-64C-P02)

*1: If booster is selected, EC2 and TO2 will be redirected to P03/$\overline{\text{INT23}}$ and P04/$\overline{\text{INT24}}$ respectively.
Segment output of P17/SEG30/AN3 - P14/SEG27/AN0 will be disabled.
*2: For product other than MB89P485, pin 31 is NC pin.

*3: Pin assignment on package top.

| Pin no. | Pin symbol | Pin no. | Pin symbol | Pin no. | Pin symbol | Pin no. | Pin symbol |
|---|---|---|---|---|---|---|---|
| 65 | A15 | 73 | A1 | 81 | O6 | 89 | A8 |
| 66 | A12 | 74 | A0 | 82 | O7 | 90 | A13 |
| 67 | A7 | 75 | O1 | 83 | O8 | 91 | A14 |
| 68 | A6 | 76 | O2 | 84 | $\overline{\text{CE}}$ | 92 | VCC |
| 69 | A5 | 77 | O3 | 85 | A10 | | |
| 70 | A4 | 78 | VSS | 86 | $\overline{\text{OE}}$ | | |
| 71 | A3 | 79 | O4 | 87 | A11 | | |
| 72 | A2 | 80 | O5 | 88 | A9 | | |

N.C.: As connected internally, do not use.

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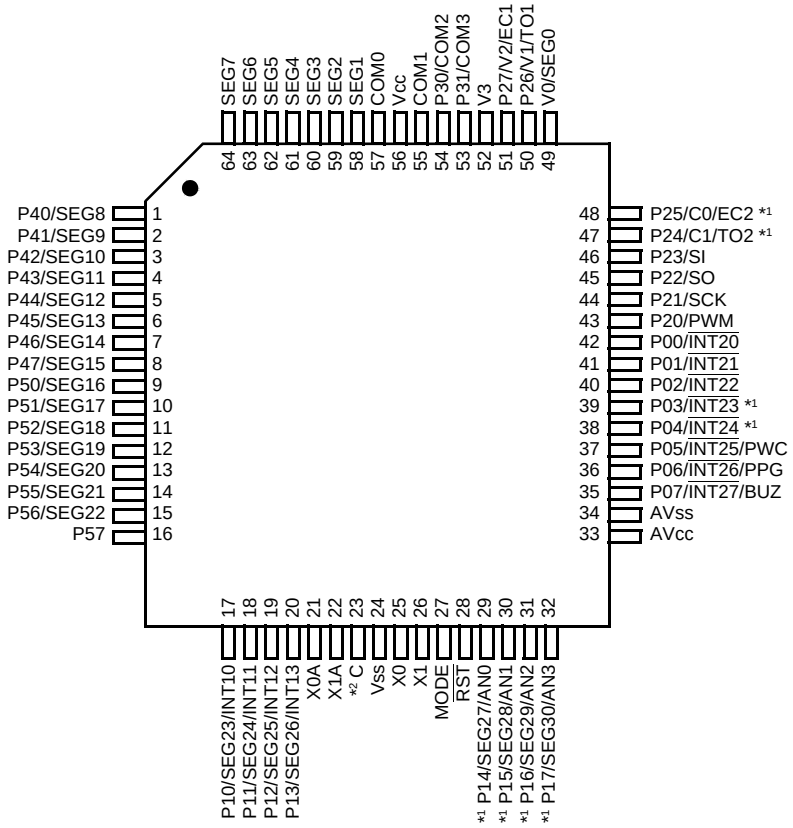
(TOP VIEW)




(FPT-64P-M09)

*1: If booster is selected, EC2 and TO2 will be redirected to P03/$\overline{\text{INT23}}$ and P04/$\overline{\text{INT24}}$ respectively. Segment output of P17/SEG30/AN3 - P14/SEG27/AN0 will be disabled.

*2: For product other than MB89P485, pin 23 is NC pin.

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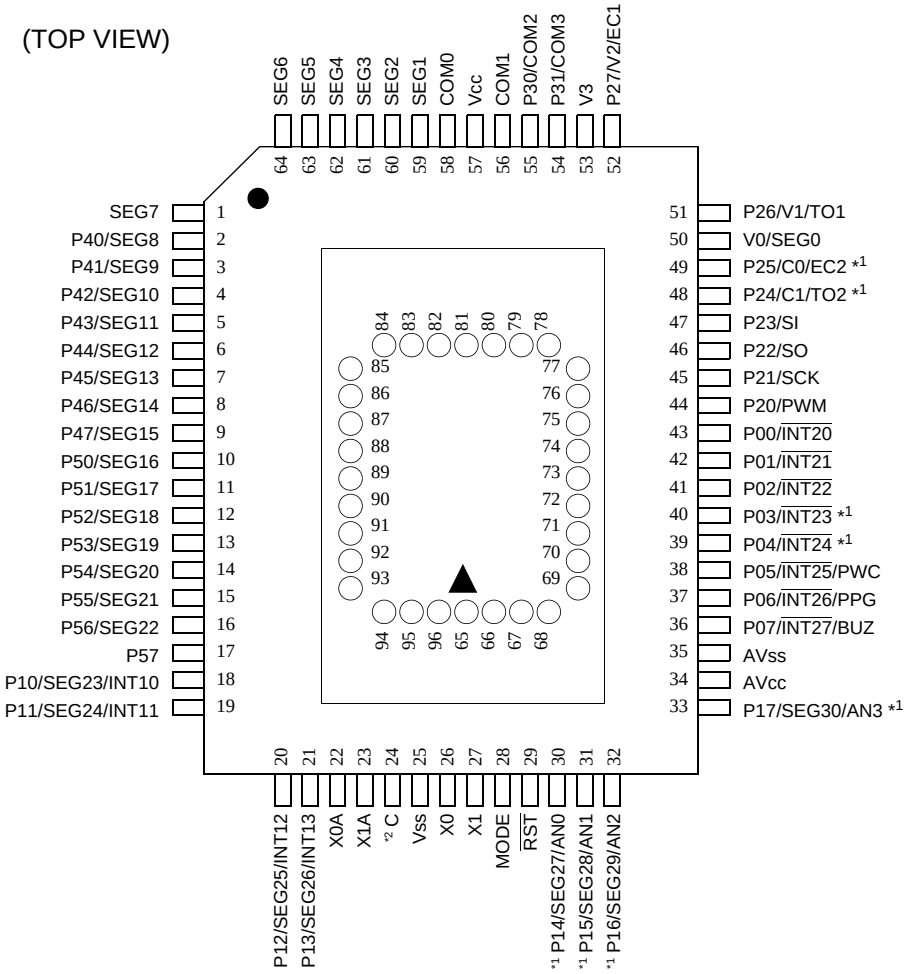
(TOP VIEW)




(MQP-64C-P01)

*1: If booster is selected, EC2 and TO2 will be redirected to P03/$\overline{\text{INT23}}$ and P04/$\overline{\text{INT24}}$ respectively. Segment output of P17/SEG30/AN3 - P14/SEG27/AN0 will be disabled.

*2: Pin 24 is NC pin.

Pin assignment on package top

| Pin no. | Pin symbol | Pin no. | Pin symbol | Pin no. | Pin symbol | Pin no. | Pin symbol |
|---|---|---|---|---|---|---|---|
| 65 | N.C. | 73 | A2 | 81 | N.C. | 89 | $\overline{\text{OE}}$ |
| 66 | $V_{PP}$ | 74 | A1 | 82 | O4 | 90 | N.C. |
| 67 | A12 | 75 | A0 | 83 | O5 | 91 | A11 |
| 68 | A7 | 76 | N.C. | 84 | O6 | 92 | A9 |
| 69 | A6 | 77 | O1 | 85 | O7 | 93 | A8 |
| 70 | A5 | 78 | O2 | 86 | O8 | 94 | A13 |
| 71 | A4 | 79 | O3 | 87 | $\overline{\text{CE}}$ | 95 | A14 |
| 72 | A3 | 80 | $V_{SS}$ | 88 | A10 | 96 | $V_{CC}$ |

N.C.: As connected internally, do not use.

## ■ PIN DESCRIPTION

| Pin number | | | Pin name | I/O circuit type | Function |
|---|---|---|---|---|---|
| SH-DIP*1 MDIP*4 | MQFP*2 | QFP*3 | | | |
| 33 | 26 | 25 | X0 | A | Connection pins for a crystal or other oscillator.<br>An external clock can be connected to X0. In this case, leave X1 open. |
| 34 | 27 | 26 | X1 | | |
| 29 | 22 | 21 | X0A | A | Connection pins for a crystal or other oscillator.<br>An external clock can be connected to X0A. In this case, leave X1A open. |
| 30 | 23 | 22 | X1A | | |
| 35 | 28 | 27 | MODE | B | Input pin for setting the memory access mode.<br>Connect directly to $V_{SS}$. |
| 36 | 29 | 28 | $\overline{RST}$ | C | Reset I/O pin. The pin is an N-ch open-drain type with pull-up resistor and a hysteresis input. The pin outputs an “L” level when an internal reset request is present. Inputting an “L” level initializes internal circuits. |
| 50 to 48 | 43 to 41 | 42 to 40 | P00/$\overline{INT20}$ to P02/$\overline{INT22}$ | D | General-purpose CMOS I/O port.<br>A hysteresis input.<br>The pin is shared with external interrupt 2 input. |
| 47 | 40 | 39 | P03/$\overline{INT23}$ | D | General-purpose CMOS I/O port.<br>A hysteresis input.<br>The pin is shared with external interrupt 2 input, and shared with 8/16-bit timer/counter 21, 22 input when booster is selected. |
| 46 | 39 | 38 | P04/$\overline{INT24}$ | D | General-purpose CMOS I/O port.<br>A hysteresis input.<br>The pin is shared with external interrupt 2 input, and shared with 8/16-bit timer/counter 21, 22 output when booster is selected. |
| 45 | 38 | 37 | P05/$\overline{INT25}$/ PWC | D | General-purpose CMOS I/O port.<br>A hysteresis input.<br>The pin is shared with external interrupt 2 input, and PWC input. |
| 44 | 37 | 36 | P06/$\overline{INT26}$/ PPG | D | General-purpose CMOS I/O port.<br>A hysteresis input.<br>The pin is shared with external interrupt 2 input, and 6-bit PPG output. |
| 43 | 36 | 35 | P07/$\overline{INT27}$/ BUZ | D | General-purpose CMOS I/O port.<br>A hysteresis input.<br>The pin is shared with external interrupt 2 input and buzzer output. |
| 25 to 28 | 18 to 21 | 17 to 20 | P10/SEG23/ INT10 to P13/ SEG26/INT13 | F/K | General-purpose N-ch open-drain I/O port.<br>A hysteresis input.<br>The pin is shared with external interrupt 1 input and LCD segment output. |

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| Pin number | | | Pin name | I/O circuit type | Function |
|---|---|---|---|---|---|
| SH-DIP*1 MDIP*4 | MQFP*2 | QFP*3 | | | |
| 37 to 40 | 30 to 33 | 29 to 32 | P14/SEG27/ AN0 to P17/ SEG30/AN3 | G/K | General-purpose N-ch open-drain I/O port.<br>An analog input.<br>The pin is shared with A/D converter input and LCD segment output.<br>LCD segment output will be disabled when booster is selected. |
| 51 | 44 | 43 | P20/PWM | E | General-purpose CMOS I/O port.<br>The pin is shared with PWM output. |
| 52 | 45 | 44 | P21/SCK | E | General-purpose CMOS I/O port.<br>The pin is shared with UART/SIO clock I/O. |
| 53 | 46 | 45 | P22/SO | E | General-purpose CMOS I/O port.<br>The pin is shared with UART/SIO data output. |
| 54 | 47 | 46 | P23/SI | D | General-purpose CMOS I/O port.<br>The pin is shared with UART/SIO data input. |
| 55 | 48 | 47 | P24/C1/TO2 | H | General-purpose CMOS I/O port.<br>The pin is shared with 8/16-bit timer 21, 22 output (it is redirected to P04/$\overline{INT24}$ when booster is selected), and as a capacitor connecting pin when booster is selected. |
| 56 | 49 | 48 | P25/C0/EC2 | F | General-purpose CMOS I/O port.<br>A hysteresis input.<br>The pin is shared with 8/16-bit timer 21, 22 input (it is redirected to P03/$\overline{INT23}$ when booster is selected), and as a capacitor connecting pin when booster is selected. |
| 58 | 51 | 50 | P26/V1/TO1 | H | General-purpose CMOS I/O port.<br>The pin is shared with 8/16-bit timer 11, 12 output, and LCD power driving pin. |
| 59 | 52 | 51 | P27/V2/EC1 | F | General-purpose CMOS I/O port.<br>A hysteresis input.<br>The pin is shared with 8/16-bit timer 11, 12 input, and LCD power driving pin. |
| 62 | 55 | 54 | P30/COM2 | I / K | General-purpose N-ch open-drain output port.<br>The pin is shared with the LCD common output. |
| 61 | 54 | 53 | P31/COM3 | I / K | General-purpose N-ch open-drain output port.<br>The pin is shared with the LCD common output. |
| 9 to 16 | 2 to 9 | 1 to 8 | P40/SEG8 to P47/SEG15 | H / K | General-purpose N-ch open-drain I/O port.<br>The pin is shared with LCD segment output. |
| 17 to 23 | 10 to 16 | 9 to 15 | P50/SEG16 to P56/SEG22 | H / K | General-purpose N-ch open-drain I/O port.<br>The pin is shared with LCD segment output. |
| 24 | 17 | 16 | P57 | J | General-purpose CMOS input port. |

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| Pin number | | | Pin name | I/O circuit type | Function |
|---|---|---|---|---|---|
| SH-DIP*1 MDIP*4 | MQFP*2 | QFP*3 | | | |
| 2 to 8 | 59 to 64, 1 | 58 to 64 | SEG1 to SEG7 | K | LCD segment output-only pins. |
| 1, 63 | 58, 56 | 57, 55 | COM0 to COM1 | K | LCD common output-only pins. |
| 60 | 53 | 52 | V3 | — | LCD driving power supply pin. |
| 57 | 50 | 49 | V0/SEG0 | — / K | LCD driving power supply pin when booster is selected.<br>LCD segment output when booster is not selected. |
| 31 | 24 | 23 | C | — | When MB89P485 is used, connect an external 0.1 μF capacitor between this pin and the ground. |
| | | | | | N.C. pin when MB89485/485L, MB89P485L or MB89PV480 is used. |
| 64 | 57 | 56 | $V_{CC}$ | — | Power supply pin (+3 V or +5 V). |
| 32 | 25 | 24 | $V_{SS}$ | — | Power supply pin (GND). |
| 41 | 34 | 33 | $AV_{CC}$ | — | A/D converter power supply pin. |
| 42 | 35 | 34 | $AV_{SS}$ | — | A/D converter power supply pin.<br>Use at the same voltage level as $V_{SS}$. |

*1: DIP-64P-M01

*2: MQP-64C-P01

*3: FPT-64P-M09

*4: MDP-64C-P02

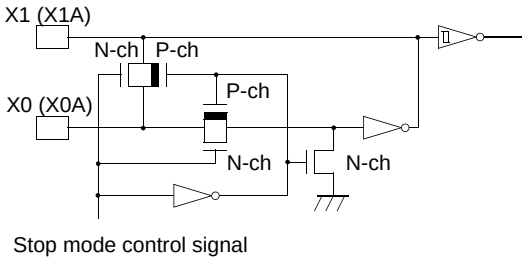
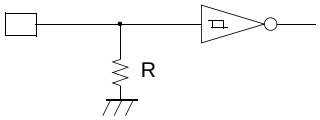
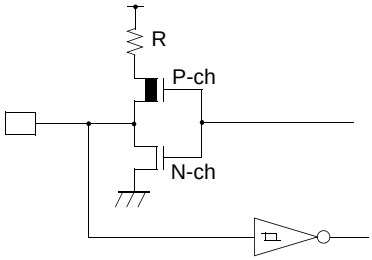
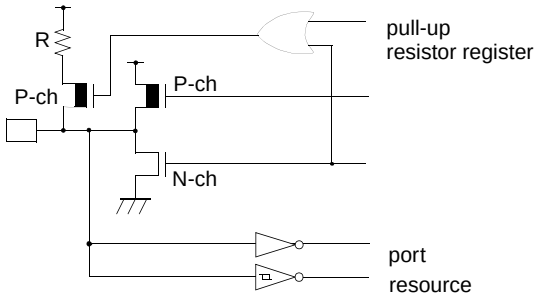
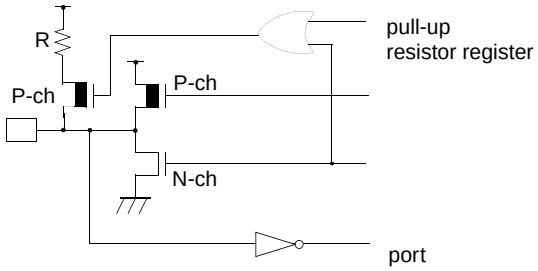
## ■ External EPROM Socket (MB89PV480 only)

| Pin number | | Pin name | I/O | Function |
|---|---|---|---|---|
| MDIP*1 | MQFP*2 | | | |
| 91 | 95 | A14 | O | Address output pins. |
| 90 | 94 | A13 | | |
| 66 | 67 | A12 | | |
| 87 | 91 | A11 | | |
| 85 | 88 | A10 | | |
| 88 | 92 | A9 | | |
| 89 | 93 | A8 | | |
| 67 | 68 | A7 | | |
| 68 | 69 | A6 | | |
| 69 | 70 | A5 | | |
| 70 | 71 | A4 | | |
| 71 | 72 | A3 | | |
| 72 | 73 | A2 | | |
| 73 | 74 | A1 | | |
| 74 | 75 | A0 | | |
| 83 | 86 | O8 | I | Data input pins. |
| 82 | 85 | O7 | | |
| 81 | 84 | O6 | | |
| 80 | 83 | O5 | | |
| 79 | 82 | O4 | | |
| 77 | 79 | O3 | | |
| 76 | 78 | O2 | | |
| 75 | 77 | O1 | | |
| 65 | 65 | N.C. | — | Internally connected pins. Always leave open. |
| 76 | 76 | | | |
| 81 | 81 | | | |
| 90 | 90 | | | |
| 65 | 66 | $V_{PP}$ | O | “H” level output pin. |
| 78 | 80 | $V_{SS}$ | O | Power supply pin (GND). |
| 84 | 87 | $\overline{CE}$ | O | Chip enable pin for the EPROM. Outputs “H” in standby mode. |
| 86 | 89 | OE | O | Output enable pin for the EPROM. Always outputs “L”. |
| 92 | 96 | $V_{CC}$ | O | Power supply pin for the EPROM. |

*1: MDP-64C-P02

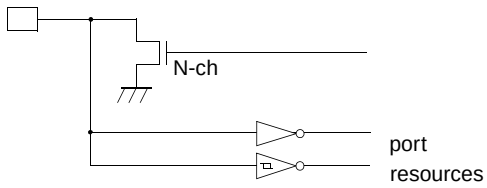
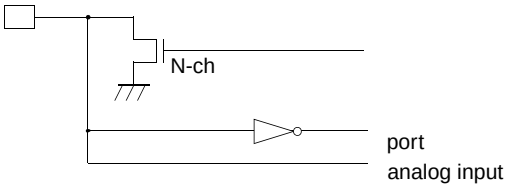
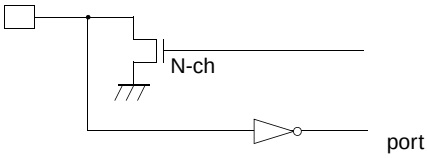
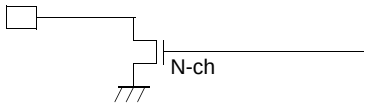
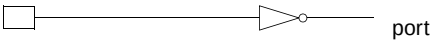
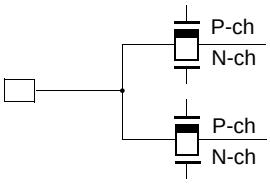
*2: MQP-64C-P01

## ■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|---|---|---|
| A |  | • Main/Sub-clock circuit<br>• Oscillation feedback resistance is approx. 500 kΩ for main clock circuit and 5 MΩ for sub-clock circuit. |
| B |  | • Hysteresis input<br>• The pull-down resistor (not available in MB89P485/P485L) Approx. 50 kΩ |
| C |  | • The pull-up resistor (P-channel) Approx. 50 kΩ<br>• Hysteresis input |
| D |  | • CMOS output<br>• CMOS input<br>• Hysteresis input<br>• Selectable pull-up resistor Approx. 50 kΩ |
| E |  | • CMOS output<br>• CMOS input<br>• Selectable pull-up resistor Approx. 50 kΩ |

*(Continued)*

*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| F |  | • N-ch open-drain output<br>• CMOS input<br>• Hysteresis input |
| G |  | • N-ch open-drain output<br>• CMOS input<br>• Analog input |
| H |  | • N-ch open-drain output<br>• CMOS input |
| I |  | • N-ch open-drain output |
| J |  | • CMOS input |
| K |  | • LCD segment output |

## ■ HANDLING DEVICES

### 1. Preventing Latch-up

Latch-up may occur on CMOS IC if voltage higher than $V_{CC}$ or lower than $V_{SS}$ is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in ■ ELECTRICAL CHARACTERISTICS is applied between $V_{CC}$ and $V_{SS}$.

When latch-up occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply ($AV_{CC}$) and analog input from exceeding the digital power supply ($V_{CC}$) when the analog system power supply is turned on and off.

### 2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

### 3. Treatment of Power Supply Pins on Microcontrollers with A/DConverter

Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = V_{SS}$ even if the A/D converter is not in use.

### 4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

### 5. Power Supply Voltage Fluctuations

Although $V_{CC}$ power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that $V_{CC}$ ripple fluctuations (P-P value) will be less than 10% of the standard $V_{CC}$ value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

### 6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset and wake-up from stop mode.

### 7. Notes on noise in the External Reset Pin ($\overline{RST}$)

If the reset pulse applied to the external reset pin ($\overline{RST}$) does not meet the specifications, it may cause malfunctions. Use caution so that the reset pulse less than the specifications will not be fed to the external reset pin ($\overline{RST}$).

## ■ PROGRAMMING OTPROM IN MB89P485/P485L WITH SERIAL PROGRAMMER

### 1. Programming the OTPROM with Serial Programmer

- All OTP products can be programmed with serial programmer.

### 2. Programming the OTPROM

- To program the OTPROM using FUJITSU MCU programmer MB91919-001.

Inquiry : Fujitsu Microelectronics Asia Pte Ltd. :TEL (65)-2810770
FAX (65)-2810220

### 3. Programming Adapter for OTPROM

- To program the OTPROM using FUJITSU MCU programmer MB91919-001, use the programming adapter listed below.

| Package | Compatible socket adapter |
|---|---|
| DIP-64P-M01 | MB91919-812 |
| FPT-64P-M09 | MB91919-813 |

Inquiry : Fujitsu Microelectronics Asia Pte Ltd. : TEL (65)-2810770
FAX (65)-2810220

### 4. OTPROM Content Protection

For product with OTPROM content protection feature (MB89P485/P485L-103, MB89P485/P485L-104), OTPROM content can be read using serial programmer if the OTPROM content protection mechanism is not activated.

One predefined area of the OTPROM ($FFFC_H$) is assigned to be used for preventing the read access of OTPROM content. If the protection code "$00_H$" is written in this address ($FFFC_H$), the OTPROM content cannot be read by any serial programmer.

Note: The program written into the OTPROM cannot be verified once the OTPROM protection code is written ("$00_H$" in $FFFC_H$). It is advised to write the OTPROM protection code at last.

### 5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

## ■ PROGRAMMING OTPROM IN MB89P485/P485L WITH PARALLEL PROGRAMMER

### 1. Programming OTPROM with Parallel Programmer

- Only products without protection feature (i.e. MB89P485/P485L-101 and MB89P485/P485L-102) can be programmed with parallel programmer. Product with protection feature (i.e. MB89P485/P485L-103 and MB89P485/P485L-104) cannot be programmed with parallel programmer.

### 2. ROM Writer Adapters and Recommended ROM Writers

- The following shows ROM writer adapters and recommended ROM writers.

Ando Electric Co., Ltd. (Parallel programmer)

| Package name | Applicable adapter model | Recommended writer |
|---|---|---|
| DIP-64P-M01 | ROM2-64SD-32DP-8LA2 | AF9708*<br>AF9709*<br>AF9723* |
| FPT-64P-M09 | ROM2-64QF2-32DP-8LA3 | |

* : For the programmer and the version of the programmer, contact the Flash Support Group, Inc.

Fujitsu Microelectronics Asia Pte Ltd. (Serial programmer)

| Package name | Applicable adapter model | Recommended writer |
|---|---|---|
| DIP-64P-M01 | MB91919-604 | MB91919-001 |
| FPT-64P-M09 | MB91919-605 | |

Inquiries : Fujitsu Microelectronics Asia Pte Ltd. : TEL (65)-2810770
Sunhayato Corp. : TEL 81-(3)-3986-7791
: FAX 81-(3)-3971-0535
E-mail : adapter@sunhayato.co.jp
Flash Support Group, Inc : FAX 81-(53)-428-8377
E-mail : support@j-fsg.co.jp

### 3. Writing Data to the OTPROM using Writer from Minato Electronics Co., Ltd.

(1) Set the OTPROM writer for the CU50-OTP (device code: cdB6DC).

(2) Load the program data to the OTPROM writer.

(3) Write data using the OTPROM writer.

### 4. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

## ■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

### 1. EPROM for Use

MBM27C256A-20TVM

### 2. Programming Socket Adapter

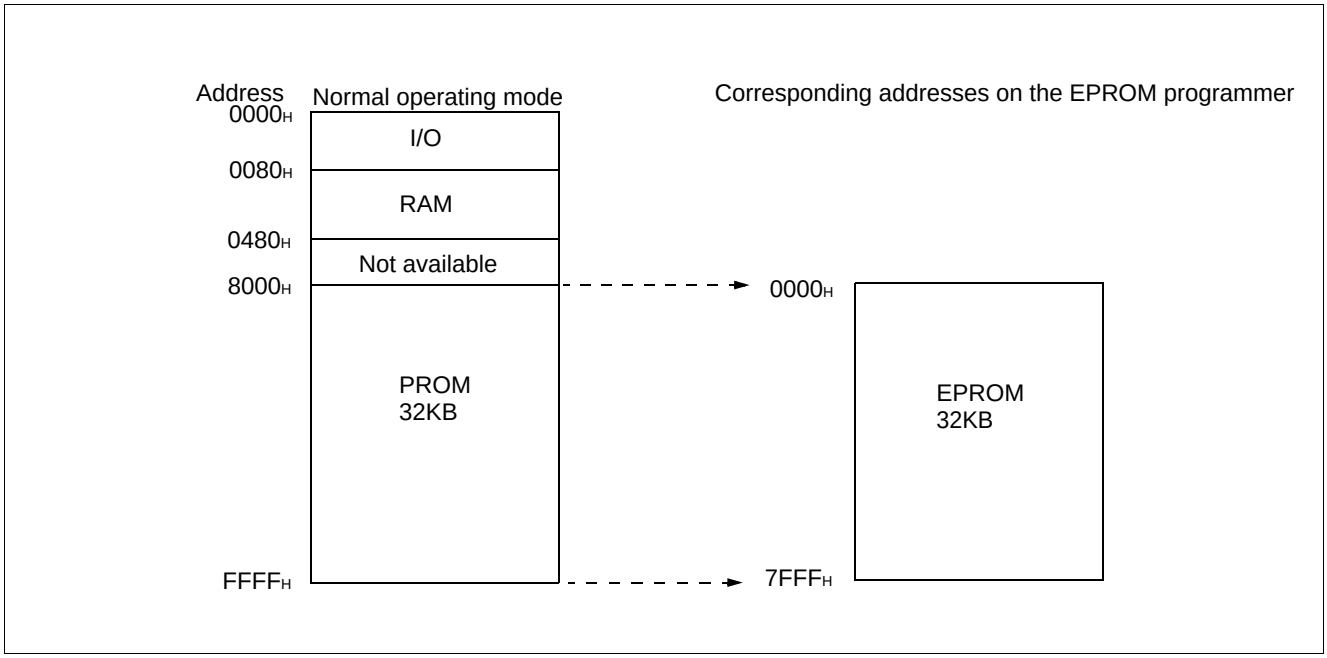
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

| Package | Adapter socket part number |
|---|---|
| LCC-32 (Rectangle) | ROM-32LC-28DP-S |

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3986-0403

### 3. Memory Space

Memory space in each mode is shown in the diagram below.



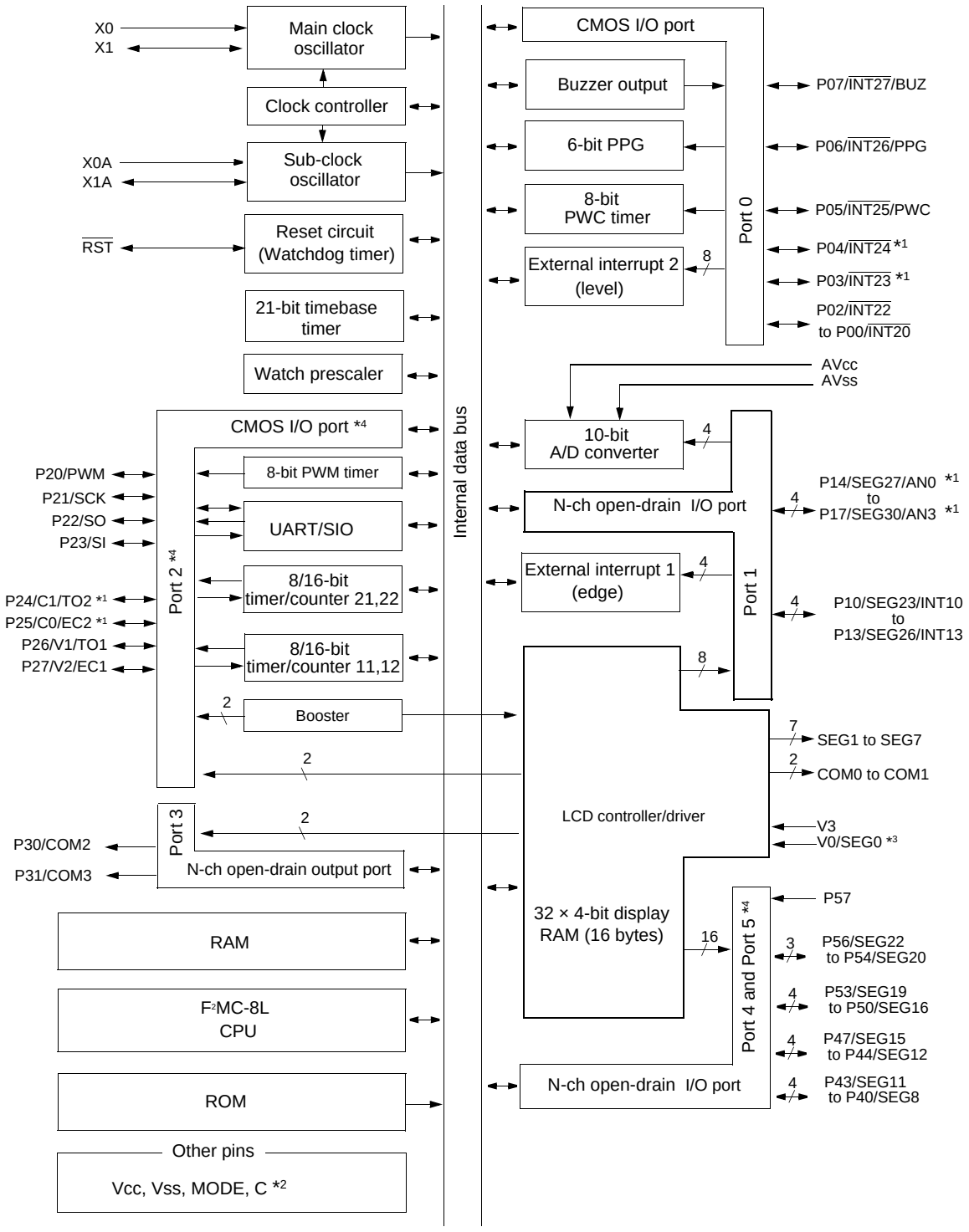

### 4. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C256.

(2) Load program data into the EPROM programmer at $0000_H$ to $7FFF_H$.

(3) Program to $0000_H$ to $7FFF_H$ with the EPROM programmer.

## ■ BLOCK DIAGRAM




*1: If booster is selected, EC2 and TO2 will be redirected to P03/$\overline{\text{INT23}}$ and P04/$\overline{\text{INT24}}$ respectively. Segment output of P14/SEG27/AN0 to P17/SEG30/AN3 will be disabled.

*2: For product other than MB89P485, C pin is NC pin.

*3: If booster is selected, it serves as V0. If booster is not selected, it serves as SEG0.

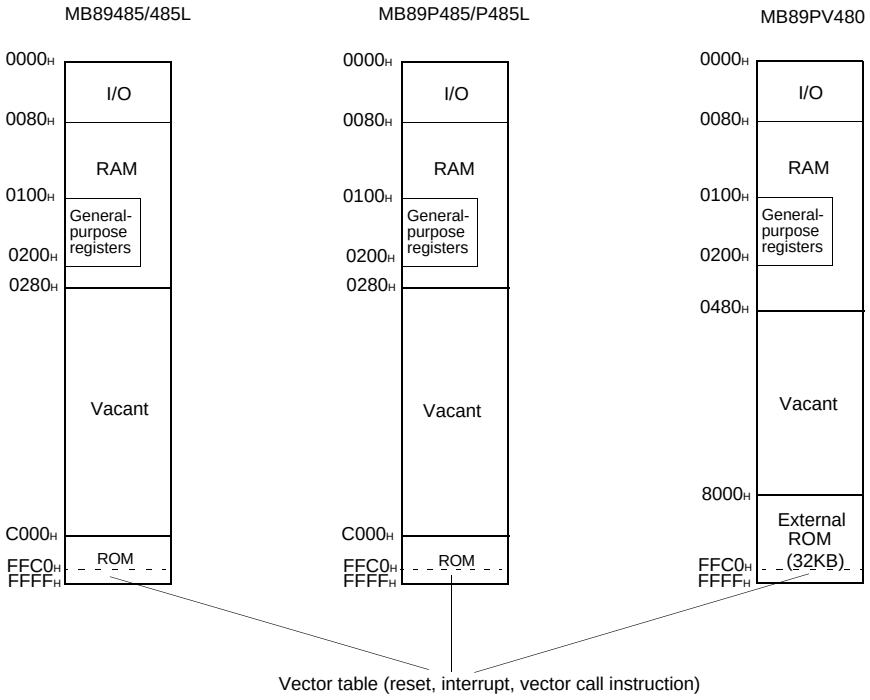
*4: P20 to P23 are CMOS I/O ports. P24 to P27 are N-ch open-drain I/O ports. P57 is input-only port.

## ■ CPU CORE

### 1. Memory Space

The microcontrollers of the MB89480 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89480 series is structured as illustrated below.

**Memory Space**



## 2. Registers

The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following registers are provided:

Program counter (PC) : A 16-bit register for indicating instruction storage positions.

Accumulator (A) : A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.

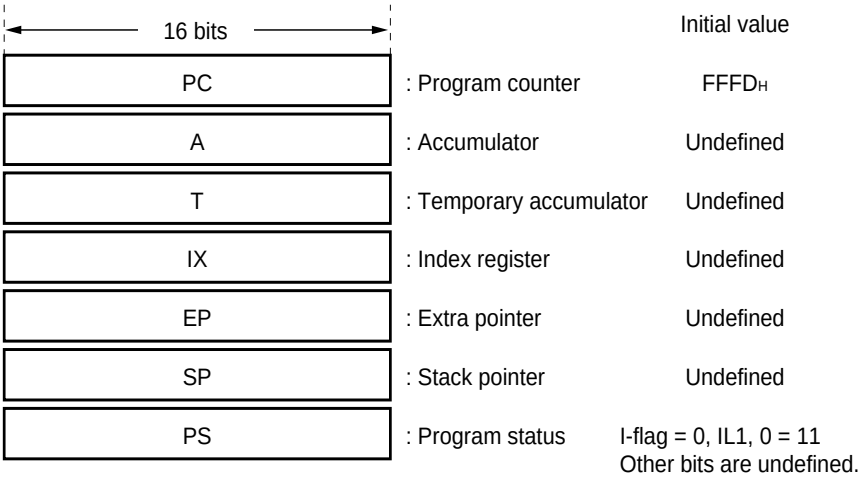
Temporary accumulator (T) : A 16-bit register for performing arithmetic operations with the accumulator. When the instruction is an 8-bit data processing instruction, the lower byte is used.

Index register (IX) : A 16-bit register for index modification.

Extra pointer (EP) : A 16-bit pointer for indicating a memory address.

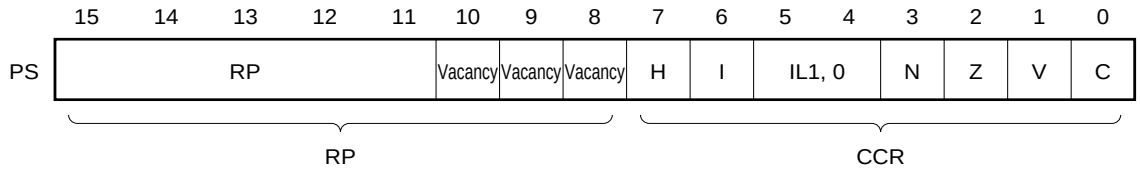
Stack pointer (SP) : A 16-bit register for indicating a stack area.

Program status (PS) : A 16-bit register for storing a register pointer, a condition code.



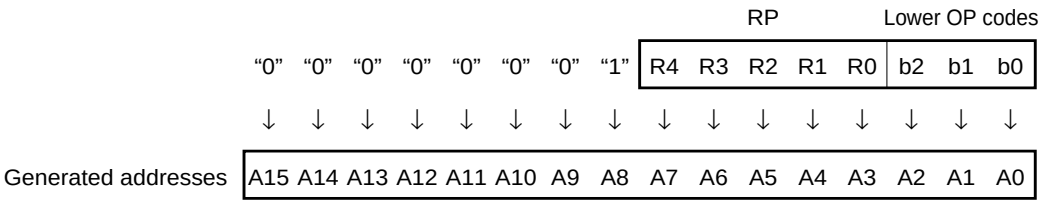

The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

**Structure of the Program Status Register**



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

**Rule for Conversion of Actual Addresses of the General-purpose Register Area**




The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag : Set to "1" when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Clear to "0" otherwise. This flag is for decimal adjustment instructions.

I-flag : Interrupt is allowed when this flag is set to "1". Interrupt is prohibited when the flag is set to "0". Clear to "0" when reset.

IL1, 0 : Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

| IL1 | IL0 | Interrupt level | Priority |
|---|---|---|---|
| 0 | 0 | 1 | High |
| 0 | 1 | | |
| 1 | 0 | 2 | |
| 1 | 1 | 3 | Low = no interrupt |

N-flag : Set to "1" if the MSB is set to "1" as the result of an arithmetic operation. Clear to "0" otherwise.

Z-flag : Set to "1" when an arithmetic operation results in "0". Clear to "0" otherwise.

V-flag : Set to "1" if a signed numeric value overflows because of an arithmetic calculation. Clear to "0" if the overflow does not occur.

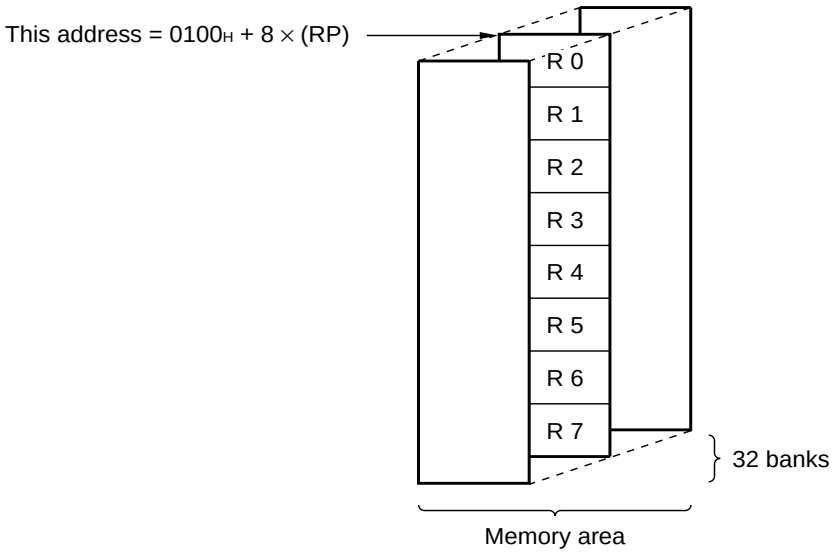
C-flag : Set to "1" when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Clear to "0" otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers. Up to a total of 32 banks can be used on the MB89480 series. The bank currently in use is indicated by the register bank pointer (RP).

**Register Bank Configuration**



## ■ I/O MAP

| Address | Register name | Register description | Read/Write | Initial value |
|---|---|---|---|---|
| $00_H$ | PDR0 | Port 0 data register | R/W | $XXXXXXXX_B$ |
| $01_H$ | DDR0 | Port 0 data direction register | W* | $00000000_B$ |
| $02_H$ | PDR1 | Port 1 data register | R/W | $XXXXXXXX_B$ |
| $03_H$ | DDR1 | Port 1 data direction register | W* | $00000000_B$ |
| $04_H$ | PDR2 | Port 2 data register | R/W | $00000000_B$ |
| $05_H$ | (Reserved) | | | |
| $06_H$ | DDR2 | Port 2 data direction register | R/W | $00000000_B$ |
| $07_H$ | SYCC | System clock control register | R/W | $X\text{-}1MM100_B$ |
| $08_H$ | STBC | Standby control register | R/W | $00010XXX_B$ |
| $09_H$ | WDTC | Watchdog timer control register | W* | $0\text{---}XXXX_B$ |
| $0A_H$ | TBTC | Timebase timer control register | R/W | $00\text{---}000_B$ |
| $0B_H$ | WPCR | Watch prescaler control register | R/W | $00\text{--}0000_B$ |
| $0C_H$ | PDR3 | Port 3 data register | R/W | $\text{------}11_B$ |
| $0D_H$ | (Reserved) | | | |
| $0E_H$ | RSFR | Reset flag register | R | $XXXX\text{----}_B$ |
| $0F_H$ | (Reserved) | | | |
| $10_H$ | PDR4 | Port 4 data register | R/W | $11111111_B$ |
| $11_H$ | (Reserved) | | | |
| $12_H$ | PDR5 | Port 5 data register | R/W | $X1111111_B$ |
| $13_H$ to $1F_H$ | (Reserved) | | | |
| $20_H$ | SMC1 | UART/SIO mode control register 1 | R/W | $00000000_B$ |
| $21_H$ | SMC2 | UART/SIO mode control register 2 | R/W | $00000000_B$ |
| $22_H$ | SRC | UART/SIO rate control register | R/W | $XXXXXXXX_B$ |
| $23_H$ | SSD | UART/SIO status/data register | R | $00001\text{---}_B$ |
| $24_H$ | SIDR/SODR | UART/SIO data register | R/W | $XXXXXXXX_B$ |
| $25_H$ | EIC1 | External interrupt 1 control register 1 | R/W | $00000000_B$ |
| $26_H$ | EIC2 | External interrupt 1 control register 2 | R/W | $00000000_B$ |
| $27_H$ | EIE2 | External interrupt 2 enable register | R/W | $00000000_B$ |
| $28_H$ | EIF2 | External interrupt 2 flag register | R/W | $\text{-------}0_B$ |
| $29_H$ to $2B_H$ | (Reserved) | | | |
| $2C_H$ | ADC1 | A/D control register 1 | R/W | $\text{-}0000000_B$ |
| $2D_H$ | ADC2 | A/D control register 2 | R/W | $\text{-}0000001_B$ |
| $2E_H$ | ADDH | A/D data register (Upper byte) | R | $\text{------}XX_B$ |
| $2F_H$ | ADDL | A/D data register (Lower byte) | R | $XXXXXXXX_B$ |
| $30_H$ | ADEN | A/D input enable register | R/W | $1111\text{----}_B$ |
| $31_H$ | PCR1 | PWC control register 1 | R/W | $0\text{-}0\text{--}000_B$ |
| $32_H$ | PCR2 | PWC control register 2 | R/W | $00000000_B$ |
| $33_H$ | PLBR | PWC reload buffer register | R/W | $XXXXXXXX_B$ |

*(Continued)*

*(Continued)*

| Address | Register name | Register description | Read/Write | Initial value |
|---|---|---|---|---|
| $34_H$ | CNTR | PWM timer control register | R/W | $0\text{-}000000_B$ |
| $35_H$ | COMR | PWM timer compare register | W* | $XXXXXXXX_B$ |
| $36_H$ | T22CR | Timer 22 control register | R/W | $000000X0_B$ |
| $37_H$ | T21CR | Timer 21 control register | R/W | $000000X0_B$ |
| $38_H$ | T22DR | Timer 22 data register | R/W | $XXXXXXXX_B$ |
| $39_H$ | T21DR | Timer 21 data register | R/W | $XXXXXXXX_B$ |
| $3A_H$ | T12CR | Timer 12 control register | R/W | $000000X0_B$ |
| $3B_H$ | T11CR | Timer 11 control register | R/W | $000000X0_B$ |
| $3C_H$ | T12DR | Timer 12 data register | R/W | $XXXXXXXX_B$ |
| $3D_H$ | T11DR | Timer 11 data register | R/W | $XXXXXXXX_B$ |
| $3E_H$ | PPGC1 | PPG control register 1 | R/W | $00000000_B$ |
| $3F_H$ | PPGC2 | PPG control register 2 | R/W | $0\text{-}000000_B$ |
| $40_H$ | BUZR | Buzzer control register | R/W | $-----000_B$ |
| $41_H$ to $5D_H$ | (Reserved) | | | |
| $5E_H$ | LCR1 | LCD controller control register 1 | R/W | $00010000_B$ |
| $5F_H$ | LCR2 | LCD controller control register 2 | R/W | $-0000000_B$ |
| $60_H$ to $6F_H$ | VRAM | LCD data RAM | R/W | $XXXXXXXX_B$ |
| $70_H$ | PURC0 | Port 0 pull up resistor control register | R/W | $11111111_B$ |
| $71_H$ | (Reserved) | | | |
| $72_H$ | PURC2 | Port 2 pull up resistor control register | R/W | $----1111_B$ |
| $73_H$ to $7A_H$ | (Reserved) | | | |
| $7B_H$ | ILR1 | Interrupt level setting register 1 | W* | $11111111_B$ |
| $7C_H$ | ILR2 | Interrupt level setting register 2 | W* | $11111111_B$ |
| $7D_H$ | ILR3 | Interrupt level setting register 3 | W* | $11111111_B$ |
| $7E_H$ | ILR4 | Interrupt level setting register 4 | W* | $11111111_B$ |
| $7F_H$ | (Reserved) | | | |

* : Bit manipulation instruction cannot be used.

- **Read/write access symbols**

  R/W : Readable and writable
  R : Read-only
  W : Write-only

- **Initial value symbols**

  0 : The initial value of this bit is “0”.
  1 : The initial value of this bit is “1”.
  X : The initial value of this bit is undefined.
  - : Unused bit.
  M : The initial value of this bit is determined by mask option.

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

($AV_{SS} = V_{SS} = 0.0$ V)

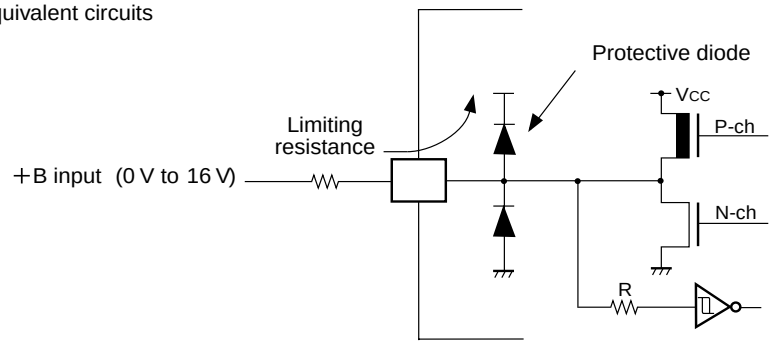
| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage | $V_{CC}$<br>$AV_{CC}$ | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V | MB89PV480, MB89P485, MB89485<br>$AV_{CC}$ must not exceed $V_{CC}$ |
| | $V_{CC}$<br>$AV_{CC}$ | $V_{SS} - 0.3$ | $V_{SS} + 4.0$ | V | MB89P485L, MB89485L<br>$AV_{CC}$ must not exceed $V_{CC}$ |
| LCD power supply voltage | V0 to V3 | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V | |
| Input voltage | $V_I$ | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V | P00 to P07, P10 to P17, P20 to P27, P40 to P47, P50 to P57 |
| Output voltage | $V_O$ | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V | P00 to P07, P10 to P17, P20 to P27, P30 to P31, P40 to P47, P50 to P56 |
| Maximum clamp current | $I_{CLAMP}$ | – 2.0 | + 2.0 | mA | * |
| Total maximum clamp current | $\sum \lvert I_{CLAMP} \rvert$ | — | 20 | mA | * |
| “L” level maximum output current | $I_{OL}$ | — | 15 | mA | |
| “L” level average output current | $I_{OLAV}$ | — | 4 | mA | Average value (operating current × operating rate) |
| “L” level total maximum output current | $\sum I_{OL}$ | — | 100 | mA | |
| “L” level total average output current | $\sum I_{OLAV}$ | — | 40 | mA | Average value (operating current × operating rate) |
| “H” level maximum output current | $I_{OH}$ | — | –15 | mA | |
| “H” level average output current | $I_{OHAV}$ | — | –4 | mA | Average value (operating current × operating rate) |
| “H” level total maximum output current | $\sum I_{OH}$ | — | –50 | mA | |
| “H” level total average output current | $\sum I_{OHAV}$ | — | –20 | mA | Average value (operating current × operating rate) |
| Power consumption | $P_D$ | — | 300 | mW | |
| Operating temperature | $T_A$ | –40 | +85 | °C | |
| Storage temperature | Tstg | –55 | +150 | °C | |

Precautions: Permanent device damage may occur if the above “Absolute Maximum Ratings” are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* :
- Applicable to pins: P00 to P07, P20 to P23, AN0 to AN3
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.

- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the Vcc pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller current is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on result.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannnot accept +B signal input.
- Sample recommended circuits :

▪ Input/Output Equivalent circuits




WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

($AV_{SS}$ = $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks | |
|---|---|---|---|---|---|---|
| | | Min | Max | | | |
| Power supply voltage | $V_{CC}$ $AV_{CC}$ | 2.2* | 5.5 | V | Operation assurance range | MB89485 |
| | | 3.5* | 5.5 | V | Operation assurance range | MB89P485 |
| | | 2.7* | 5.5 | V | Operation assurance range | MB89PV480 |
| | | 1.5 | 5.5 | V | Retains the RAM state in stop mode | MB89485, MB89P485, MB89PV480 |
| | | 2.2* | 3.6 | V | Operation assurance range | MB89485L, MB89P485L |
| | | 1.5 | 3.6 | V | Retains the RAM state in stop mode | |
| LCD power supply voltage | V0 to V3 | Vss | Vcc | V | | |
| Operating temperature | $T_A$ | –40 | +85 | °C | | |

* : These values depend on the operating conditions and the analog assurance range. See Figure 1, 2, 3 and "5. A/D Converter Electrical Characteristics."

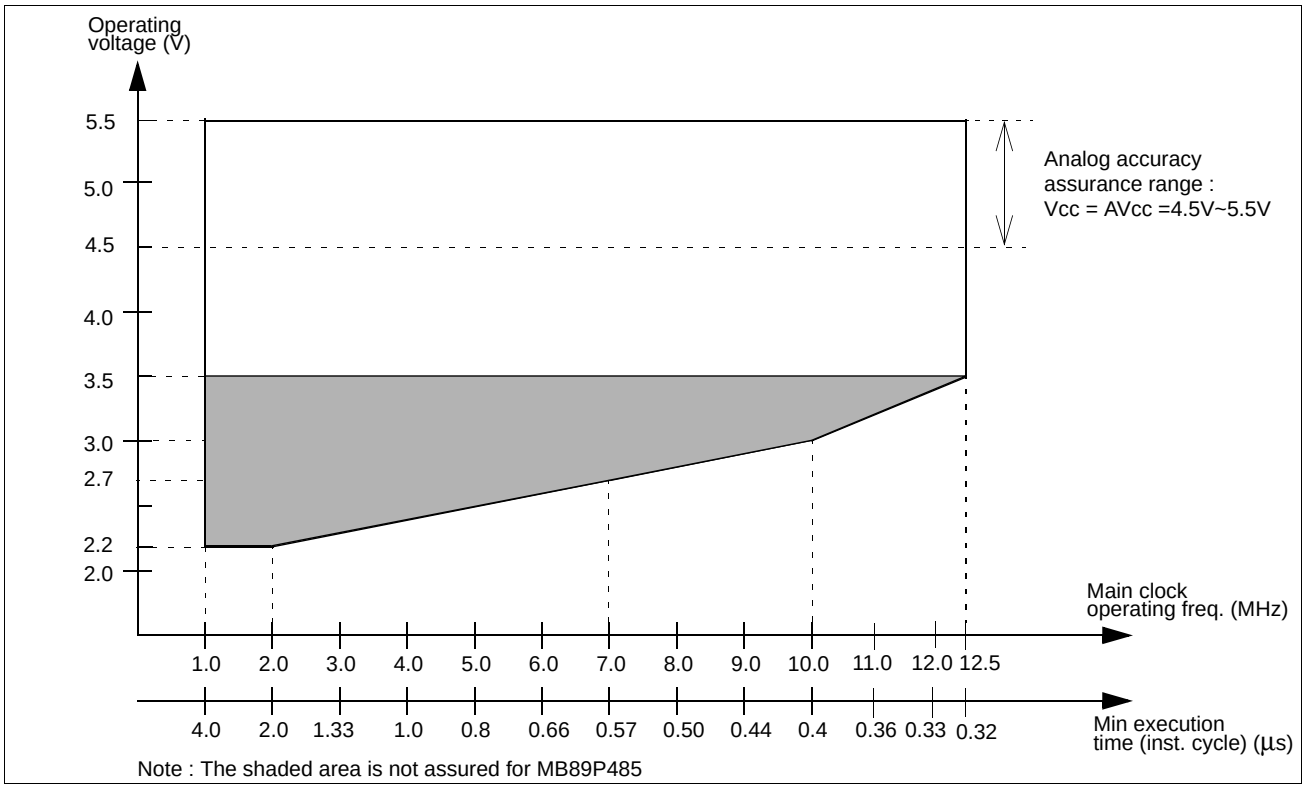



**Figure 1 Operating Voltage vs. Main Clock Operating Frequency (MB89P485/485)**

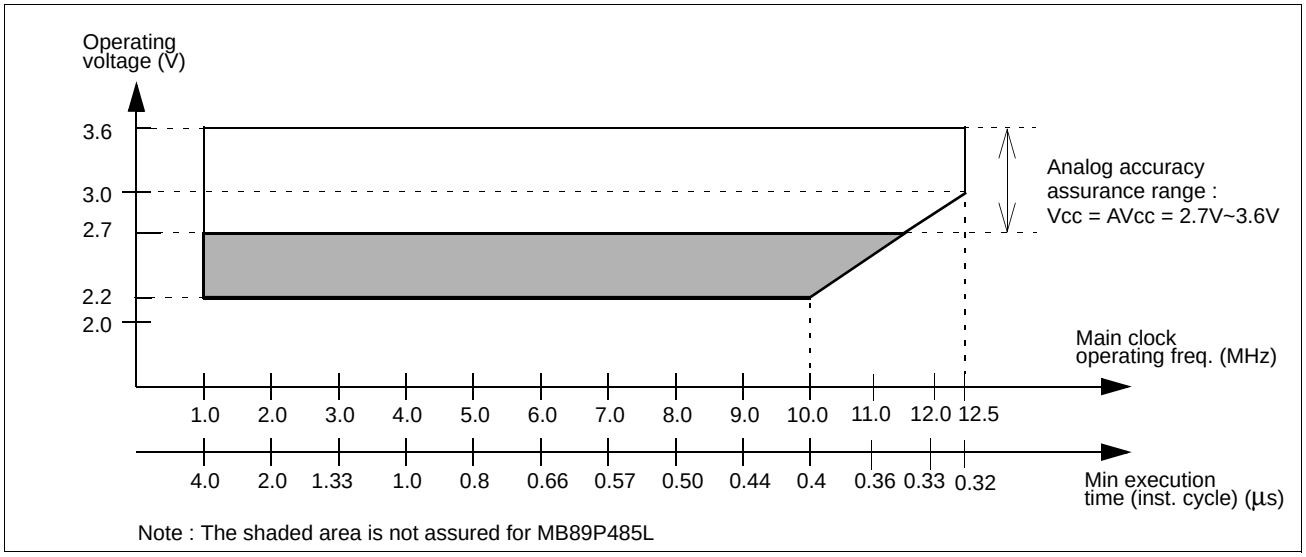



**Figure 2 Operating Voltage vs. Main Clock Operating Frequency (MB89P485L/485L)**

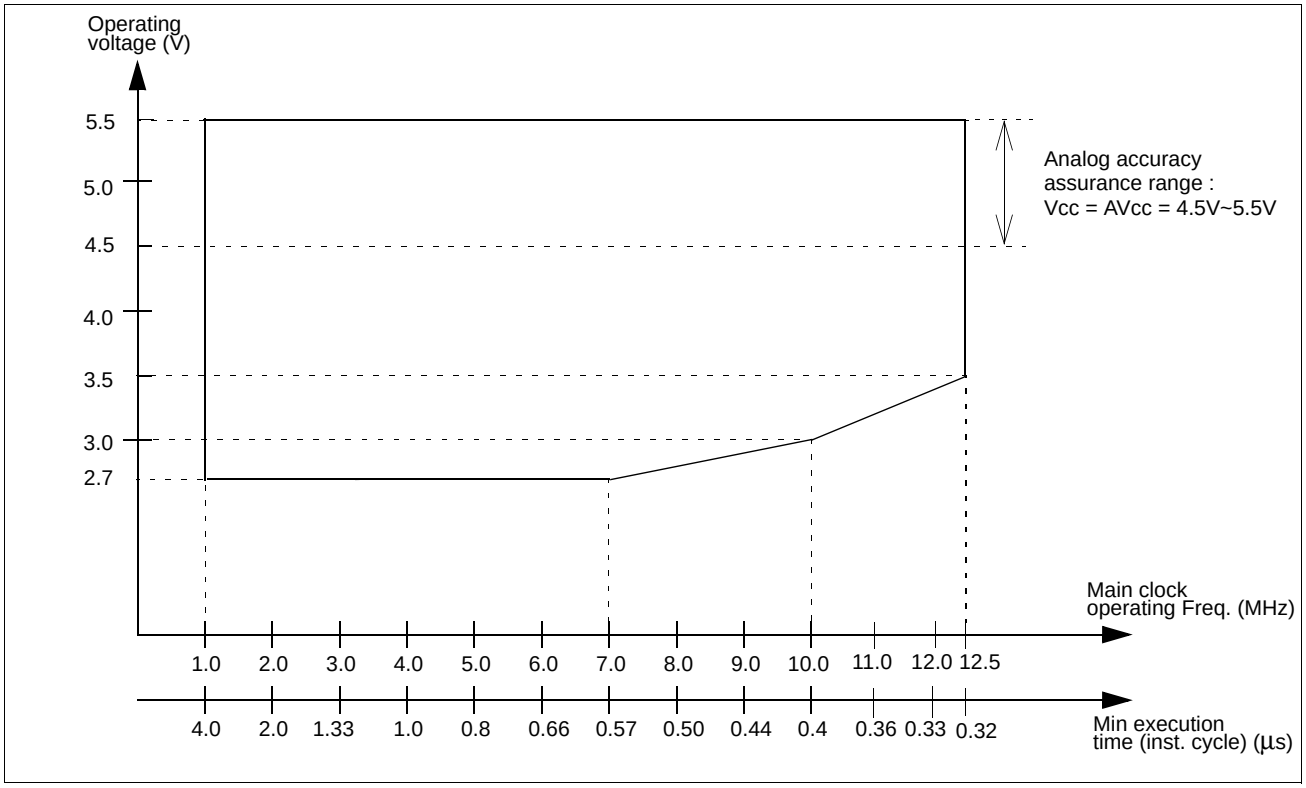



**Figure 3 Operating Voltage vs. Main Clock Operating Frequency (MB89PV480)**

Figure 1, 2 and 3 indicate the operating frequency of the external oscillator at an instruction cycle of $4/F_{CH}$.

Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

### 3. DC Characteristics

($AV_{CC} = V_{CC} = 5.0$ V for MB89PV480, MB89P485, MB89485, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)
$AV_{CC} = V_{CC} = 3.0$ V for MB89P485L, MB89485L, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level input voltage | $V_{IH}$ | P00 to P07, P10 to P17, P20 to P27, P40 to P47, P50 to P57 | — | 0.7 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | |
| | $V_{IHS}$ | $\overline{RST}$, MODE, EC1, EC2, PWC, SCK, SI, INT10 to INT13, $\overline{INT20}$ to $\overline{INT27}$ | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | |
| "L" level input voltage | $V_{IL}$ | P00 to P07, P10 to P17, P20 to P27, P40 to P47, P50 to P57 | — | $V_{SS}$ – 0.3 | — | 0.3 $V_{CC}$ | V | |
| | $V_{ILS}$ | $\overline{RST}$, MODE, EC1, EC2, PWC, SCK, SI, INT10 to INT13, $\overline{INT20}$ to $\overline{INT27}$ | — | $V_{SS}$ – 0.3 | — | 0.2 $V_{CC}$ | V | |
| Open-drain output pin application voltage | $V_D$ | P10 to P17, P24 to P27, P30 to P31, P40 to P47, P50 to P56 | — | $V_{SS}$ – 0.3 | — | $V_{CC}$ + 0.3 | V | Product without booster |
| | | | | | | V3 | | Product with booster |
| "H" level output voltage | $V_{OH}$ | P00 to P07, P20 to P23 | $I_{OH}$ = –2.0 mA | 4.0 | — | — | V | MB89PV480, MB89P485, MB89485 |
| | | | | 2.2 | — | — | V | MB89P485L, MB89485L |
| "L" level output voltage | $V_{OL}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P31, P40 to P47, P50 to P56, $\overline{RST}$ | $I_{OL}$ = 4.0 mA | — | — | 0.4 | V | MB89PV480, MB89P485, MB89485 |
| | | P00 to P07, P20 to P23, $\overline{RST}$ | | — | — | 0.4 | V | MB89P485L, MB89485L |
| | | P10 to P17, P24 to P27, P30 to P31, P40 to P47, P50 to P56 | $I_{OL}$ = 2.0 mA | — | — | 0.4 | V | MB89P485L, MB89485L |

*(Continued)*

*(Continued)*

($AV_{CC}$ = $V_{CC}$ = 5.0 V for MB89PV480, MB89P485, MB89485, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)
$AV_{CC}$ = $V_{CC}$ = 3.0 V for MB89P485L, MB89485L, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input leakage current | $I_{LI}$ | P00 to P07, P10 to P17, P20 to P27, P40 to P47, P50 to P57 | 0.45 V < $V_I$ < $V_{CC}$ | –5 | — | +5 | µA | Without pull-up resistor |
| Open-drain output leakage current | $I_{LOD}$ | P10 to P17, P24 to P27, P30 to P31, P40 to P47, P50 to P56 | 0.45 V < $V_I$ < $V_{CC}$ | –5 | — | +5 | µA | |
| Pull-down resistance | $R_{DOWN}$ | MODE | $V_I$ = $V_{CC}$ | 25 | 50 | 100 | kΩ | Except MB89P485, MB89P485L |
| Pull-up resistance | $R_{PULL}$ | P00 to P07, P20 to P23, $\overline{RST}$ | $V_I$ = 0.0 V | 25 | 50 | 100 | kΩ | When pull-up resistor is selected (except $\overline{RST}$) |
| Power supply current | $I_{CC1}$ | $V_{CC}$ | $F_{CH}$ = 10 MHz, $t_{inst}$ = 0.4 µs, Main clock run mode | — | 6 | 13 | mA | MB89485 |
| | | | | — | 3 | 7 | | MB89485L |
| | | | | — | 5 | 10 | | MB89P485 |
| | | | | — | 4 | 8 | | MB89P485L |
| | $I_{CC2}$ | | $F_{CH}$ = 10 MHz, $t_{inst}$ = 6.4 µs, Main clock run mode | — | 0.9 | 3 | mA | MB89485 |
| | | | | — | 0.4 | 1.5 | | MB89485L |
| | | | | — | 0.9 | 3 | | MB89P485 |
| | | | | — | 0.5 | 2 | | MB89P485L |
| | $I_{CCS1}$ | | $F_{CH}$ = 10 MHz, $t_{inst}$ = 0.4 µs, Main clock sleep mode | — | 2 | 5 | mA | MB89485 |
| | | | | — | 1 | 2.5 | | MB89485L |
| | | | | — | 2.5 | 5 | | MB89P485 |
| | | | | — | 1.2 | 2.5 | | MB89P485L |
| | $I_{CCS2}$ | | $F_{CH}$ = 10 MHz, $t_{inst}$ = 6.4 µs, Main clock sleep mode | — | 0.7 | 2 | mA | MB89485 |
| | | | | — | 0.3 | 1 | | MB89485L |
| | | | | — | 0.9 | 2 | | MB89P485 |
| | | | | — | 0.4 | 1 | | MB89P485L |
| | $I_{CCL}$ | | $F_{CL}$ = 32.768 kHz, $T_A$ = +25°C, Sub-clock run mode | — | 40 | 85 | µA | MB89485 |
| | | | | — | 22 | 50 | | MB89485L |
| | | | | — | 400 | 800 | | MB89P485 |
| | | | | — | 25 | 50 | | MB89P485L |

*(Continued)*

($AV_{CC}$ = $V_{CC}$ = 5.0 V for MB89PV480, MB89P485, MB89485, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)
$AV_{CC}$ = $V_{CC}$ = 3.0 V for MB89P485L, MB89485L, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current | $I_{CCLS}$ | $V_{CC}$ | $F_{CL}$ = 32.768 kHz, $T_A$ = +25°C, Sub-clock sleep mode | — | 15 | 30 | µA | MB89485 |
| | | | | — | 7 | 15 | | MB89485L |
| | | | | — | 12 | 30 | | MB89P485 |
| | | | | — | 7 | 15 | | MB89P485L |
| | $I_{CCT}$ | | $T_A$ = +25°C, Watch mode, Main clock stop mode | — | 2 | 10 | µA | MB89485 |
| | | | | — | 1 | 5 | | MB89485L |
| | | | | — | 5 | 15 | | MB89P485 |
| | | | | — | 1 | 5 | | MB89P485L |
| | $I_{CCH}$ | | $T_A$ = +25°C, Sub-clock stop mode | — | 1 | 5 | µA | MB89485 |
| | | | | — | 0.8 | 4 | | MB89485L |
| | | | | — | 3 | 10 | | MB89P485 |
| | | | | — | 0.8 | 4 | | MB89P485L |
| | $I_A$ | $AV_{CC}$ | A/D conversion active | — | 1.3 | 6 | mA | MB89485 |
| | | | | — | 1 | 3 | | MB89485L |
| | | | | — | 1.3 | 6 | | MB89P485 |
| | | | | — | 1 | 3 | | MB89P485L |
| | $I_{AH}$ | | $T_A$ = +25°C, A/D conversion stop | — | 1 | 5 | µA | MB89485 |
| | | | | — | 0.8 | 4 | | MB89485L |
| | | | | — | 1 | 5 | | MB89P485 |
| | | | | — | 0.8 | 4 | | MB89P485L |
| Common output impedance | $R_{VCOM}$ | COM0 to COM3 | V1 to V3 = +3.0 V | — | — | 2.5 | kΩ | MB89P485L, MB89485L |
| | | | V1 to V3 = +5.0 V | | | | | MB89PV480, MB89P485, MB89485 |
| Segment output impedance | $R_{VSEG}$ | SEG0 to SEG30 | V1 to V3 = +3.0 V | — | — | 15 | kΩ | MB89P485L, MB89485L |
| | | | V1 to V3 = +5.0 V | | | | | MB89PV480, MB89P485, MB89485 |
| LCD divided resistance | $R_{LCD}$ | — | Between $V_{CC}$ and $V_{SS}$ | 300 | 500 | 750 | kΩ | |

*(Continued)*

*(Continued)*

($AV_{CC}$ = $V_{CC}$ = 5.0 V for MB89PV480, MB89P485, MB89485, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)
$AV_{CC}$ = $V_{CC}$ = 3.0 V for MB89P485L, MB89485L, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| LCD controller/ driver leakage current | $I_{LCDL}$ | V0 to V3, COM0 to COM3, SEG0 to SEG30 | — | — | — | ±1 | µA | |
| Booster for LCD driving output voltage | $V_{V3}$ | V3 | V1 = 1.5 V | 4.3 | 4.5 | 4.7 | V | Products with booster only |
| | $V_{V2}$ | V2 | V1 = 1.5 V | 2.9 | 3.0 | 3.1 | V | |
| Reference input voltage for LCD driving | $V_{V1}$ | V1 | $I_{IN}$ = 0.0 µA | 1.4 | 1.5 | 1.7 | V | |
| Reference voltage input impedance | $R_{RIN}$ | V1 | — | 8.5 | 9.8 | 11 | kΩ | |
| Input capacitance | $C_{IN}$ | Other than $V_{CC}$, $V_{SS}$, $AV_{CC}$, $AV_{SS}$ | f = 1 MHz | — | 5 | 15 | pF | |

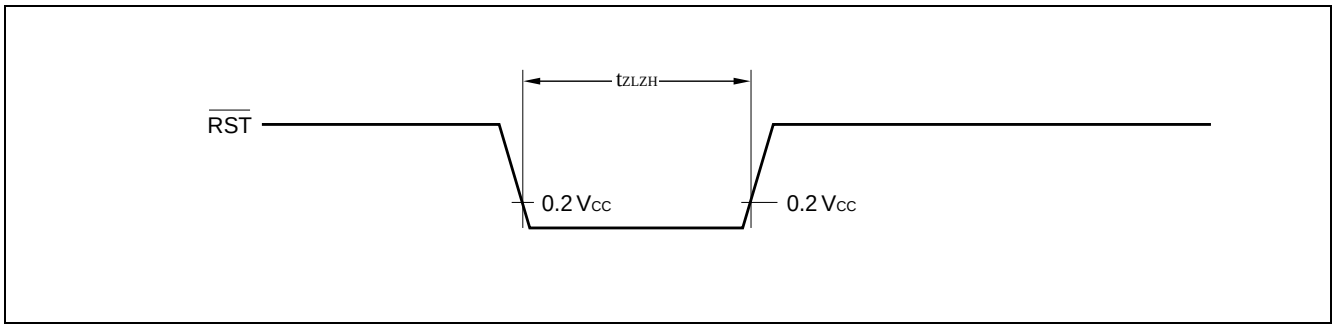
## 4. AC Characteristics

(1) Reset Timing

($AV_{CC} = V_{CC} = 5.0$ V for MB89PV480, MB89P485, MB89485, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)
$AV_{CC} = V_{CC} = 3.0$ V for MB89P485L, MB89485L, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| $\overline{RST}$ "L" pulse width | $t_{ZLZH}$ | — | 48 $t_{HCYL}$ | — | ns | |

Note : $t_{HCYL}$ is the oscillation cycle ($1/F_{CH}$) to input to the X0 pin.
The MCU operation is not guaranteed when the "L" pulse width is shorter than $t_{ZLZH}$.

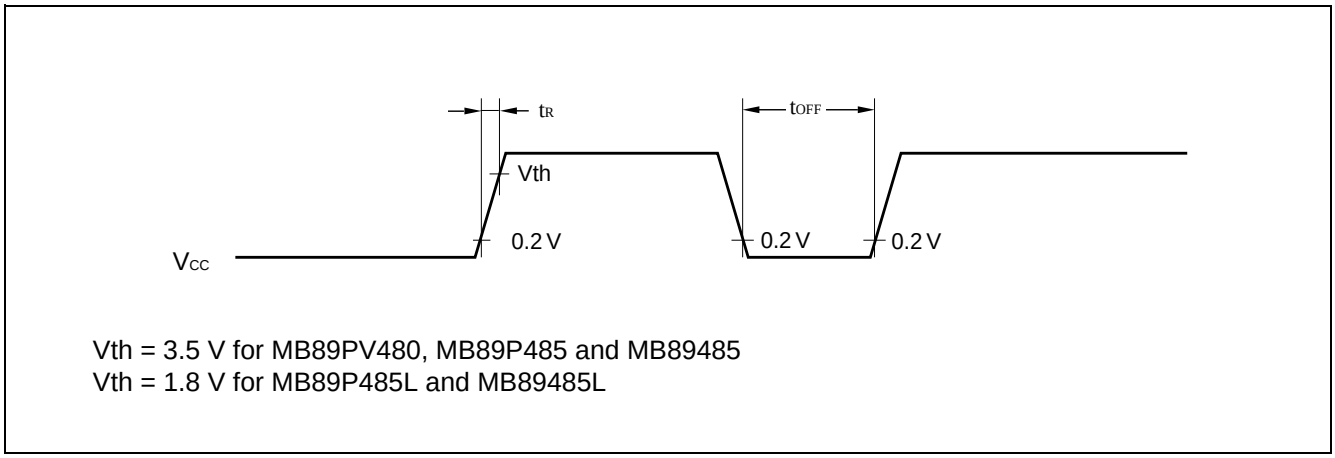



(2) Power-on Reset

($AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Power supply rising time | $t_R$ | — | — | 50 | ms | |
| Power supply cut-off time | $t_{OFF}$ | | 1 | — | ms | Due to repeated operations |

Note : Make sure that power supply rises within the selected oscillation stabilization time.
Rapid changes in power supply voltage may cause a power-on reset. If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.



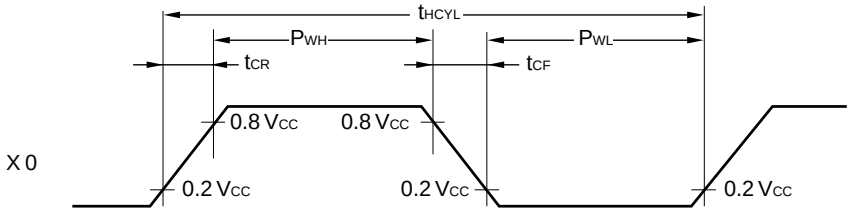

Vth = 3.5 V for MB89PV480, MB89P485 and MB89485
Vth = 1.8 V for MB89P485L and MB89485L

(3) Clock Timing

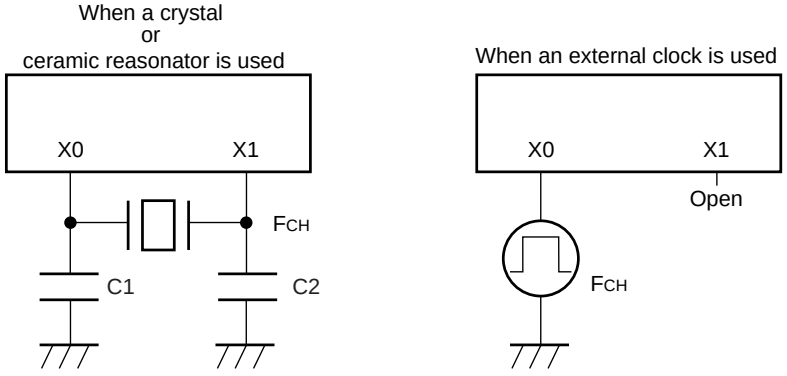
($AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Clock frequency | $F_{CH}$ | X0, X1 | 1 | — | 12.5 | MHz | |
| | $F_{CL}$ | X0A, X1A | — | 32.768 | — | kHz | |
| Clock cycle time | $t_{HCYL}$ | X0, X1 | 80 | — | 1000 | ns | |
| | $t_{LCYL}$ | X0A, X1A | — | 30.5 | — | µs | |
| Input clock pulse width | $P_{WH}$<br>$P_{WL}$ | X0 | 20 | — | — | ns | External clock |
| | $P_{WHL}$<br>$P_{WLL}$ | X0A | — | 15.2 | — | µs | |
| Input clock rising/falling time | $t_{CR}$<br>$t_{CF}$ | X0, X0A | — | — | 10 | ns | |

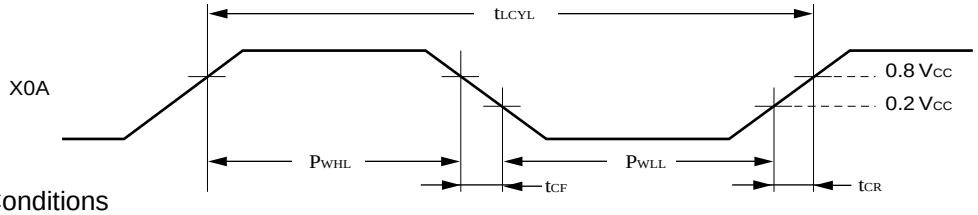
X0 and X1 Timing and Conditions




Main Clock Conditions

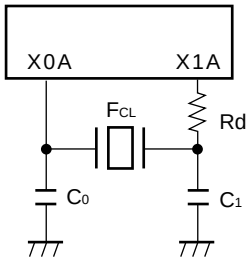


Sub-clock Timing and Conditions

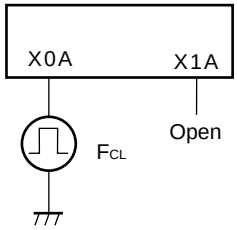



Sub-clock Conditions

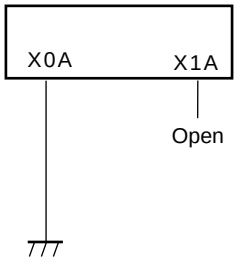
When a crystal or ceramic oscillator is used




When an external clock is used




When subclock is not used




(4) Instruction Cycle

| Parameter | Symbol | Value | Unit | Remarks |
|---|---|---|---|---|
| Instruction cycle (minimum execution time) | $t_{inst}$ | $4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$ | µs | $(4/F_{CH})t_{inst}$ = 0.32 µs when operating at $F_{CH}$ = 12.5 MHz |
| | | $2/F_{CL}$ | µs | $t_{inst}$ = 61.036 µs when operating at $F_{CL}$ = 32.768 kHz |

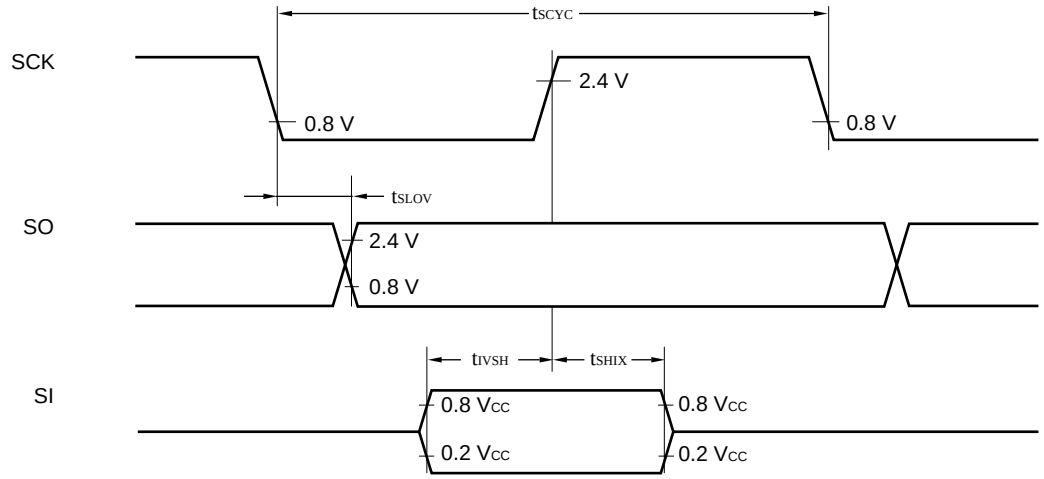
(5) Serial I/O Timing

($AV_{CC}$ = $V_{CC}$ = 5.0 V for MB89PV480, MB89P485, MB89485,
$AV_{CC}$ = $V_{CC}$ = 3.0 V for MB89P485L, MB89485L
$AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

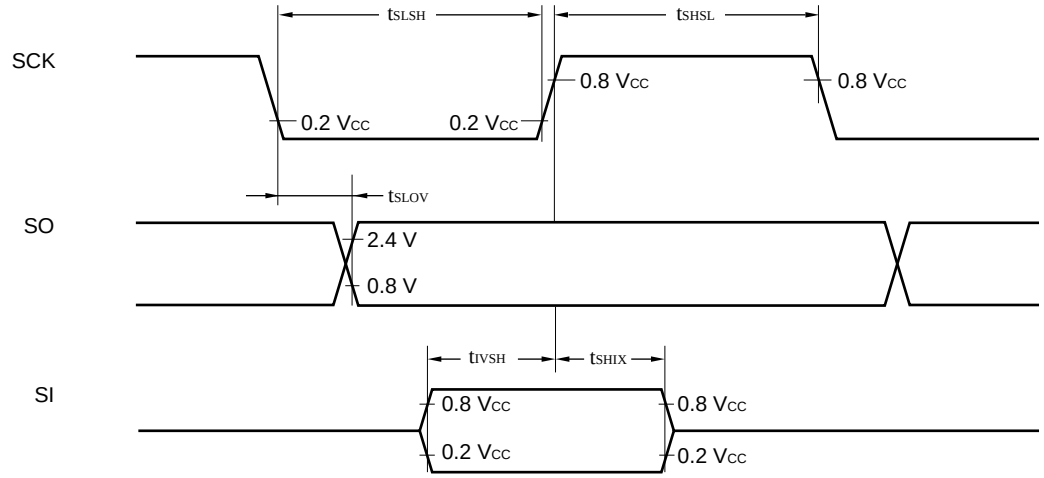
| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK | Internal shift clock mode | 2 $t_{inst}$* | — | µs |
| SCK ↓ → SO time | $t_{SLOV}$ | SCK, SO | | –200 | 200 | ns |
| Valid SI → SCK ↑ | $t_{IVSH}$ | SI, SCK | | 1/2 $t_{inst}$* | — | µs |
| SCK ↑ → valid SI hold time | $t_{SHIX}$ | SCK, SI | | 1/2 $t_{inst}$* | — | µs |
| Serial clock “H” pulse width | $t_{SHSL}$ | SCK | External shift clock mode | 1 $t_{inst}$* | — | µs |
| Serial clock “L” pulse width | $t_{SLSH}$ | | | 1 $t_{inst}$* | — | µs |
| SCK ↓ → SO time | $t_{SLOV}$ | SCK, SO | | 0 | 200 | ns |
| Valid SI → SCK ↑ | $t_{IVSH}$ | SI, SCK | | 1/2 $t_{inst}$* | — | µs |
| SCK ↑ → valid SI hold time | $t_{SHIX}$ | SCK, SI | | 1/2 $t_{inst}$* | — | µs |

* : For information on $t_{inst}$, see “(4) Instruction Cycle.”

Internal Clock Operation




External Clock Operation

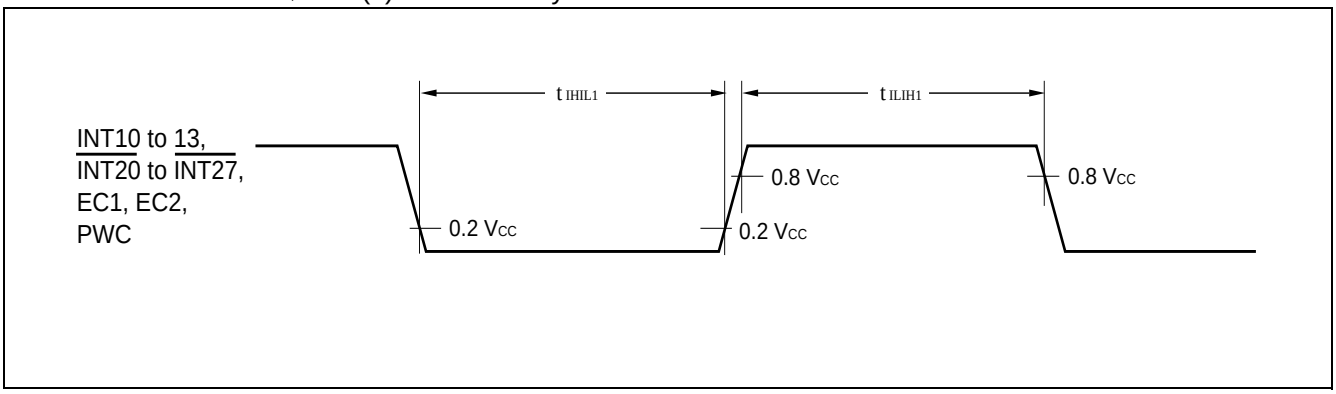


(6) Peripheral Input Timing

($AV_{CC}$ = $V_{CC}$ = 5.0 V for MB89PV480, MB89P485, MB89485
$AV_{CC}$ = $V_{CC}$ = 3.0 V for MB89P485L, MB89485L
$AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Peripheral input “H” pulse width 1 | $t_{ILIH1}$ | $\overline{INT10}$ to $\overline{INT13}$, $\overline{INT20}$ to $\overline{INT27}$, EC1, EC2, PWC | 2 $t_{inst}$* | — | µs | |
| Peripheral input “L” pulse width 1 | $t_{IHIL1}$ | | 2 $t_{inst}$* | — | µs | |

* : For information on $t_{inst}$, see “(4) Instruction Cycle.”



## 5. A/D Converter Electrical Characteristics

(1) A/D Converter Electrical Characteristics

( $AV_{CC} = V_{CC}$ = 4.5 V to 5.5 V for MB89PV480, MB89P485, MB89485,
$AV_{CC} = V_{CC}$ = 2.7 V to 3.6 V for MB89P485L, MB89485L,
$AV_{SS} = V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

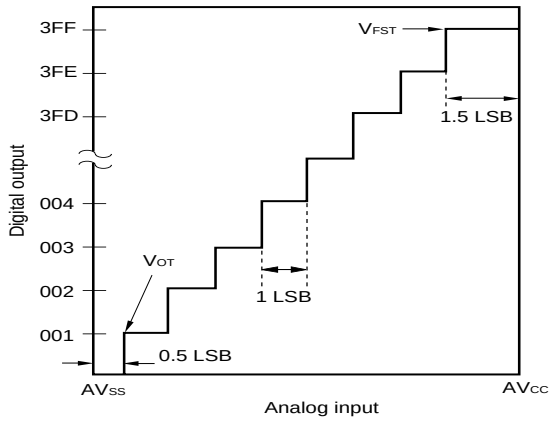
| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | 10 | — | bit | |
| Total error | | | — | — | ±4.0 | LSB | |
| Linearity error | | | — | — | ±2.5 | LSB | |
| Differential linearity error | | | — | — | ±1.9 | LSB | |
| Zero transition voltage | $V_{OT}$ | | $AV_{SS}$ – 1.5 LSB | $AV_{SS}$ + 0.5 LSB | $AV_{SS}$ + 2.5 LSB | mV | |
| Full-scale transition voltage | $V_{FST}$ | | $AV_{CC}$ – 4.5 LSB | $AV_{CC}$ – 2.5 LSB | $AV_{CC}$ - 0.5 LSB | mV | |
| A/D mode conversion time | — | | — | — | 60 tinst* | µs | |
| Analog port input current | $I_{AIN}$ | AN0 to AN3 | — | — | 10 | µA | |
| Analog input voltage | $V_{AIN}$ | | $AV_{SS}$ | — | $AV_{CC}$ | V | |

* : For information on $t_{inst}$, see "(4) Instruction Cycle" in "4. AC Characteristics".

(2) A/D Converter Glossary

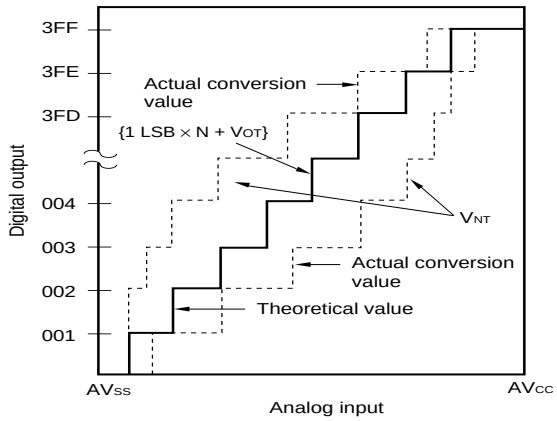
- Resolution
  Analog changes that are identifiable with the A/D converter.
  When the number of bits is 10, analog voltage can be divided into $2^{10}$ = 1024.
- Linearity error (unit: LSB)
  The deviation of the straight line connecting the zero transition point ("00 0000 0000" ↔ "00 0000 0001") with the full-scale transition point ("11 1111 1111" ↔ "11 1111 1110") from actual conversion characteristics.
- Differential linearity error (unit: LSB)
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value.
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values.

Theoretical I/O characteristics



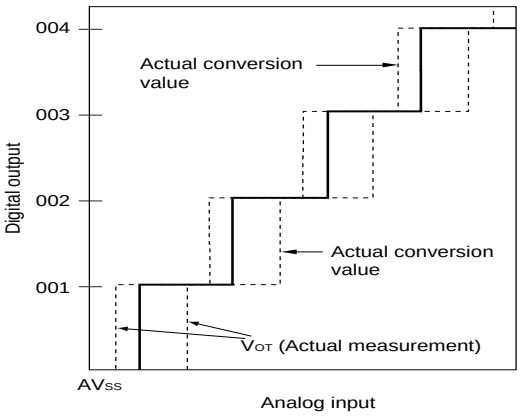

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ (\text{V})$$

Total error

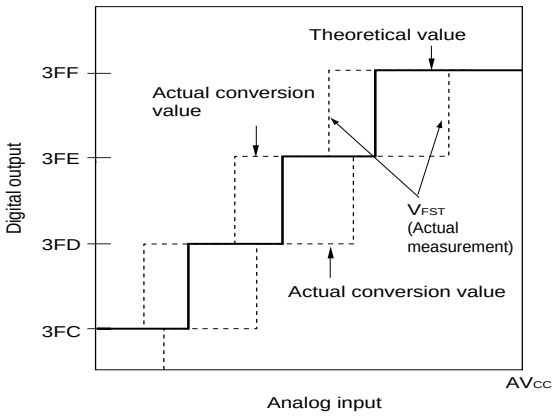



$$\text{Total error} = \frac{V_{NT} - \{1\ \text{LSB} \times N + 0.5\ \text{LSB}\}}{1\ \text{LSB}}$$

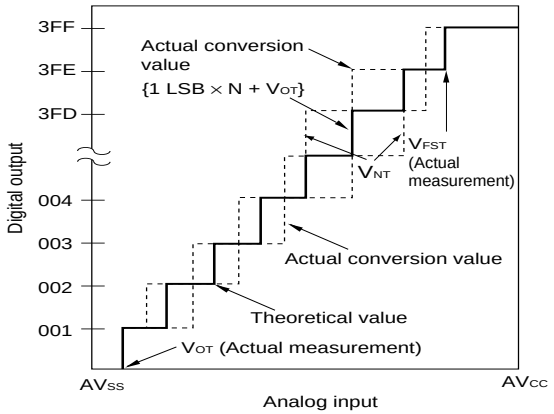
Zero transition error




Full-scale transition error

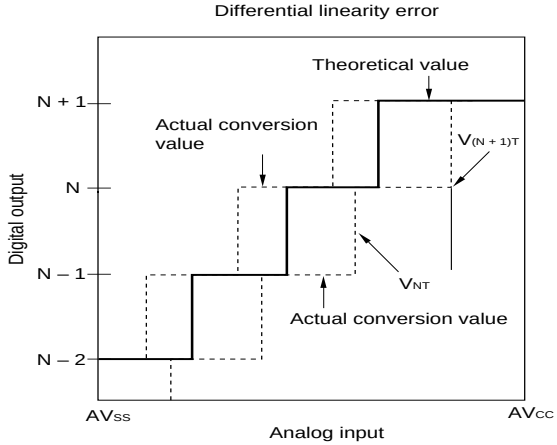



Linearity error




$$\text{Linearity error} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

Differential linearity error




$$\text{Differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

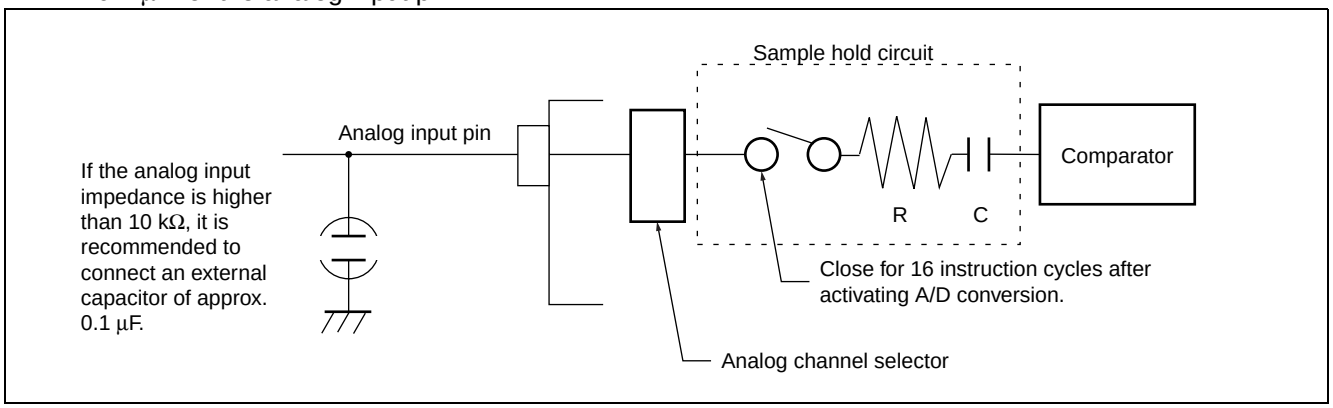
(3) Notes on Using A/D Converter

- Input impedance of the analog input pins

  The A/D converter used for the MB89480 series contains a sample and hold circuit as illustrated below to fetch analog input voltage into the sample and hold capacitor for 16 instruction cycles after activation A/D conversion.

  For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low.

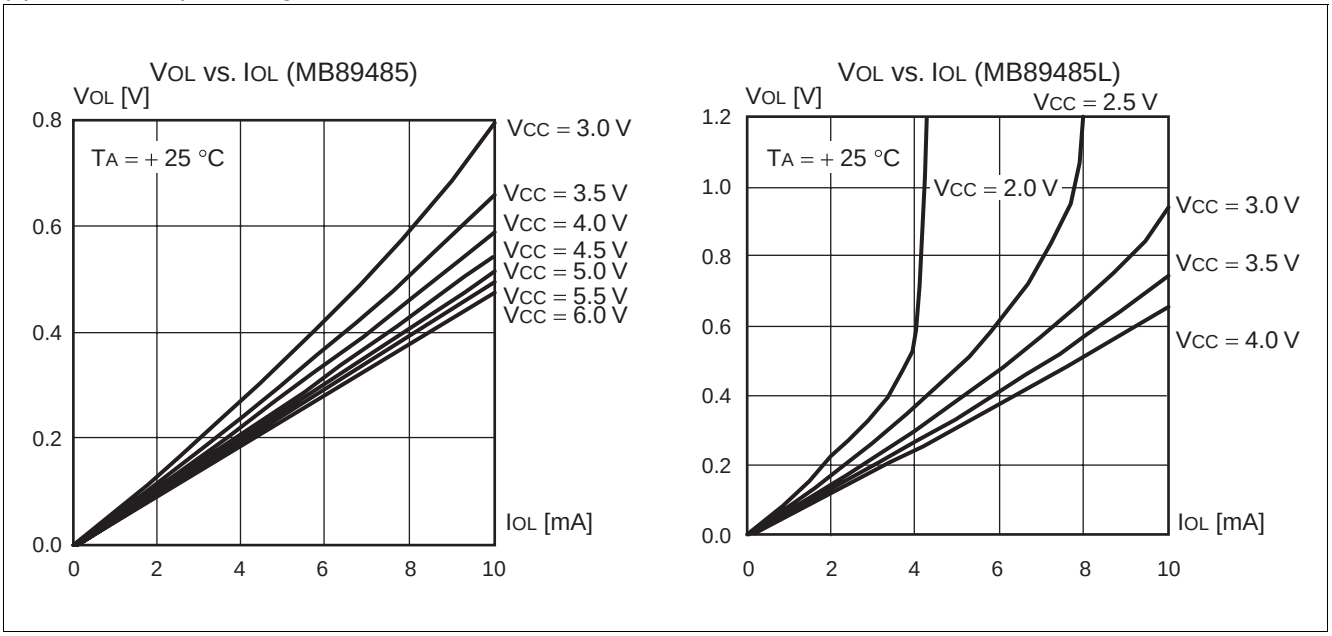
  Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of about 0.1 μF for the analog input pin.



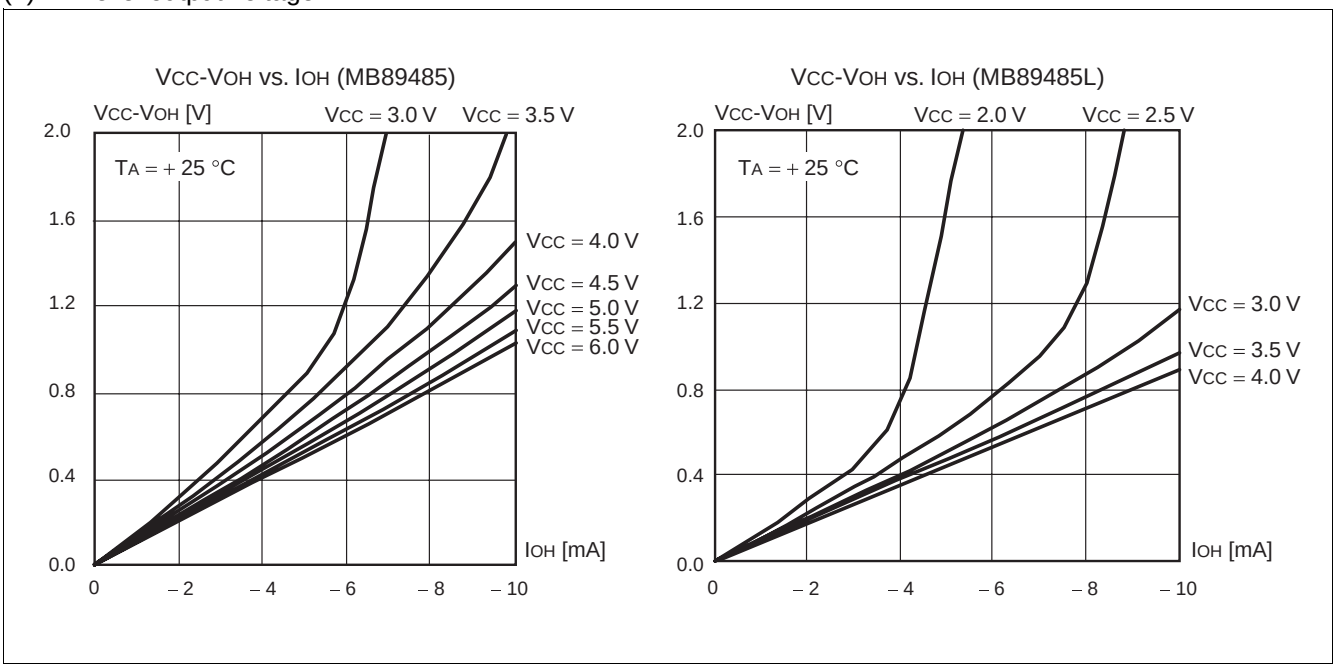

| | MB89485 MB89PV480 | MB89485L | MB89P485 | MB89P485L |
|---|---|---|---|---|
| R: analog input equivalent resistance | 2.2 kΩ | 2.8 kΩ | 2.6 kΩ | 7.1 kΩ |
| C: analog input equivalent capacitance | 45 pF | 46 pF | 28 pF | 48.3 pF |

## ■ EXAMPLE CHARACTERISTICS

(1) "L" level output voltage

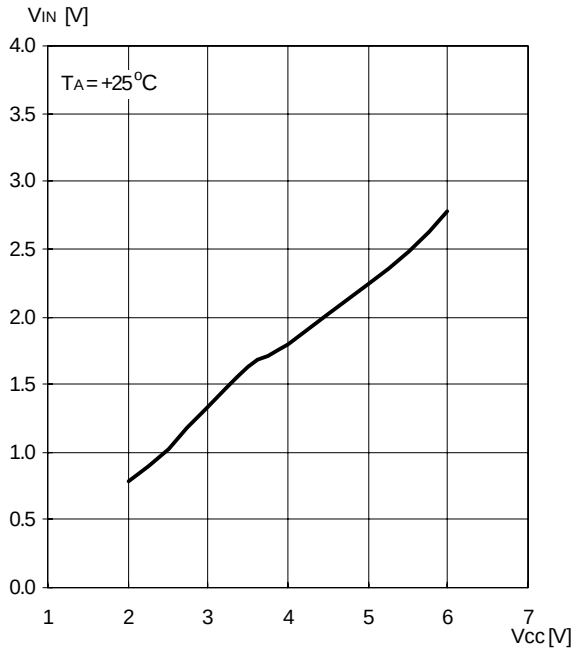



(2) "H" level output voltage

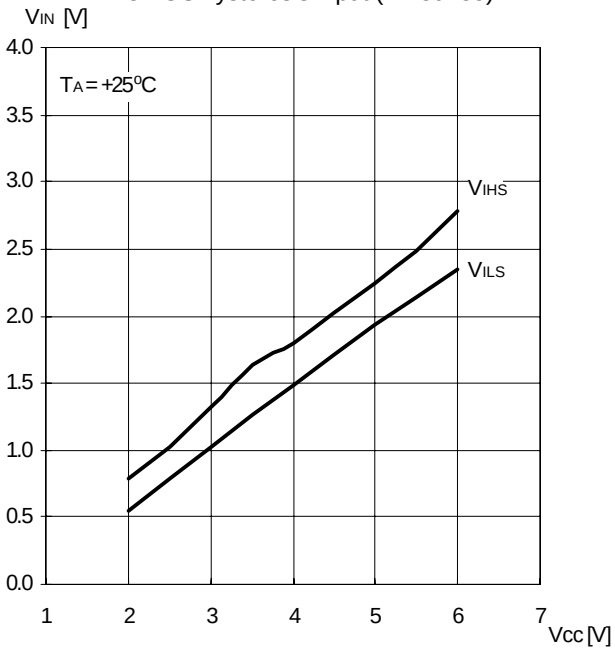


(3) "H" level input voltage/"L" level input voltage

CMOS input (MB89485)



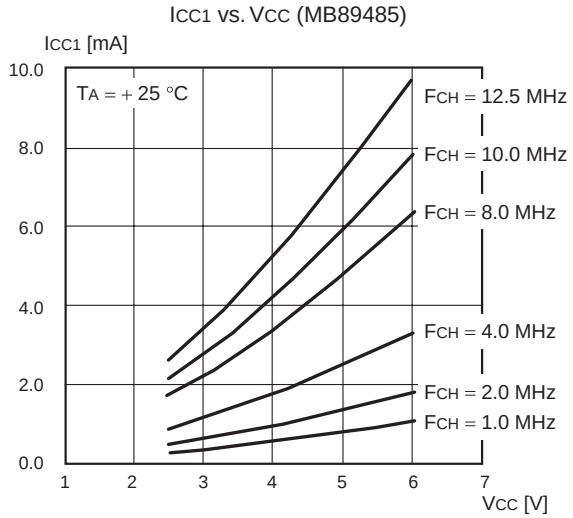

CMOS hysteresis input (MB89485)

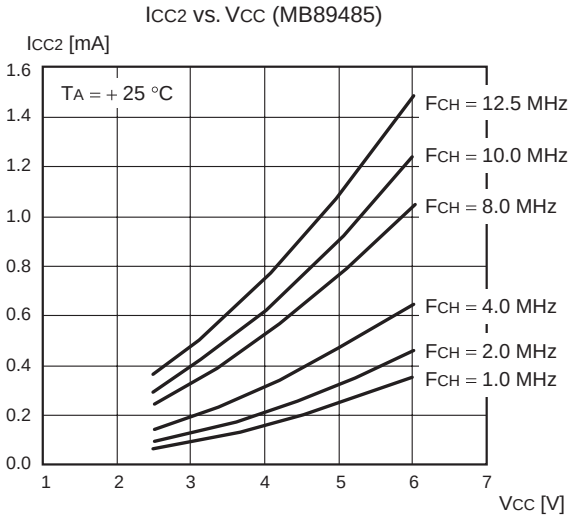


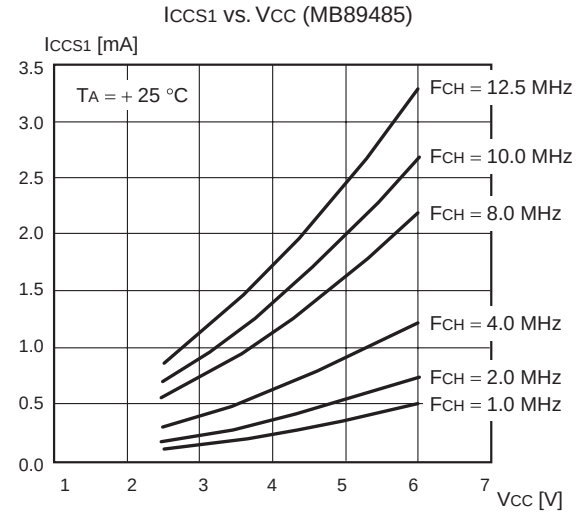

$V_{IHS}$ : Threshold when input voltage in hysteresis characteristics is set to “H” level.

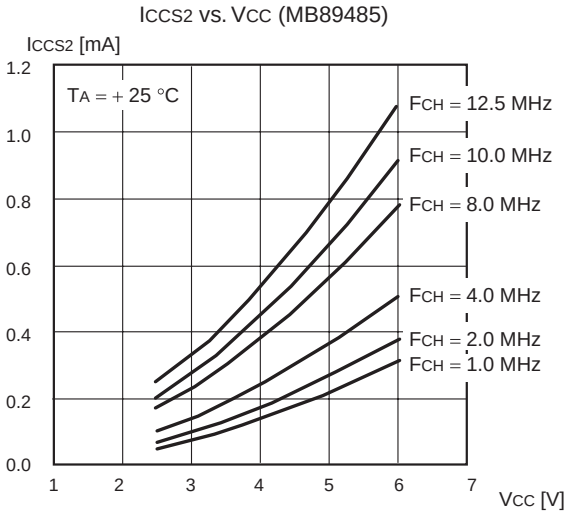
$V_{ILS}$ : Threshold when input voltage in hysteresis characteristics is set to “L” level.

(4) Power supply current (External clock)



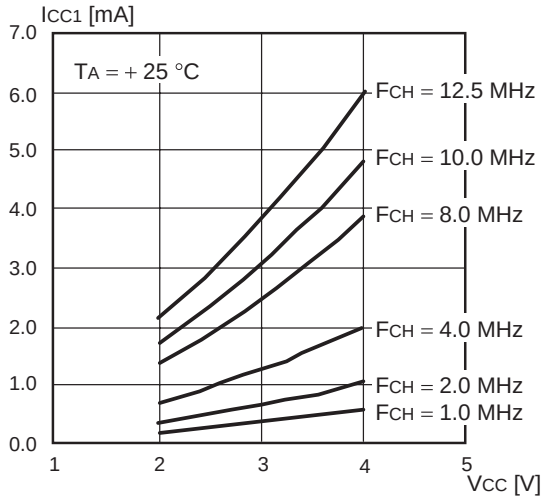



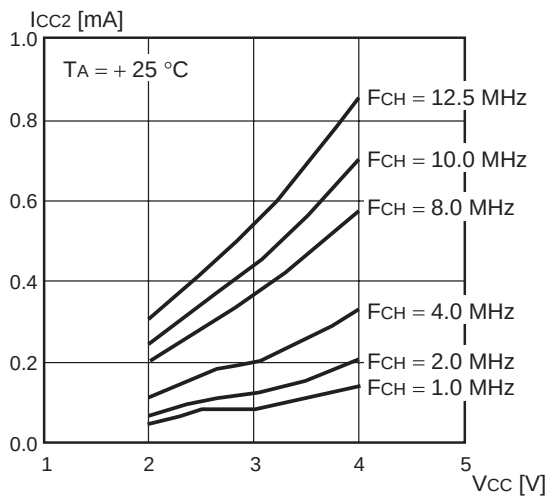

*(Continued)*

*(Continued)*

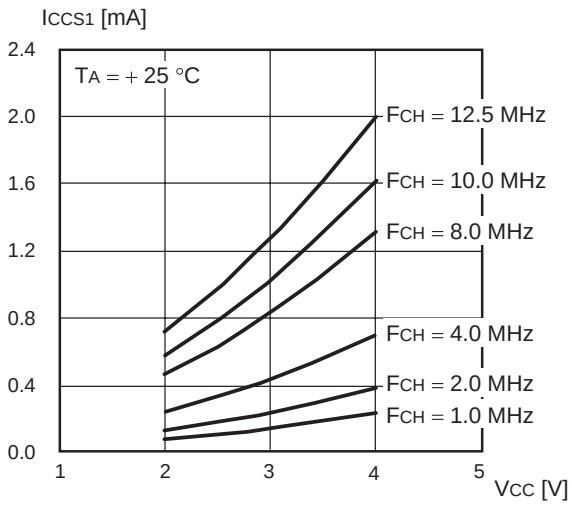
ICC1 vs. VCC (MB89485L)



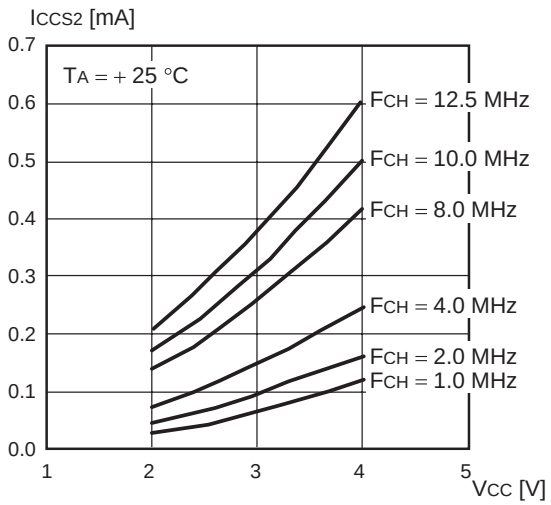

ICC2 vs. VCC (MB89485L)




ICCS1 vs. VCC (MB89485L)

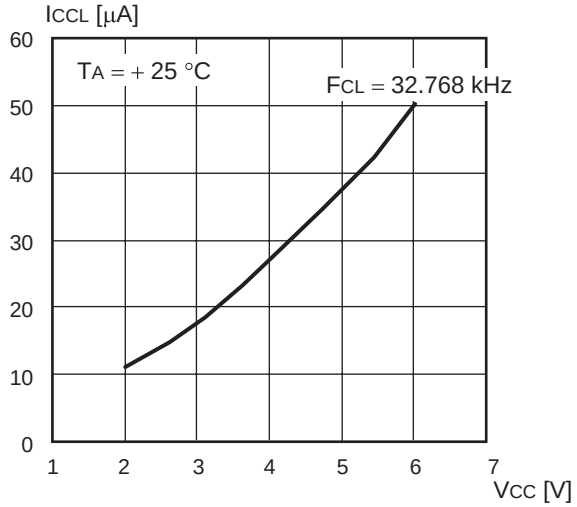



ICCS2 vs. VCC (MB89485L)

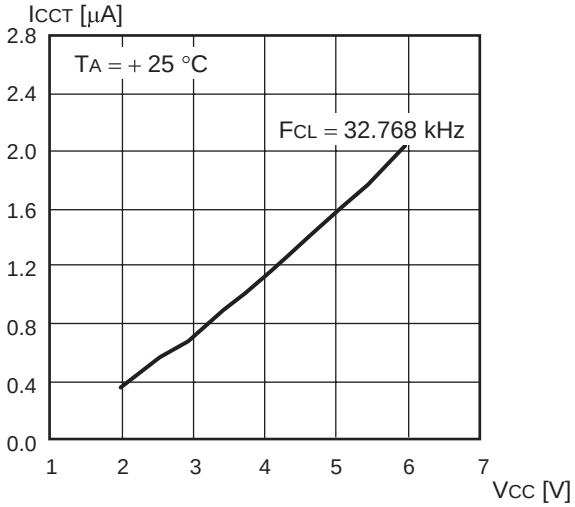


*(Continued)*

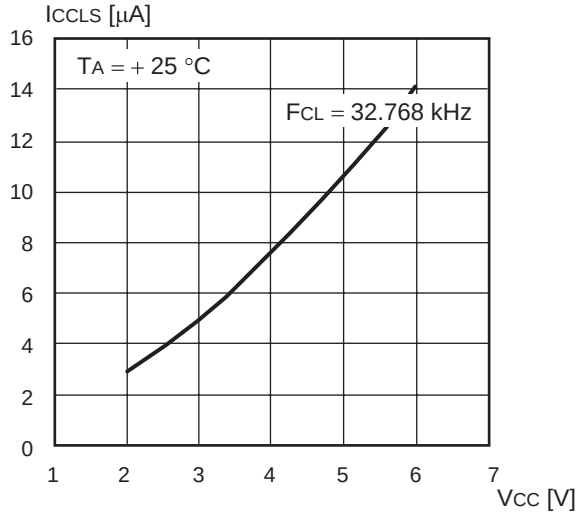
ICCL vs. VCC (MB89485)



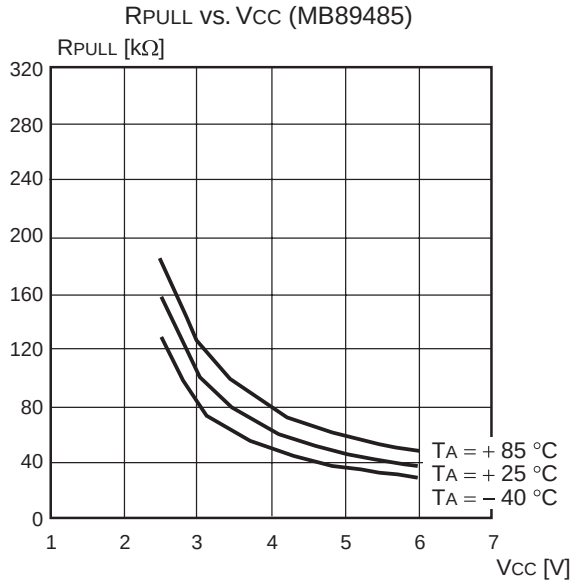

ICCT vs. VCC (MB89485)

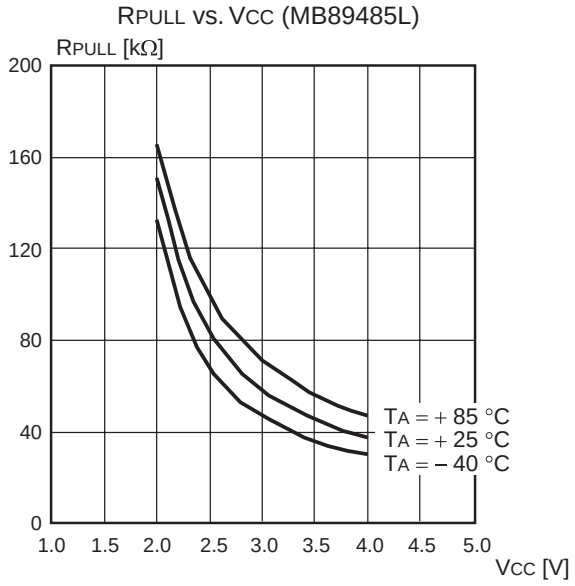



ICCLS vs. VCC (MB89485)



(5) Pull-up resistance



## ■ MASK OPTIONS

| No. | Part number | MB89485 | MB89485L | MB89P485 | MB89P485L | MB89PV480 |
|---|---|---|---|---|---|---|
| | **Specifying procedure** | **Specify when ordering mask** | | **Setting not possible** | | **Setting not possible** |
| 1 | Booster selection (KSV)<br>• Internal resistor ladder<br>• Booster | Selectable | | 101/103 : Internal resistor ladder<br>102/104: Booster | | 101 : Internal resistor ladder<br>102: Booster |
| 2 | Selection of OTPROM content protection feature<br>• No protection feature<br>• With protection feature | — | | 101/102 : No protection<br>103/104 : With protection | | — |
| 3 | Selection of oscillation stabilization time (OSC)<br>$2^{14}/F_{CH}$ (approx.1.3 ms)<br>$2^{17}/F_{CH}$ (approx.10.5 ms)<br>$2^{18}/F_{CH}$ (approx.21.0 ms) | Selectable OSC | | $2^{18}/F_{CH}$ (approx.21.0 ms) | | $2^{18}/F_{CH}$ (approx.21.0 ms) |
| 4 | Selection of power-on stabilization time<br>• Nil<br>• $2^{17}/F_{CH}$ | Selectable | Fixed to nil | $2^{17}/F_{CH}$ | Fixed to nil | Fixed to nil |

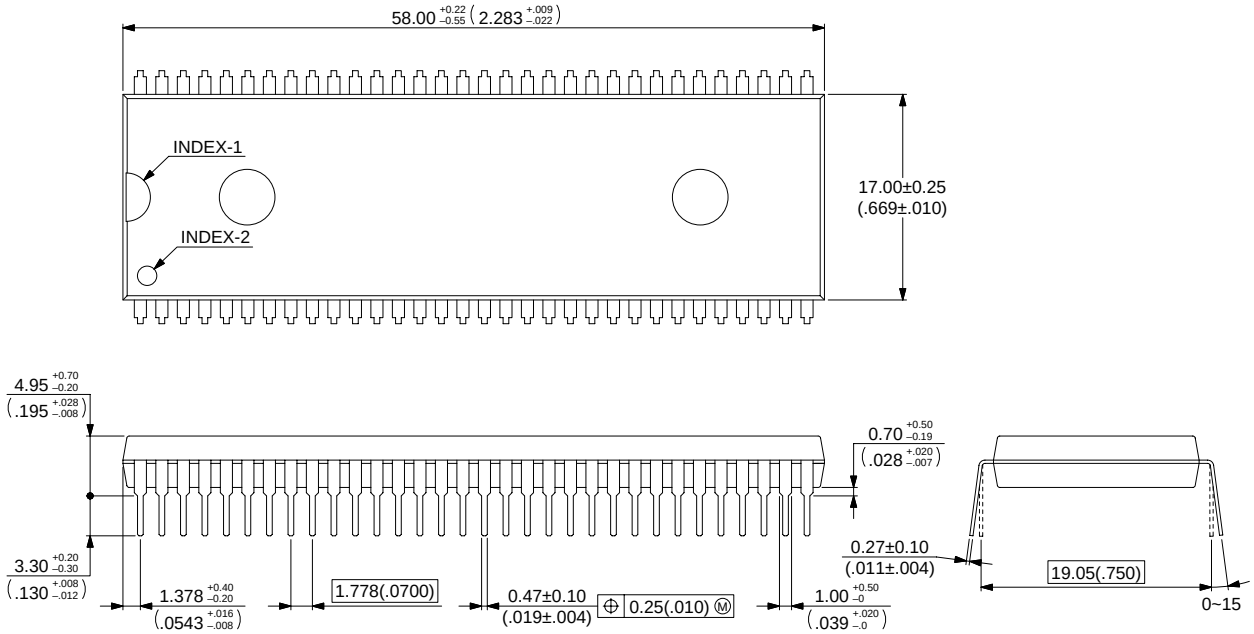
## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB89485PFM<br>MB89P485-101PFM<br>MB89P485-102PFM<br>MB89P485-103PFM<br>MB89P485-104PFM<br>MB89485LPFM<br>MB89P485L-101PFM<br>MB89P485L-102PFM<br>MB89P485L-103PFM<br>MB89P485L-104PFM | 64-pin Plastic QFP<br>(FPT-64P-M09) | 101: With internal resistor ladder, without content protection<br>102: With booster, without content protection<br>103: With internal resistor ladder, with content protection<br>104: With booster, with content protection |
| MB89485P-SH<br>MB89P485-101P-SH<br>MB89P485-102P-SH<br>MB89P485-103P-SH<br>MB89P485-104P-SH<br>MB89485LP-SH<br>MB89P485L-101P-SH<br>MB89P485L-102P-SH<br>MB89P485L-103P-SH<br>MB89P485L-104P-SH | 64-pin Plastic SH-DIP<br>(DIP-64P-M01) | |
| MB89PV480-101C-SH<br>MB89PV480-102C-SH | 64-pin Ceramic MDIP<br>(MDP-64C-P02) | |
| MB89PV480-101CF<br>MB89PV480-102CF | 64-pin Ceramic MQFP<br>(MQP-64C-P01) | |

## ■ PACKAGE DIMENSIONS

64-pin Plastic SH-DIP
(DIP-64P-M01)

Note: Pins width and pins thickness include plating thickness.

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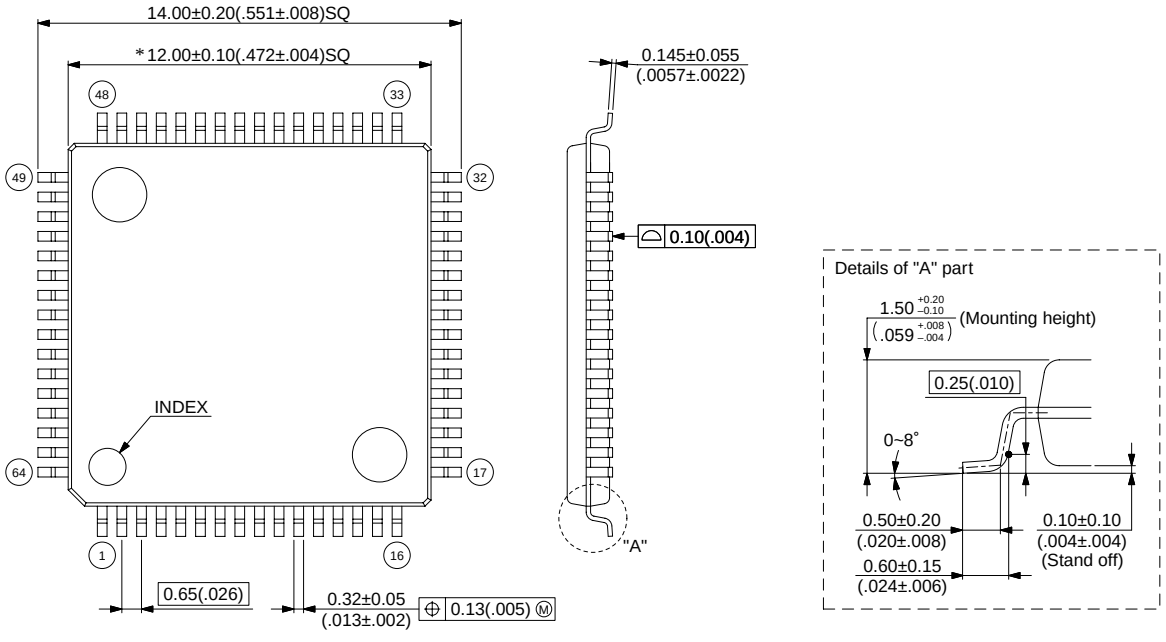
Dimensions in mm (inches)
Note : The values in parenthese are reference values.

*(Continued)*

64-pin Plastic LQFP
(FPT-64P-M09)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar remainder.

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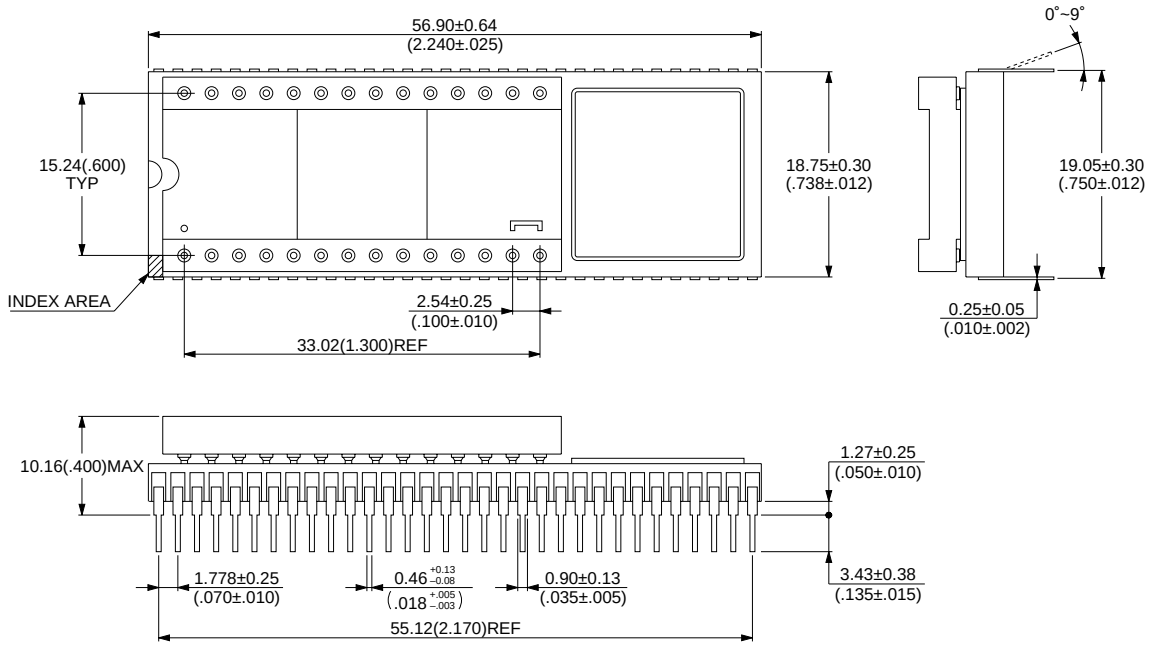
Dimensions in mm (inches)
Note : The values in parentheses are reference values.

*(Continued)*

64-pin Ceramic MDIP
(MDP-64C-P02)

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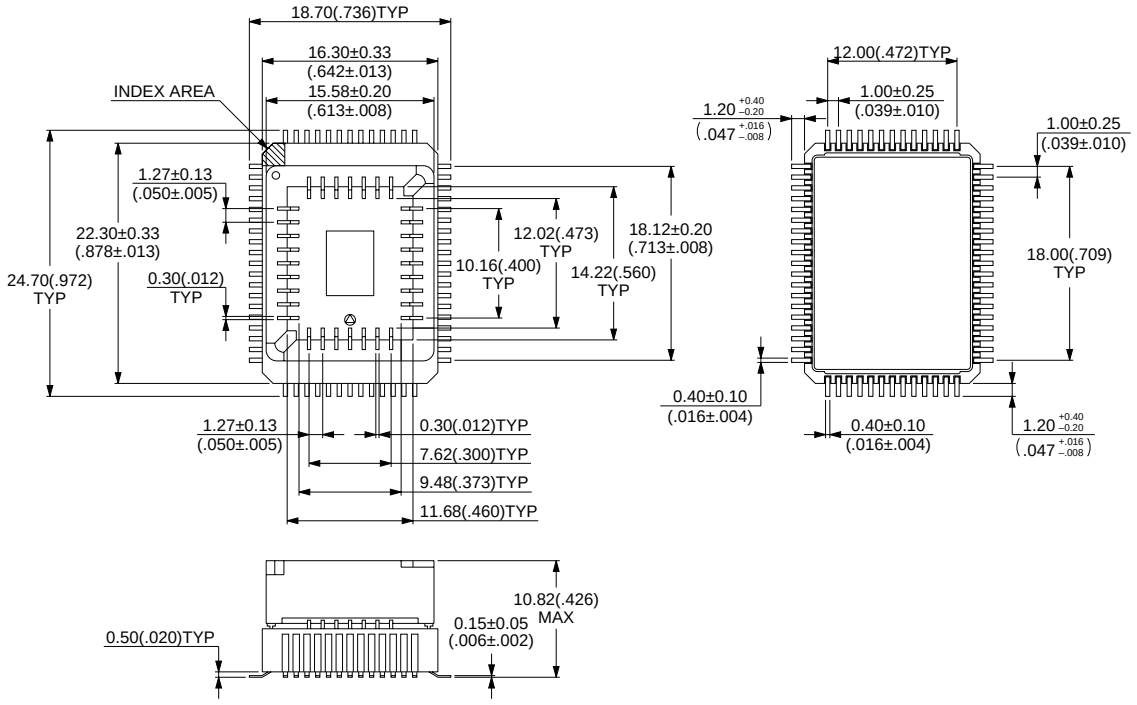
Dimensions in mm (inches)
Note : The values in parentheses are reference values.

*(Continued)*

*(Continued)*

64-pin Ceramic MQFP
(MQP-64C-P01)

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Dimensions in mm (inches)
Note : The values in parentheses are referent value.

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