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MR9730

TELEVIEW 525 LINE VIDEO GENERATOR

The Video Generator Chip is one of a set of LSI chips used in the Plessey Semiconductor TELEVIEW Teletext/Viewdata system. It reads the contents of a Page Store and generates outputs suitable for driving a normal 525 line Colour Television receiver to display the contents of the Page Store.

The chip also monitors the composite synchronising signals within the receiver and locks the total TELEVIEW system onto the incoming signals. When no transmission is taking place the chip develops a composite sync. signal which is used to synchronise the receiver.

A full set of colour display facilities is provided by the device.

The device is fabricated in Plessey Semiconductors N-Channel metal gate MOS process providing direct TTL interfacing, high speed and good reliability.

FEATURES

- Interlaced 525 line operation
- 24 Row x 40 Character display
- Character Set options available
- On and Off Hours operation
- Half Page Expansion
- Boxed Clock and Header on Teletext
- Direct interfacing with the TELEVIEW busses
- Provides master timing signals for the other TELE-VIEW chips to indicate the status of the display scan
- Can address up to eight Page Stores
- Provides the address information to scan the allocated Page Store
- Provides composite synchronising signals for the receiver for 'Off-Hours' working
- Provides comprehensive set of display facilities
- Can receive Teletext on lines 7-18

DISPLAY FACILITIES

- 1. Provides the following display facilities controlled by 'control' characters read from the store i.e. via the TELETEXT/VIEWDATA transmission.
- (a) Alpha-numerics/Graphics in seven colour set.
- (b) Colour or black backgrounds.
- (c) Selected characters can be concealed.
- (d) Selected characters can be flashed
- (e) 'Boxed' characters can be inserted into the normal Television Picture. This can be done manually or automatically.
- (f) Characters may be either single or double height.

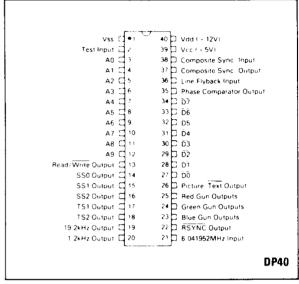


Fig.1 Pin connections - top view

- (g) Graphics characters may be contiguous or separated.
- (h) Graphics characters may be 'held' during other control characters.
- (i) Special graphics for high resolution applications.
- 2. Provides the following display facilities controlled from the users keyboard/keypad via the control chip.
- (a) Switch between normal and data video.
- (b) Teletext or Viewdata Operation.
- (c) Clock time can be boxed into a normal picture (Teletext only).
- (d) Display of one half of a page in double height.
- (e) Black and white output of data in Mix Mode.
- (f) Inhibiting of character rounding and flashing.
- (g) Enabling of a cursor.
- (h) Inhibit the display until updated.
- (i) Reveal 'concealed' characters.
- (j) Can display and store in any of the eight stores independently.

PIN FUNCTIONS

Pin Number	Name	Function
1	Vss	This is the negative supply for the chip and is used as a reference for all the electrical parameters.
2	Test Input	This input should be connected to Vss or left open.
3–12	A0-A9	These pins are connected to the Address Bus of the TELEVIEW system. They are used for address Input/Output.
13	Read/Write Output	This output is used to drive the Random Access Memories forming the Page Memory.
14-16	SS0-SS2 Outputs	These binary coded outputs are used to select the required page Store.
17, 18	TS1, TS2 Outputs	These outputs are generated by the Video Generator from the status of the raster scan and are used to indicate this status to other chips within the TELEVIEW system.
19, 20	19.2kHz and 1.2kHz Outputs	These outputs provide 19.2kHz and 1.2kHz square wave signals which are used by the UAR/T as reception and transmission clocks respectively.
21	6MHz Input	This input is fed from a 6.041952MHz oscillator which is phase locked to the normal transmission for Teletext ON Hours operation. During OFF Hours working a free running crystal oscillator is normally used.
22	RSYNC Output	This output is an open-drain output and is used to indicate the presence of Teletext lines to the D.A. Chip and Data Grabber. The timing of this signal is indicated in Fig. 7.
23–25	Red, Green and Blue Outputs	These outputs are push-pull outputs which go high to turn on the relevant colour gun for displaying. These outputs are closely matched for propagation delay and rise and fall times.
26	Picture/Text Output	This output is used by the TELEVIEW system to indicate to the receiver if data is to be displayed and is used to change the display from normal video to data video from the Red, Green and Blue chip outputs. In the mix mode this generates monochrome video. It will then be matched to the gun outputs for propagation delay and rise and fall times.
27-34	D0-D7 Inputs	The Data Inputs form the communication highway between the Video Generator and the Control Processor and Page Memory.
35	Phase Comparator Output	In on-hours operation the display Line Flyback signal is compared for phase with an internal $64\mu s$ period signal derived from the 6MHz display clock. The output is a pulse which produces a voltage for controlling the frequency of a 6MHz display oscillator, thus locking the display to the incoming picture. In off-hours operation this open drair output goes high permanently, and thus can be used as an indication of on-hours/off-hours status. When this output is high the oscillator must run fast and when this output is low the oscillator must run slow. If the Phase Comparator output is not used it must be connected to Vcc via a 4K7 resistor.
36	Line Flyback Input	The Line Flyback input is a signal from the display deflection circuitry which is used for positioning the display on the T.V. screen. Line Flyback pulses are positive. This input must be provided at all times.
37	Comp. Sync Output	This output is an open drain output. In on-hours working it outputs a regenerated composite syne, signal from the comp, sync, input. In off-hours working it outputs an internally generated composite sync.
38	Comp. Sync. Input	The Composite sync, input monitors the composite sync/video being received and extracts synchronising information and 'on-hours/off hours' information for the Video Generator. This input must be predominantly high for 'off-hours' switching. Sync, pulses are negative.
39	Vcc	This pin is connected to the +5.0V supply.
40	Vdd	This pin is connected to the +12.0V supply.

CHIP DESCRIPTION

The Video Generator Chip contains the logic and control functions to interrogate a selected TELEVIEW Page Store and display the contained information at the correct period within the raster scan on a normal TV receiver. The chip also generates the master timing signals TS1 and TS2 which indicate the raster status to the Control processor and Data Acquisition chips.

The basic block diagram of the chip is shown in Fig.4 and major functional blocks are described below.

1. Comp Sync. Generator and On-Hours Detector

The prime function of this block is to detect negative going sync. signals from the incoming mixed sync. and to synchronise the TELEVIEW system with the transmitted signal. When the incoming transmission is turned off. (i.e. goes 'Off-hours'), this is recognised by the detector after at least 300ms of missing sync. pulses. An internally generated Composite Sync. signal is then switched to the Composite Sync. Out pin. Thus the receiver will continue in lock but synchronised to the Video Generator, Similarly if the normal transmission resumes the fact that external sync. pulses are being received is recognised by the Video Generator and the chip will re-synchronise itself with the incoming transmission. Because the Video Generator is aware of the status of the mixed sync, at all times the chip can detect frame sync., line sync, and even or odd frames. Thus with this information the chip can continuously monitor the current line number. The relevant sections of the line scan are decoded and are indicated externally by the TS1, TS2 time slot outputs. These signals are fully described in Fig.6, but there are four periods i.e.

(i) Writing to RAM. TS10
This occurs during lines 7 to 18 under control of the D.A. chip.

(ii) Reading from RAM, TS00

This occurs under control of the Video Generator chip between lines 37 and 253, and is when the display is active.

(iii) Data Interchange Period, TS11

The Interchange of information between D.A., Control Processor and Video Generator occurs during this period (19–47).

(iv) Spare TS01

During lines 289-6 the Video Generator does not use the Data Bus.

As the chip is aware of the raster status the chip also starts and stops the address counter/latch combination which is used to scan the relevant Page Memory. The form of the generated sync. pulses are shown in Fig.5.

2. Character Counter and Address Logic

The address counter is a binary counter which is incremented at the Character Display Rate (1MHz). It can also be loaded from a latch which contains the start address of each character row. Since each character consists of 9 vertical lines of raster scan, the counter is incremented 40 times from a start address and then

is reloaded with the same start address ready for the next raster scan of the same forty characters. This occurs eight times. On the last line the counter is incremented an extra once and this new address is stored in the latch. This address being the start address of the next row of forty characters. The above sequence is then repeated.

If displaying only one half of a page with all characters in double height, the Video Generator scans the same forty addresses seventeen times and stores the new address on the eighteenth raster scan. If it is in the bottom half of the page, the address counter must be initialized to 480.

The display format of 40 characters, each 1µs wide, occurs on a line of 64µs duration thus leaving a border of 12µs on each end of the character row. This address counter is actually started some 4µs before the start of the proper character display thus allowing time for address generation, RAM access time, ROM access time and display processing, these actions being pipelined. Facilities are also provided such that the output address can be reduced by 40 thus allowing accessing of the character in the row above. This is a necessary operation for a 'Double Height' display option which will be described later. This facility is inhibited when displaying only one half of a page. The address so produced is presented on the address bus and the required Page Memory is activated by the Store Select Outputs. The address drivers are tristate thus allowing easy bus interface, being active for $40\mu s$ starting $3.5-6\mu s$ after LFB.

3. Input Latches and Character Read-Only Memory

The data being read from the required Page Memory is placed on the Data Bus and is latched into the Data Bus latches. A total of 450ns is allowed for the RAM read cycle and thus quite slow Random Access memories may be used. Having been latched by the Video Generator chip the seven bit character is used to address the character Read Only Memory. This memory is organised as 96 characters each of 45 dots (5 x 9 array).

4. Data Control Latches (Colour, Background, Control) Certain characters indicate to the Video Generator a change in display status. These characters are contained within columns 0 and 1 of the character set as shown in fig. 6 and may be used to change character colour, background colour, height, etc. These facilities, and the control of them, are fully described in the British Broadcasting Teletext Specification (Sept. 1976) published by the BBC, IBA and BREMA.

5. Output Logic and Drivers

The output logic reads the character ROM into a six bit parallel to serial shift register. This operation occurs at the left-hand side of the character to be displayed, the data in the register is then shifted out at 6MHz (character dot-rate) the data bits selecting between character and background information. This information is used to drive the fast Gun output drivers. These outputs have to be closely matched for propagation delay and rise and fall time to ensure good legibility.

DATA INTERCHANGE

During the TS11 timeslot the Video Generator can receive information from other devices attached to the TELEVIEW system busses. This is normally used by the control chip to update the control and display latches within the Video Generator. The Video Generator is enabled to receive by putting the address 1111XOXXX on the address highway (active high).

The latches are updated by the following control words, active low signalling, most significant bit is a strobe.

Highway Free	0	0	0	0	0	0	0	0	
Control Word 1	1	0	0	0	Т	S	S	s	
Control Word 2	1	0	0	1	x	C ₄	C_6	C ₅)
Control Word 3	1	0	1	0	C_{10}	C ₉	C_8	C ₇	Teletext
Control Word 4	1	0	1	1	C ₁₄	C ₁₃	C ₁₂	C_{11})
Control Word 2	1	0	0	1	×	F	0	0)
Control Word 3	1	0	1	0	b ₇	C	b_6	b ₅	Viewdata
Control Word 4	1	0	1	1	b ₄	b_3	b_2	b_1	
Store Select									
for Display	1	1	0	0	SP	D	d	d	
Key Data	1	1	0	1	*	Р	*	*	
Other Facilities	1	1	1	0	Х	вн	М	вс	

The Control bits are as follows:-

Т	TELETEXT MODE i.e. NOT VIEWDATA
Sss	Identification of Store being written to
Ddd	Identification of Store being displayed from

(a) Teletext	
C ₄	Erases rows $1-23$ of Store defined by Sss and resets Reveal if Sss = Ddd
C ₅	Newsflash
C ₆	Subtitle
С,	Suppress Header
C ₈	Update Indicator
C ₉	No action
C ₁₀	Inhibit display
C ₁₁	No action
$C_{12} - C_{14}$	Switches rounding OFF and flashing OFF if all set

(b) Viewdata

$b_2 - b_4$	Switches rounding OFF and flashing OFF if all set
$b_7 - b_1$	Cursor Control Bits
001 0001	Cursor ON The two Control Words that make up these codes must be transmitted in
001 0100	Cursor OFF) numerical order in the same TS11 timeslot.
F	Form feed, erases store defined by Sss, resets Reveal if Sss = Ddd
SP	Sets Picture/Text to picture (for initialization)
P	P Key pressed. Resets Reveal, Half Page Expansion, Newsflash/Subtitle (Auto Box), Suppress header, Inhibit display, update.
M	Mix Mode
BC	Box Clock (Teletext only)
ВН	Box Header (Teletext only)
***	These are coded as follows:
001	Picture/Text Key pressed
010	Reveal/Conceal Key pressed
011	1/2 Page Key Pressed (Cycles Full, Top, Bottom, Full etc).
100	Update/Clear Key pressed
111	Hold (not used by MR9730)

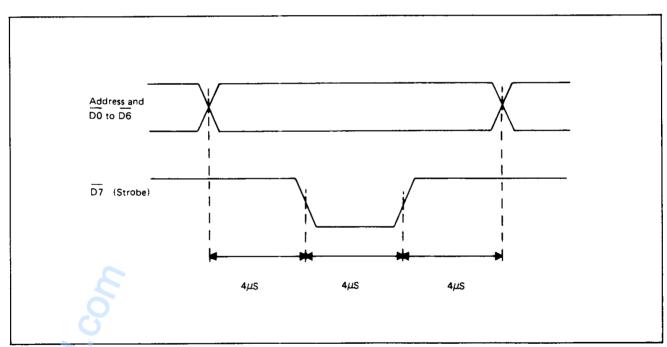


Fig.2 Typical timing diagram for input data strobing

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Logic is contained on the Video Generator chip to process the Display Modes as described in the Broadcast Teletext Specifications. These facilities are outlined below. Some extra facilities are also included.

1. Character Set

The chip can display 96 Alphanumerics characters and 64 Graphics shapes which may be either contiguous or separated. The alphanumeric format is determined by a 4320 bit Read Only Memory organised as:

96 (characters) \times 5 (dots) \times 9 (lines) = 4320

This can be programmed for different character fonts

The graphics shapes are determined directly from the bits of the character code (Fig.8).

2. Display and Background Colour

The characters and the background can be displayed in one of seven colours. In addition the background may be black. This information is stored in two sets of three latches representing character and background colours.

3. Conceal and Flash

Selected characters can be concealed and optionally revealed by the viewer. Selected characters can be flashed on command. The flashing is controlled by an on-chip flash oscillator. During the flash period or when concealed, only background information is displayed. The flash rate is 1.56Hz.

4. Boxing

Text or graphics characters can be boxed into a normal video picture when required. This is achieved by means of the Picture/Text output which can be used externally to switch the guns between Picture and Text signals.

5. Double Height

Double height characters are characters contained between the control characters "Double Height" and "normal Height" (or end of line). When a "Double Height" control character is read from the RAM only the top half of the subsequent character(s) are displayed during the 9 raster scans. During the next 9 scan lines, 40 is subtracted from the addresses being output on A0-A9 so the same 40 addresses are read from another 8 times. Characters which are not double height are displayed as the background colour and the bottom(s) of the double height character(s) is (are) displayed.

6. Hold Graphics

When this latch is set, any subsequent control characters (except change Double/Normal Height or Change Alpha/Graphics) are displayed as the last graphics character.

7. Special Graphics

While in Graphics Mode the Special Graphics command will give a special high resolution facility. In this mode there is a one to one correspondence between data bits b_1 , b_2 , b_3 , b_4 , b_5 , b_7 and the six dots in each horizontal line of a character. This gives a possible graphics resolution of 6 x 18 for each character.

8. Box Clock

The last eight characters of the top row (Row 0) of a Teletext page can be boxed in double height into a normal television picture.

9. Half-page Operation

This allows either the top or bottom half of a normal Teletext/Viewdata page to be displayed over the whole screen, with each character in double height. This makes the display easier to read from a distance. Double height characters are ignored in this mode.

10. Monochrome Output

In normal operation this is the Picture/Text output and is used to blank the normal picture information for boxing newsflashes or displaying a page of teletext information.

In the mix mode this outputs Monochrome text information which is matched to the Gun Output signals in delay and drive. This can be used to superimpose text onto a picture by "cutting away" the picture below text data or as an output for Monochrome displays or printers. In this mode coloured backgrounds are suppressed for viewing clarity. The output is at a low level to display a character.

11. Character Rounding Inhibit

Normally characters are rounded, i.e. half dots are added to smooth diagonals on an interlaced television display. This can be switched off and flashing inhibited when outputting to a printer.

12. Cursor

The cursor is stored as the 8th bit in the Page Store Data Character. It is displayed as a flashing bar on the bottom line of a character. The flashing is complementary to the normal character flashing and any character information on the bottom line (tails or graphics information) is suppressed to improve legibility.

SIGNAL DETECTION CRITERIA

(For On Hours Operation)

The Video Generator detection circuitry for incoming sync, signals is designed to prevent mis-operation in the presence of noise. The criteria for detection is defined below.

1. Line Sync

The Comp. Video Input must be negative for greater than $3\mu s$.

The Comp. Video Input must be negative for greater than $10\mu s$ and at least 260 lines (Line Flyback pulses) must have occurred since the previous Frame Sync. detection.

3. Odd Frame Detection

Odd Frame Detection occurs when a Line Flyback pulse falls in a window 326-354µs after Frame Sync. Detection. However this detection must disagree with the internal Odd/Even frame status for 2 successive full frames before the internal status is inverted.

4. On-Hours/Off-Hours Detection

The incoming line flyback and line sync. pulses are compared to determine whether a valid transmission is being received. Lack of coincidences/frame are accumulated and if more than 16/Frame occur for a period 350–1000ms logic deems that a valid transmission is not being received and the chip switches 'OFF Hours'. If however, less than eight occur in any two successive ½ frames, the logic deems that a valid Composite Sync. s being received and the system goes 'ON Hours'.

For the chip to be able to look for synchronism the following phase relationship between Line Flyback and Comp. Sync. must be satisfied.

- (a) Earliest back edge of LFB is $2\mu s$ after start of Comp. Sync.
- (b) Latest leading edge of LFB is $2\mu s$ after start of Comp. Sync.
- (c) Latest back edge of LFB is 12μs after start of Comp. Sync.

The minimum length of the LFB pulse is $8\mu s$.

5. 6MHz Display Oscillator

The 6.041952MHz display oscillator must run fast in the OFF Hours mode but not so fast that the ON/OFF Hours detection criteria cannot be satisfied. This sets a maximum offset of +1.5kHz, the minimum offset is set by lock time criteria and would typically be +0.5kHz.

The frequency range of the oscillator must extend below the 6.0MHz nominal frequency. The minimum frequency should be at least -0.5kHz but can be as low as convenient.

COMPOSITE SYNC INPUT

On chip D.C. restore is provided which allows simple interfacing to the television, either composite sync. signals or video being acceptable.

As the Composite Sync/Video signal from the television may not be referenced to the system earth it is a.c. coupled to the chip.

A typical Interface Circuit is shown in Fig.3.

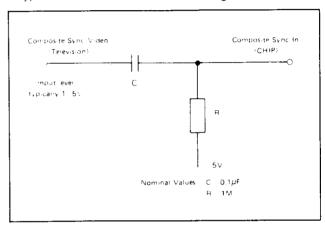


Fig.3 Typical interface circuit

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to Vss \dots -0.3 to +15V Storage temperature range. -55° C to +150 $^{\circ}$ C

Standard Conditions (unless otherwise indicated)

Vss = 0V (substrate voltage)

 $Vcc = +5V \pm 5\%$

 $Vdd = +12V \pm 10\%$

Operating Temperature (Ta) = 0° C to $+70^{\circ}$ C

Clock Frequency 6.041952MHz

*Exceeding these ratings could cause permanent damage Functional operation is not guaranteed under these conditions Operating ranges are specified below.

Characteristic	Min	Typ**	Max	Units	Conditions	
INPUTS Comp. Sync.						
Input Logic High	1.0		Vcc	V		
Input Logic Low	-0.3		0.05	V	See Note 1	
Input Capacitance	1		15	pF	Vin = 0V	
LSource		50		μА	Vin = $0V$ at $25^{\circ}C$	

Characteristic	Min	Тур	Max	Units	Conditions
6MHz					
Input Logic High	2.8		Vdd	V	
Input Logic Low	Vss		0.4	V	
Input Capacitance			25	ρF	Vin = 0V
Mark to Space Ratio	40:60		60:40		
Frequency	1.0		6.5	MHz	
Input Leakage			10	μΑ	Vin = 12V
All Other Inputs					
Input Logic High	2.2		Vdd	V	
Input Logic Low	Vss		0.8	V	
Input Capacitance			15	рF	Vin = 0V
Input Leakage			10	μΑ	Vin = 12V
OUTPUTS					
Addresses, Read/Write					
Store Select (Tri-State)					
Logic High Output	2.4		Vcc	V	loh = 320μA
Logic Low Output	Vss	0.2	0.45	V	lol = 3.2mA
Capacitance			15	pF	Vo = 0V @ 1 MHz
Trise Tfall			200	ns	C load = 200pF
Leakage (disabled)]		10	μΑ	Vo = 0V, 5V
Time Slots (TS1, TS2) (Push-Pull)					
Logic High Output	2.4		Vcc	V	loh = 320μA
Logic Low Output	Vss	0.2	0.45	V	lol = 3.2mA
Trise Tfall			200	ns	C load = 200pF
Comp. Sync (Open Drain)		:			
Logic Low Output	Vss		0.45	V	lol = 1.6mA
Logic High Leakage			10	μΑ	Vo = 12V
Capacitance			20	рF	Vo = 0V
Delay from Comp. Sync. In.		·	1	μs	ON Hours only
RSYNC (Open Drain)					
Logic Low Output	Vss		0.45	l v	lol = 4.0mA
Logic High Leakage			10	μΑ	Vo = 5V
Capacitance			15	pF	Vo = 0V
Phase Comparator (Open Drain)					
Logic Low Output	Vss		0.45	V	lol = 4.0mA
Logic High Leakage			10	μа	Vo = 5V
Capacitance			15	рF	Vo = 0V
R.G.B. Gun Outputs					
Picture/Text Output				1	
(Tristate)					
Logic High Output	Vcc-1		Vcc	V	I source = 2mA
Logic Low Output	Vss		1	V	I sync. = 5mA
Capacitance			20	рF	Vo = 0V
Trise T fall (10%-90%)			30	ns	Co = 30pF
Differential Trise T fall			30	ns	Co = 30pF Note 2
Leakage (disabled)			10	μΑ	Vo = 0,5V
19.2kHz, 1.2kHz Outputs			1		
Logic High Output	2.4		Vcc	V	$loh = -32\mu A$
Logic Low Output	Vss	0.2	0.4	\ \ \	lol = 320μA
Trise T fall			1	ms	C load = 100pF
POWER					
Vcc Supply		25	40	mA	Vcc = 5V
Vdd Supply		50	80	mA	Vdd = 12V

376 Note 1: Voltages below -0.3 volts should be current limited to 1mA. Note 2: Picture/Text matched in mix mode only.

Typical values are at +25°C and nominal voltages.

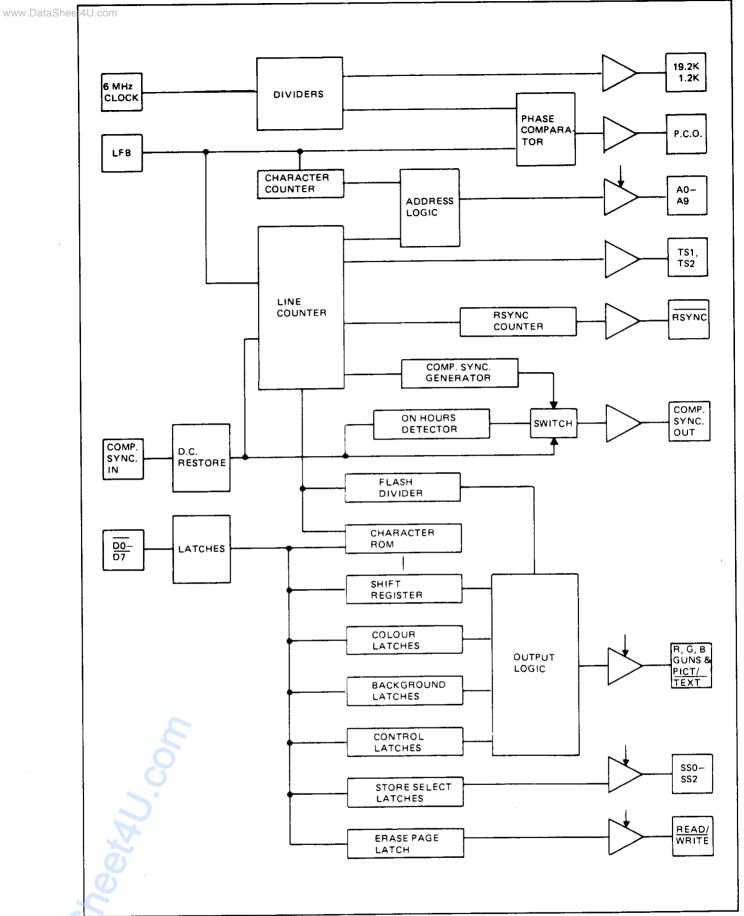


Fig.4 Block diagram

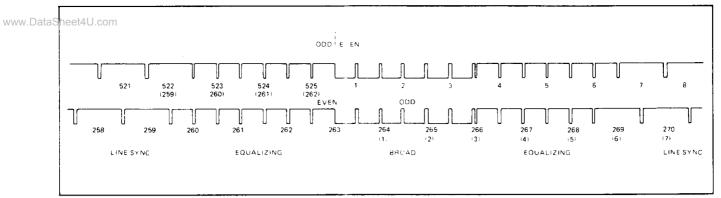


Fig.5 NTSC sync pulses

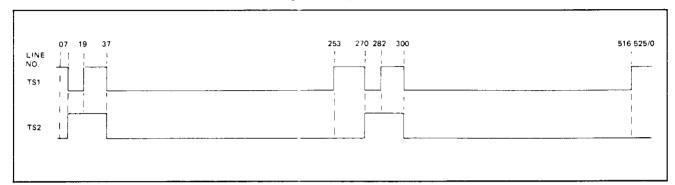


Fig.6 Time slot outputs

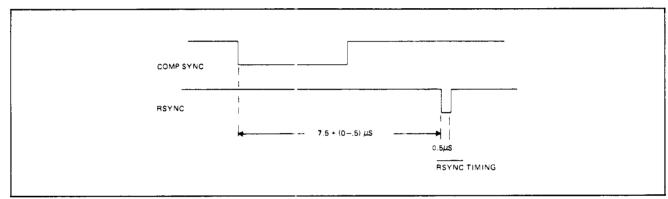


Fig.7 RSYNC timing

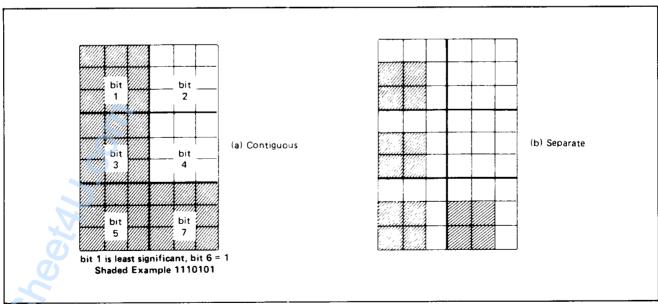


Fig.8 Graphics format

	b6 <u>b5</u>		000	001	0.	⁰ 1 ₀		1	¹ 0 ₀	101	¹ 1 ₀		111				
Bits	b4	b3	ь2	b1	Row	0	1	2	2a	3	За	4	5	6	l 6a	7	7a
	0	0	0	0	0	NULO	DLE®	_		0		@	P	<u> </u>		<u>р</u>	
	0	0	0	1	1	Alpha ⁿ Red	Graphics Red	<u>-</u>		1	a _	<u>A</u>	<u>a</u>	a		_ _ _	
	0	0	1	0	2	Alpha ⁿ Green	Graphics Green			2		 B	<u> </u>	<u>b</u>		<u>r</u>	
	0	0	1	1	3	Alpha ⁿ Yellow	Graphics Yellow	<u>£</u>		3		<u>C</u>	 S	<u>c</u>		<u>s</u>	
	0	1	0	0	4	Alpha ⁿ Blue	Graphics Blue	\$	 	4		 D	T -	<u>d</u>	5	<u>t</u>	
	0	1	0	1	5	Alpha ⁿ Magenta	Graphics Magenta	<u>%</u>		5		E	 	e	_	u	
	0	1	1	0	6	Alpha ⁿ Cyan	Graphics Cyan	<u>&</u>		6	2	F	 <u>V</u>	f f	5	<u>v</u>	Z
	0	1	1	1	7	Alpha ⁿ ② White	Graphics White			$\left \frac{-}{7} \right $		<u>G</u>	$\frac{1}{w}$	 _g	5	_w_	
	1	0	0	0	8	Flash	Conceal Display	<u>(</u>		8	Z	 	<u>X</u>	<u>h</u>	! <u> </u>	<u>×</u>	
	1	0	0	1	9	Steady	Contiguous Graphics)		9	5	1	<u>Y</u>	<u>i</u>	5	<u>y</u>	5
	1	0	1	0	10	End Box	Separated Graphics	*	1	;	2	J	<u>Z</u>	j		<u>z</u>	
	,	0	1	1	11	Start Box	ESC [©]	+			7	K	-	<u>k</u>	1	1/4	
	1	1	0	0	12	Normal [©] Height	Black [©] Background	<u>, </u>		<		L	$\frac{1}{\frac{1}{2}}$	<u> </u>		11	
	1	1	0	1	13	Double Height	New Background	· · ·		=		<u>M</u>		<u>m</u>	5	3/4	
	1	1	1	0	14	Special Graphics	Hold Graphics		_	>		N	1 1	<u>n</u>		÷	
	5	7	1	1	15	Normal D Graphics	Release [©] Graphics	/		?		0		0	! 5		

These control characters are reserved for compatibility with other data codes

These control characters are presumed before each row begins

Codes may be referred to by their column and rowled 2/5 refers to %

Character rectangle

Black represents display colour White represents background

Fig.9 Teletext character codes (501 character set)