LC03-6R2

Low Capacitance Surface Mount TVS for High-Speed Data Interfaces

The LC03–6 transient voltage suppressor is designed to protect equipment attached to high speed communication lines from ESD, EFT, and lighting.

Features:

- SO–8 Package
- Peak Power – 2000 Watts 8 x 20 μS
- ESD Rating:
  IEC 61000–4–2 (ESD) 15 kV (air) 8 kV (contact)
  IEC 61000–4–4 (EFT) 40 A (5/50 ns)
  IEC 61000–4–5 (lighting) 23 (8/20 μs)
- UL Flammability Rating of 94V–0

Typical Applications:

- High Speed Communication Line Protection

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Power Dissipation 8 x 20 μS @ T_A = 25°C (Note 1)	P_{pk}	2000	W
Junction and Storage Temperature Range	T_J, T_{stg}	–55 to +150	°C
Lead Solder Temperature – Maximum 10 Seconds Duration	T_L	260	°C

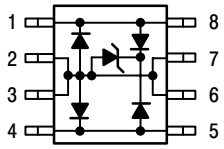
1. Non–repetitive current pulse 8 x 20 μS exponential decay waveform

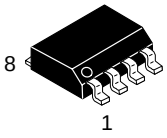
ON Semiconductor®

http://onsemi.com

SO–8 LOW CAPACITANCE VOLTAGE SUPPRESSOR 2 kW PEAK POWER 6 VOLTS

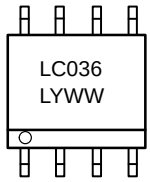
PIN CONFIGURATION AND SCHEMATIC





SO–8
CASE 751
PLASTIC

MARKING DIAGRAM



LC036= Device Code
L = Location Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
LC03–6R2	SO–8	2500/Tape & Reel

ELECTRICAL CHARACTERISTICS

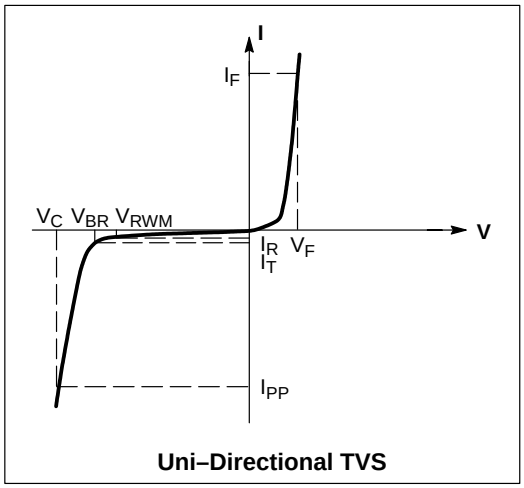
Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage @ I_t = 1.0 mA	V_{BR}	6.8	–	–	V
Reverse Leakage Current @ V_{RWN} = 5.0 Volts	I_R	N/A	–	20	μA
Maximum Clamping Voltage @ I_{PP} = 50 A, 8 x 20 μS	V_C	N/A	–	15	V
Maximum Clamping Voltage @ I_{PP} = 100 A, 8 x 20 μS	V_C	N/A	–	20	V
Between I/O Pins and Ground @ V_R = 0 Volts, 1.0 MHz	Capacitance	–	16	25	pF
Between I/O Pins @ V_R = 0 Volts, 1.0 MHz	Capacitance	–	8.0	12	pF

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

UNIDIRECTIONAL (Circuit tied to Pins 1 and 3 or 2 and 3)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
ΘV_{BR}	Maximum Temperature Coefficient of V_{BR}
I_F	Forward Current
V_F	Forward Voltage @ I_F
Z_{ZT}	Maximum Zener Impedance @ I_{ZT}
I_{ZK}	Reverse Current
Z_{ZK}	Maximum Zener Impedance @ I_{ZK}



Uni–Directional TVS

TYPICAL CHARACTERISTICS

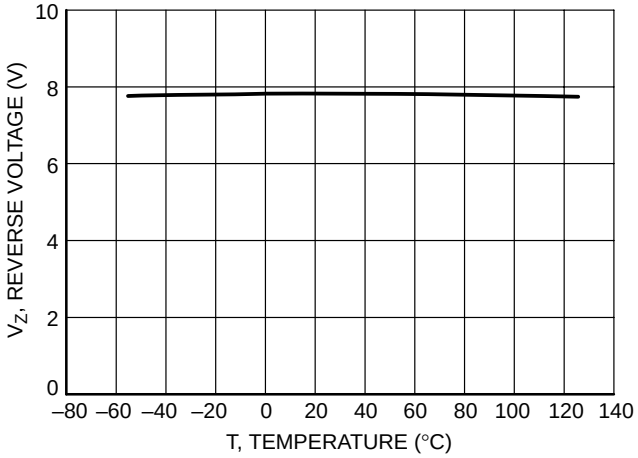


Figure 1. Reverse Voltage versus Temperature

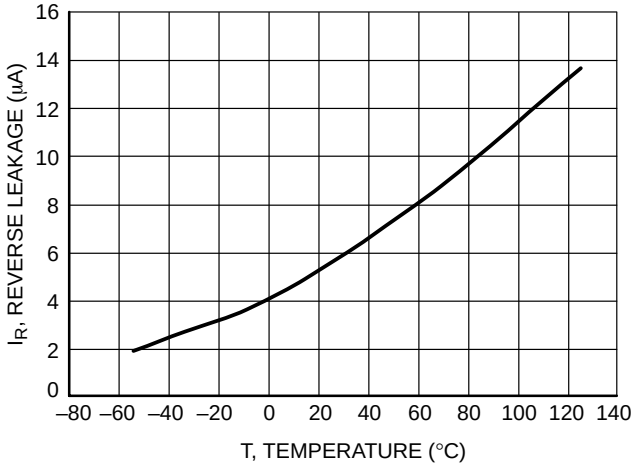


Figure 2. Reverse Leakage versus Temperature

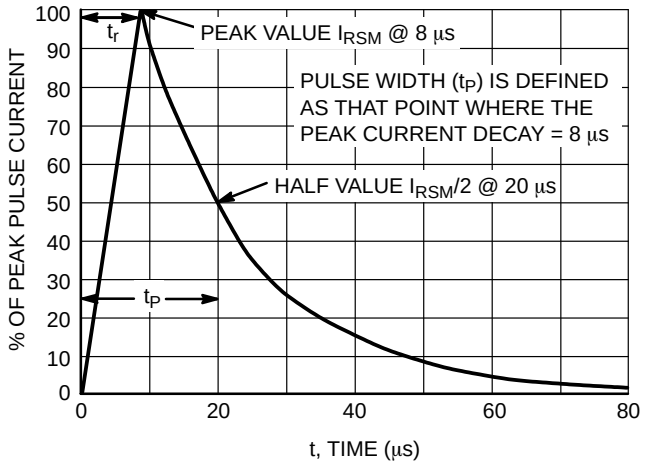


Figure 3. 8 × 20 μs Pulse Waveform

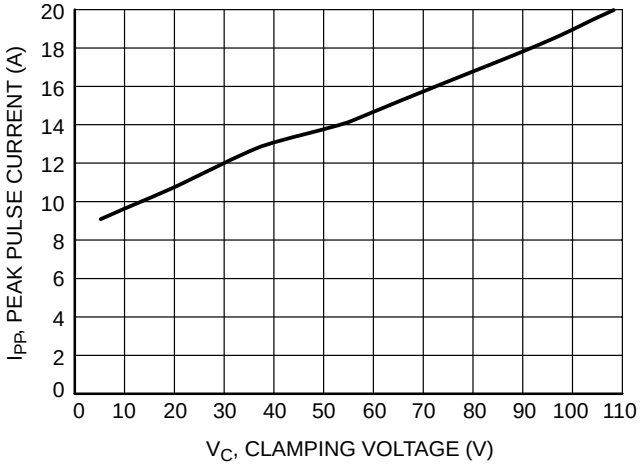


Figure 4. Clamping Voltage versus Peak Pulse Current

APPLICATIONS INFORMATION

The LC03–6 ON Semiconductor's device is a TVS Diode array designed to protect sensitive electronics such as communications systems, computers, and computer peripherals against damage due to transient over–voltage conditions caused by lightning, electrostatic discharge (ESD), and electrical fast transients (EFT). Because of its relative low capacitance (<25 pf), it can be used in high speed I/O data lines such as USB 1.1 ports.

The integrated design of the LC03–6 device offers high surge rating, low capacitance steering diodes, and a TVS diode integrated in a single package (SO–8). In addition, this device offers compliance to Bellcore 1089 requirements (intra–building).

LC03–6 Device's Configurations Options

Protection of Two High–speed I/O Data Lines

The LC03–6 device is able to protect two high speed data lines against transient over–voltage conditions by driving them to a fixed reference point for clamping purposes. Depending in the application's requirements, the LC03–6 device can be configured for protection in either differential mode (Line–to–Line) or common mode (Line–to–ground). The Figure 5 shows the connection for Differential mode (Line–to–Line) and Common mode (Line–to–Ground) protection. The inputs and outputs of the I/O data lines are connected at terminals 1 to 8, and 4 to 5 while the terminals 2, 3, 6 and 7 are connected to ground; for better performance, it is recommended to minimize parasitic inductances by using ground planes and minimizing the PCB trace lengths for the ground return connections.

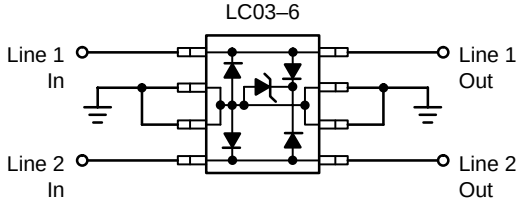


Figure 5. Configuration for Differential and Common Mode Protection

If differential protection is required by some particular applications, then the configuration for differential protection is made as shown in the Figure 6:

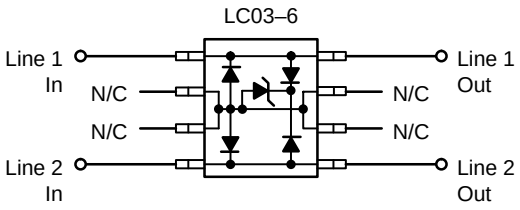


Figure 6. Configuration for Differential Protection (Line–to–Line)

T1/E1 Linecard Protection (Intra–Building)

The Figure 7 shows a typical schematic for a T1/E1 line card protection circuit. The LC03–6 device is connected between Tip & Ring on the transmit and receive line pairs. it provides protection to metallic and common mode lightning surges per Bellcore 1089 intra–building (For further information, see Bellcore 1089 standard). A metallic voltage is defined as a difference of potential between the T and R terminals of a telecommunications pair. Currents caused by lightning, in the absence of protector operation and with balanced terminal equipment and telecommunications loop, cause Tip and Ring conductors to attain the same potential hence do not produce metallic transients. Common mode surges are suppressed by the isolation of the transformer.

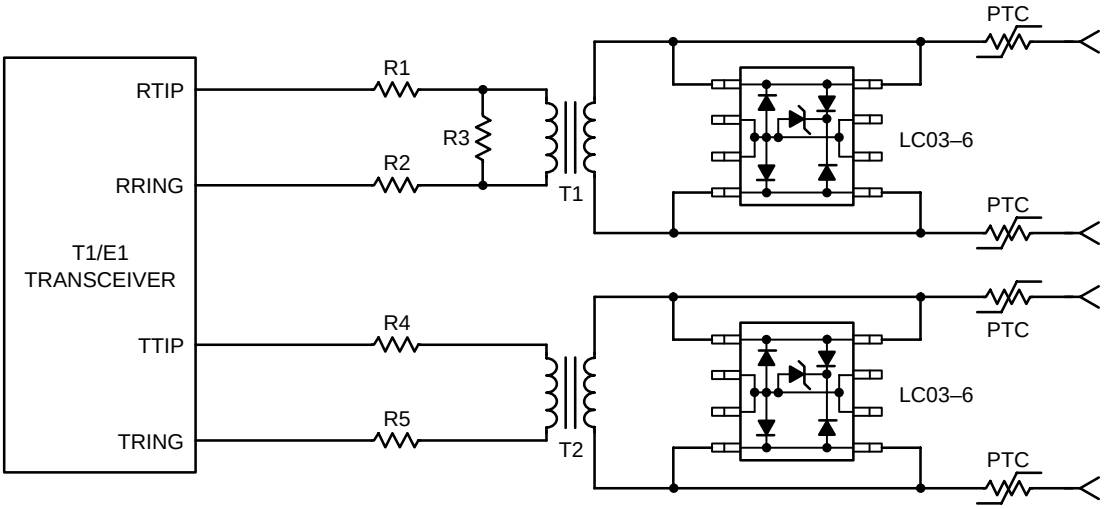


Figure 7. Typical T1 Line Card Protection

ESD Protection in USB 1.1 Port Applications

As know, a USB port is composed of four lines. The lines D+ & D– are used for bi–directional data transmission, and the remaining two lines are reserved for bus voltage and ground. Since USB is a hot plugging and unplugging system, all its four lines have the risk to receive ESD conditions in the real field of the application.

Typical ESD protection techniques are commonly formed by the combination of different discrete semiconductor products which make this technique obsolete and non–efficient because the interconnections of the discrete devices increase the parasitic inductance effects during a transient condition which reduces significantly the performance of the ESD protection circuit. The LC03–6 device provides a unique TVS Diode array designed to protect two I/O data lines (single USB port) against damage due to ESD conditions or transient voltage conditions. Because of its low capacitance, it can be used in high speed I/O data lines such as USB 1.1 components. In addition to its low capacitance characteristics, the LC03–6 device from ON Semiconductor complies with the most common industrial standards for ESD, EFT and surge protection: IEC61000–4–2, IEC61000–4–4, IEC61000–4–5. The Figure 8 illustrates how to connect the LC03–6 device in combination with the SRDA05–4 device to protect USB 1.1 ports against ESD conditions:

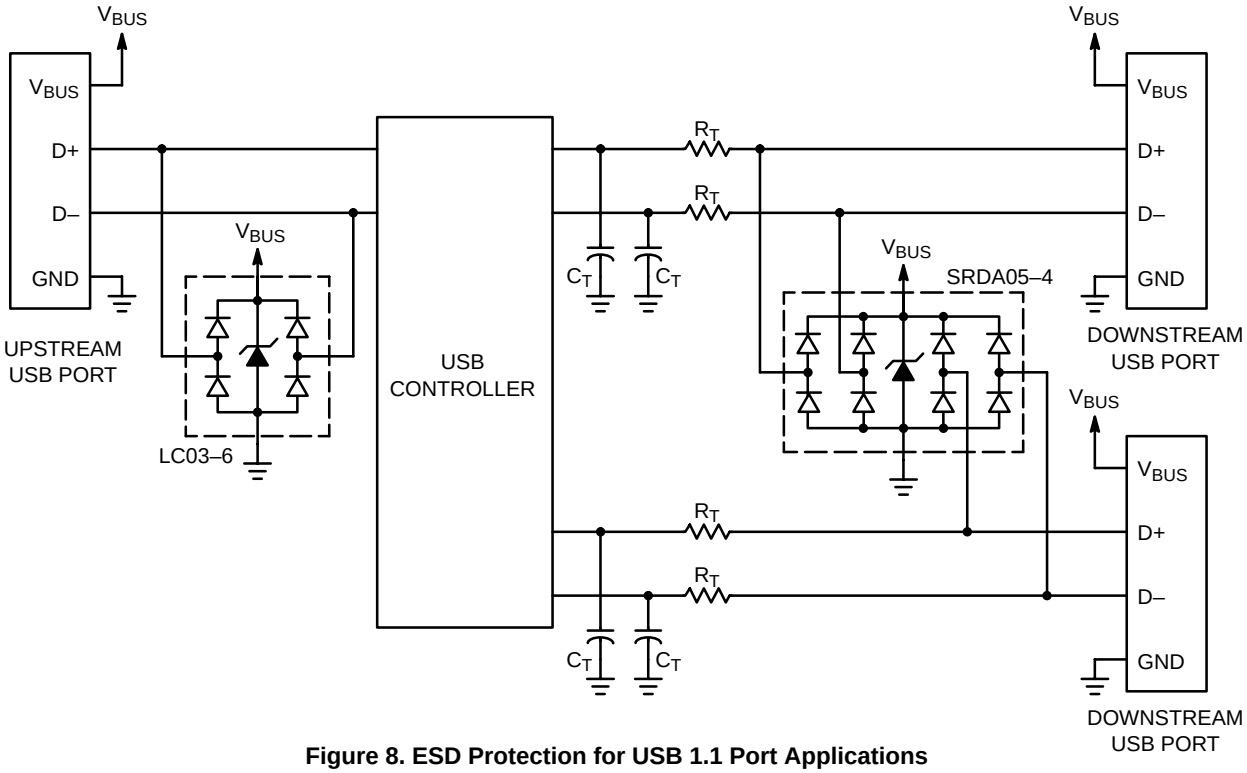
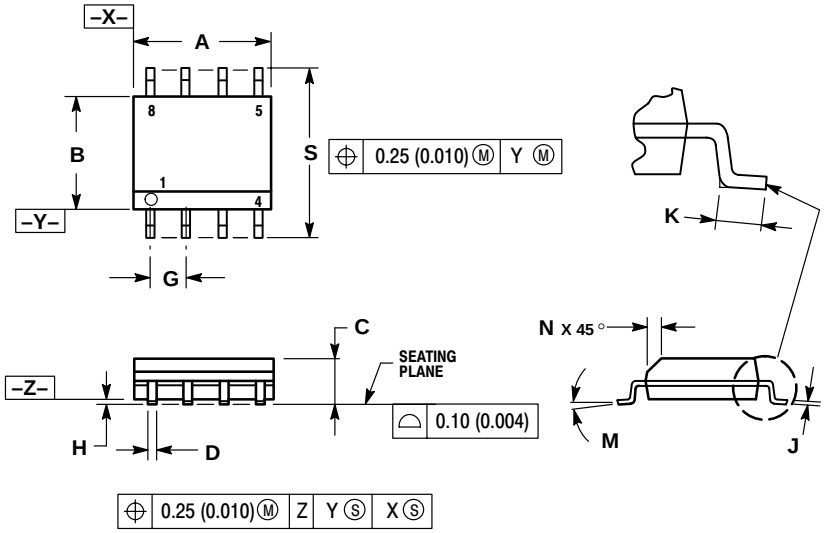


Figure 8. ESD Protection for USB 1.1 Port Applications

Transient Voltage Suppressor – Surface Mount

2 kW Peak Power

SO–8
CASE 751–07
ISSUE W



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031
Phone: 81–3–5740–2700
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local
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