FUJITSU

NMOS SINGLE-CHIP
4-BIT MICROCOMPUTER

MB8840/
MB8840H
SERIES

NMOS SINGLE-CHIP 4-BIT MICROCOMPUTER

TM336-A871: January 1987

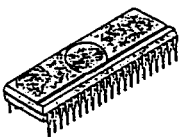
The Fujitsu MB8840 and MB8840H series are NMOS single chip microcomputer. Its architecture and instruction set are same as the CMOS MB8850 series.

The MB8840 series consists of the MB8842, 43, 44, 46, 47, and 48. And high-speed version of MB8840H series consists of the MB8841H and 45H. These series contain max. 2K by 8-bit mask ROM (program memory), max. 128 by 4-bit static RAM (data memory), max. 37 I/O lines (including serial port), and 8-bit timer/counter, a clock generator, and programmable logic array (PLA).

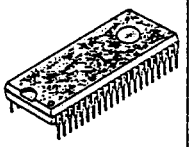
They are fabricated by the NMOS process, and operate with a single power supply and a max. 6MHz (4MHz) clock with prescaler over the temperature range of -30°C to +70°C. Minimum instruction execution time is 3.0μs of the MB8840 series and 2.0μs of the MB8840H series. And they are packaged in a 42-pin plastic standard/shrink DIP, 28-pin plastic standard/shrink DIP, or 48-pin plastic flat package.

For user's development of the MB8840 and MB8840H series based system, Fujitsu provides the MB8840/50 cross-assembler and host-emulator which run on the CP/M-86 or PC-DOS machine (cross-assembler also run on the Intellec series III MDS), and the MB2115 series evaluation board system, and the MB8850U/H piggyback EPROM evaluation devices which have external 2K x 8-bit EPROM. These development tools enables users to minimize their development time and cost.

MB8841HM/43M MB8841H-PSH/43-PSH

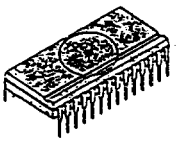


42-PIN PLASTIC STANDARD DIP
(DIP-42P-M01)

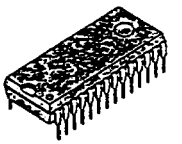


42-PIN PLASTIC SHRINK DIP
(DIP-42P-M02)

MB8842M/44M MB8842-PSH/44-PSH

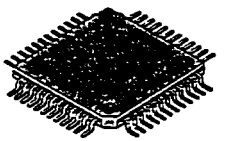


28-PIN PLASTIC STANDARD DIP
(DIP-28P-M02)



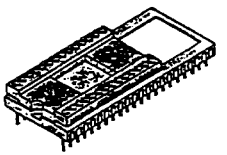
28-PIN PLASTIC SHRINK DIP
(DIP-28P-M03)

MB8845HM/46M/47M/48M



48-PIN PLASTIC FLAT PACKAGE
(FPT-48P-M02)

MB8850U/50H



42-PIN CERAMIC MODULE
(MDP-42C-P04)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FEATURES

- CMOS Single-chip 4-bit Microcomputer

- Program Memory:
  - o MB8841H/42 (MB8845H/46): 2K x 8-bit mask ROM
  - o MB8843/44 (MB8847/48) : 1K x 8-bit mask ROM

- Data Memory:
  - o MB8841H/42 (MB8845H/46): 128 x 4-bit static RAM
  - o MB8843/44 (MB8847/48) : 64 x 4-bit static RAM

- I/O Lines:
  - -MB8841H/43 (MB8845H/47):
    - o K-Port: 4-bit parallel input-only port
    - o P-Port: 4-bit parallel output-only port
    - o O-Port: 8-bit parallel output-only port
    - o R-Port: Four 4-bit parallel or 16 individual input/output ports
    - o C-Port: Serial I/O, interrupt input, timer/counter input, and timing output
  - -MB8842/44 (MB8846/48):
    - o K-Port: 4-bit parallel input-only port
    - o O-Port: 8-bit parallel output-only port
    - o R-Port: Two 4-bit parallel and one 3-bit parallel or 11 individual input/output ports
    - o C-Port: Interrupt input and timer/counter input

- Five Selectable Output Port Types for O-, P-, and R-Ports with Mask Option:
  - o Standard open-drain
  - o Standard pull-up
  - o High-current open-drain
  - o 12V interface open-drain (MB8841H/45H only)
  - o High-current pull-up (MB8841H/45H only)

- On-chip Mask-programmable PLA (Programmable Logic Array) for Data Conversion at O-Port

- 8-bit Programmable Timer/Counter with Two Clock Modes:
  - o Internal clock (Timer)
  - o External clock (Counter)

- Serial I/O with 4-bit Serial Buffer/Two Clock Modes (MB8841H/43/45H/47):
  - o Internal clock
  - o External clock

- Mask Option Serial Port Output Latch:
  - o With prescaler
  - o Without prescaler

- On-chip Clock Generator:
  - o Crystal/ceramic Resonator or External Clock Drive

- Mask Option Divid-by-two Clock Prescaler for Expanding Clock Range

- Single-level Three Priority Source Maskable Interrupt:
  - o External
  - o Timer/counter overflow
  - o Serial buffer full/empty

FEATURES (Continued)

- 4 Nesting Levels for Subroutine Call

- Instruction Set: Same as MB8850F/50B/50H series instruction set
  - o Number of instructions : 70(MB8841H/43/45H/47), 69(MB8842/44/46/48)
  - o Instruction length/cycle: 1 byte/1 cycle or 2 bytes/2 cycles
  - o Execution time :
    - o MB8841H/45H : 2 µs min. using 6 MHz clock with prescaler (or 3 MHz clock without prescaler)
    - o MB8842/43/46/48: 3 µs min. using 4 MHz clock with prescaler (or 2 MHz clock without prescaler)

- Single Power Supply Three Supply Voltage Versions:
  - o 4.5V to 5.5V (Active mode)

- Wide Operating Temperature Range:
  - o T_A= -30°C to +70°C

- Silicon-gate NMOS Process

- Five Package Types:
  - -MB8841H/43
    - o 42-pin plastic standard DIP: (Suffix M)
    - o 42-pin plastic shrink DIP: (Suffix -PSH)
  - -MB8842/44
    - o 28-pin plastic standard DIP: (Suffix M)
    - o 28-pin plastic shrink DIP: (Suffix -PSH)
  - -MB8845H/46/47/48
    - o 48-pin plastic flat package: (Suffix M)

- Powerful Development Support:
  - o Intellec Series III MDS cross-assembler (SM05212-A010)
  - o CP/M-86 and PC-DOS cross-assembler (SM07412-A012/SMXXXXX-XXXX)
  - o CP/M-86 and PC-DOS host emulator software for monitoring evaluation board and symbolic debugging (SM07412-G022/SMXXXXX-XXXX)
  - o MB2115 series evaluation board (-01, -02, -04, and -33A) for software debugging
  - o MB8850U and MB8850H CMOS piggyback EPROM evaluation device

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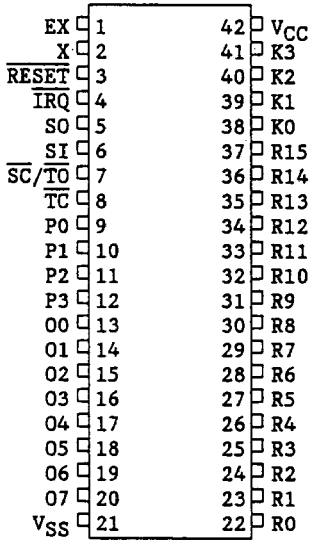
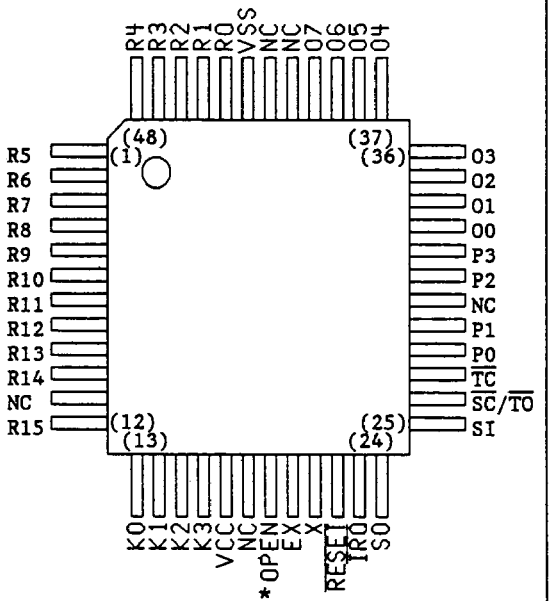
Fig. 1: PIN ASSIGNMENT

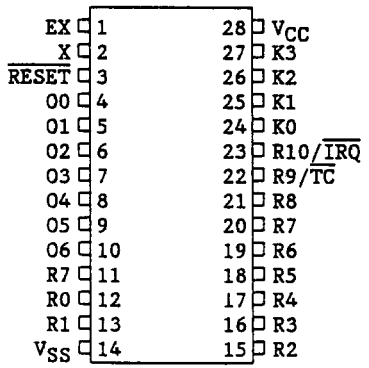
MB8841H/43(Top View)



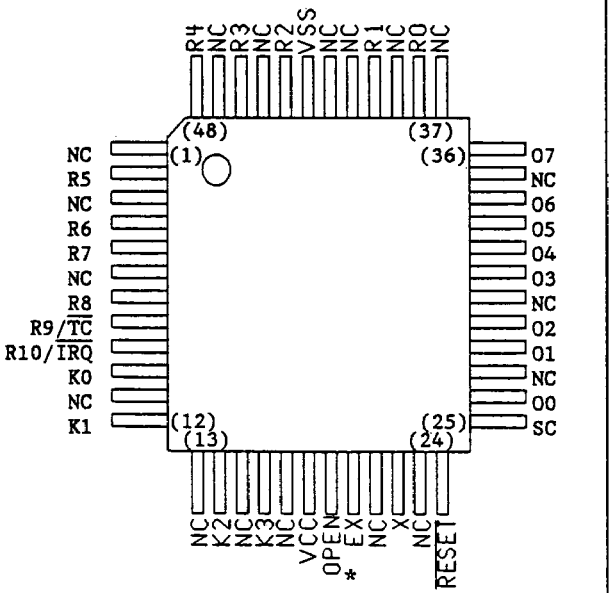
MB8845H/47 (Top view)



MB8842/44(Top View)



MB8846/48 (Top view)



* : This pin should not be connected must be left open.

Fig. 2: MB8841H/43/45H/47 LOGIC SYMBOLS

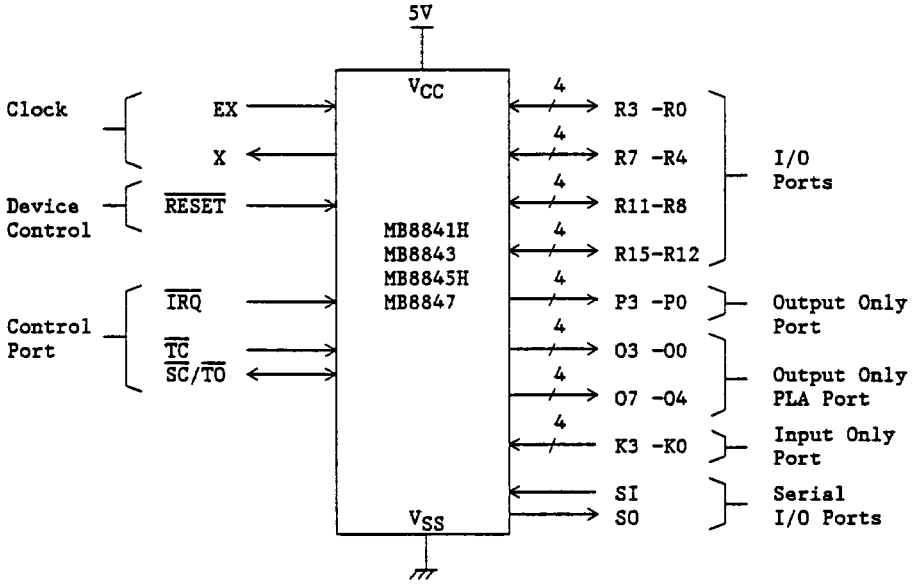


Fig. 3: MB8841H/43/45H/47 BLOCK DIAGRAMS

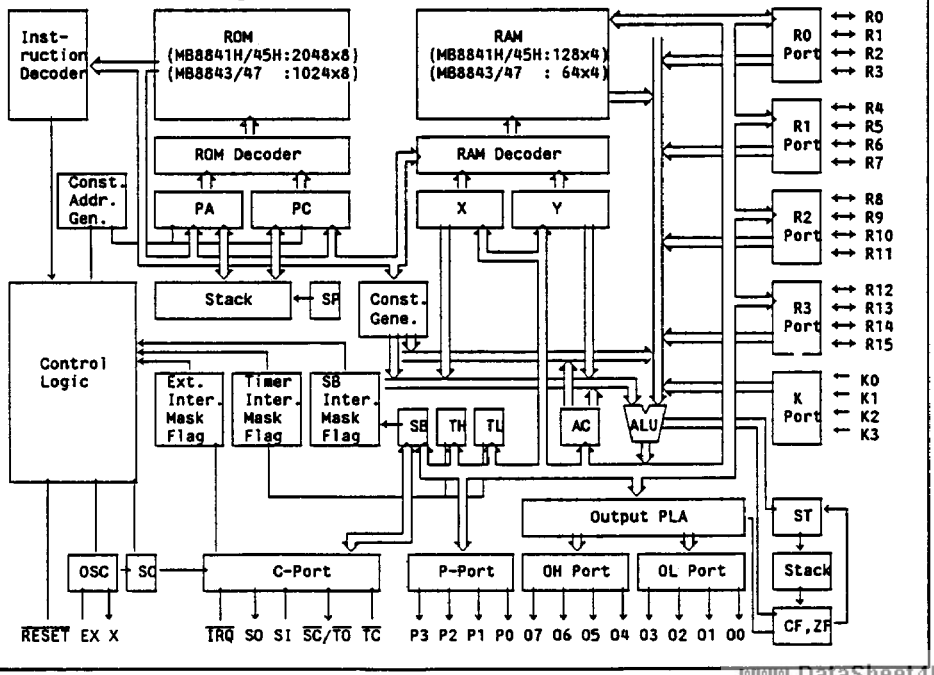
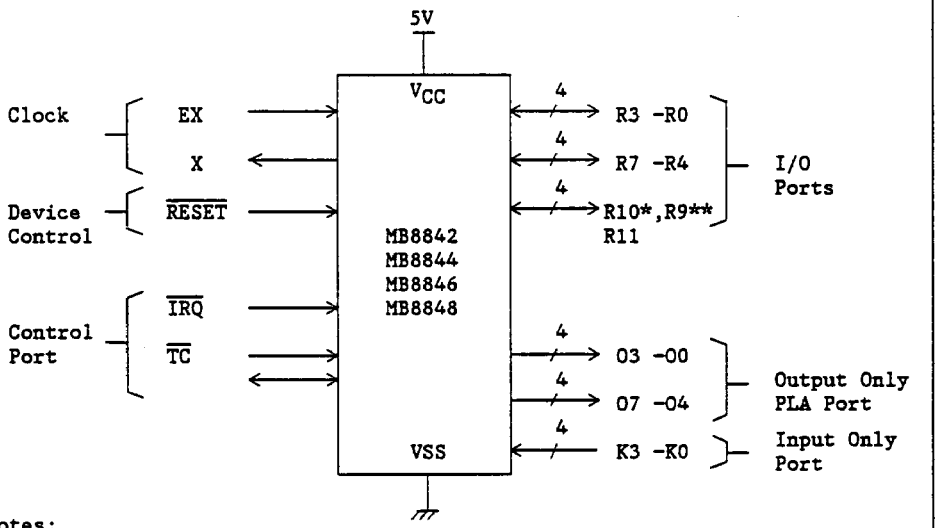
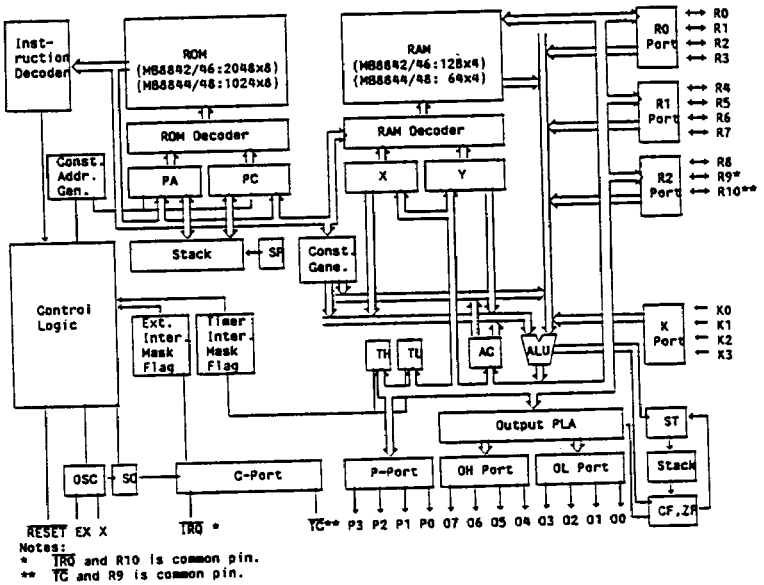


Fig. 4: MB8842/44/46/48 LOGIC SYMBOLS



Notes:
* IRQ and R10 is common pin.
** TC and R9 is common pin.

Fig. 5: MB8842/44/46/48 BLOCK DIAGRAMS



PIN DESCRIPTION

Fig. 1 and Table 1 show the pin assignment and pin description of the MB8840 and MB8840H series.

Table 1: PIN DESCRIPTION

Symbol	Pin No. MB8841H (MB8845H, MB8844 (MB8848))	Pin No. MB8842 (MB8846) MB8844 (MB8848)	Type	Name & Function
• Power Supply				
V_{CC}	42 (19)	28 (19)	-	+5V DC power supply pin.
V_{SS}	21 (41)	14 (41)	-	Ground pin.
• Clock				
EX	1 (20)	1 (20)	I	**Oscillator Input**: Input to the inverting amplifier that forms the on-chip oscillator. An external crystal/ceramic resonator or RC-network is connected between the EX and X pins. Either of these two oscillation types can be selected using mask option. When an external oscillator is used, the EX pin receives the external oscillator signal. This pin is a non-hysteresis input when the crystal/ceramic oscillator is selected, and a hysteresis input when the RC-network oscillator is selected. * MB8840 series crsytal/ceramic resonator and RC-network oscillator circuit is same.
X	2 (21)	2 (21)	O	**Oscillator Output**: Output of the inverting amplifier that forms the on-chip oscillator, and input to the internal clock generator. An external crystal/ceramic resonator or RC-network is connected between the EX and X pins. Either of these two oscillator types can be selected using mask option. When an external oscillator is used, the X pin should be left open.
• Device Control				
$\overline{RESET}$	3 (22)	3 (24)	I	**Reset**: An external reset input to the internal reset circuit. A low level on the $\overline{RESET}$ pin forcedly stops the MCU's operations, and initializes its internal state. After the $\overline{RESET}$ pin returns high, the MCU restarts execution of program from address #0 (of page #0). The $\overline{RESET}$ pulse must be low for at least two instruction cycles (12 clock periods: 6μs at 4MHz crystal with prescaler) while the oscillator is stably running after power on. An external capacitor (with an internal pull-up resistor) or RC-network, whose time constant should be enough longer than the reset time required, is needed as the external reset circuit.

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No. MB8841H (MB8845H) MB8844 (MB8848)	Pin No. MB8842 (MB8846) MB8844 (MB8848)	Type	Name & Function
• Device Control (Continued)				
$\overline{RESET}$	3 (22)	3 (24)	I	A power-on reset operation requires an external RC-network, whose time constant should be than the supply voltage (V_{CC}) rise time and the oscillator stabilization time. This pin is a hysteresis input with an internal pullup resistor.
• C-Port				
$\overline{IRQ}$	4 (23)	23 (9)	I	**Interrupt Request**: A maskable external interrupt input. The falling edge of $\overline{IRQ}$ pulse sets the external interrupt request flag to generate an external interrupt request, only if the external interrupt is enabled in advance by EN instruction. Also, the $\overline{IRQ}$ pin state, which is reflected in the external interrupt input flag (IF) regardless of enabling/disabling the external interrupt, is testable using TSTI instruction. (When $\overline{IRQ}$=L, IF=1; otherwise IF=0.) The $\overline{IRQ}$ pin is common to the R10 pin (MB8842/46 and MB8844/48). Either of them is selectable using software. This pin is a non-hysteresis input with an internal pullup resistor.
$\overline{TC}$	8 (27)	22 (8)	I	**Timer/Counter**: An external count clock input to the on-chip timer/counter. The falling edge of $\overline{TC}$ pulse increments the timer/counter by one bit when the external count clock (counter) mode is enabled by EN instruction. This pin is inactive when the external count clock mode is disabled by DIS instruction or reset. This $\overline{TC}$ pin is common to the R9 pin (MB8842/46 and MB8844/48). Either of them is selectable using software. This pin is a non-hysteresis input with an internal pullup resistor.
$\overline{SC}/\overline{TO}$	7 (26)	-	I/O	**Shift Clock/Timing Output**: One of the shift clock input ($\overline{SC}$), shift clock output ($\overline{SC}$), and synchronous timing output ($\overline{TO}$) is enabled using EN instruction.
			I	$\overline{SC}$: 1) Shift clock input to the on-chip serial port: When the external shift clock mode is enabled for the serial port, the falling edge of the external $\overline{SC}$ clock shifts the contents of the serial buffer one bit right

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No. MB8841H (MB8845H) MB8844 (MB8848)	Pin No. MB8842 (MB8846) MB8844 (MB8848)	Type	Name & Function
• C-port (Continued)				
$\overline{SC}/\overline{TO}$	7 (26)	-	I/O	(from MSB to LSB). This input is inactive when the external clock mode is disabled by DIS instruction or reset. This pin is a non-hysteresis input. 2) Shift clock output from the on-chip serial port: When the internal shift clock mode is enabled, the internal shift clock (the on-chip state counter output ϕ1: 1/6 of clock generator frequency) shifts the contents of the serial buffer one bit right. In this mode, an internal timing signal, which is generated by the on-chip state counter outputs, ϕ1 and ϕ2 is output onto the $\overline{SC}$ pin for synchronization.
			O	$\overline{TO}$: Synchronous timing output: When the timing output is enabled, the internal timing signal same as the $\overline{SC}$ output in the internal shift clock mode is output onto the $\overline{TO}$ pin. By DIS instruction or reset, the $\overline{TO}$ pin is disabled and stops issuing the timing output.
SI	6 (25)	-	I	**Serial Data Input**: Data input to the on-chip serial buffer register. The falling edge of the external or internal shift clock ($\overline{SC}$) shifts the data bit on the SI pin into the MSB of the serial buffer when the serial port is enabled by EN instruction. This pin is inactive when the serial port is disabled by DIS instruction or reset. This pin is a non-hysteresis input with an internal pull-up resistor.
SO	5 (24)	-	O	**Serial Data Output**: Data output of the on-chip serial buffer register. An output latch can be provided for the SO pin using mask option. Without the output latch, the LSB data of the serial buffer appears directly to the SO pin. With the output latch implemented, the LSB data is output to the SO pin after it is shifted into the output latch at the falling edge of the external or internal shift clock ($\overline{SC}$). This pin is set high by reset when the output latch is implemented.

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Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No. MB8841H (MB8845H, MB8844, MB8848)	Pin No. MB8842 (MB8846, MB8844, MB8848)	Type	Name & Function
• I/O Port				
K3-K0	41-38 (16-13)	27-24 (16,14, 12,10)	I	**K-Port**: A 4-bit parallel non-latched input-only port. K0 is LSB. 4-bit data on K-Port is input into the accumulator by INK instruction. These pins are internally pullup.
P3-P0	12- 9 (32,31, 29,28)	-	O	**P-Port**: A 4-bit parallel latched output-only port. P0 is LSB. 4-bit data in the accumulator is output to P-Port by OUTP instruction. Refer to Table 4 User mask options for available masking option.
O3-O0, O7-O4	16-13, (36-33) 20-17 (40-37)	7- 4 (31,29, 28,26) 11- 8 (36,34, 33,32)	O	**O-Port**: An 8-bit parallel latched output-only port with the on-chip mask-programmable PLA (Programmable Logic Array) for output data conversion. Depending on user's PLA pattern, this port functions as a dual 4-bit parallel output or an 8-bit parallel PLA output. Dual 4-bit parallel output: By OUTO instruction, 4-bit data in the accumulator is output, without conversion, onto the lower nibble (O3-O0) or upper nibble (O7-O4) of O-Port, depending on whether the carry flag (CF) is "0" or "1". 8-bit parallel PLA output: By OUTO instruction, 4-bit data in the accumulator and the carry flag (CF) bit are converted into 8-bit data through the PLA array, and the 8-bit data is output to O-Port. Depending on user's PLA pattern, 32 kinds of 8-bit data conversions are possible. For example, it can be encoded into 8-segment data for LED display. Refer to Table 4 User mask options for available masking option.
R3 -R0, R7 -R4, R11, R10-R8, R15-R12	25-22, (49-44) 29-26, (3-1, 48) 33,(7) 32-30, (6-4) 37-34 (12, 10-8)	16,15, 13,12 (46,44, 40,38) 20-17 (5,4, 2,48) - 23-22, (9-7)	I/O	**R-Port**: This port functions as four 4-bit parallel input (non-latched)/output (latched) ports, or 16 individual input (non-latched)/output (latched) lines, depending on instructions. Parallel I/O: Each 4-bit port is named R-Port #0 (R3-R0), R-Port #1 (R7-R4), R-Port #2 (R11-R8), and R-Port #3 (R15-R12), and is indirectly addressed by the Y-register (Port #). 4-bit data in the accumulator is output to an addressed port of R-Ports #0 to #3 by OUT instruction. 4-bit data on the addressed port is input into the accumulator by IN instruction. (Before IN instruction, the

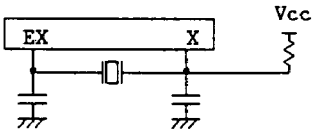
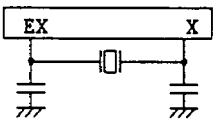
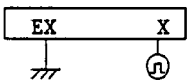
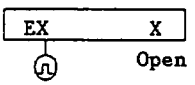
Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No. MB8841H (MB8845H) MB8844 (MB8848)	Pin No. MB8842 (MB8846) MB8844 (MB8848)	Type	Name & Function
• I/O Port (Continued)				
R3 -R0,	25-22, (49-44)	16,15, 13,12 (46,44, 40,38)	I/O	port to be addressed must be set up to "1" state (input) mode).) Individual I/O: Each line from R15 to R0 is indirectly addressed by the Y-register (Bit #). The addressed line is individually set/reset by SETR/RSTR instruction, and especially each line of R-Port #0 (R3-R0) is directly set/reset by SETD/RSTD instruction. The addressed line is individually testable by TSTR instruction, and each line of R-Port #2 (R11-R8) is directly testable in paticular by TSTD instruction. (Before the TSTR and TSTD instructions, the line to be addressed must be set up to "1" (input mode).) Refer to Table 4 User mask options for available masking option. MB8842/46: The R9 pin is common to the $\overline{TC}$ pin. and MB8844/48 R10 is $\overline{IRQ}$ pin.
R7 -R4,	29-26, (3-1, 48)	20-17 (5,4, 2,48)		
R11,	33,(7)	-		
R10-R8,	32-30, (6-4)	23-22, (9-7)		
R15-R12	37-34 (12, 10-8)			

Note: Parenthis number is applied to MB8845H/46/47/48.

DIFFERENCES BETWEEN MB8840 SERIES AND MB8840H SERIES

Table 2: DIFFERENCES BETWEEN MB8840 SERIES AND MB8840H SERIES

Device / Item	MB8840 Series	MB8840H Series
Operating Frequency Range (Minimum Instruction Execution Time)	fc=0.5MHz to 2MHz without prescaler, or 1MHz to 4MHz with prescaler (12µs to 3µs)	fc=0.5MHz to 3MHz without prescaler, or 4Mz to 8MHz with prescaler (3µs to 1.5µs)
Clock Circuit Configuration	Crystal/Ceramic oscillation 	Crystal/Ceramic oscillation 
	External clock drive 	External clock drive 
K-Port Input Level	Standard threshold input	Standard or high threshold input (Mask option)
Output Port Level During Reset	High level (Fixed)	High or low level (Mask option) (O0-3 & R0-3 are fixed at high)
Output Port Type (O-, P-, and R-Ports)	· Standard open-drain · Standard pull-up · High-current open-drain (Mask option)	· Standard open-drain · Standard pull-up · High-current open-drain · High-current pull-up · 12V-interface open-drain (Mask option)
Members	· MB8842M/-PSH, MB8846M · MB8843M/-PSH, MB8847M · MB8844M/-PSH, MB8848M	· MB8841HM/-PSH, MB8845HM

INPUT/OUTPUT CIRCUITS

All input-only pins are internally pulled up, and all output-only and input/output pins except O-, P-, and R-Ports have push-pull output buffer (standard pull-up). O-, P-, and R-Ports can have push-pull (standard or high-current* pull-up) or open-drain (standard, high-current, or 12V-interface*) buffer using mask option.

* MB8840H series only

Table 3: INPUT/OUTPUT CIRCUITS

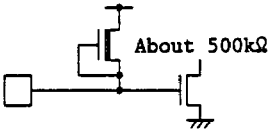
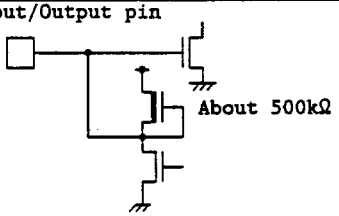
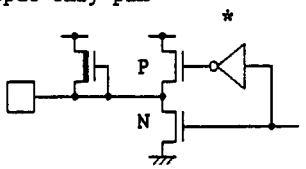
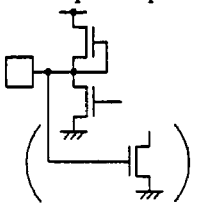
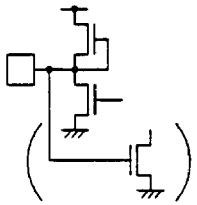
Pin	Circuit	Note
$\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, $\overline{\text{TC}}$, SI, K-Port	• Input only pin 	IIL ≤ -60μA (VCC = 5.5V, VIL = 0.4V)
$\overline{\text{SC}}$/$\overline{\text{TO}}$	• Input/Output pin 	IIL ≤ -3.2μA (VCC = 5.5V, VIL = 0.4V)
SO	• Output only pin 	VOH ≥ 2.4V (VCC = 4.5V, IOH = -200μA) VOL ≤ 0.4V (VCC = 4.5V, IOL = 1.8mA)
O-Ports, P-Ports, R-Ports	• Standard pull-up 	VOH ≥ 2.4V (VCC = 4.5V, IOH = -200μA) VOL ≤ 0.4V (VCC = 4.5V, IOL = 1.8mA) Internal pullup resistor approx. 5kΩ.
	• High-current pull-up (MB8841H/45H) 	VOH ≥ 2.4V (VCC = 4.5V, IOH = -200μA) VOL ≤ 0.4V (VCC = 4.5V, IOL = 1.8mA) VOL ≤ 2.0V (VCC = 4.5V, IOH = 20 mA)

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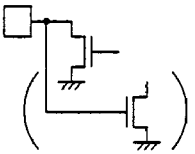
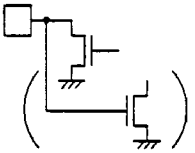
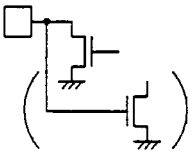
Table 3: INPUT/OUTPUT CIRCUITS (Continued)

Pin	Circuit	Note
O-Ports, P-Ports, R-Ports	• Standard open-drain 	VOL ≤ 0.4V (VCC = 4.5V, IOL = 1.8mA) (With 5kΩ pull-up resister)
	• High-current open-drain 	VOL ≤ 0.4V (VCC = 4.5V, IOL = 1.8mA) VOL ≤ 2.0V (VCC = 4.5V, IOH = 20 mA) (With 5kΩ pull-up resistor)
	• 12V interface open-drain (MB8841H/45H) 	VOL ≤ 0.4V (VCC = 4.5V, IOL = 1.8mA) (With 5kΩ pull-up resistor)

USER MASK OPTIONS

The MB8840 series has the following mask options, which must be specified by the customer on the attached data release form when devices are ordered.

Table 4: MB8840 SERIES USER MASK OPTIONS

Optional Feature	Symbol	Option	Option No.	Note
Clock Prescaler	CLK	No	0	f_C=0.5 MHz to 2.0 MHz
		Yes	1	f_C=1.0 MHz to 4.0 MHz
Output PLA Data	SPLA	4-bit parallel output	0	
		8-bit parallel output	1	Customer's output PLA data is needed.
Serial Port Output Latch	SRL	No	0	
		Yes	1	
Output Port Type	PORT	Standard open-drain	0/L	Output port circuit option selected must be the same for all O-, P-, and R-Ports.
		Standard pull-up	1/M	
		High-current open-drain	2/K	

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USER MASK OPTIONS

The MB8840H series has the following mask options, which must be specified by the customer on the attached data release form when devices are ordered.

Table 4: MB8840H SERIES USER MASK OPTIONS

Optional Feature	Symbol	Option	Option No.	Note
Clock Prescaler	CLK	No	0	f_C=0.5 MHz to 3.0 MHz
		Yes	1	f_C=1.0 MHz to 6.0 MHz
Oscillator Circuit	OSC	Crystal/ceramic OSC or external clock*	0	* When only external clock drive is used, we recommend RC-network oscillator.
		RC-network OSC or external clock*	1	We recommend no clock prescaler.
Output PLA Data	SPLA	4-bit parallel output	0	
		8-bit parallel output	1	Customer's output PLA data is needed.
Serial Port Output Latch	SRL	No	0	
		Yes	1	
Output Port Type	PORT	High-current open-drain	1/K	Output port circuit option selected must be the same for all O-, P-, and R-Ports.
		Standard open-drain	2/L	
		Standard pull-up	3/M	
		12V interface open-drain	4/G	
		High-current pull-up	5/T	
Output Port Level During Reset	RST	Low	0	
		High	1	O3-O0 and R3-R0 fixed high.
K-Port Input Threshold Level	STOP	Standard threshold	0	VIH=2.0V to VCC VIL=0.3V to 0.8V
		High threshold	1	VIH=2.4V to VCC VIL=-0.3V to 1.2V

NOTES ON OPERATION

- **Treatment of Unused Pins**

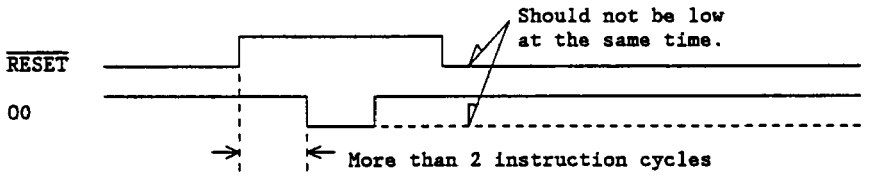
  Unused input pins should be pulled up or down with external resistors or they may cause some malfunction. (However, the X pin should be open when an external clock oscillator is used.)

- **Special Function of O0 Pin**

  The O0 pin has another function as a test terminal, in addition to its normal function O-Port. If the O0 pin is forced low while the $\overline{\text{RESET}}$ pin is low, the MCU is placed in the test mode. Therefore, the O0 pin should not be forced low while the $\overline{\text{RESET}}$ pin is low (when all output ports are initialized).

  Especially when the open-drain is selected for the output port option, the O0 pin should be externally pulled up because such open-drain outputs are subject to noise disturbance, if left floating.

  At least 2 instruction cycles are required to change O0 pin from high to low after releasing reset ($\overline{\text{RESET}}$: Low → High)



- **Supply Voltage**

  Malfunction may occur even within the recommended operating supply voltage if the supply voltage changes rapidly. Therefore, the supply voltage should be regulated as well as possible. The following conditions are recommended for the power supply:
  (1) V_{CC} ripple (peak-to-peak value) at commercial frequency (50Hz to 60Hz): Less than 10% of typical V_{CC} value.
  (2) V_{CC} transient change rate (such as at switching of power supply): Less than 0.1V/ms.

INSTRUCTION SET DESCRIPTION

The MB8840 and MB8840H series instruction set includes 70 (69) instructions, 93% of which are single-byte and single-cycle, and 7% two-byte and two-cycle. The MB8840 and MB8840H series instruction set is exactly the same as the MB8850 series instruction set, and is divided into ten functional groups:

- Register-to-register transfer
- Register-to-memory transfer
- Constant transfer
- Arithmetic and logical operations
- Bit manipulation
- Control
- Input/Output
- Branch
- Flag manipulation
- Other

Tables 5 and 6 summarize the MB8840 and MB8840H series instruction set.

Table 5: INSTRUCTION SET SUMMARY

	Mnemonic +operand	Code (Hex.)	Flag/Status ZF	CF	ST	Byte/ Cycle	Operation
Register-to-Register Transfer	TATH	05	·	·	·	1/1	TH←(AC)
	TATL	06	·	·	·	1/1	TL←(AC)
	TAS	07	·	·	·	1/1	SB←(AC)
	TAY	04	·	·	·	1/1	Y←(AC)
	TSA	17	↕	·	·	1/1	AC←(SB)
	TTHA	15	↕	·	·	1/1	AC←(TH)
	TTLA	16	↕	·	·	1/1	AC←(TL)
	TYA	14	↕	·	·	1/1	AC←(Y)
	XX	1B	↕*1	·	·	1/1	(AC)≠(X)
Register-to-Memory Transfer	L	0D	↕	·	·	1/1	AC←{M(X,Y)}
	LS	2B	↕	·	·	1/1	SB←{M(X,Y)}
	ST	1D	·	·	·	1/1	M(X,Y)←(AC)
	STDC	1A	↕*2	·	↓C	1/1	M(X,Y)←(AC), Y←(Y)-1
	STIC	0A	↕*2	·	↓C	1/1	M(X,Y)←(AC), Y←(Y)+1
	STS	2A	↕	·	·	1/1	M(X,Y)←(SB)
	X	0B	↕*1	·	·	1/1	(AC)≠{M(X,Y)}
	XD D	50-53*	↕*1	·	·	1/1	(AC)≠{M(0,D)}; D=0 to 3 (X=0, Y=D)
	XYD D	54-57*	↕*2	·	·	1/1	(Y) ≠{M(0,D)}; D=4 to 7 (X=0, Y=D)
Constant Transfer	CLA	90	↓	·	·	1/1	AC←0 (Included in LI instruction)
	LI imm	90-9F*	↕	·	·	1/1	AC←imm; imm=0 to 15
	LXI imm	58-5F*	↕	·	·	1/1	X3←0, X2 to X0←imm; imm=0 to 7
	LYI imm	80-8F*	↕	·	·	1/1	Y ←imm; imm=0 to 15
Arithmetic & Logical Operations	ADC	0E	↕	↕	↓C	1/1	AC←(AC)+{M(X,Y)}+(CF)
	AI imm	70-7F*	↕	↕	↓C	1/1	AC←(AC)+imm; imm=0 to 15
	AND	0F	↕	·	↓Z	1/1	AC←(AC)∩{M(X,Y)}
	C	2E	↕	↕	↓Z	1/1	{M(X,Y)}-(AC)
	CI imm	B0-BF*	↕	↕	↓Z	1/1	imm-(AC); imm=0 to 15
	CYI imm	A0-AF*	↕	↕	↓Z	1/1	imm-(Y) ; imm=0 to 15
	DAA	10	·	↕	↓C	1/1	AC←(AC)+6 if (AC)>9 or (CF)=1
	DAS	11	·	↕	↓C	1/1	AC←(AC)+10 if (AC)>9 or (CF)=1
	DCA	7F	↕	↕	↓C	1/1	AC←(AC)+15 (Included in AI instruc-
	DCM	19	↕	·	↓C	1/1	M(X,Y)←{M(X,Y)}-1 tion)
	DCY	18	·	·	↓C	1/1	Y←(Y)-1
	EOR	2F	↕	·	↓Z	1/1	AC←{M(X,Y)}⊕(AC)

Table 5: INSTRUCTION SET SUMMARY (Continued)

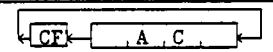
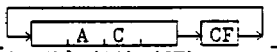
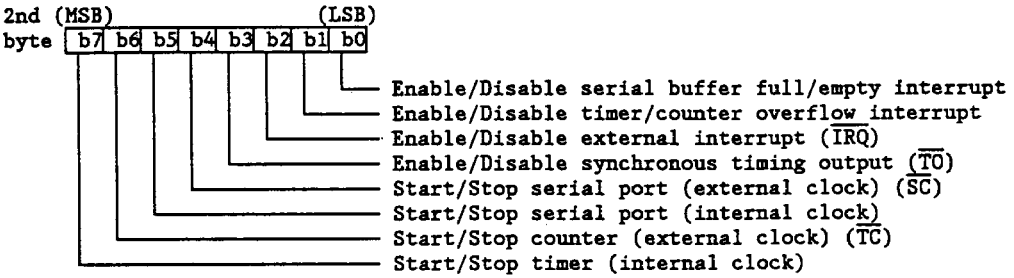
	Mnemonic +Operand	Code (Hex.)	Flag/Status ZF	CF	ST	Byte/ Cycle	Operation
Arithmetic & Logical Operation	ICA	71	↕	↕	↓C	1/1	AC←(AC)+1 (Included in AI instruc-
	ICM	09	↕	·	↓C	1/1	M(X,Y)←{M(X,Y)}+1 tion)
	ICY	08	↕	·	↓C	1/1	Y←(Y)+1
	NEG	2D	·	·	↓Z	1/1	AC←$\overline{(AC)}$+1
	OR	1F	↕	·	↓Z	1/1	AC←{M(X,Y)}∪(AC)
	ROL	0C	↕	↕	↓C	1/1	
	ROR	1C	↕	↕	↓C	1/1	
	SBC	1E	↕	↕	↓C	1/1	AC←{$\overline{M(X,Y)}$}-(AC)-(CF)
Bit Manipulation	RBIT bp	34-37*	·	·	·	1/1	{M(X,Y)}bp←0; bp=0 to 3
	SBIT bp	30-33*	·	·	·	1/1	{M(X,Y)}bp←1; bp=0 to 3
	TBA bp	4C-4F*	·	·	↓Z	1/1	(AC)bp-1 ; bp=0 to 3
	TBIT bp	38-3B*	·	·	↓Z	1/1	{M(X,Y)}bp-1; bp=0 to 3
Control	EN imm	3E00-3EFF*	·	·	·	2/2	Enable the internal resources by the operand byte (2nd byte); *3
	DIS imm	3F00-3FFF*	·	·	·	2/2	Disable the internal resources by the operand byte (2nd byte); *3
Input/ Output	IN	13	↕	·	·	1/1	AC←(R)Y ; Y=0 to 3 (Port #)
	INK	12	↕	·	·	1/1	AC←(K)
	OUT	03	·	·	·	1/1	(R)Y←(AC); Y=0 to 3 (Port #)
	OUTO *4	01	·	·	·	1/1	O←OPLA(AC, CF); OPLA: Output PLA function determined
	OUTP	02	·	·	·	1/1	P←(AC) by PLA pattern
	RSTD d	44-47*	·	·	·	1/1	(R)d←0; d=0 to 3 (Bit # of Port #0)
	RSTR	22	·	·	·	1/1	(R)Y←0; Y=0 to 15 (Bit #)
	SETD d	40-43*	·	·	·	1/1	(R)d←1; d=0 to 3 (Bit # of Port #0)
	SETR	20	·	·	·	1/1	(R)Y←1; Y=0 to 15 (Bit #)
	TSTD d	48-4B*	·	·	↓Z	1/1	(R)d-1; d=8 to 11 (Bit #)
	TSTR	24	·	·	↓Z	1/1	(R)Y-1; Y=0 to 15 (Bit #)
Branch	CALL addr	6000-67FF *	·	·	·	2/2	If ST=1, Subroutine Call for addr; addr=0 to 2047 ST=0, Not Subroutine Call.
	JMP addr	C0-FF*	·	·	·	1/1	If ST=1, Branch to addr; addr=0 to 63 ST=0, No Branch.
	JPA addr	3D00-3DFF *	·	·	·	2/2	Branch always to addr on page #n; addr=(AC) x 4, n=0 to 31
	JPL addr	6800-6FFF *	·	·	·	2/2	If ST=1, Branch to addr; addr=0 to 2047 ST=0, No Branch.
	RTI	3C	·	·	·	1/1	Return From Interrupt Routine
	RTS	2C	·	·	·	1/1	Return From Subroutine
Flag Manipulation	RSTC	23	·	↓	·Z	1/1	CF←0
	SETC	21	·	↑	·Z	1/1	CF←1
	TSTC	28	·	·	↓CF	1/1	(CF)-1
	TSTI	25	·	·	↓IF	1/1	(IF)-1, (If $\overline{IRQ}$=L, IF=1)
	TSTS	27	·	·	↓SF	1/1	(SF)-1, SF←0
	TSTV	26	·	·	↓VF	1/1	(VF)-1, VF←0
	TSTZ	29	·	·	↓ZF	1/1	(ZF)-1
Other	NOP	00	·	·	·	1/1	No Operation

Table 5: INSTRUCTION SET SUMMARY (Continued)

Notes:

*1: ZF is set or reset depending on contents of AC after instruction execution.
*2: ZF is set or reset depending on contents of Y after instruction execution.
*3: Each bit of the operand (the second byte) functions as follows:



*4: MB8841H/43/45H/47

Symbols and Abreviations

Symbols	Meaning
←	Is transferred to
⇄	Is exchanged with
+	Arithmetic plus
-	Arithmetic minus
⊕	Logical exclusive or
∩	Logical OR
∪	Logical AND
$\overline{\quad}$ (Overline)	Negation
( )	Contents of parenthesis
↑	Set to "1" always
↓	Set to "0" always
↕	Affected (set or reset) by operation results
↓C	Set to "0" due to carry (not carry flag)
↓CF	Set to "0" due to carry flag
↓IF	Set to "0" due to interrupt flag
↓SF	Set to "0" due to serial buffer full/empty flag
↓VF	Set to "0" due to timer/counter overflow flag
↓Z	Set to "0" due to zero (not zero flag)
↓ZF	Set to "0" due to zero flag
·	Not affected

Abbreviations	Meaning
AC	Accumulator
addr	Jump address
bp	Bit pointer (that is part of the instruction code)
C	Carry
CF	Carry flag
d	Direct line number (that is part of the instruction code)
D	Direct data memory address (that is part of the instruction code)
IF	Interrupt flag
imm	Immediate data
IRQ	Interrupt request
K	K-Port (K3 to K0)
LSB	Least significant bit
M(X,Y)	Data memory (RAM) location indirectly addressed by data pointer (X- and Y-registers)
M(0,D)	Data memory (RAM) location directly addressed by "D" bits in the instruction code, in page #0 (X=0)
MSB	Most significant bit
O	O-Port (O7 to O0)
OPLA	Output programmable logic array
P	P-Port (P3-P0)
R	R-Port (#0: R3-R0, #1: R7-R4, #2: R11-R8, #3: R15-R12)
(R)Y; Y=n	① R-Port #n specified by Y-register (Y=0 to 3) ② R-Port bit n specified by Y-register (Y=0 to 15)
(R)d; d=n	R-Port bit n specified by "d" bits in the instruction code
SB	Serial buffer register
SF	Serial buffer full/empty flag
ST	Status flag
TH	Timer/counter high nibble
TL	Timer/counter low nibble
VF	Timer/counter overflow flag
X	X-register (that indicates page # in data memory RAM)
Xn	The n-th bit of X-register
Y	Y-register
Z	Zero
ZF	Zero flag

Table 6: INSTRUCTION CODE SUMMARY

H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	OUTO	*OUTP	OUT	TAY	TATH	TATL	TAS	ICY	ICM	STIC	X	ROL	L	ADC	AND
1	DAA	DAS	INK	IN	TYA	TTHA	TTLA	TSA	DCY	DCM	STDC	XX	ROR	ST	SBC	OR
2	SETR	SETC	RSTR	RSTC	TSTR	TSTI	TSTV	TSTS	TSTC	TSTZ	STS	LS	RTS	NEG	C	EOR
3	SBIT bp				RBIT bp				TBIT bp				RTI	JPA addr	EN imm	DIS imm
4	SETD d				RSTD d				TSTD d				TBA bp			
5	XD D				XYD D				LXI imm							
6	CALL addr								JPL addr							
7		(ICA)			AI imm											(DCA)
8	LYI imm															
9	(CLA)				LI imm											
A	CYI imm															
B	CI imm															
C	JMP addr															
D																
E																
F																

Notes: : 1-byte/1-cycle instruction : 2-byte/2-cycle instruction

* MB8841H/43/45H/47 only

PRODUCT LINEUP AND DEVELOPMENT TOOLS

The MB8840 and MB8840H series consists of the MB8842/46, MB8843/47, MB8844/48, and MB8841H/45H. The MB8850U1/U2 are available as piggyback EPROM evaluation devices. See Table 7

Table 7: MB8840 AND MB8840H SERIES PRODUCT LINEUP & DEVELOPMENT TOOLS

	MB8841HM/-PSH (MB8845HM)	MB8842M/-PSH (MB8846M)	MB8843M/-PSH (MB8847M)	MB8844M/-PSH (MB8848M)
ROM Size	2K x 8 bits (On-chip mask ROM	2K x 8 bits (On-chip mask ROM	1K x 8 bits (On-chip mask ROM	1K x 8 bits (On-chip mask ROM
RAM Size (Directly addressed locations)	128 x 4 bits (0-7)	128 x 4 bits (0-7)	64 x 4 bits (0-7)	64 x 4 bits (0-7)
I/O Port:	Total 37 lines	Total 25 lines	Total 37 lines	Total 25 lines
-Input only port	4	4	4	4
-Output only port	12	8	12	8
-I/O port	16	11	16	11
-Control port:	Total 5 lines	Total 2 lines	Total 5 lines	Total 2 lines
SI	Yes	No	Yes	No
$\overline{SO}$	Yes	No	Yes	No
$\overline{SC}$/$\overline{TO}$	Yes	No	Yes	No
$\overline{IRQ}$	Yes	Yes	Yes	Yes
$\overline{RESET}$	Yes	Yes	Yes	Yes
Output Port Type of O-, P-, R-Port	· STD O/D · STD P/U · H/C O/D · H/C P/U · 12V O/D (Mask option)	· STD O/D · STD P/U · H/C O/D (Mask option)	· STD O/D · STD P/U · H/C O/D (Mask option)	· STD O/D · STD P/U · H/C O/D (Mask option)
Output PLA Pattern	33 patterns · Dual 4-bit parallel output · 8-bit PLA output (32 patterns)	33 patterns · Dual 4-bit parallel output · 8-bit PLA output (32 patterns)	33 patterns · Dual 4-bit parallel output · 8-bit PLA output (32 patterns)	33 patterns · Dual 4-bit parallel output · 8-bit PLA output (32 patterns)
Stack Depth (Nesting level)	4 levels	4 levels	4 levels	4 levels
Timer/Counter:	Yes	Yes	Yes	Yes
-Buffer size	8 bits	8 bits	8 bits	8 bits
-Clock source	Internal/ External	Internal/ External	Internal/ External	Internal/ External
Serial I/O:	Yes	No	Yes	No
-Buffer size	4 bits	4 bits	4 bits	4 bits
-Clock source	Internal/ External	-	Internal/ External	-
-Output latch	Yes/No (Mask option)	-	Yes/No (Mask option)	-

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Table 7: MB8840 AND MB8840H SERIES PRODUCT LINEUP & DEVELOPMENT TOOLS (Continued)

	MB8841HM/-PSH (MB8845HM)	MB8842M/-PSH (MB8846M)	MB8843M/-PSH (MB8847M)	MB8844M/-PSH (MB8848M)
Clock Generator: -Oscillator type	Yes · Crystal/ External · RC-network/ External	Yes · Crystal/ RC-network/ External	Yes · Crystal/ RC-network/ External	Yes · Crystal/ RC-network/ External
-Clock frequency (With prescaler)	0.5MHz-3MHz (1MHz-6MHz)	0.5MHz-2MHz (1MHz-4MHz)	0.5MHz-2MHz (1MHz-4MHz)	0.5MHz-2MHz (1MHz-4MHz)
Clock Prescaler (Divid-by-two)	Yes/No (Mask option)	Yes/No (Mask option)	Yes/No (Mask option)	Yes/No (Mask option)
Interrupt Functions: -Nesting level -Interrupt source	Yes Single level 3 sources	Yes Single level 3 sources	Yes Single level 3 sources	Yes Single level 3 sources
Instruction Set: -Number -Length/cycle	70 1/1 or 2/2	69 1/1 or 2/2	70 1/1 or 2/2	69 1/1 or 2/2
Min. Instruction Execution Time	2µs at 3MHz (Without prescaler)	3µs at 2MHz (Without prescaler)	3µs at 2MHz (Without prescaler)	3µs at 2MHz (Without prescaler)
Power Supply	Single +5V	Single +5V	Single +5V	Single +5V
Operating Temp. Range:	-30°C to +70°C	-30°C to +70°C	-30°C to +70°C	-30°C to +70°C
Process	CMOS	CMOS	CMOS	CMOS
Package	· DIP-42P · SH-DIP-42P (· QFP-48P)	· DIP-28P · SH-DIP-28P (· QFP-48P)	· DIP-42P · SH-DIP-42P (· QFP-48P)	· DIP-28P · SH-DIP-28P (· QFP-48P)
Development tool: -Hardware	MB2115-01 : CRT unit (Common) MB2115-02 : Monitor board with keyboard (Common) MB2115-04 : EPROM writer (Common) MB2115-33A : DUE board			
-Software	SM05212-A010: Intellec series III MDS cross-assembler SM07412-A012: CP/M-86 cross-assembler SM0XXXX-AXXX: PC-DOS cross-assembler SM07412-G022: CP/M-86 host emulator SM0XXXX-GXXX: PC-DOS host emulator			

Notes: STD: Standard
H/C: High-current
12V: 12V-interface
O/D: Open-drain
P/U: Pull-up

MB8840H SERIES ELECTRICAL CHARACTERISTICS

- **ABSOLUTE MAXIMUM RATINGS** (MB8841H/45H)†

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	-0.3		+7.0	V	
	V_{SS}		0		V	
Input Voltage	V_{IN}	-0.3		+7.0	V	
Output Voltage	V_{OUT}	-0.3		+7.0	V	
		-0.3		+15.0	V	12V interface open-drain
Power Dissipation	P_D			600	mW	
Operating Ambient Temperature	T_A	-30		+70	°C	
Storage Temperature	T_{STG}	-55		+150	°C	

† Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- **RECOMMENDED OPERATING CONDITIONS** (MB8841H/45H)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}		0		V	
Input High Voltage	V_{IHS1}	VSS+3.0		V_{CC}	V	$\overline{RESET}$, $\overline{IRQ}$, $\overline{TC}$, $\overline{SC}/\overline{TO}$
	V_{IHS2}	VSS+4.0		V_{CC}	V	EX
	V_{IH}	VSS+2.0		V_{CC}	V	R-Port, SI, K-Port (Standard threshold)
		VSS+2.4		V_{CC}	V	K-Port(High threshold)
Input Low Voltage	V_{ILS1}	VSS-0.3		V_{SS}+0.8	V	$\overline{RESET}$, $\overline{IRQ}$, $\overline{TC}$, $\overline{SC}/\overline{TO}$
	V_{ILS2}	VSS-0.3		V_{SS}+0.8	V	EX
	V_{IL}	VSS-0.3		V_{SS}+0.8	V	R-Port, SI, K-Port (Standard threshold)
		VSS-0.3		V_{SS}+1.2	V	K-Port(High threshold)
Operating Ambient Temperature	T_A	-30		+70	°C	

• **DC CHARACTERISTICS** (MB8841H/45H)
(Recommended operating conditions unless otherwise noted.)

Output Circuit Option	Parameter	Symbol	Pin/Port	Condition	Value Min.	Value Typ.	Value Max.	Unit
All Outputs Port	Output High Voltage *	V_{OH}	O-,P-,R-Ports SC/TO, SO	V_{CC}=4.5V I_{OH}=-200μA	2.4			V
		V_{OHC}	O-,P-,R-Ports SC/TO, SO	V_{CC}=4.5V I_{OH}=-10μA	4.0			V
	Output Low Voltage **	V_{OL}	O-,P-,R-Ports SC/TO, SO	V_{CC}=4.5V I_{OL}=1.8mA			0.4	V
	Input Leakage Current *	I_{IL}	R-Port, SC/TO	V_{CC}=5.5V V_{IL}=0.4V			3.2	mA
			EX, K-Port, RESET, IRQ, TC, SI	V_{CC}=5.5V V_{IL}=0.4V			-60	μA
	Power Dissipation	P_D		V_{CC}=5.5V		350		mW

* When an open-drain output option is used, O, P, R-Ports is excluded from the V_{OH} and I_{IL} specifications.
** When an open-drain output is used, this parameter is specified with an external 5kΩ pull-up resistor connected.

12V-Interface Open-drain	Output Leakage Current (Off state)	I_{leak}	O-Port, P-Port, R-Port	V_{CC}=5.5V V_{OH}=13.2V			40	μA
	Output Low Voltage	V_{OL}	O-Port, P-Port, R-Port	V_{CC}=4.5V I_{OL}=1.8mA			0.4	V
High Current Pull-up	Output Low Voltage	V_{OL}	O-Port, P-Port, R-Port	V_{CC}=4.5V I_{OL}=20mA			2.0	V
High Current Open-Drain	Output Leakage Current (Off state)	I_{leak}	O-Port, P-Port, R-Port	V_{CC}=5.5V V_{OH}=5.5V			20	μA
	Output Low Voltage	V_{OL}	O-Port, P-Port, R-Port	V_{CC}=4.5V I_{OL}=20mA			2.0	V
Standard Open-drain	Output Leakage Current (Off state)	I_{leak}	O-Port, P-Port, R-Port	V_{CC}=5.5V V_{OH}=5.5V			20	μA

- **AC CHARACTERISTICS** (MB8841H/45H)

CLOCK TIMING (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin	Condition	Value Min.	Value Max.	Unit	Remarks
Clock Frequency	f_C	EX, X	Crystal/ceramic OSC, RC-network OSC or external clock drive: Figs. 6 and 7	0.5	3	MHz	Without prescaler
				1	6		With prescaler
Clock Cycle Time	t_{cyc}	EX, X	Figs. 6 and 7	0.33	2	µs	
Input Clock Pulse Width	P_{WCH}, P_{WCL}	EX	External clock drive(with X open): Figs. 6 and 7	140		ns	Without prescaler
				70			With prescaler
Input Clock Rise/Fall Time	t_{cr}, t_{cf}	EX	External clock drive(with X open): Figs. 6 and 7	5	200	ns	

1

Fig. 6: CLOCK TIMING

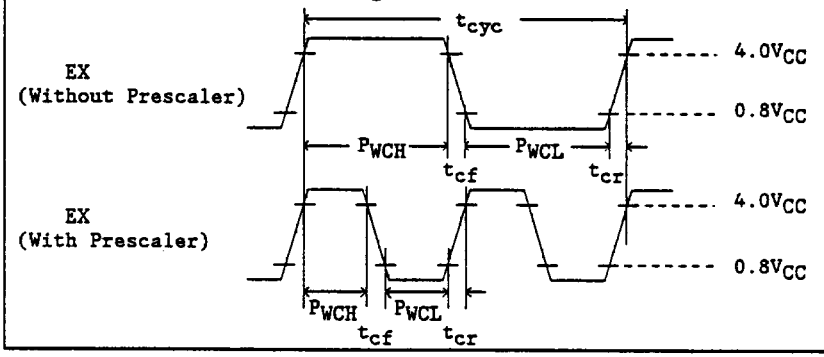
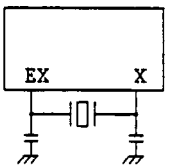
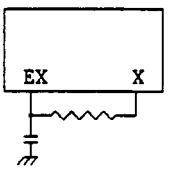


Fig. 7: CLOCK CIRCUIT CONFIGURATIONS

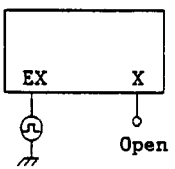
(1) Crystal/Ceramic Oscillator



(2) RC-Network Oscillator*

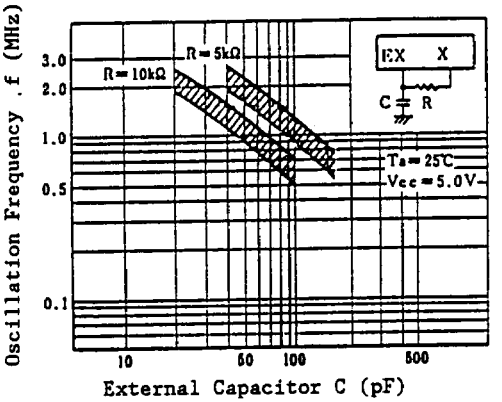


(3) External Clock Drive



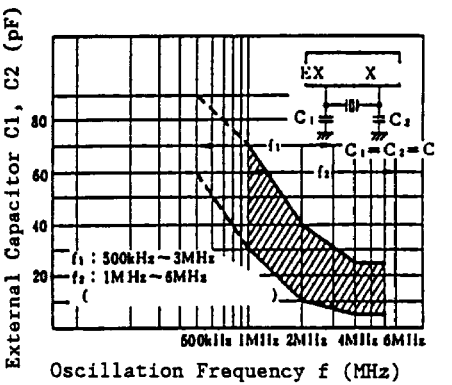
* When the RC-network oscillator is used, the following conditions must be met:
1) The prescaler is not used.
2) V_{CC}=5V±10%
3) T_A=-30°C to +70°C
4) f_C does not exceed 3MHz (Max. clock frequency is about 2.4MHz at V_{CC}=5V and T_A=25°C.)

Fig. 8: RC-NETWORK OSCILLATOR CHARACTERISTICS (EXAMPLE)



Note:
When the RC-network oscillator is used, the following conditions must be met:
1) The prescaler is not used. 2) V_{CC}=5V±10%
3) T_A=-30°C to 70°C 4) f_C does not exceed 2.4 MHz.

Fig. 9: CRYSTAL OSCILLATOR CHARACTERISTICS (EXAMPLE)



Notes:
1) The cross-hatched portion is an area where the on-chip oscillator has stable characteristics and short stabilization time when a typical crystal resonator is used. This chart gives an target value of the external capacitor to realize the desired frequency. When an exact frequency is needed, capacitor value should be determined, adjusted to individual crystal resonator characteristics.

2) Generally speaking, crystal resonators with lower oscillation frequency tend to have longer stabilization time and wider characteristic variations which affect on-chip oscillator characteristics. So, we recommend a high-frequency crystal resonator with on-chip 1/2 prescaler.

OUTPUT TIMING (MB8841H/45H)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
O-, P-, R-Port Delay Time	t_{PDH}	P3-P0,07-00, R15-R0	Fig. 10		1000	ns
	t_{PDL}				350	
Serial Port Delay Time	t_{SDH}	SO	Fig. 10		600	ns
	t_{SDL}				600	

Notes:
1. A 5kΩ pull-up is required when open-drain output is used.
2. All the output loading values are 100pF + 1TTL. See figure below.

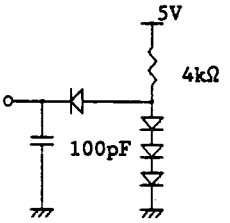
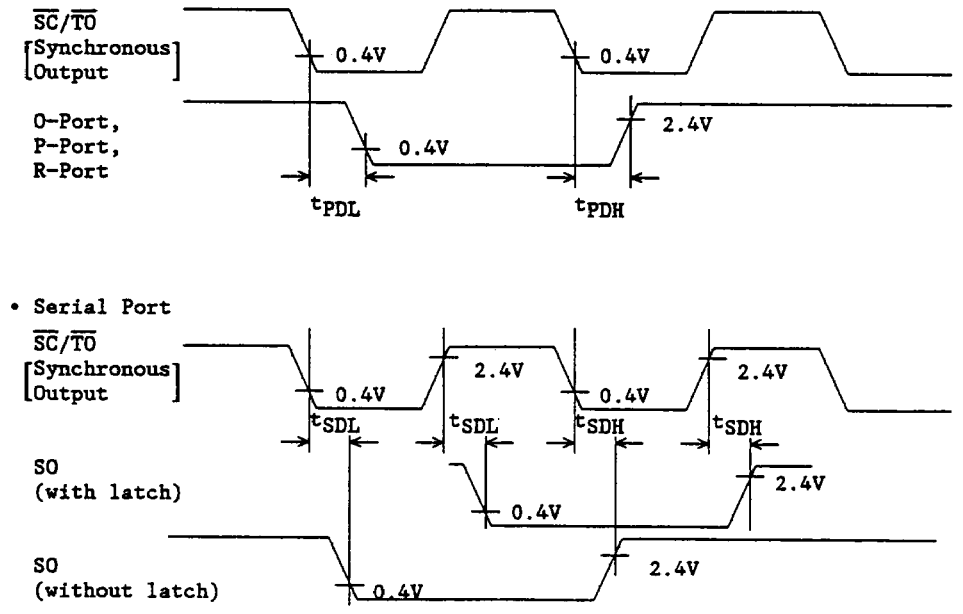


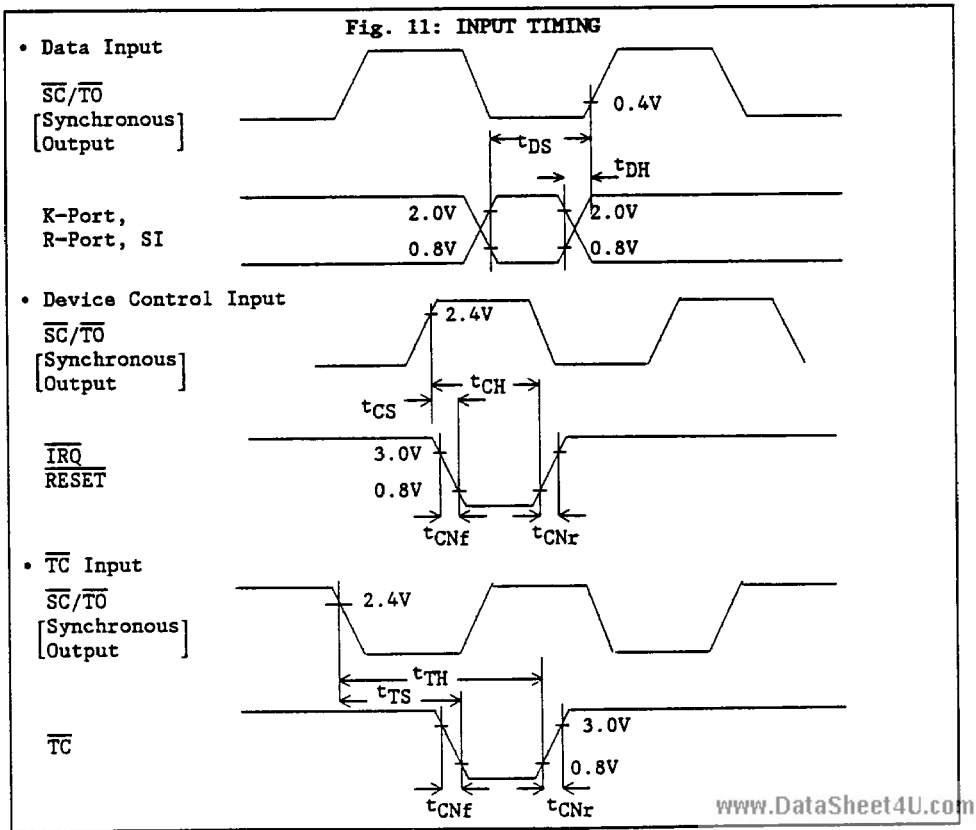
Fig. 10: OUTPUT TIMING



INPUT TIMING (MB8841H/45H)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
Input Data Setup Time	t_{DS}	K-Port, R-Port, SI	Fig. 11	$t_{cyc}+1000$		ns
Input Data Hold Time	t_{DH}				$t_{cyc}-50$	
Device Control Setup Time	t_{CS}	$\overline{RESET}$	Fig. 11		$2t_{cyc}-200$	ns
		$\overline{IRQ}$			$t_{cyc}-200$	
Device Control Hold Time	t_{CH}	$\overline{RESET}$	Fig. 11	$2t_{cyc}+50$		ns
		$\overline{IRQ}$		$t_{cyc}+50$		
Timing Input Setup Time	t_{TS}	$\overline{TC}$	Fig. 11		$2t_{cyc}-200$	ns
Timing Input Hold Time	t_{TH}	$\overline{TC}$	Fig. 11	$2t_{cyc}+50$		ns
Control Signal Rise and Fall Time	t_{CNr}, t_{CNf}	$\overline{SC}/\overline{TO}$, $\overline{IRQ}$, $\overline{RESET}$, $\overline{TC}$	Fig. 11	Should be less than 200ns		

Fig. 11: INPUT TIMING



MB8840 SERIES ELECTRICAL CHARACTERISTICS

- **ABSOLUTE MAXIMUM RATINGS** (MB8842/43/44/46/47/48)†

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	-0.3		+7.0	V	
	V_{SS}		0		V	
Input Voltage	V_{IN}	-0.3		+7.0	V	
Output Voltage	V_{OUT}	-0.3		+7.0	V	
Power Dissipation	P_D			600	mW	
Operating Ambient Temperature	T_A	-30		+70	°C	
Storage Temperature	T_{STG}	-55		+150	°C	

† Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- **RECOMMENDED OPERATING CONDITIONS** (MB8842/43/44/46/47/48)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}		0		V	
Input High Voltage	V_{IHS1}	VSS+3.0		V_{CC}	V	$\overline{RESET}$, $\overline{IRQ}$, $\overline{TC}$, $\overline{SC}/\overline{TO}$
	V_{IHS2}	VSS+4.0		V_{CC}	V	X
	V_{IH}	VSS+2.0		V_{CC}	V	R-Port, SI, K-Port
Input Low Voltage	V_{ILS1}	VSS-0.3		V_{SS}+0.8	V	$\overline{RESET}$, $\overline{IRQ}$, $\overline{TC}$, $\overline{SC}/\overline{TO}$
	V_{ILS2}	VSS-0.3		V_{SS}+0.8	V	X
	V_{IL}	VSS-0.3		V_{SS}+0.8	V	R-Port, SI, K-Port
Operating Ambient Temperature	T_A	-30		+70	°C	

1

• **DC CHARACTERISTICS** (MB8842/43/44/46/47/48)
(Recommended operating conditions unless otherwise noted.)

Output Circuit Option	Parameter	Symbol	Pin/Port	Condition	Value Min.	Value Typ.	Value Max.	Unit
All Outputs Port	Output High Voltage *	V_{OH}	O-, P-, R-Ports SC/TO, SO	V_{CC}=4.5V I_{OH}=-200μA	2.4			V
		V_{OHC}	O-, P-, R-Ports SC/TO, SO	V_{CC}=4.5V I_{OH}=-10μA	4.0			V
	Output Low Voltage **	V_{OL}	O-, P-, R-Ports SC/TO, SO	V_{CC}=4.5V I_{OL}=1.8mA			0.4	V
	Input Leakage Current *	I_{IL}	R-Port, SC/TO	V_{CC}=5.5V V_{IL}=0.4V			3.2	mA
			X, K-Port, RESET, IRQ, TC, SI	V_{CC}=5.5V V_{IL}=0.4V			-60	μA
	Power Dissipation	P_D		V_{CC}=5.5V		300		mW

* When an open-drain output option is used, O, P, R-Ports is excluded from the V_{OH} and I_{IL} specifications.
** When an open-drain output is used, this parameter is specified with an external 5kΩ pull-up resistor connected.

High Current Open-Drain	Output Leakage Current (Off state)	I_{leak}	O-Port, P-Port, R-Port	V_{CC}=5.5V V_{OH}=5.5V			20	μA
	Output Low Voltage	V_{OL}	O-Port, P-Port, R-Port	V_{CC}=4.5V I_{OL}=20mA			2.0	V
Standard Open-drain	Output Leakage Current (Off state)	I_{leak}	O-Port, P-Port, R-Port	V_{CC}=5.5V V_{OH}=5.5V			20	μA

- **AC CHARACTERISTICS** (MB8842/43/44/46/47/48)

CLOCK TIMING (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin	Condition	Value Min.	Value Max.	Unit	Remarks
Clock Frequency	f_C	EX, X	Crystal/ceramic OSC, RC-network OSC or external clock drive: Figs. 12 and 13	0.5	2	MHz	Without prescaler
				1	4		With prescaler
Clock Cycle Time	t_{cyc}	EX, X	Figs. 12 and 13	0.5	2	µs	
Input Clock Pulse Width	P_{WCH}, P_{WCL}	X	External clock drive(EX pin grounded) Figs. 12 and 13	225		ns	Without prescaler
				100			With prescaler
Input Clock Rise/Fall Time	t_{cr}, t_{cf}	X	External clock drive(EX pin grounded) Figs. 12 and 13	5	200	ns	

Fig. 12: CLOCK TIMING

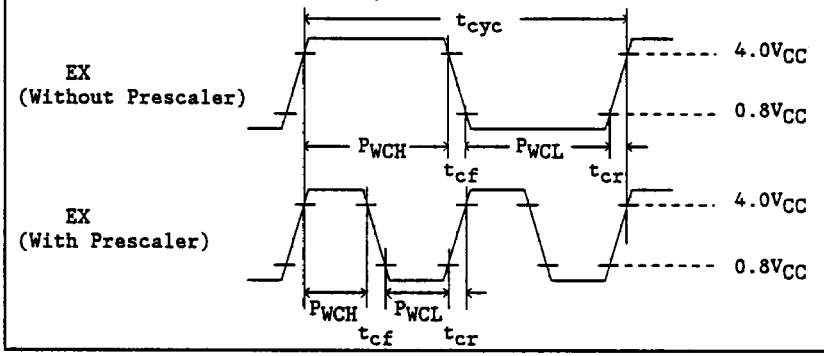
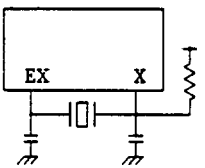
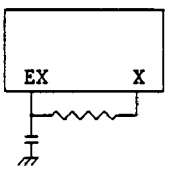


Fig. 13: CLOCK CIRCUIT CONFIGURATIONS

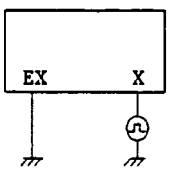
(1) Crystal/Ceramic Oscillator



(2) RC-Network Oscillator*

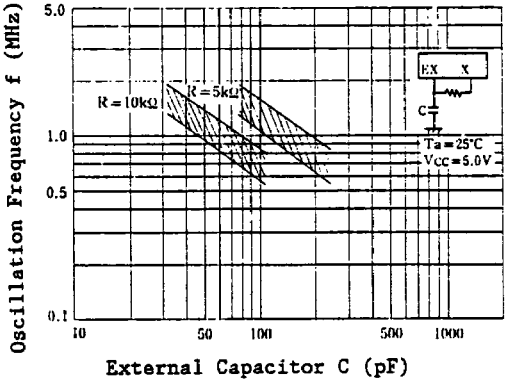


(3) External Clock Drive



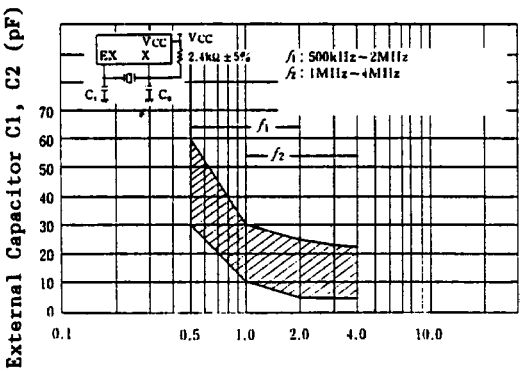
* When the RC-network oscillator is used, the following conditions must be met:
1) The prescaler is not used.
2) V_{CC}=5V±10%
3) T_A=−30°C to +70°C
4) f_C does not exceed 2MHz (Max. clock frequency is about 1.6MHz at V_{CC}=5V and T_A=25°C.)

Fig. 14: RC-NETWORK OSCILLATOR CHARACTERISTICS (EXAMPLE)



Note:
When the RC-network oscillator is used, the following conditions must be met:
1) The prescaler is not used. 2) V_{CC}=5V±10%
3) T_A=-30°C to 70°C 4) f_C does not exceed 1.6 MHz.

Fig. 15: CRYSTAL OSCILLATOR CHARACTERISTICS (EXAMPLE)



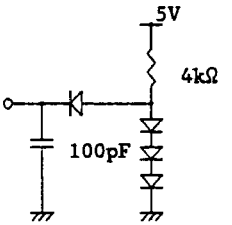
Notes:
1) The cross-hatched portion is an area where the on-chip oscillator has stable characteristics and short stabilization time when a typical crystal resonator is used. This chart gives an target value of the external capacitor to realize the desired frequency. When an exact frequency is needed, capacitor value should be determined, adjusted to individual crystal resonator characteristics.

2) Generally speaking, crystal resonators with lower oscillation frequency tend to have longer stabilization time and wider characteristic variations which affect on-chip oscillator characteristics. So, we recommend a high-frequency crystal resonator with on-chip 1/2 prescaler.

OUTPUT TIMING (MB8842/43/44/46/47/48)
(Recommended operating conditions unless otherwise noted.)

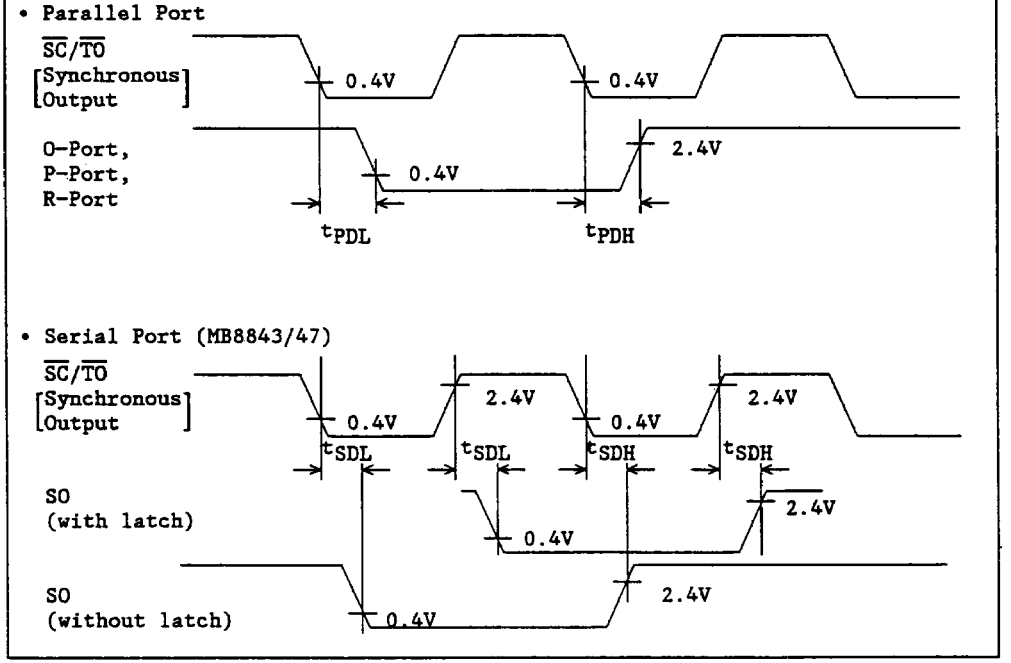
Parameter	Symbol	Pin/Port	Condi-tions	Value		Unit
				Min.	Max.	
O-, P-, R-Port Delay Time	t_{PDH}	O-,P-, R-Port	Fig. 16		1000	ns
	t_{PDL}				350	
Serial Port Delay Time	t_{SDH}	SO(MB8843/47)	Fig. 16		600	ns
	t_{SDL}				600	

Notes:
1. A 5kΩ pull-up is required when open-drain output is used.
2. All the output loading values are 100pF + 1TTL. See figure below.



1

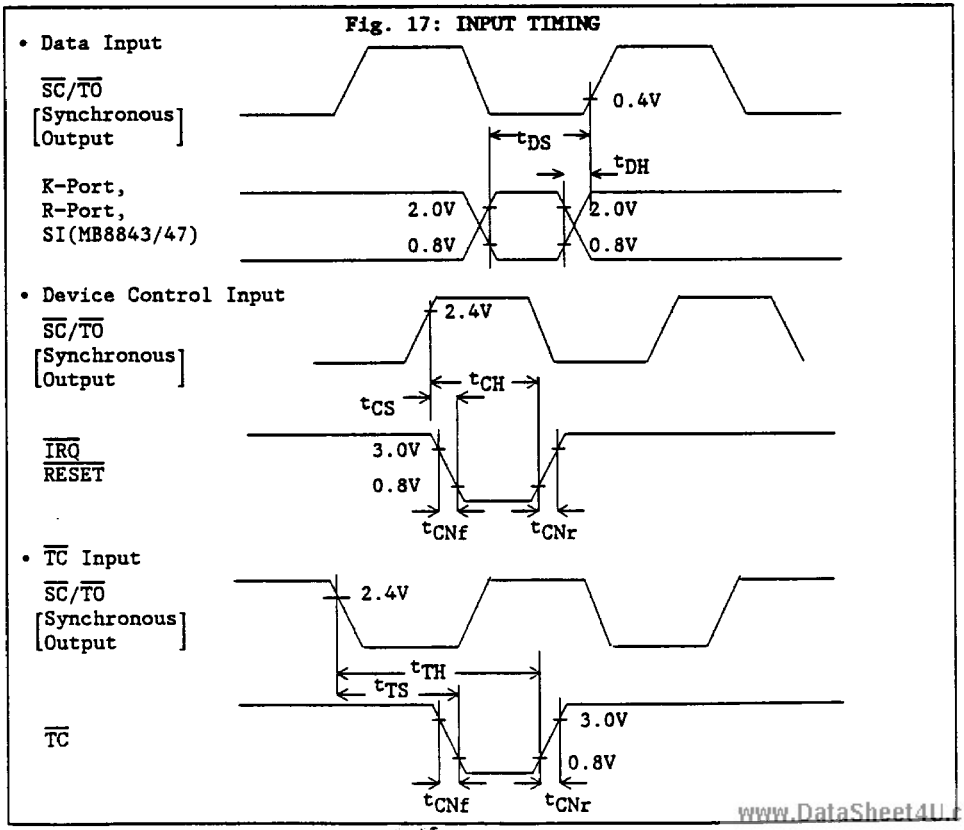
Fig. 16: OUTPUT TIMING



INPUT TIMING (MB8842/43/44/46/47/48)
(Recommended operating conditions unless otherwise noted.)

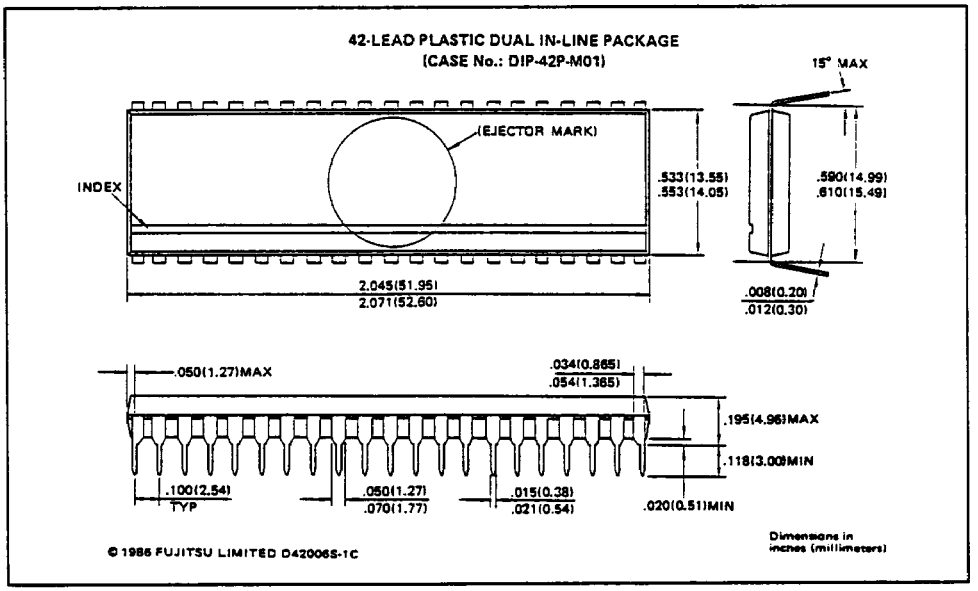
Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
Input Data Setup Time	t_{DS}	K-Port, R-Port, SI(MB8843/47)	Fig. 17	t_{cyc}+1000		ns
Input Data Hold Time	t_{DH}				t_{cyc}-50	
Device Control Setup Time	t_{CS}	$\overline{RESET}$	Fig. 17		$2t_{cyc}$-200	ns
		$\overline{IRQ}$			t_{cyc}-200	
Device Control Hold Time	t_{CH}	$\overline{RESET}$	Fig. 17	$2t_{cyc}$+50		ns
		$\overline{IRQ}$		t_{cyc}+50		
Timing Input Setup Time	t_{TS}	$\overline{TC}$	Fig. 17		$2t_{cyc}$-200	ns
Timing Input Hold Time	t_{TH}	$\overline{TC}$	Fig. 17	$2t_{cyc}$+50		ns
Control Signal Rise and Fall Time	t_{CNr}, t_{CNf}	$\overline{IRQ}$, $\overline{RESET}$, $\overline{TC}$, $\overline{SC}/\overline{TO}$(MB8843/47)	Fig. 17	Should be less than 200ns		

Fig. 17: INPUT TIMING

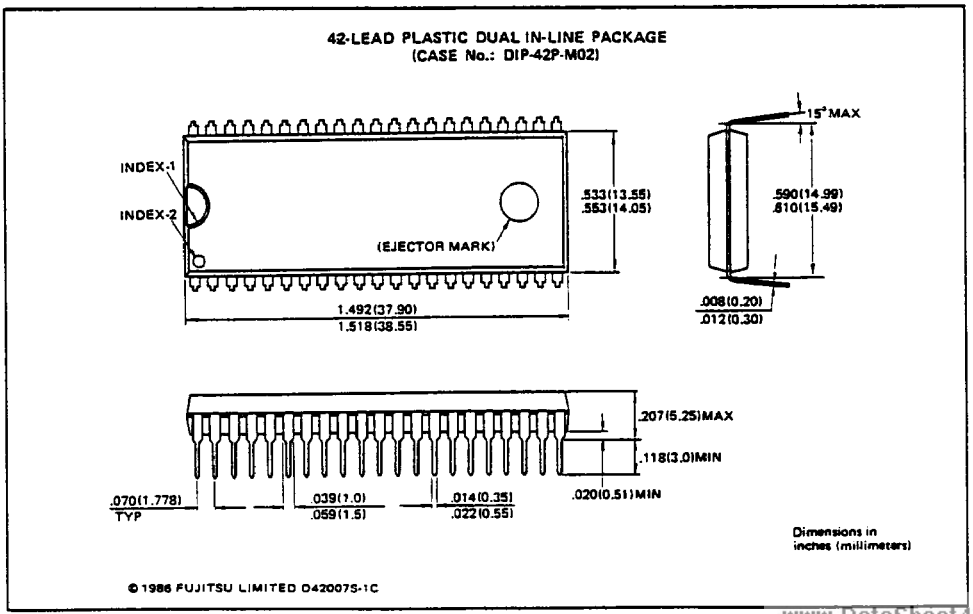


PACKAGE DIMENSIONS

• MB8841HM/43M: 42-PIN PLASTIC STANDARD DIP

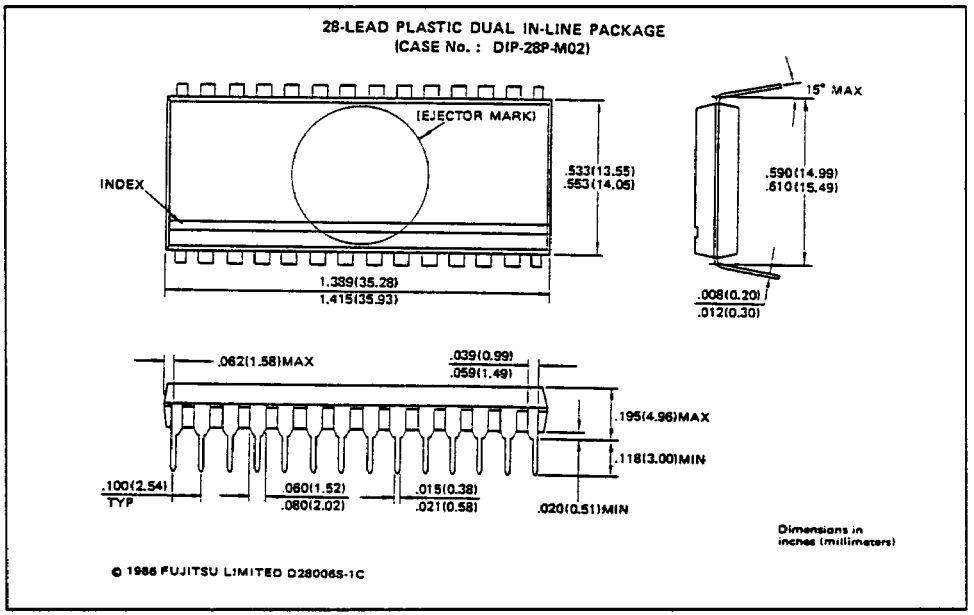


• MB8841H-PSH/43-PSH: 42-PIN PLASTIC SHRINK DIP

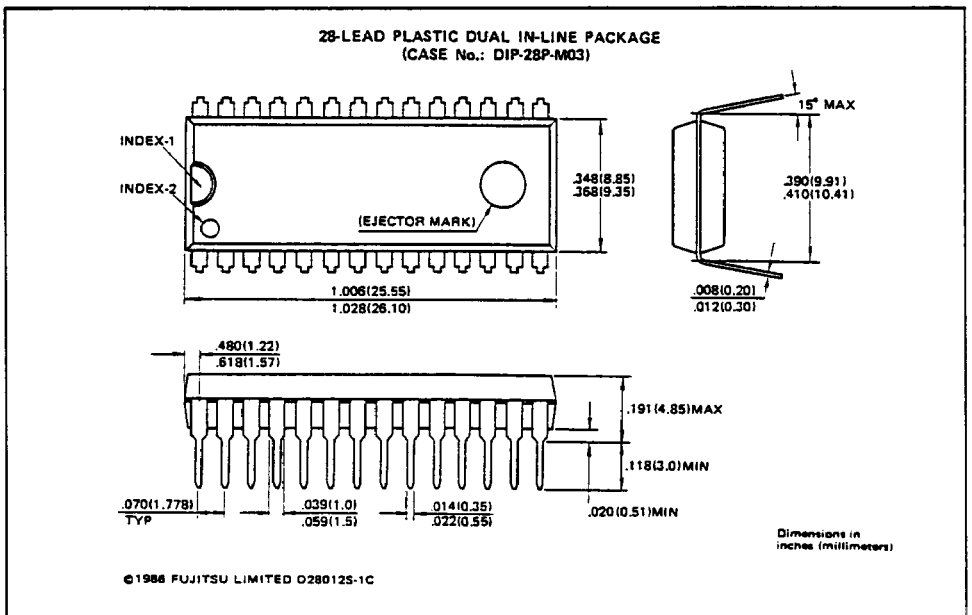


PACKAGE DIMENSIONS

• MB8842M/44M: 28-PIN PLASTIC STANDARD DIP

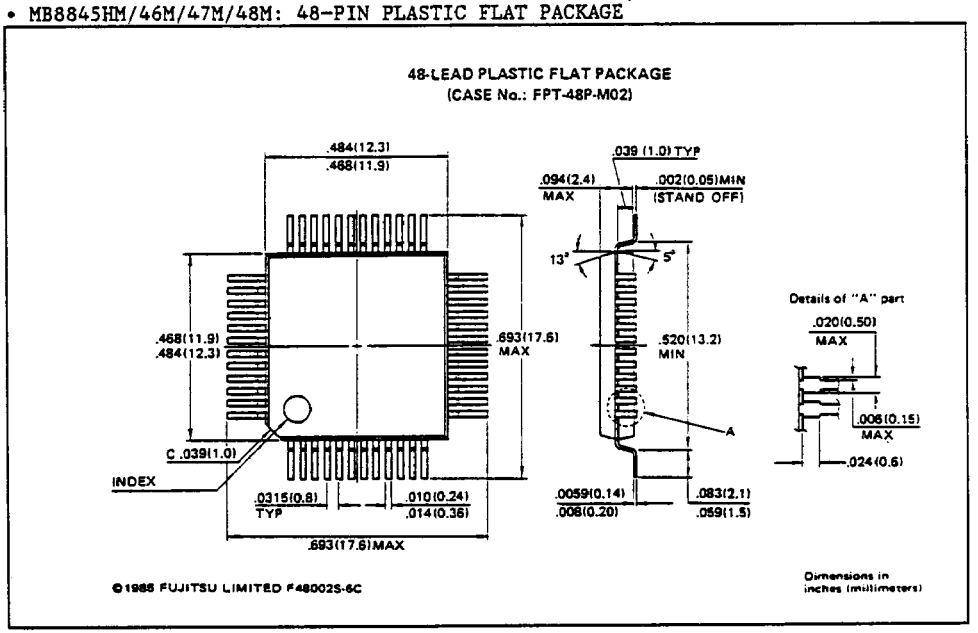


• MB8842-PSH/44-PSH: 28-PIN PLASTIC SHRINK DIP



PACKAGE DIMENSIONS(Continues)

• MB8845HM/46M/47M/48M: 48-PIN PLASTIC FLAT PACKAGE



• MB8850U1/U2-C AND MB8850H-C: 42-PIN CERAMIC MODULE