❑ MN101E30R

Type	MN101E30R	MN101EF30R
Internal ROM type	Mask ROM	FLASH
ROM (byte)	928K	
RAM (byte)	6K	
Package (Lead-free)	QFP100-P-1818B (Under development)	
Minimum Instruction Execution Time	50 ns (at 2.2 V to 5.5 V, 20 MHz) * at internal 2 , 3 , 4 , 5 , 6 , 8 , 10 times oscillation used	50 ns (at 2.2 V to 5.5 V, 20 MHz)

■ Interrupts

6 external interrupts, 30 internal interrupts
RESET, Watchdog, External 0 to 4, Timer 0 to 4, Timer 6, Timer 7 (2 systems), Timer 8 (2 systems), Timer 9 (2 systems), Time base, Serial 0 (2 systems), Serial1 (2 systems), Serial 2 (2 systems), Serial 3 (2 systems), Serial 4, Serial 5, A/ D conversion finish, Automatic transfer (2 systems), Key interrupts, end of single tone, end of phrase

■ Timer Counter

Timer counter 0 : 8-bit × 1
(timer pulse output, event count, added pulse (2-bit) system PWM output, generation of remote control carrier, simple pulse measurement, real time output control)

Timer counter 1 : 8-bit × 1
(timer pulse output, event count, 16-bit cascade connected (timer 0, 1) timer synchronous output event)

Timer counter 2 : 8-bit × 1
(timer pulse output, event count, added pulse (2-bit) system PWM output, simple pulse measurement, 24-bit cascade connected (timer 0, 1, 2), timer synchronous output event, real timer output control)

Timer counter 3 : 8-bit × 1
(timer pulse output, event count, generation of remote control carrier, 16-bit cascade connected (timer 2, 3), 32-bit cascade connected (timer 0, 1, 2, 3))

Timer counter 4 : 8-bit × 1
(timer pulse output, added pulse (2-bit) system PWM output, event count, serial transfer clock, simple pulse measurement)

Timer counter 6 : 8-bit free run timer, time base timer

Timer counter 7 : 16-bit × 1
(timer pulse output, event count, High accuracy PWM, High performance IGBT output (cycle/duty continuous variable) timer synchronous output event, input capture (Both edge available), real timer output control), double buffer compare register

Timer counter 8 : 16-bit × 1
(timer pulse output, event count, High accuracy PWM output (cycle/duty continuous variable) pulse width measurement, input capture (Both edge available), 32-bit cascade connected (Timer 7 , 8), 32-bitPWM output, synchronous output event), double buffer compare register

Timer counter 9 : 16-bit × 1
(timer pulse output, event count, High accuracy PWM output (cycle/duty continuous variable), pulse width measurement, input capture (Both edge available), real timer output control), double buffer compare register

Timer counter A : 8-bit × 1 (event count, Serial transfer clock timer, clock for function (timer, serial, LCD))

Watchdog timer

■ Serial interface

Serial 0 ~ 3 : UART (full duplex) / synchronous × 1
Serial 4 : multi master I²C / synchronous × 1
Serial 5 : I²C slave × 1

■ DMA controller

2 systems (External request/internal event request/software request maximum transfer cycles are 255)

■ I/O Pins

I/O	86	common use, Specified pull-up/pull-down resistor available, Input/output selectable (bit-unit)

■ A/D converter

10-bit × 12-ch.

■ D/A converter

8-bit × 4-ch.

20-bit × 1-ch.

■ Display control function

LCD

55 segments × 4 commons (static, 1/2, 1/3, 1/4 duty) 1/3 bias, Usable if VLC1 ≤ VDD

■ Special Ports

Buzzer output, remote control carrier signal output, high-current drive port

■ ROM Correction

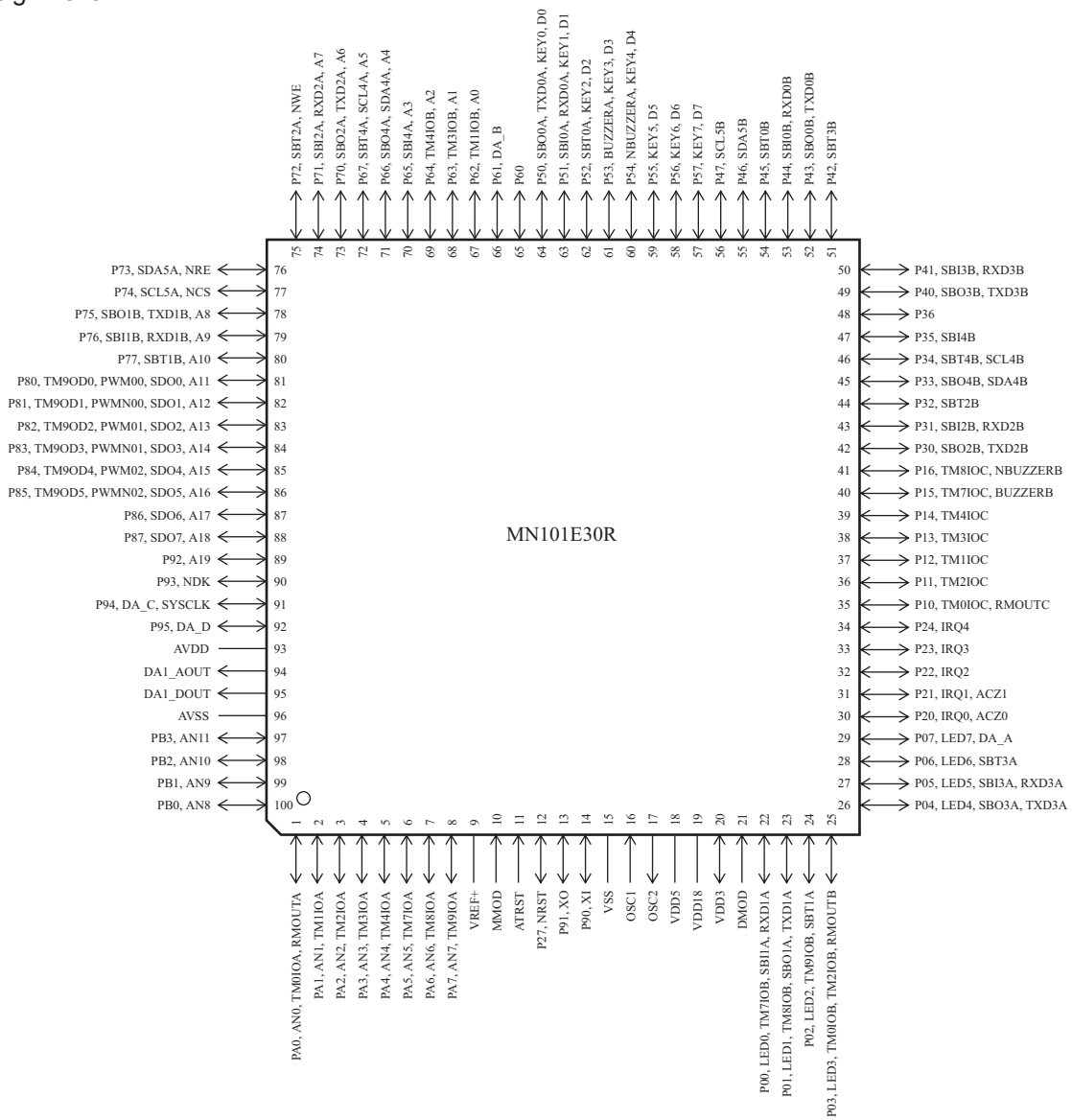
Correcting address designation : up to 7 addresses possible

■ Development tools

In-circuit Emulator

PX-ICE101E ＋ PRBV101E30-QFP100-P-1818B (Under development)

■ Pin Assignment



QFR100-P-1818B

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