# MP7636A

15 V CMOS Microprocessor Compatible Double-Buffered, Multiplying 16-Bit Digital-to-Analog Converter

## FEATURES

- **Four Quadrant Multiplication**
- **16-Bit Monotonicity**
- **Lower Data Bus Feedthrough @ $\overline{CS}$ = 1**
- **Low Feedthrough Error**
- **Low Power Consumption**
- **TTL/5 V CMOS Compatible**
- **Double Buffered**
- **Decoded DAC Approach**
- **Latch-Up Free**

## BENEFITS

- **High Accuracy Performance at Low Cost**
- **Easy Interface with 8-Bit Microprocessors**
- **Simple Upgrade of MP1230A Family to High Accuracy (Pin Compatible)**
- **Reduced Board Space**
- **16-Bit Bus Version: MP7626**

## GENERAL DESCRIPTION

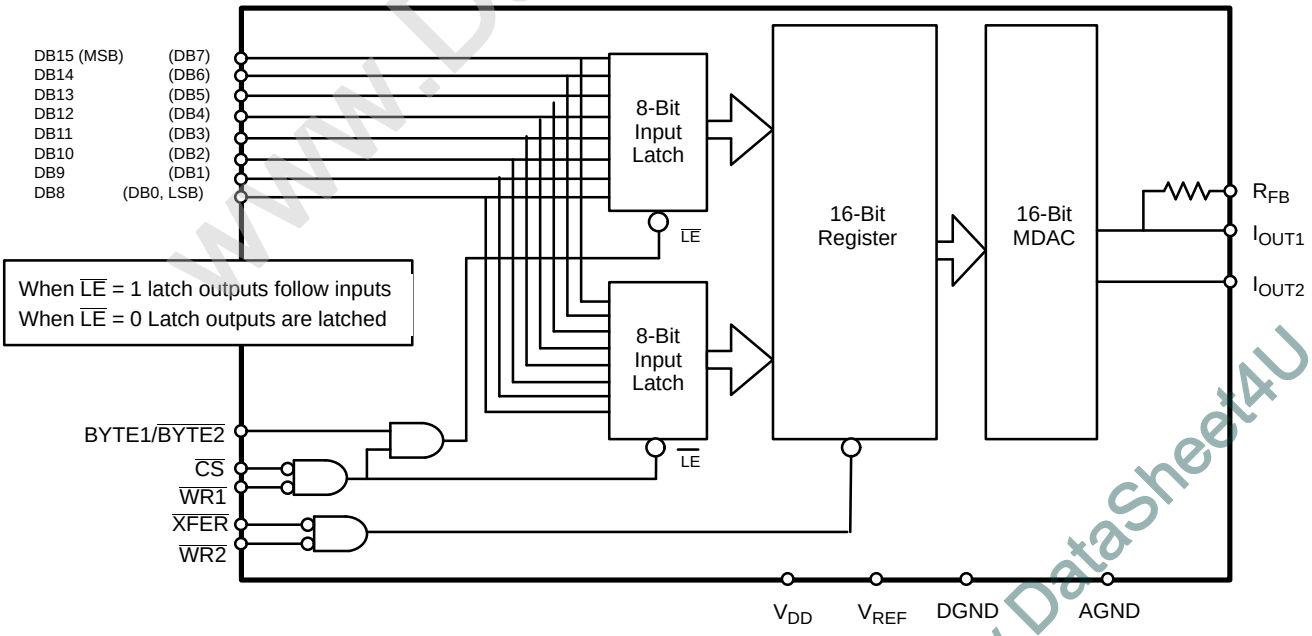
The MP7636A is manufactured using advanced thin film resistors on a double metal CMOS process. The MP7636A incorporates a unique bit decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. 16-bit differential non-linearity is achieved with minimal laser trim.

The MP7636A is packaged in a 20-pin 300 mil wide DIP and is a direct 16-bit replacement for the 12-bit DAC1230 series. Full pin-for-pin compatibility allows existing systems to be upgraded to 16 bits without hardware modification.

The MP7636A provides 16-bit data loading through 8 input data lines for direct interface to 8-bit data buses. All data loading and data transfer operations are identical to the WRITE cycle of a static RAM.

The MP7636A uses a unique circuit which significantly reduces transients in the supplies during DATA bus transitions at $\overline{CS}$ = 1.

## SIMPLIFIED BLOCK DIAGRAM



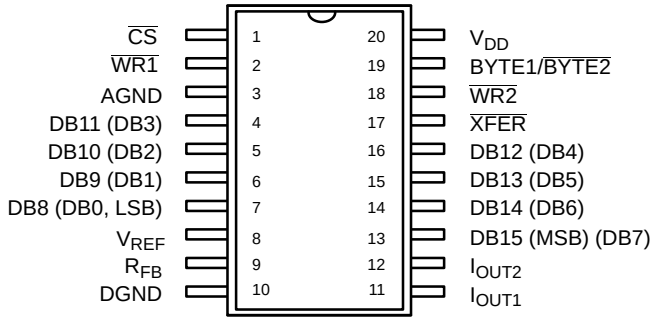
## ORDERING INFORMATION

| Package Type | Temperature Range | Part No. | INL (LSB) | DNL (LSB) | Gain Error (% FSR) |
|---|---|---|---|---|---|
| SOIC | –40 to +85°C | MP7636AJS | ±4 | ±4 | 0.1 |
| SOIC | –40 to +85°C | MP7636AKS | ±2 | ±2 | 0.1 |

*Contact factory for non-compliant military processing

## PIN CONFIGURATION

*See Packaging Section for Package Dimensions*




**20 Pin SOIC (Jedec, 0. 300")**
**S20**

## PIN OUT DEFINITIONS

| PIN NO. | NAME | DESCRIPTION |
|---|---|---|
| 1 | $\overline{CS}$ | Chip Select (Active Low) |
| 2 | $\overline{WR1}$ | Write1 (Active Low) |
| 3 | AGND | Analog Ground |
| 4 | DB11 (DB3) | Data Input Bit 11 (MSB) Data Input Bit 3 |
| 5 | DB10 (DB2) | Data Input Bit 10 Data Input Bit 2 |
| 6 | DB9 (DB1) | Data Input Bit 9 Data Input Bit 1 |
| 7 | DB8 (DB0) | Data Input Bit 8 Data Input Bit 0 (LSB) |
| 8 | $V_{REF}$ | Reference Input Voltage |
| 9 | $R_{FB}$ | Internal Feedback Resistor |
| 10 | DGND | Digital Ground |
| 11 | $I_{OUT1}$ | Current Output 1 |

| PIN NO. | NAME | DESCRIPTION |
|---|---|---|
| 12 | $I_{OUT2}$ | Current Output 2 |
| 13 | DB15 (MSB) (DB7) | Data Input Bit 15 (Most Significant Bit) Data Input Bit 7 |
| 14 | DB14 (DB6) | Data Input Bit 14 Data Input Bit 6 |
| 15 | DB13 (DB5) | Data Input Bit 13 Data Input Bit 5 |
| 16 | DB12 (DB4) | Data Input Bit 12 Data Input Bit 4 |
| 17 | $\overline{XFER}$ | Transfer Control Signal (Active Low) |
| 18 | $\overline{WR2}$ | Write 2 (Active Low) |
| 19 | BYTE1/ $\overline{BYTE2}$ | Byte Sequence Control |
| 20 | $V_{DD}$ | Power Supply |

## ELECTRICAL CHARACTERISTICS
**($V_{DD}$ = + 15 V, $V_{REF}$ = +10 V unless otherwise noted)**

| Parameter | Symbol | 25°C Min | 25°C Typ | 25°C Max | Tmin to Tmax Min | Tmin to Tmax Max | Units | Test Conditions/Comments |
|---|---|---|---|---|---|---|---|---|
| **STATIC PERFORMANCE[1]** | | | | | | | | FSR = Full Scale Range |
| Resolution (All Grades) | N | 16 | | | 16 | | Bits | |
| Integral Non-Linearity (Relative Accuracy) | INL | | | | | | LSB | Best Fit Straight Line Spec. (Max INL – Min INL) / 2 |
| J, S | | | | ±4 | | ±4 | | |
| K, L, T | | | | ±2 | | ±2 | | |
| Differential Non-Linearity | DNL | | | | | | LSB | All grades guaranteed monotonic over full operating temperature range. |
| J, S | | | | ±4 | | ±4 | | |
| K, T | | | | ±2 | | ±2 | | |
| L | | | | ±1 | | ±2 | | |
| Gain Error | GE | | | ±0.1 | | ±0.1 | % FSR | Using Internal $R_{FB}$ |
| Gain Temperature Coefficient[2] | $TC_{GE}$ | | | | | ±2 | ppm/°C | ΔGain/ΔTemperature |
| Power Supply Rejection Ratio | PSRR | | | ±50 | | ±50 | ppm/% | $\lvert\Delta Gain/\Delta V_{DD}\rvert$ $\Delta V_{DD}$ = ± 5% |
| Output Leakage Current | $I_{OUT}$ | | | ±10 | | ±200 | nA | $I_{OUT1}$ only |
| **DYNAMIC PERFORMANCE[2]** | | | | | | | | |
| Current Settling Time | $t_S$ | | 2 | | | | µs | To 1/2 LSB |
| AC Feedthrough at $I_{OUT1}$ | $F_T$ | | 2 | | | | mV p-p | $R_L$=100Ω, $C_{EXT}$=13pF $V_{REF}$ = 20 V p-p Sine wave @ 10kHz |
| **REFERENCE INPUT** | | | | | | | | |
| Input Resistance | $R_{IN}$ | 2.5 | | 7.5 | 2.5 | 7.5 | kΩ | |
| **LOGIC INPUTS[3]** | | | | | | | | |
| Input High Voltage | $V_{INH}$ | 3.0 | 2.4 | | 3.0 | | V | |
| Input Low Voltage | $V_{INL}$ | | | 0.8 | | 0.8 | V | |
| Input Current | $I_{LKG}$ | | | ±1 | | ±1 | µA | |
| Input Capacitance | | | | | | | | |
| Data | $C_{IN}$ | | 5 | | | | pF | |
| Control | $C_{IN}$ | | 5 | | | | pF | |
| **ANALOG OUTPUTS[2]** | | | | | | | | |
| Output Capacitance | | | | | | | | |
| | $C_{OUT1}$ | | | 280 | | | pF | DAC all 1's |
| | $C_{OUT1}$ | | | 120 | | | pF | DAC all 0's |
| | $C_{OUT2}$ | | | 100 | | | pF | DAC all 1's |
| | $C_{OUT2}$ | | | 240 | | | pF | DAC all 0's |

## ELECTRICAL CHARACTERISTICS (CONT'D)

| Parameter | Symbol | 25°C Min | 25°C Typ | 25°C Max | Tmin to Tmax Min | Tmin to Tmax Max | Units | Test Conditions/Comments |
|---|---|---|---|---|---|---|---|---|
| **POWER SUPPLY[5]** | | | | | | | | |
| Functional Voltage Range[2] | $V_{DD}$ | 4.5 | | 16.5 | 5.0 | 16.5 | V | |
| Supply Current | $I_{DD}$ | | | 1 | | 1 | mA | All digital inputs 0 V or $V_{DD}$ |
| **SWITCHING CHARACTERISTICS[2, 4]** | | | | | | | | |
| $\overline{CS}$ to $\overline{WR}$ Set-Up Time | $t_{CS}$ | 150 | | | | | ns | |
| $\overline{CS}$ to $\overline{WR}$ Hold Time | $t_{CH}$ | 10 | | | | | ns | |
| Data Valid to $\overline{WR}$ Set-Up Time | $t_{DS}$ | 70 | | | | | ns | |
| Data Valid to $\overline{WR}$ Hold Time | $t_{DH}$ | 70 | | | | | ns | |
| $\overline{WR}$, $\overline{XFER}$ Pulse Width | $t_W$ | 150 | | | | | ns | |

**NOTES:**

(1) Full Scale Range (FSR) is 10V for unipolar mode.
(2) Guaranteed but not production tested.
(3) Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
(4) See timing diagram.
(5) Specified values guarantee functionality. Refer to other parameters for accuracy.

**Specifications are subject to change without notice**

## ABSOLUTE MAXIMUM RATINGS ($T_A$ = +25°C unless otherwise noted)[1, 2, 3]

Voltage at Any Digital Input ..... GND –0.5 to $V_{DD}$ +0.5 V
Voltage at $V_{REF}$ Input ..... ±25 V
DC Voltage Applied to $I_{OUT1}$ or $I_{OUT2}$ GND –0.5 V to +17 V
Supply Voltage ($V_{DD}$) ..... +17 $V_{DC}$

AGND to DGND ..... ±1 V
(Functionality Guaranteed ±0.5 V)
Storage Temperature Range ..... –65°C to 150°C
Package Power Dissipation Rating to 75°C
SOIC ..... 900mW
Derates above 75°C ..... 12mW/°C

**NOTES:**

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

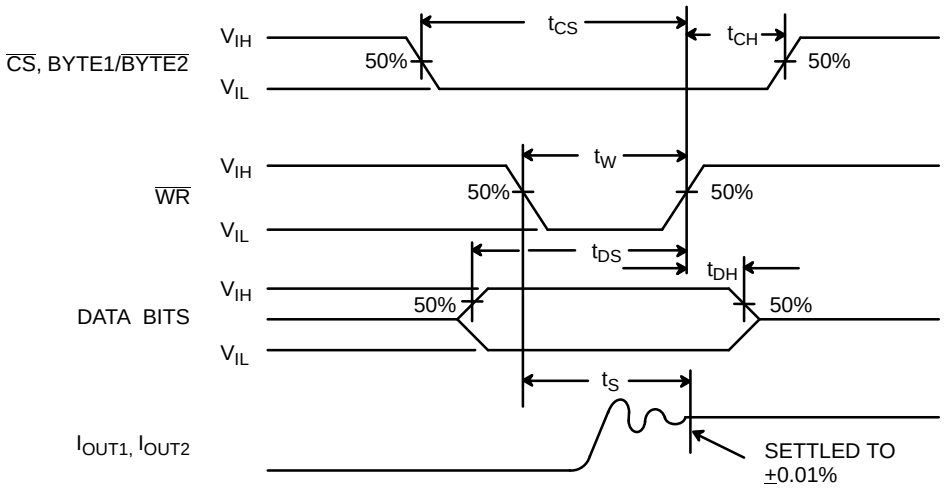
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

3 GND refers to AGND and DGND.

## APPLICATION NOTES

***Refer to Section 8 for Applications Information***

## TIMING DIAGRAM




## DEFINITION OF CONTROL SIGNALS:

$\overline{CS}$: Chip Select (Active low).
It will enable $\overline{WR1}$.

$\overline{WR1}$: Write 1 (Active low)
The $\overline{WR1}$ is used to load the digital data bits (DB) into the input latch.

BYTE1/$\overline{BYTE2}$: Byte sequence control.
The BYTE1/$\overline{BYTE2}$ control pin is used to select MSB and LSB both input latches.

$\overline{WR2}$: Write 2 (Active low).
It will enable $\overline{XFER}$.

$\overline{XFER}$: Transfer control signal (Active low).
This signal, in combination with $\overline{WR2}$, causes the 16-bit data which is available in the input latches to transfer to the DAC register.

DB0 to DB15: Digital Inputs.
DB0 is the least significant digital input (LSB) and DB15 is the most significant digital input (MSB).

$I_{OUT1}$: DAC Current Output 1 Bus.
$I_{OUT1}$ is a maximum for a digital code of all 1's in the DAC register, and is zero for all 0's in the DAC register.

$I_{OUT2}$: DAC Current Output 2 Bus.
$I_{OUT2}$ is a complement of $I_{OUT1}$. The ladder termination has been tied to $I_{OUT2}$ internally.

$R_{FB}$: Feedback Resistor.
This internal feedback resistor should always be used (not an external resistor) since it matches the resistors in the DAC and tracks these resistor over temperature.

$V_{REF}$: Reference Voltage Input.
This input connects an external precision voltage source to the internal DAC. The $V_{REF}$ can be selected over the range of +25V to –25V or the analog signal for a 4-quadrant multiplying mode application.

$V_{DD}$: Power Supply Voltage.
This is the power supply pin for the part. The $V_{DD}$ can be from +5 V DC to +15 V DC, however optimum voltage is +15 V DC.

AGND: Analog Ground.
Back gate of the DAC N-channel current steering switches.

DGND: Digital Ground .

The timing diagrams for updating the DAC register are shown in *Figures 1* and *2.*

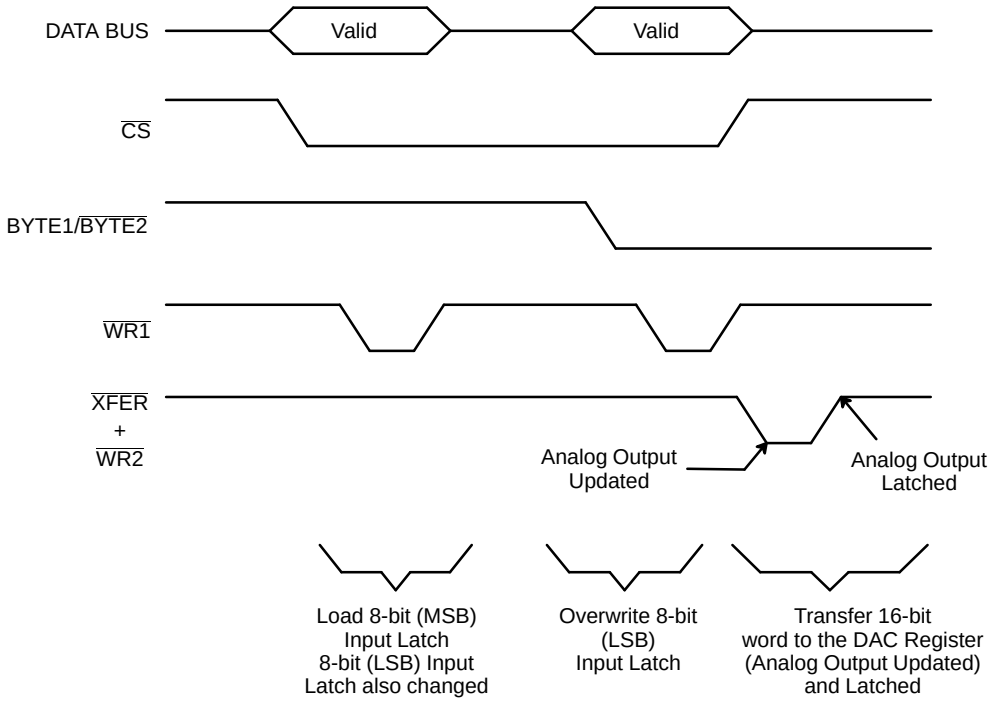



**Figure 1. Typical Interface with an 8-bit Data Bus**

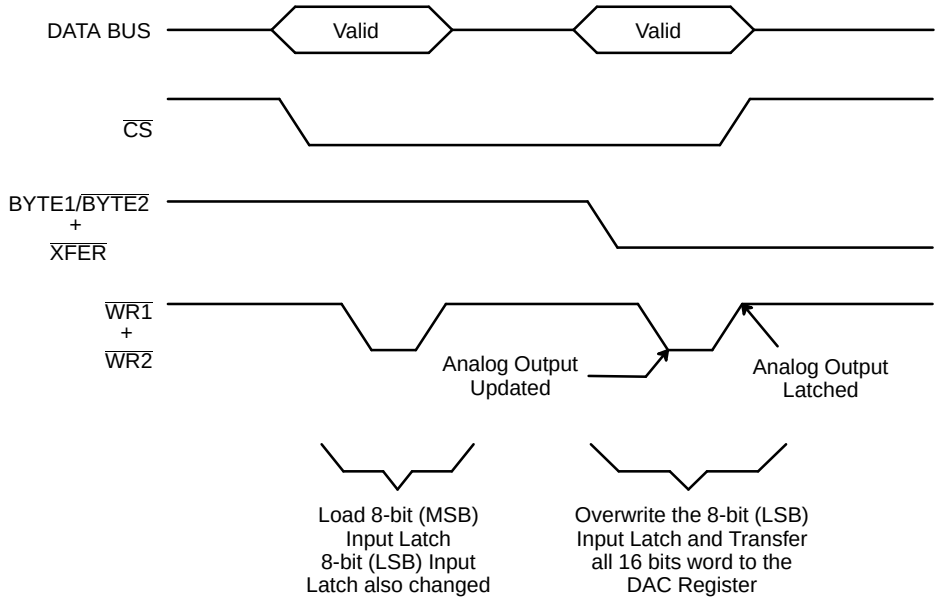
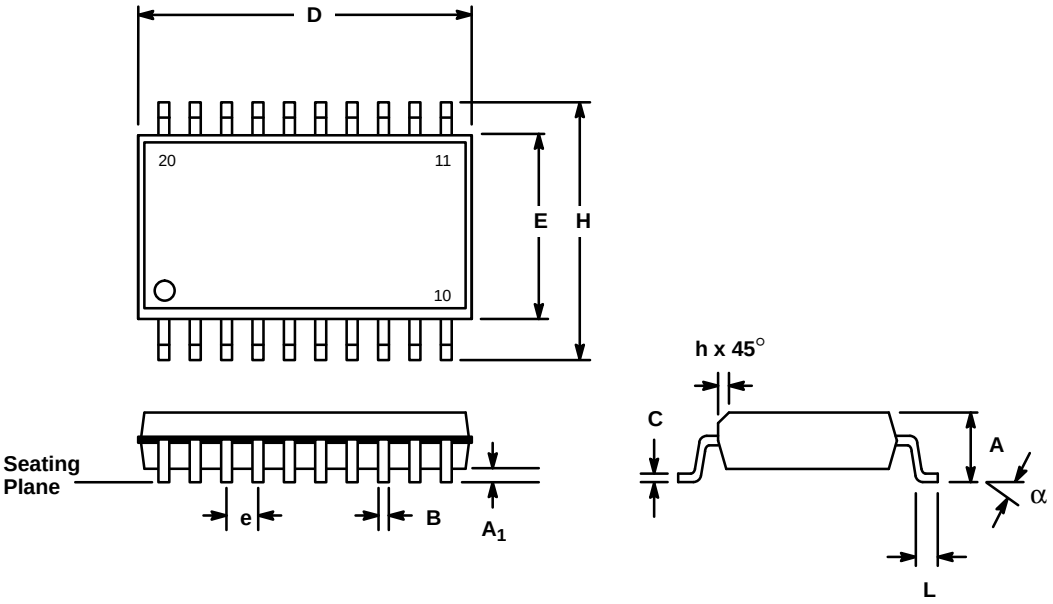
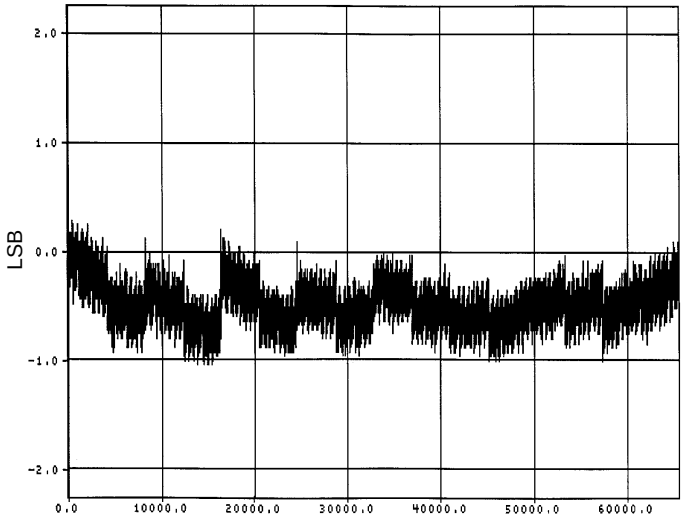



**Figure 2. Automatic Transfer**

## 20 LEAD SMALL OUTLINE
## (300 MIL JEDEC SOIC)
## S20




| SYMBOL | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.097 | 0.104 | 2.464 | 2.642 |
| $A_1$ | 0.0050 | 0.0115 | 0.127 | 0.292 |
| B | 0.014 | 0.019 | 0.356 | 0.483 |
| C | 0.0091 | 0.0125 | 0.231 | 0.318 |
| D | 0.500 | 0.510 | 12.70 | 12.95 |
| E | 0.292 | 0.299 | 7.42 | 7.59 |
| e | 0.050 BSC | | 1.27 BSC | |
| H | 0.400 | 0.410 | 10.16 | 10.41 |
| h | 0.010 | 0.016 | 0.254 | 0.406 |
| L | 0.016 | 0.035 | 0.406 | 0.889 |
| α | 0° | 8° | 0° | 8° |




**Graph 1. Relative Accuracy vs. Digital Code**