

184pin Two Bank Unbuffered DDR SDRAM MODULE Based on DDR333 16Mx8 SDRAM

Features

- 184-Pin Unbuffered 8-Byte Dual In-Line Memory Module
- 32Mx64 Double Data Rate (DDR) SDRAM DIMM
- Performance :

Speed Sort	PC2700		Unit
	2.5	2	
DIMM CAS Latency	166	133	MHz
f CK Clock Frequency	6	7.5	ns
t CK Clock Cycle	333	266	MHz
f DQ DQ Burst Frequency			

- Intended for 166 MHz and 133 MHz applications
- Inputs and outputs are SSTL-2 compatible
- V_{DD} = 2.5Volt ± 0.2, V_{DDQ} = 2.5Volt ± 0.2
- Single Pulsed RAS interface
- SDRAMs have 4 internal banks for concurrent operation
- Module has two physical banks
- Differential clock inputs
- Data is read or written on both clock edges

- DRAM DLL aligns DQ and DQS transitions with clock transitions. Also aligns QFC transitions with clock during Read cycles
- Address and control signals are fully synchronous to positive clock edge
- Programmable Operation:
 - DIMM CAS Latency: 2, 2.5
 - Burst Type: Sequential or Interleave
 - Burst Length: 2, 4, 8
 - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 12/10/2 Addressing (row/column/bank)
- 15.6 μs Max. Average Periodic Refresh Interval
- Serial Presence Detect
- Gold contacts
- SDRAMs in 66-pin TSOP Type II Package

Description

NT256D64S8HA0G-6 is an unbuffered 184-Pin Double Data Rate (DDR) Synchronous DRAM Dual In-Line Memory Module (DIMM), organized as a dual-bank high-speed memory array. The 32Mx64 module is a two-bank DIMM that uses sixteen 16Mx8 DDR SDRAMs in 400 mil TSOP packages. The DIMM achieves high-speed data transfer rates of up to 333MHz. The DIMM is intended for use in applications operating from 133 MHz to 166 MHz clock speeds with data rates of 266 to 333 MHz. Clock enable CKE0 and / or CKE1 controls all devices on the DIMM.

Prior to any access operation, the device CAS latency and burst type/ length/operation type must be programmed into the DIMM by address inputs A0-A11 and I/O inputs BA0 and BA1 using the mode register set cycle.

These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers.

The DIMM uses serial presence detects implemented via a serial EEPROM using the two-pin IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The last 128 bytes are available to the customer.

All NANYA 184 DDR SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint.

Ordering Information

Part Number	Speed	Organization	Leads	Power	
NT256D64S8HA0G-6	166MHz (7ns @ CL = 2.5)	PC2700	32Mx64	Gold	2.5V
	133MHz (7.5ns @ CL= 2)				

Pin Description

CK0, CK1, CK2 CK0, CK1, CK2	Differential Clock Inputs	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	DQS0-DQS7, DQS9-DQS16	Bidirectional data strobes
RAS	Row Address Strobe		
CAS	Column Address Strobe	VDD	Power (2.5V)
WE	Write Enable	VDDQ	Supply voltage for DQs(2.5V)
S0, S1	Chip Selects	VSS	Ground
A0-A9, A11	Address Inputs	NC	No Connect
A10/AP	Address Input/Autoprecharge	SCL	Serial Presence Detect Clock Input
BA0, BA1	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
VREF	Ref. Voltage for SSTL_2 inputs	SA0-2	Serial Presence Detect Address Inputs
VDDID	VDD Identification flag.	VDDSPD	Serial EEPROM positive power supply(2.5V)

Pinout

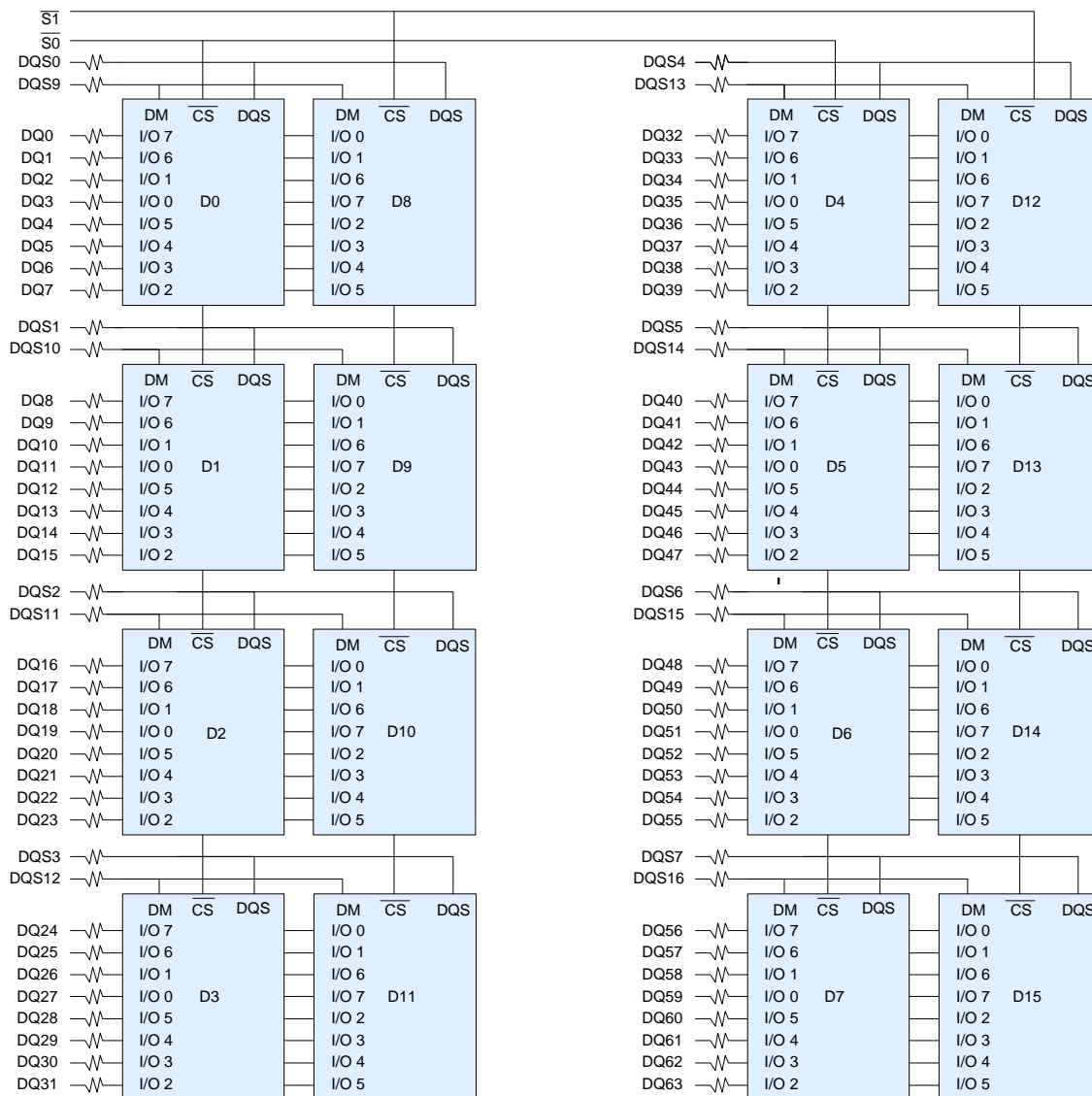
Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREF	93	Vss	32	A5	124	Vss	62	VDDQ	154	RAS
2	DQ0	94	DQ4	33	DQ24	125	A6	63	WE	155	DQ45
3	Vss	95	DQ5	34	Vss	126	DQ28	64	DQ41	156	VDDQ
4	DQ1	96	VDDQ	35	DQ25	127	DQ29	65	CAS	157	S0
5	DQS0	97	DQS9	36	DQS3	128	VDDQ	66	Vss	158	S1
6	DQ2	98	DQ6	37	A4	129	DQS12	67	DQS5	159	DQS14
7	VDD	99	DQ7	38	VDD	130	A3	68	DQ42	160	Vss
8	DQ3	100	Vss	39	DQ26	131	DQ30	69	DQ43	161	DQ46
9	NC	101	NC	40	DQ27	132	Vss	70	VDD	162	DQ47
10	NC	102	NC	41	A2	133	DQ31	71	NC	163	NC
11	Vss	103	NC	42	Vss	134	NC	72	DQ48	164	VDDQ
12	DQ8	104	VDDQ	43	A1	135	NC	73	DQ49	165	DQ52
13	DQ9	105	DQ12	44	NC	136	VDDQ	74	Vss	166	DQ53
14	DQS1	106	DQ13	45	NC	137	CK0	75	CK2	167	NC
15	VDDQ	107	DQS10	46	VDD	138	CK0	76	CK2	168	VDD
16	CK1	108	VDD	47	NC	139	Vss	77	VDDQ	169	DQS15
17	CK1	109	DQ14	48	A0	140	NC	78	DQS6	170	DQ54
18	Vss	110	DQ15	49	NC	141	A10	79	DQ50	171	DQ55
19	DQ10	111	CKE1	50	Vss	142	NC	80	DQ51	172	VDDQ
20	DQ11	112	VDDQ	51	NC	143	VDDQ	81	Vss	173	NC
21	CKE0	113	NC	52	BA1	144	NC	82	VDDID	174	DQ60
22	VDDQ	114	DQ20		KEY		KEY	83	DQ56	175	DQ61
23	DQ16	115	NC	53	DQ32	145	Vss	84	DQ57	176	Vss
24	DQ17	116	Vss	54	VDDQ	146	DQ36	85	VDD	177	DQS16
25	DQS2	117	DQ21	55	DQ33	147	DQ37	86	DQS7	178	DQ62
26	Vss	118	A11	56	DQS4	148	VDD	87	DQ58	179	DQ63
27	A9	119	DQS11	57	DQ34	149	DQS13	88	DQ59	180	VDDQ
28	DQ18	120	VDD	58	Vss	150	DQ38	89	Vss	181	SA0
29	A7	121	DQ22	59	BA0	151	DQ39	90	NC	182	SA1
30	VDDQ	122	A8	60	DQ35	152	Vss	91	SDA	183	SA2
31	DQ19	123	DQ23	61	DQ40	153	DQ44	92	SCL	184	VDDSPD

Note: All pin assignments are consistent for all 8-byte unbuffered versions.

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0 , CK1, CK2	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
$\overline{CK0}$, $\overline{CK1}$, $\overline{CK2}$	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{S0}$, $\overline{S1}$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
\overline{RAS} , \overline{CAS} , \overline{WE}	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, \overline{RAS} , \overline{CAS} , \overline{WE} define the operation to be executed by the SDRAM.
VREF	Supply		Reference voltage for SSTL-2 inputs
VDDQ	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA0, BA1	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP A11	(SSTL)	-	During a Bank Activate command cycle, A0-A11 defines the row address (RA0-RA11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 define the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 - DQ63,	(SSTL)	-	Data and Check Bit input/output pins operate in the same manner as on conventional DRAMs.
DQS0 - DQS7 DQS9 - DQS16	(SSTL)	Active High	Data strobes: Output with read data, input with write data. Edge aligned with read data, centered on write data. Used to capture write data.
VDD , VSS	Supply		Power and ground for the DDR SDRAM input buffers and core logic
SA0 – SA2		-	Address inputs. Connected to either VDD or VSS on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to VDD to act as a pullup.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to VDD to act as a pullup.
VDDSPD	Supply		Serial EEPROM positive power supply.

Functional Block Diagram (2 Bank, 16Mx8 DDR SDRAMs)



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.5 to VDDQ+0.5	V
V_{IN}	Voltage on Input relative to Vss	-0.5 to +3.6	V
V_{DD}	Voltage on VDD supply relative to Vss	-0.5 to +3.6	V
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-0.5 to +3.6	V
T_A	Operating Temperature (Ambient)	0 to+70	°C
T_{STG}	Storage Temperature (Plastic)	-55 to +150	°C
P_D	Power Dissipation	16	W
I_{OUT}	Short Circuit Output Current	50	mA

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance

Parameter	Symbol	Max.	Units	Notes
Input Capacitance: $CK0, \overline{CK0}, CK1, \overline{CK1}, CK2, \overline{CK2}$	C11	24	pF	1
Input Capacitance: A0-A11, BA0, BA1, $\overline{WE}, \overline{RAS}, \overline{CAS}$	C12	60	pF	1
Input Capacitance: $CKE0, CKE1, \overline{S0}, \overline{S1}$	C13	30	pF	1
Input/Output Capacitance DQ0-63; DQS0-7, 9-16	C101	14	pF	1,2

1. $V_{DDQ} = V_{DD} = 2.5V \pm 0.2V$, $f = 100$ MHz, $T_A = 25$ °C, $V_{OUT} (DC) = V_{DDQ}/2$, $V_{OUT} (Peak\ to\ Peak) = 0.2V$.

2. DQS inputs are grouped with I/O pins reflecting the fact that they are matched in loading to DQ and DQS to facilitate trace matching at the board level.

DC Electrical Characteristics and Operating Conditions

($T_A = 0\text{ }^\circ\text{C} \sim 70\text{ }^\circ\text{C}$; $V_{DDQ} = 2.5V \pm 0.2V$; $V_{DD} = 2.5V \pm 0.2V$, See AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	2.3	2.7	V	1
V_{DDQ}	I/O Supply Voltage	2.3	2.7	V	1
V_{SS} , V_{SSQ}	Supply Voltage, I/O Supply Voltage	0	0	V	
V_{REF}	I/O Reference Voltage	$0.49 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	1,2
V_{TT}	I/O Termination Voltage (System)	$V_{REF} - 0.04$	$V_{REF} + 0.04$	V	1,3
$V_{IH(DC)}$	Input High (Logic1) Voltage	$V_{REF} + 0.15$	$V_{DDQ} + 0.3$	V	1
$V_{IL(DC)}$	Input Low (Logic0) Voltage	-0.3	$V_{REF} - 0.15$	V	1
$V_{IN(DC)}$	Input Voltage Level, CK and \overline{CK} Inputs	-0.3	$V_{DDQ} + 0.3$	V	1
$V_{ID(DC)}$	Input Differential Voltage, CK and \overline{CK} Inputs	0.30	$V_{DDQ} + 0.6$	V	1,4
I_I	Input Leakage Current Any input $0V \leq V_{IN} \leq V_{DD}$; (All other pins not under test = 0V)	-5	5	μA	1
I_{OZ}	Output Leakage Current (DQs are disabled; $0V \leq V_{out} \leq V_{DDQ}$)	-5	5	μA	1
I_{OH}	Output High Current ($V_{OUT} = V_{DDQ} - 0.373V$, min V_{REF} , min V_{TT})	-16.8	-	mA	1
I_{OL}	Output Low Current ($V_{OUT} = 0.373$, max V_{REF} , max V_{TT})	16.8	-	mA	1

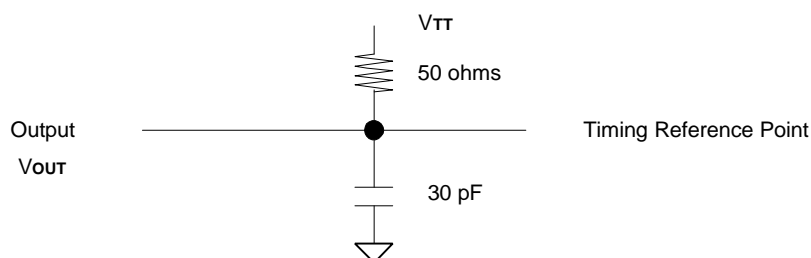
1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to $0.5 V_{DDQ}$ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
3. V_{TT} is not applied directly to the DIMM. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} , and must track variations in the DC level of V_{REF} .
4. V_{ID} is the magnitude of the difference between the input level on CK and the input level on \overline{CK} .

AC Characteristics

(Notes 1-5 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, Operating, Standby, and Refresh Currents, and Electrical Characteristics and AC Timing.)

1. All voltages referenced to VSS .
2. Tests for AC timing, I_{DD} , and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load. Refer to the AC Output Load Circuit below.
4. AC timing and I_{DD} tests may use a V_{IL} to V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK, \overline{CK}), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$ unless otherwise specified.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.

AC Output Load Circuits



AC Operating Conditions

($T_A = 0\text{ }^{\circ}\text{C} \sim 70\text{ }^{\circ}\text{C}$; $V_{DDQ} = 2.5\text{V} \pm 0.2\text{V}$; $V_{DD} = 2.5\text{V} \pm 0.2\text{V}$, See AC Characteristics)

Symbol	Parameter/Condition	Min	Max	Unit	Notes
$V_{IH(AC)}$	Input High (Logic 1) Voltage.	$V_{REF} + 0.31$	-	V	1, 2
$V_{IL(AC)}$	Input Low (Logic 0) Voltage.	-	$V_{REF} - 0.31$	V	1, 2
$V_{ID(AC)}$	Input Differential Voltage, CK and \overline{CK} Inputs	0.62	$V_{DDQ} + 0.6$	V	1, 2, 3
$V_{IX(AC)}$	Input Differential Pair Cross Point Voltage, CK and \overline{CK} Inputs	$(0.5 * V_{DDQ}) - 0.2$	$(0.5 * V_{DDQ}) + 0.2$	V	1, 2, 4

1. Input skew rate = 1V/ ns .
2. Inputs are not recognized as valid until V_{REF} stabilizes.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on \overline{CK} .
4. The value of V_{IX} is expected to equal $0.5 * V_{DDQ}$ of the transmitting device and must track variations in the DC level of the same.

Operating, Standby, and Refresh Currents

($T_A = 0\text{ }^{\circ}\text{C} \sim 70\text{ }^{\circ}\text{C}$; $V_{DDQ} = 2.5\text{V} \pm 0.2\text{V}$; $V_{DD} = 2.5\text{V} \pm 0.2\text{V}$, See AC Characteristics)

Symbol	Parameter/Condition	PC2700	Unit	Notes	
I _{DD0}	Operating Current : one bank; active / precharge; $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1160	mA	1,2	
I _{DD1}	Operating Current : one bank; active / read / precharge; Burst = 2; $t_{RC} = t_{RC}(\text{MIN})$; $CL=2.5$; $t_{CK} = t_{CK}(\text{MIN})$; $I_{OUT} = 0\text{mA}$; address and control inputs changing once per clock cycle	1360	mA	1,2	
I _{DD2P}	Precharge Power-Down Standby Current : all banks idle; power-down mode; $CKE \leq V_{IL}(\text{MAX})$; $t_{CK} = t_{CK}(\text{MIN})$	240	mA	1,2	
I _{DD2N}	Idle Standby Current : $CS \geq V_{IH}(\text{MIN})$; all banks idle; $CKE \geq V_{IH}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; address and control inputs changing once per clock cycle	560	mA	1,2	
I _{DD3P}	Active Power-Down Standby Current : one bank active; power-down mode; $CKE \leq V_{IL}(\text{MAX})$; $t_{CK} = t_{CK}(\text{MIN})$	240	mA	1,2	
I _{DD3N}	Active Standby Current : one bank; active / precharge; $CS \geq V_{IH}(\text{MIN})$; $CKE \geq V_{IH}(\text{MIN})$; $t_{RC} = t_{RAS}(\text{MAX})$; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	960	mA	1,2	
I _{DD4R}	Operating Current : one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; $CL = 2.5$; $t_{CK} = t_{CK}(\text{MIN})$; $I_{OUT} = 0\text{mA}$	1800	mA	1,2	
I _{DD4W}	Operating Current : one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; $CL=2.5$; $t_{CK} = t_{CK}(\text{MIN})$	1680	mA	1,2	
I _{DD5}	Auto-Refresh Current :	$t_{RC} = t_{RFC}(\text{MIN})$	2400	mA	1,2
		$t_{RC} = 15.625\text{ }\mu\text{s}$	252	mA	1,2,4
I _{DD6}	Self-Refresh Current : $CKE \leq 0.2\text{V}$	32	mA	1,2,3	

AC Timing Specifications for DDR SDRAM Devices Used on Module

(TA = 0 °C ~ 70 °C ; VDDQ = 2.5V ± 0.2V; VDD = 2.5V ± 0.2V, See AC Characteristics)

Symbol	Parameter	-6		Unit	Notes	
		Min.	Max.			
tAC	DQ output access time from CK/ $\overline{\text{CK}}$	-0.7	+0.7	ns	1,2,3,4	
tDQSK	DQS output access time from CK/ $\overline{\text{CK}}$	-0.7	+0.7	ns	1,2,3,4	
tCH	CK high-level width	0.45	0.55	tCK	1,2,3,4	
tCL	CK low-level width	0.45	0.55	tCK	1,2,3,4	
tCK	Clock cycle time	CL=2.5	6	12	ns	1,2,3,4
		CL=2	7.5	12	ns	1,2,3,4
tDH	DQ and DM input hold time	0.45		ns	1,2,3,4,15,16	
tDS	DQ and DM input setup time	0.45		ns	1,2,3,4,15,16	
tDIPW	DQ and DM input pulse width (each input)	1.75		ns	1,2,3,4	
tHZ	Data-out high-impedance time from CK/ $\overline{\text{CK}}$	-0.7	+0.7	ns	1, 2, 3, 4, 5	
tLZ	Data-out low-impedance time from CK/ $\overline{\text{CK}}$	-0.7	+0.7	ns	1, 2, 3, 4, 5	
tDQSQ	DQS-DQ skew (DQS & associated DQ signals)		0.4	ns	1,2,3,4	
tHP	Minimum half CLK period for any given cycle; defined by CLK high(tCH) or CLK low (tCL) time	tCH or tCL		tCK	1,2,3,4	
tQH	Data output hold time from DQS	tHP - 0.75ns		tCK	1,2,3,4	
tDQSS	Write command to 1st DQS latching transition	0.75	1.25	tCK	1,2,3,4	
tDQSL,H	DQS input low (high) pulse width (write cycle)	0.35		tCK	1,2,3,4	
tDSS	DQS falling edge to CK setup time (write cycle)	0.2		tCK	1,2,3,4	
tDSH	DQS falling edge hold time from CK (write cycle)	0.2		tCK	1,2,3,4	
tMRD	Mode register set command cycle time	2		tCK	1,2,3,4	
tWPRES	Write preamble setup time	0		ns	1, 2, 3, 4, 7	
tWPST	Write postamble	0.40	0.60	tCK	1, 2, 3, 4, 6	
tWPRE	Write preamble	0.25		tCK	1,2,3,4	
tIH	Address and control input hold time (fast slew rate)	0.75		ns	2, 3, 4, 9, 11,12	
tIS	Address and control input setup time (fast slew rate)	0.75		ns	2, 3, 4, 9, 11,12	
tIH	Address and control input hold time (slow slew rate)	0.8		ns	2, 3, 4,10, 11,12, 14	
tIS	Address and control input setup time (slow slewrate)	0.8		ns	2, 3, 4,10, 11,12, 14	
tIPW	Input pulse width	2.2		ns	2, 3, 4,12	
tRPRE	Read preamble	0.9	1.1	tCK	1,2,3,4	
tRPST	Read postamble	0.40	0.60	tCK	1,2,3,4	
tRAS	Active to Precharge command	42	120,000	ns	1,2,3,4	
tRC	Active to Active/Auto-refresh command period	60		ns	1,2,3,4	
tRFC	Auto-refresh to Active/Auto-refresh command period	72		ns	1,2,3,4	
tRCD	Active to Read or Write delay	18		ns	1,2,3,4	
tRAP	Active to Read Command with Autoprecharge	18		ns	1,2,3,4	
tRP	Precharge command period	18		ns	1,2,3,4	
tRRD	Active bank A to Active bank B command	12		ns	1,2,3,4	
tWR	Write recovery time	15		ns	1,2,3,4	
tDAL	Auto precharge write recovery + precharge time	(tWR/tCK) + (tRP/tCK)		tCK	1, 2, 3, 4, 13	
tWTR	Internal write to read command delay	1		tCK	1,2,3,4	
tXSNR	Exit self-refresh to non-read command	75		ns	1,2,3,4	
tXSRD	Exit self-refresh to read command	200		tCK	1,2,3,4	
tREFI	Average Periodic Refresh Interval		15.6	µs	1, 2, 3, 4, 8	

AC Timing Specification Notes

- Input slew rate = 1V/ns.
- The $\overline{CK}/\overline{CK}$ input reference level (for timing reference to $\overline{CK}/\overline{CK}$) is the point at which \overline{CK} and \overline{CK} cross: the input reference level for signals other than $\overline{CK}/\overline{CK}$, is VREF.
- Inputs are not recognized as valid until VREF stabilizes.
- The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (Note 3) is VTT.
- tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
- The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
- The specific requirement is that DQS be valid (high, low, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from high to low at this time, depending on tDQSS.
- A maximum of eight Auto refresh commands can be posted to any given DDR SDRAM device.
- For command/address input slew rate ≥ 1.0 V/ns. Slew rate is measured between VOH (AC) and VOL (AC).
- For command/address input slew rate ≥ 0.5 V/ns and < 1.0 V/ns. Slew rate is measured between VOH (AC) and VOL (AC).
- $\overline{CK}/\overline{CK}$ slew rates are ≥ 1.0 V/ns.
- These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester characterization.
- For each of the terms in parentheses, if not already an integer, round to the next highest integer. tCK is equal to the actual system clock cycle time. For example, for PC2100 at CL= 2.5, tDAL = (15ns/7.5ns) +(20ns/7.0ns) = 2 + 3 = 5.
- An input setup and hold time derating table is used to increase tIS and tIH in the case where the input slew rate is below 0.5 V/ns.

Input Slew Rate	Delta (tIS)	Delta (tIH)	Unit	Note
0.5 V/ns	0	0	ps	1,2
0.4 V/ns	+50	0	ps	1,2
0.3 V/ns	+100	0	ps	1,2

1. Input slew rate is based on the lesser of the slew rates determined by either V IH (AC) to V IL (AC) or V IH (DC) to V IL (DC) , similarly for rising transitions.
2. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

- An input setup and hold time derating table is used to increase tDS and tDH in the case where the I/O slew rate is below 0.5 V/ns.

Input Slew Rate	Delta (tDS)	Delta (tDH)	Unit	Note
0.5 V/ns	0	0	ps	1,2
0.4 V/ns	+75	+75	ps	1,2
0.3 V/ns	+150	+150	ps	1,2

1. I/O slew rate is based on the lesser of the slew rates determined by either V IH (AC) to V IL (AC) or V IH (DC) to V IL (DC) , similarly for rising transitions.
2. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

- An I/O Delta Rise, Fall Derating table is used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ.

Delta Rise and Fall Rate	Delta (tDS)	Delta (tDH)	Unit	Note
0.0 ns/V	0	0	ps	1,2,3,4
0.25 ns/V	+50	+50	ps	1,2,3,4
0.5 ns/V	+100	+100	ps	1,2,3,4

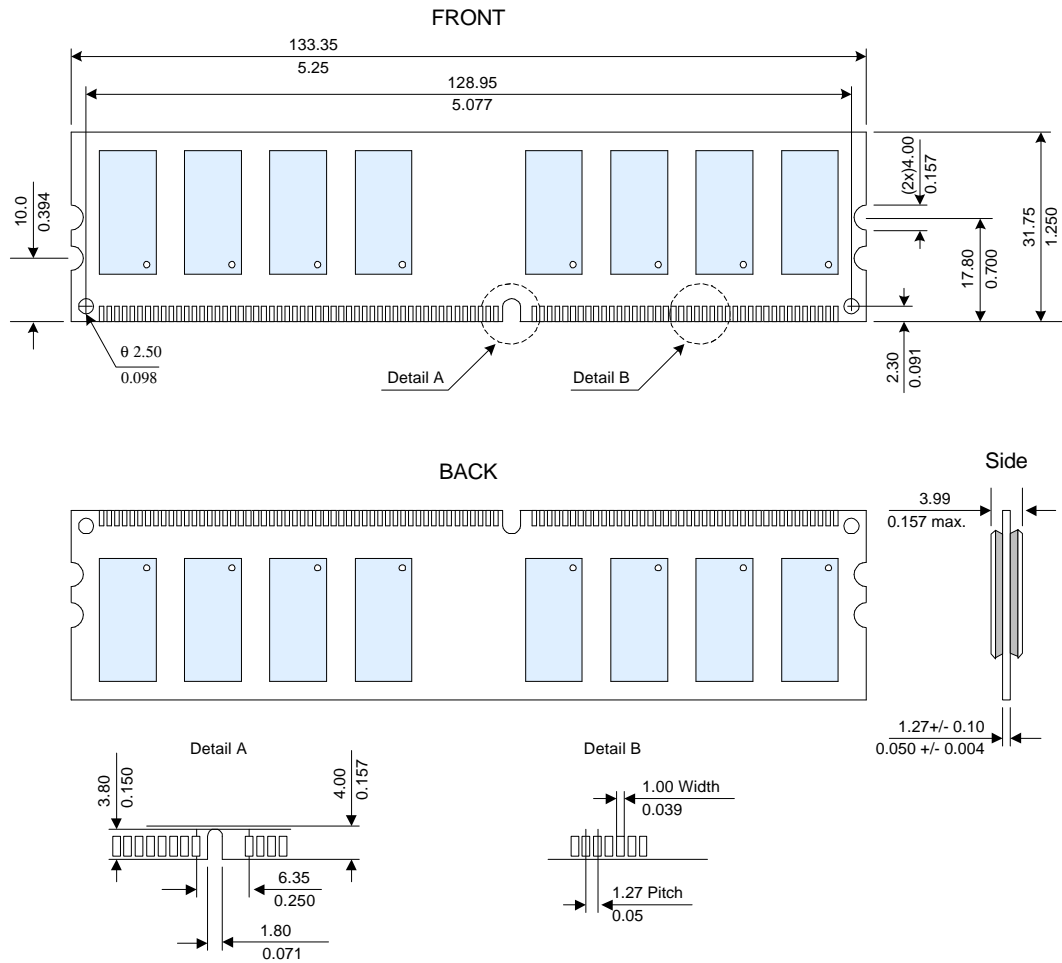
1. Input slew rate is based on the lesser of the slew rates determined by either V IH (AC) to V IL (AC) or V IH (DC) to V IL (DC) , similarly for rising transitions.
2. Input slew rate is based on the larger of AC to AC delta rise, fall rate and DC to DC delta rise, fall rate.
3. The delta rise, fall rate is calculated as: $[1/(\text{slew rate } 1)] - [1/(\text{slew rate } 2)]$
For example: slew rate 1 = 0.5 V/ns; slew rate 2 = 0.4 V/ns. Delta rise, fall = (1/0.5) - (1/0.4) [ns/V] = -0.5 ns/V
Using the table above, this would result in an increase in tDS and tDH of 100 ps.
4. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

Serial Presence Detect

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		-6			-6			
0	Number of Serial PD Bytes Written during Production	128			80			
1	Total Number of Bytes in Serial PD device	256			08			
2	Fundamental Memory Type	SDRAM DDR			07			
3	Number of Row Addresses on Assembly	12			0C			
4	Number of Column Addresses on Assembly	10			0A			
5	Number of DIMM Bank	2			02			
6.	Data Width of Assembly	X64			40			
7	Data Width of Assembly (cont')	X64			00			
8	Voltage Interface Level of this Assembly	SSTL 2.5V			04			
9	SDRAM Device Cycle Time at CL=2.5	6ns			60			
10	SDRAM Device Access Time from Clock at CL=2.5	0.7ns			70			
11	DIMM Configuration Type	Non-Parity			00			
12	Refresh Rate/Type	15.6µs / SR			80			
13	Primary SDRAM Width	X8			08			
14	Error Checking SDRAM Device Width	N/A			00			
15	SDRAM Device Attributes : Minimum Clock Delay, Random Column Access	1 Clock			01			
16	SDRAM Device Attributes: Burst Length Supported	2,4,8			0E			
17	SDRAM Device Attributes: Number of Device Banks	4			04			
18	SDRAM Device Attributes: $\overline{\text{CAS}}$ Latency	2, 2.5			0C			
19	SDRAM Device Attributes: $\overline{\text{CS}}$ Latency	0			01			
20	SDRAM Device Attributes: WE Latency	1			02			
21	SDRAM Module Attributes	Differential Clock			20			
22	SDRAM Device Attributes: General	+/-0.2V Voltage Tolerance			00			
23	Minimum Clock Cycle at CL=2	7.5ns			75			
24	Maximum Data Access Time from Clock at CL=2	± 0.7ns			70			
25	Minimum Clock Cycle Time at CL=1	N/A			00			
26	Maximum Data Access Time from Clock at CL=1	N/A			00			
27	Minimum Row Precharge Time (tRP)	18ns			48			
28	Minimum Row Active to Row Active delay (tRRD)	12ns			30			
29	Minimum RAS to CAS delay (tRCD)	18ns			48			
30	Minimum RAS Pulse Width (tRAS)	42ns			2A			
31	Module Bank Density	128MB			20			
32	Address and Command Setup Time Before Clock	0.75ns			75			
33	Address and Command Hold Time After Clock	0.75ns			75			
34	Data Input Setup Time Before Clock	0.45ns			45			
35	Data Input Hold Time After Clock	0.45ns			45			
36-61	Reserved	Undefined			00			
62	SPD Revision	0			00			
63	Checksum Data				E8			
64-71	Manufacturer's JEDED ID Code	NANYA			7F7F7F0B00000000			
72	Module Manufacturing Location	N/A			00			
73-90	Module Part number	N/A	N/A	N/A	00	00	00	
91-92	Module Revision Code	N/A			00			
93-94	Module Manufacturing Data	Year / Week Code			yy/ww			1,2
95-98	Module Serial Number	Serial Number			00			
99-255	Reserved	Undefined			00			

1. yy= Binary coded decimal year code, 0-99(Decimal), 00-63(Hex)
2. ww= Binary coded decimal year code, 01-52(Decimal), 01-34(Hex)

Package Dimensions



Note : All dimensions are typical unless otherwise stated.

Unit : $\frac{\text{Millimeters}}{\text{Inches}}$

Revision Log

Date	Rev.	Descriptions
11/2001	Preliminary *1	Initial release

[Note]

*1 Preliminary: PRODUCTS AND SPECIFICATIONS DISCUSSED HEREIN ARE FOR EVALUATION AND REFERENCE PURPOSES ONLY AND ARE SUBJECT TO CHANGE BY NANYA WITHOUT NOTICE. PRODUCTS ARE ONLY WARRANTED BY NANYA TO MEET MICRON'S PRODUCTION DATA SHEET SPECIFICATIONS.