1 PRODUCT OVERVIEW

OVERVIEW

The S3C7335 single-chip CMOS microcontroller has been designed for high performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers).

With features such as LCD direct drive capability, 4-channel A/D converter, 8-bit timer/counter, watch timer and PLL frequency synthesizer, it offers you an excellent design solution for a wide variety of applications that require LCD functions and audio applications.

Up to 56 pins of the 80-pin QFP package, it can be dedicated to I/O. Eight vectored interrupts provide fast response to internal and external events. In addition, the S3C7335's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

OTP

The S3C7335 microcontroller is also available in OTP (One Time Programmable) version, S3P7335. The S3P7335 microcontroller has an on-chip 16-Kbyte one-time-programmable EPROM instead of masked ROM. The S3P7335 is comparable to S3C7335, both in function and in pin configuration.

FEATURES

Memory

- 512-nibble RAM
- 16K-byte ROM

I/O Pins

- Input only: 4 pins
- Output only: 28 pins
- I/O: 24 pins

LCD Controller/Driver

- Maximum 14-digit LCD direct drive capability
- 28 segment x 4 common signals
- Display modes: Static, 1/2 duty (1/2 bias)
  1/3 duty (1/2 or 1/3 bias), 1/4 duty (1/3 bias)

8-Bit Basic Timer

- Programmable interval timer functions
- Watch-dog timer function

8-Bit Timer/Counter

- Programmable 8-bit timer
- External event counter
- Arbitrary clock frequency output
- External clock signal divider
- Serial I/O interface clock generator

Watch Timer

- Time interval generation
  : 0.5 s, 3.9 ms at 32.768 kHz
- Frequency outputs to BUZ pin
- Clock source generation for LCD

8-Bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- Data direction selectable (LSB-first or MSB-first)
- Internal or external clock source

A/D Converter

- 4-channels with 8-bit resolution

Bit Sequential Carrier Buffer

- Support 16-bit serial data transfer in arbitrary format

PLL Frequency Synthesizer

- Level = 300 mVp-p (min)
- AMVCO range = 0.5 MHz to 30 MHz
- FMVCO range = 30 MHz to 150 MHz

16-Bit Intermediate Frequency (IF) Counter

- Level = 300 mVp-p (min)
- AMIF range = 100 kHz to 1 MHz
- FMIF range = 5 MHz to 15 MHz

FEATURES (Continued)

Interrupts

- Four internal vectored interrupts
- Four external vectored interrupts
- Two quasi-interrupts

Memory-Mapped I/O Structure

- Data memory bank 15

Three Power-Down Modes

- Idle: Only CPU clock stops
- Stop1: Main system or subsystem clock stops
- Stop2: Main system and subsystem clock stop
- CE low: PLL and IFC stop

Oscillation Sources

- Crystal or ceramic oscillator for main system clock
- Crystal for subsystem clock
- Main system clock frequency: 4.5 MHz (Typ)
- Subsystem clock frequency: 32.768 kHz (Typ)
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.9, 1.8, 14.2 μs at 4.5 MHz
- 122 μs at 32.768 kHz (subsystem)

Operating Temperature

- – 40 °C to 85 °C

Operating Voltage Range

- 1.8 V to 5.5 V at 3MHz
- PLL/IFC operation: 2.5V to 3.5V or 4.0V to 5.5V

Package Type

- 80-pin QFP

BLOCK DIAGRAM

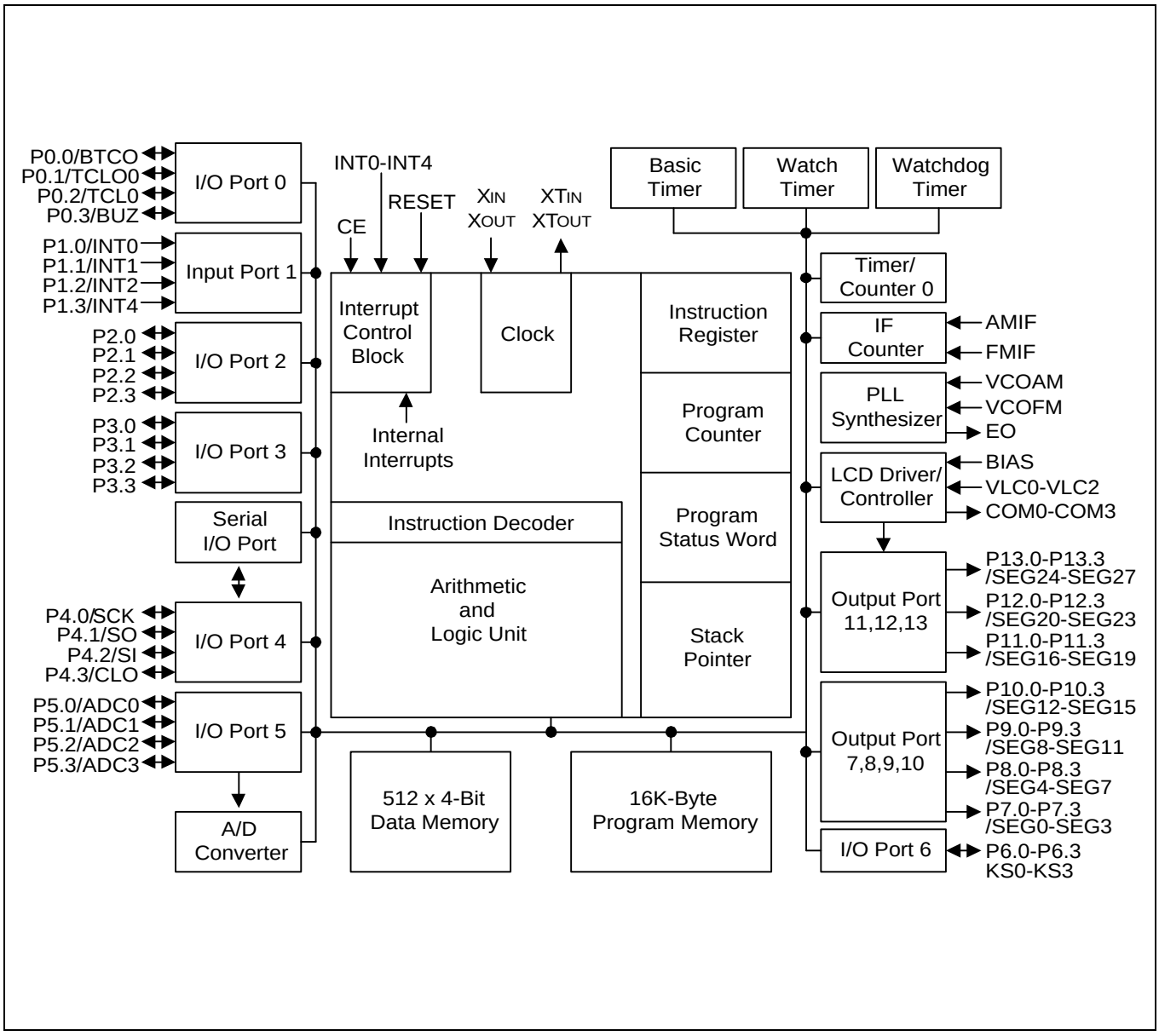


Figure 1-1. S3C7335 Simplified Block Diagram

PIN ASSIGNMENTS

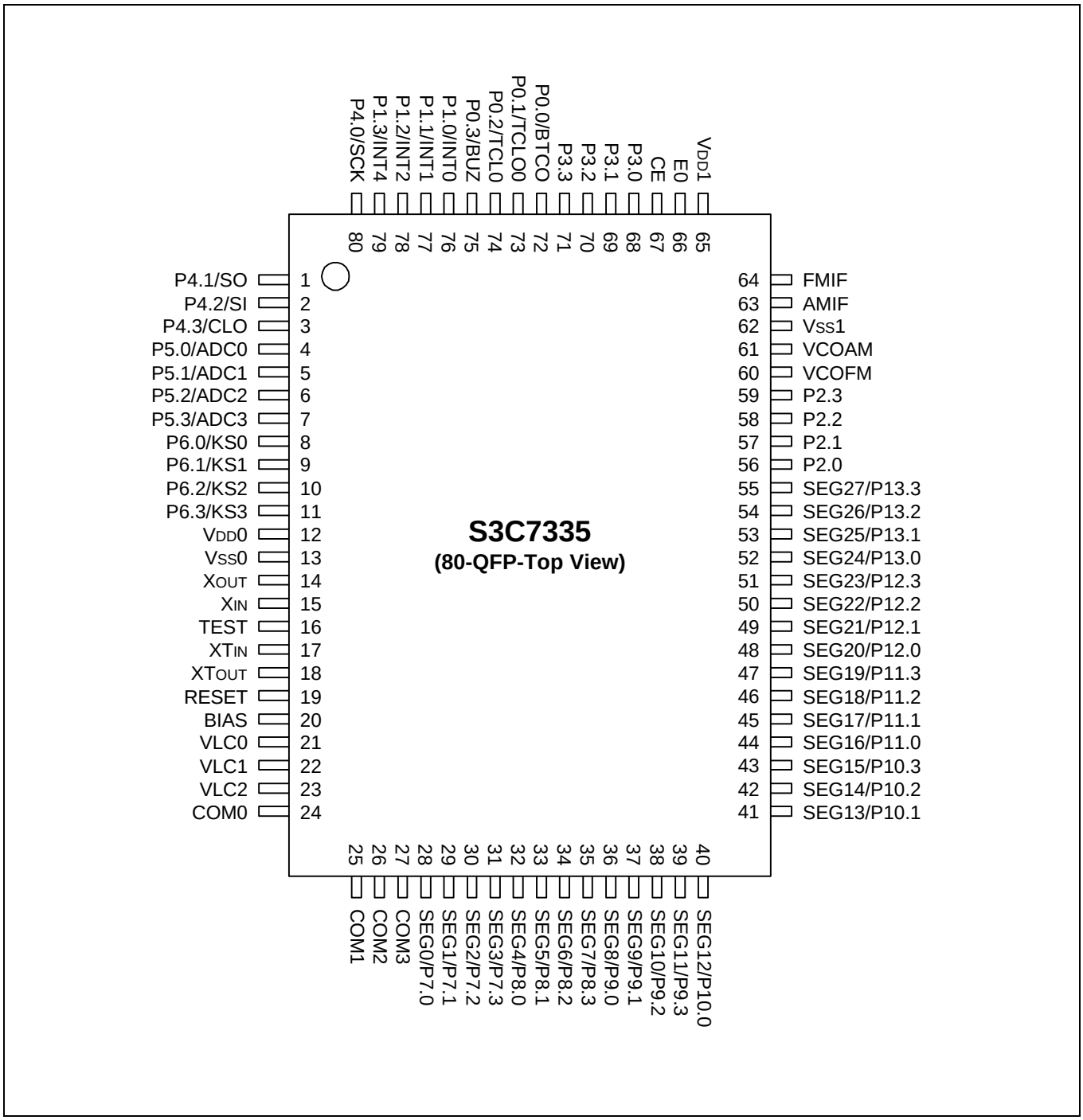


Figure 1-2. S3C7335 80-QFP Pin Assignment

PIN DESCRIPTIONS

Table 1-1. S3C7335 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin	Reset Value	Circuit Type
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit or 4-bit read, write, and test are possible. Pull-up resistors can be configured by software.	72 73 74 75	BTCO TCLO0 TCL0 BUZ	Input	D-2 D-2 D-4 D-2
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit or 4-bit read and test are possible. Pull-up resistors can be configured by software.	76 77 78 79	INT0 INT1 INT2 INT4	Input	A-4
P2.0-P2.3 P3.0-P3.3	I/O	4-bit I/O ports. 1-bit, 4-bit or 8-bit read, write and test are possible. Pull-up resistors can be configured by software. Ports 2 and 3 can be paired to support 8-bit data transfer.	56-59 68-71	–	Input	D-2
P4.0 P4.1 P4.2 P4.3	I/O	4-bit I/O ports. 1-bit, 4-bit or 8-bit read, write and test are possible. Pull-up resistors can be configured by software.	80 1 2 3	SCK SO SI CLO	Input	D-4 D-2 D-4 D-2
P5.0 P5.1 P5.2 P5.3	I/O	Ports 4 and 5 can be paired to support 8-bit data transfer.	4 5 6 7	ADC0 ADC1 ADC2 ADC3	Input	F-10
P6.0 P6.1 P6.2 P6.3	I/O	4-bit I/O port. 1-bit, 4-bit or 8-bit read, write and test are possible. Pull-up resistors can be configured by software.	8 9 10 11	KS0 KS1 KS2 KS3	Input	D-7
P7.0 P7.1 P7.2 P7.3	O	1-bit or 4-bit output port. Alternatively used for LCD segment output.	28 29 30 31	SEG0 SEG1 SEG2 SEG3	Output	H-28
P8.0 P8.1 P8.2 P8.3	O	1-bit or 4-bit output port. Alternatively used for LCD segment output.	32 33 34 35	SEG4 SEG5 SEG6 SEG7	Output	H-28
P9.0 P9.1 P9.2 P9.3	O	1-bit or 4-bit output port. Alternatively used for LCD segment output.	36 37 38 39	SEG8 SEG9 SEG10 SEG11	Output	H-28
P10.0 P10.1 P10.2 P10.3	O	1-bit or 4-bit output port. Alternatively used for LCD segment output.	40 41 42 43	SEG12 SEG13 SEG14 SEG15	Output	H-28

Table 1-1. S3C7335 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin	Reset Value	Circuit Type
P11.0 P11.1 P11.2 P11.3	O	1-bit or 4-bit output port. Alternatively used for LCD segment output.	44 45 46 47	SEG16 SEG17 SEG18 SEG19	Output	H-28
P12.0 P12.1 P12.2 P12.3	O	1-bit or 4-bit output port. Alternatively used for LCD segment output.	48 49 50 51	SEG20 SEG21 SEG22 SEG23	Output	H-28
P13.0 P13.1 P13.2 P13.3	O	1-bit or 4-bit output port. Alternatively used for LCD segment output.	52 53 54 55	SEG24 SEG25 SEG26 SEG27	Output	H-28
COM0- COM3	O	Common signal output for LCD display	24-27	–	Output	H
BIAS	I	LCD power control	20	–	Input	–
V_{LC0} V_{LC1} V_{LC2}	I	LCD power supply. Voltage dividing resistors are assignable by software	21 22 23	–	Input	–
V_{DD0}	–	Main power supply	12	–	–	–
V_{SS0}	–	Main Ground	13	–	–	–
RESET	I	System reset pin	19	–	Input	B
X_{OUT} X_{IN}	–	Crystal, or ceramic oscillator pin for main system clock. (For external clock input, use X_{IN} and input X_{IN}'s reverse phase to X_{OUT})	14 15	–	–	–
XT_{OUT} XT_{IN}	–	Crystal oscillator pin for subsystem clock. (For external clock input, use XT_{IN} and input XT_{IN}'s reverse phase to XT_{OUT})	18 17	–	–	–
TEST	I	Test signal input (must be connected to V_{SS} for normal operation)	16	–	–	–
CE	I	Input pin for checking device power. Normal operation is high level and PLL/IFC operation is stopped at low level.	67	–	Input	B-5
VCOFM VCOAM	I	External VCOFM/AM signal inputs.	60 61	–	Input	B-4
EO	O	PLL's phase error output	66	–	Output	A-2
FMIF AMIF	I	FM/AM intermediate frequency signal inputs.	64 63	Input	–	B-4
V_{DD1}	–	PLL/IFC power supply	65	–	–	–
V_{SS1}	–	PLL/IFC ground	62	–	–	–

Table 1-1. S3C7335 Pin Descriptions (Concluded)

Pin Name	Pin Type	Description	Number	Share Pin	Reset Value	Circuit Type
BTCO	I/O	Basic timer overflow output signal	72	P0.0	Input	D-2
TCLO0	I/O	Timer/counter 0 clock output signal	73	P0.1	Input	D-2
TCL0	I/O	External clock input for timer/counter 0	74	P0.2	Input	D-4
BUZ	I/O	2,4,8 or 16 kHz frequency output for buzzer sound for 4.19 MHz main system clock or 32.768 kHz subsystem clock	75	P0.3	Input	D-2
INT0 INT1	I	External interrupt. The triggering edges (rising/falling) are selectable. Only INT0 is synchronized with system clock.	76 77	P1.0 P1.1	Input	A-4
INT2	I	Quasi-interrupt with detection of rising edge signal.	78	P1.2		
INT4	I	External interrupt input with detection of rising or falling edges.	79	P1.3		
SCK	I/O	SIO interface clock signal	80	P4.0	Input	D-4
SI	I/O	SIO interface data input signal	1	P4.2		
SO	I/O	SIO interface data output signal	2	P4.1		
CLO	I/O	CPU clock output	3	P4.3		
KS0-KS3	I/O	Quasi-interrupt input with falling edge detection	8-11	P6.0-P6.3	Input	D-7
ADC0-ADC3	I/O	ADC input ports.	4-7	P5.0-P5.3	Input	F-10
SEG0-SEG3	O	LCD segment signal output.	28-31	P7.0-P7.3	Output	H-28
SEG4-SEG27	O	LCD segment signal output.	32-55	P8-P13	Output	H-28

PIN CIRCUIT DIAGRAMS

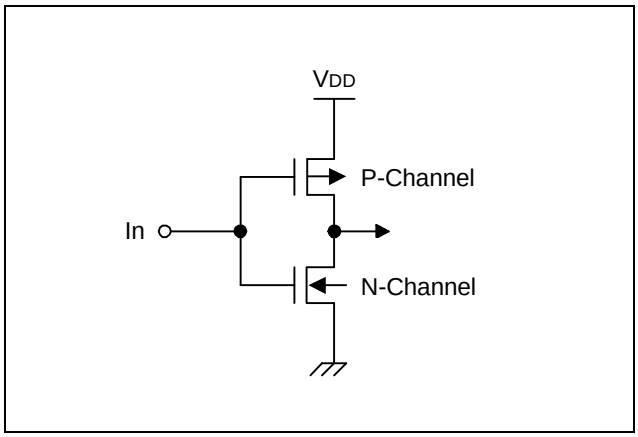


Figure 1-3. Pin Circuit Type A

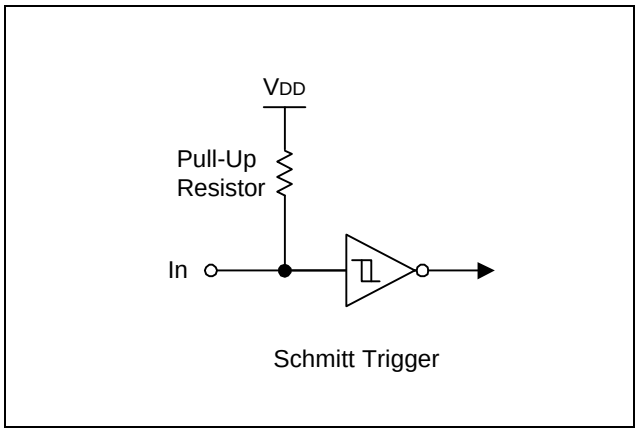


Figure 1-6. Pin Circuit Type B (RESET)

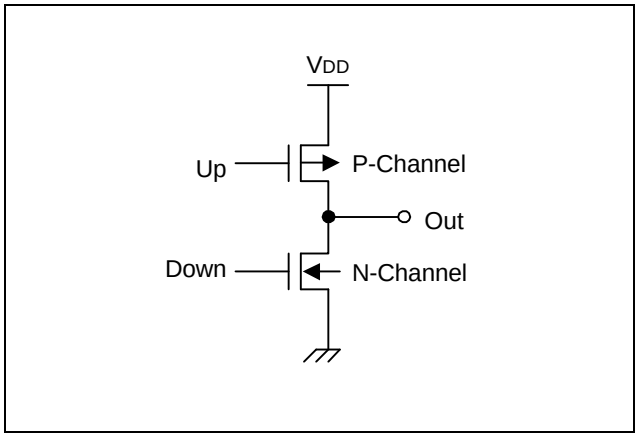


Figure 1-4. Pin Circuit Type A-2(EO)

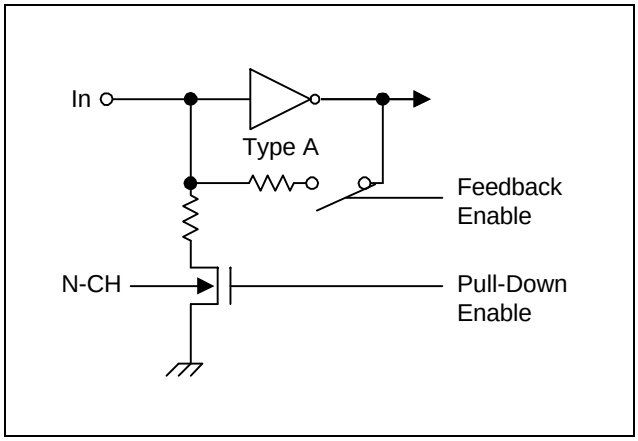


Figure 1-7. Pin Circuit Type B-4

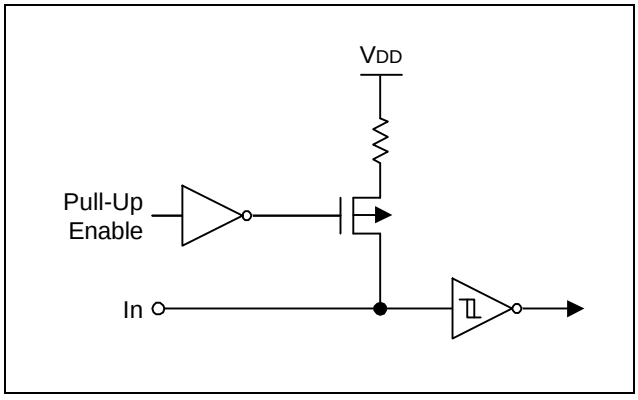


Figure 1-5. Pin Circuit Type A-4 (P1)

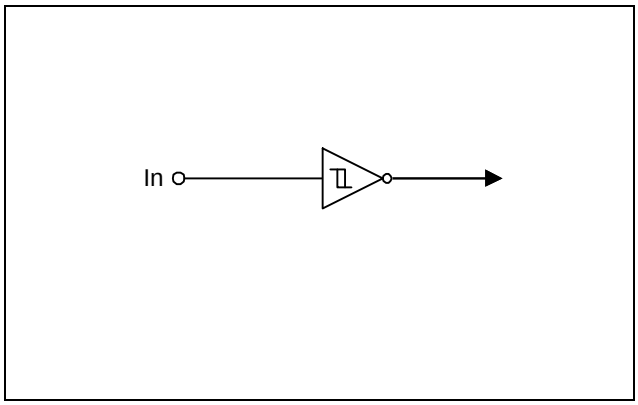


Figure 1-8. Pin Circuit Type B-5(CE)

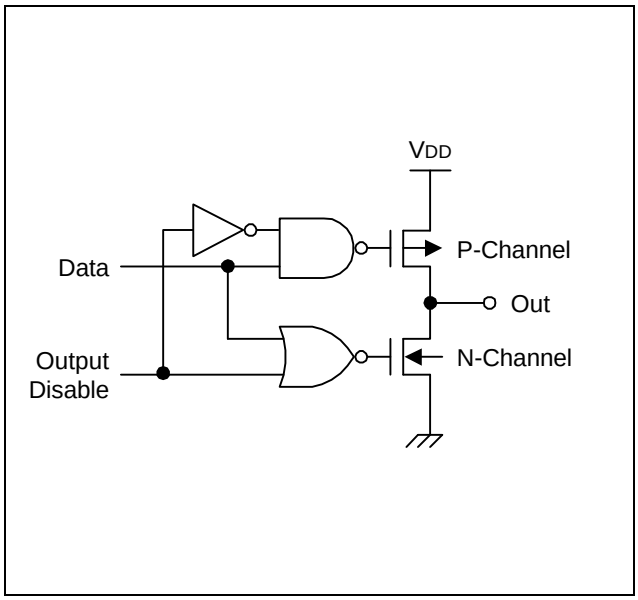


Figure 1-9. Pin Circuit Type C

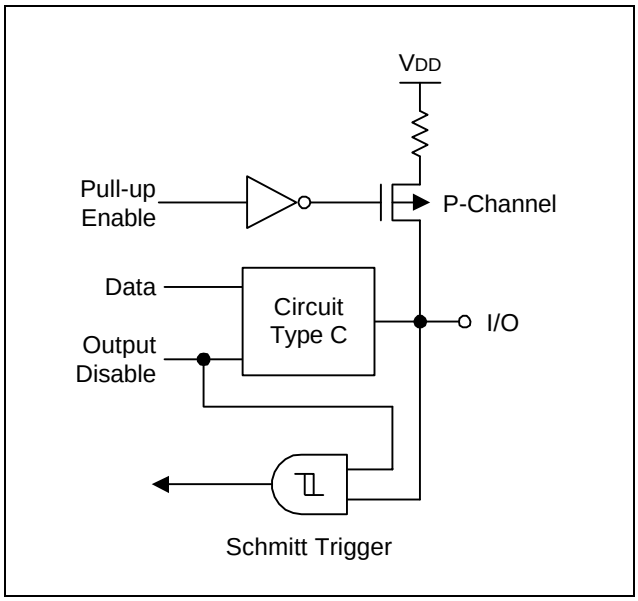


Figure 1-11. Pin Circuit Type D-4

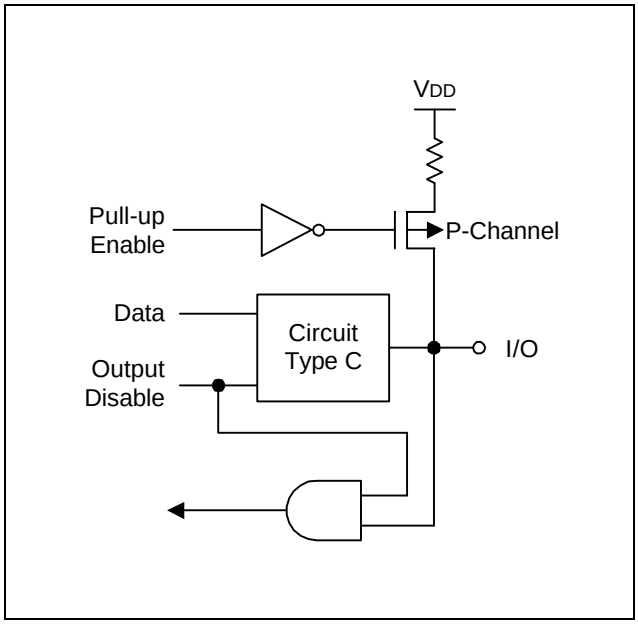


Figure 1-10. Pin Circuit Type D-2

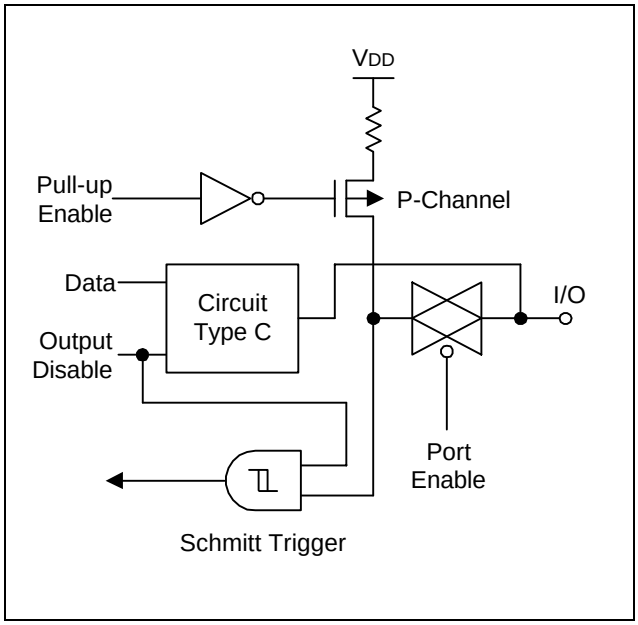


Figure 1-12. Pin Circuit Type D-7 (P6)

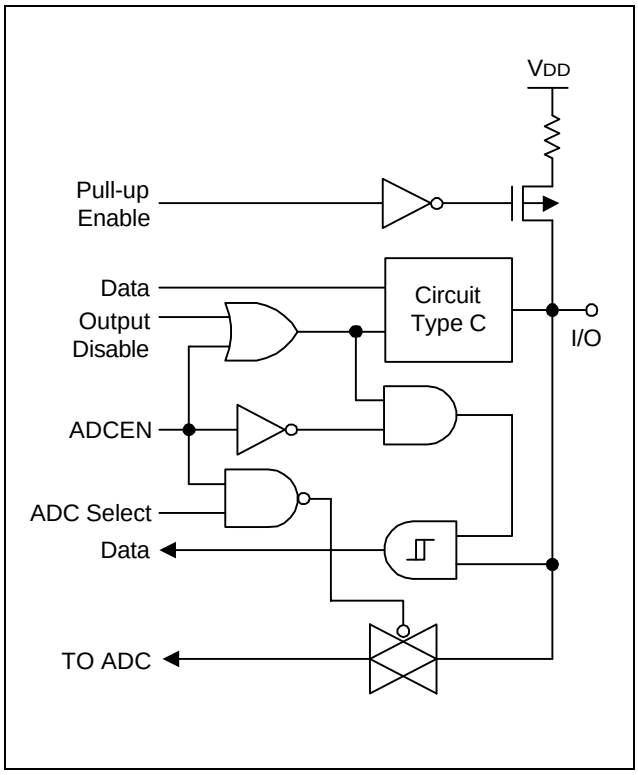


Figure1-13. Pin Circuit Type F-10 (P5)

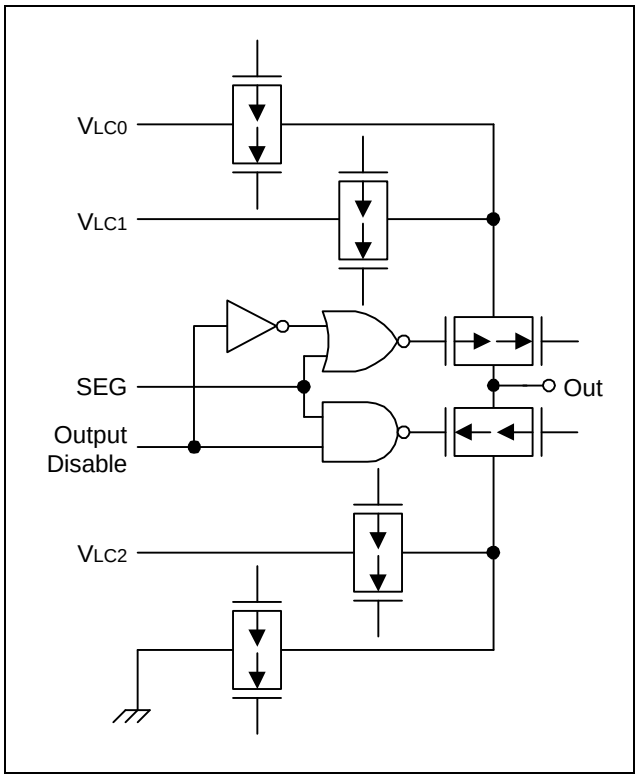


Figure 1-15. Pin Circuit Type H-4

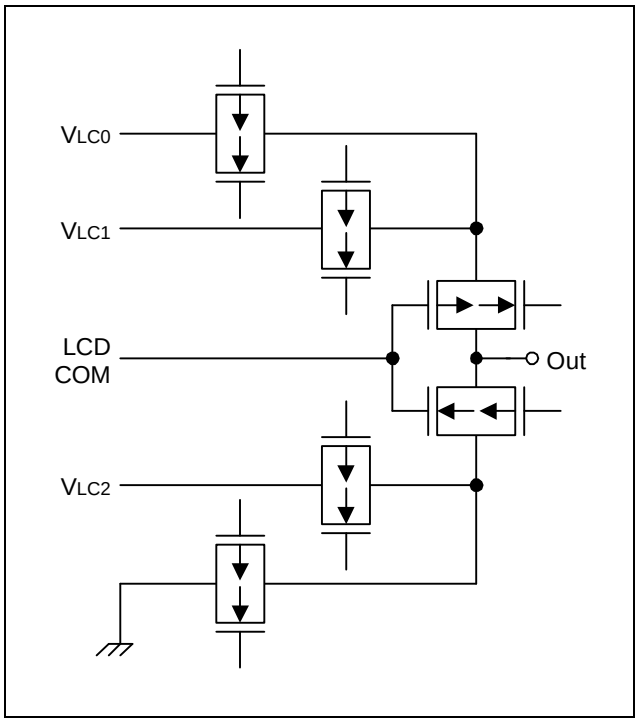


Figure 1-14. Pin Circuit Type H (COM0-COM3)

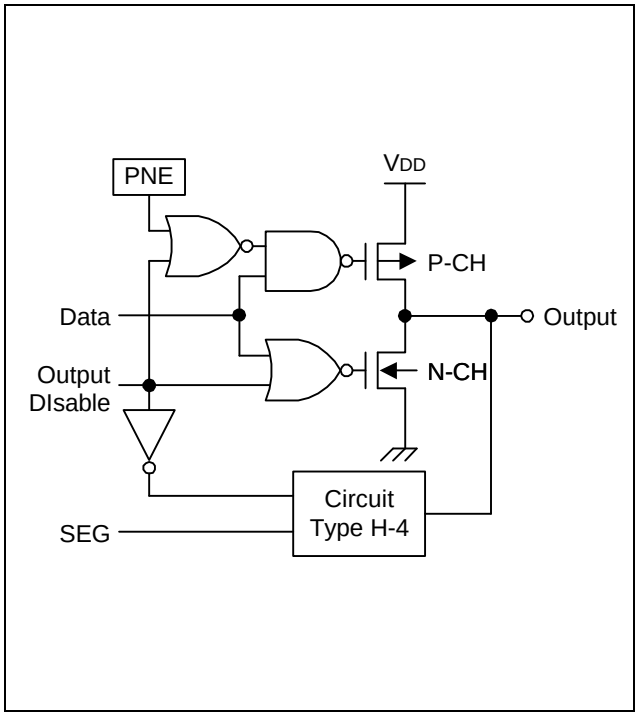


Figure 1-16. Pin Circuit Type H-28 (P7-P13)

17 ELECTRICAL DATA

OVERVIEW

In this section, information on S3C7335 electrical characteristics is presented as tables and graphics. The information is arranged in the following order:

Standard Electrical Characteristics

— Absolute maximum ratings
— D.C. electrical characteristics
— System clock oscillator characteristics
— I/O capacitance
— A.C. electrical characteristics
— Operating voltage range

Miscellaneous Timing Waveforms

— A.C timing measurement point
— Clock timing measurement at X_{IN}
— Clock timing measurement at XT_{IN}
— Input timing for RESET
— Input timing for external interrupts and Quasi-Interrupts

Stop Mode Characteristics and Timing Waveforms

— RAM data retention supply voltage in stop mode
— Stop mode release timing when initiated by RESET
— Stop mode release timing when initiated by an interrupt request

Table 17-1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply voltage	V_{DD}	–	- 0.3 to + 6.5	V
Input voltage	V_{IN}	Applies to all I/O ports	- 0.3 to V_{DD} + 0.3	
Output voltage	V_O	–	- 0.3 to V_{DD} + 0.3	
Output current high	I_{OH}	One I/O port active	- 15	mA
		All I/O ports active	-30	
Output current low	I_{OL}	One I/O port active	+ 30 (peak value)	
			+ 15 (note)	
		Total value for output ports	+ 100 (peak value)	
			+ 60 *	
Operating temperature	T_A		- 40 to + 85	°C
Storage temperature	T_{STG}		- 65 to + 150	

NOTE: The values for output current low (I_{OL}) are calculated as Peak Value $\times\sqrt{\text{Duty}}$.

Table 17-2. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input high voltage	V_{IH1}	All input pins except those specified below	0.7 V_{DD}	–	V_{DD}	V
	V_{IH2}	P0.2, P1, P4.0, P4.2, P5, P6, CE and RESET	0.8 V_{DD}		V_{DD}	
	V_{IH3}	X_{IN}, X_{OUT}, XT_{IN}, and XT_{OUT}	V_{DD}–0.1		V_{DD}	
Input low voltage	V_{IL1}	All input pins except those specified below	–	–	0.3 V_{DD}	
	V_{IL2}	P0.2, P1, P4.0, P4.2, P5, P6, CE and RESET			0.2 V_{DD}	
	V_{IL3}	X_{IN}, X_{OUT}, XT_{IN}, and XT_{OUT}			0.1	
Output high voltage	V_{OH1}	V_{DD} = 4.5 V to 5.5 V, EO; I_{OH} = – 1 mA	V_{DD}–2.0	–	V_{DD}	
	V_{OH2}	V_{DD} = 4.5 V to 5.5 V; Other output ports; I_{OH} = – 1 mA	V_{DD}–1.0		V_{DD}	
Output low voltage	V_{OL1}	V_{DD} = 4.5 V to 5.5 V, EO; I_{OL} = 1 mA,	–	–	2.0	
	V_{OL2}	V_{DD} = 4.5 V to 5.5 V Other output ports; I_{OL} = 10 mA	–	–	2	
Input high leakage current(note)	I_{LIH}	V_{IN} = V_{DD} All input pins	–	–	3	µA
Input low leakage current(note)	I_{LIL}	V_{IN} = 0 V All input pins	–	–	- 3	
Output high leakage current(note)	I_{LOH}	V_{OUT} = V_{DD} All output pins	–	–	3	

NOTE: Except for X_{IN} , X_{OUT}, XT_{IN} and XT_{OUT}.

Table 17-2. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
V_{LC0} output voltage	V_{LC0}	T_A = 25 °C	0.6 V_{DD}– 0.2	0.6 V_{DD}	0.6 V_{DD} + 0.2	V
V_{LC1} output voltage	V_{LC1}	T_A = 25 °C	0.4 V_{DD}– 0.2	0.4 V_{DD}	0.4 V_{DD} + 0.2	
V_{LC2} output voltage	V_{LC2}	T_A = 25 °C	0.2 V_{DD}– 0.2	0.2 V_{DD}	0.2 V_{DD} + 0.2	
COM output voltage deviation	V_{DC}	V_{DD} = 5V, (V_{LC0} - $COM_{i\ I = 0 - 3}$) IO = ± 15 µA (I = 0 - 3)	–	± 45	± 120	mV
SEG output voltage deviation	V_{DS}	V_{DD} = 5V, (V_{LC0} - $COM_{i\ I = 0 - 3}$) IO = ± 15 µA (I = 0 - 3)		± 45	± 120	
LCD output voltage deviation	R_{LCD}	T_A = 25 °C	70	100	150	KΩ
Oscillator feed back resistors	R_{OSC1}	V_{DD} = 5.0 V, T_A = 25 °C X_{IN} = V_{DD}, X_{OUT} = 0 V	300	600	1500	
	R_{OSC2}	V_{DD} = 5.0 V, T_A = 25 °C XT_{IN} = V_{DD}, XT_{OUT} = 0 V	1500	3000	4500	
Pull-down resistor	R_D	V_{DD} = 5.0 V, V_{IN} = V_{DD}; VCOFM, VCOAM, AMIF, and FMIF	15	30	45	
Pll-up Resistor	R_{L1}	V_{IN} = 0 V; V_{DD} = 5 V Ports 1, 2, 3, 4, 5, and 6	25	47	100	
		V_{DD} = 3 V	50	95	200	
	R_{L2}	V_{IN} = 0 V; V_{DD} = 5 V RESET	100	220	400	
		V_{DD} = 3 V	200	450	800	

Table 17-2. D.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

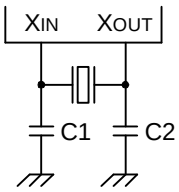
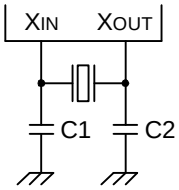
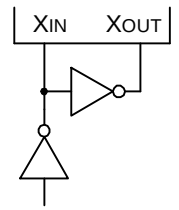
Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current(1)	I_{DD1} (2)	Main operating, PLL operating: PCON = 0011B, SCMOD = 0000B CE = V_{DD}; Crystal oscillator C1 = C2 = 22 pF V_{DD} = 5 V ± 10%	4.5 MHz	–	5.5	27	mA
	I_{DD2} (2)	CE Low, PCON = 0011B, SCMOD = 0000B CE = 0 V Crystal oscillator C1 = C2 = 22 pF V_{DD} = 5 V ± 10%	6.0 MHz	–	3.5	8	
			4.5 MHz		2.5	5.5	
		V_{DD} = 3 V ± 10%	6.0 MHz		1.6	4	
			4.5 MHz		1.2	3	
	I_{DD3} (2)	Main idle mode, PCON = 0111B, SCMOD =0000B Crystal oscillator C1 = C2 = 22 pF V_{DD} = 5 V ± 10%	6.0 MHz	–	1.0	2.5	
			4.5 MHz		0.9	2.0	
		V_{DD} = 3 V ± 10%	6.0 MHz		0.5	1.0	
			4.5MHz		0.4	0.8	
	I_{DD4}(2)	Sub operating mode: PCON = 0011B, SCMOD = 1001B CE = 0 V; V_{DD} = 3 V ± 10% 32 kHz crystal oscillator		–	15	30	uA
	I_{DD5} (2)	Sub idle mode: PCON = 0111B, SCMOD = 1001B CE = 0 V; V_{DD} = 3 V ± 10% 32 kHz crystal oscillator		–	6	15	
	IDD6(2)	Stop mode: CPU = fxt/4, SCMOD = 1101B CE = 0 V; V_{DD} = 5 V ± 10%		–	0.5	3	
	I_{DD7}(2)	Stop mode: CPU = fx/4, SCMOD = 0100B V_{DD} = 5 V ± 10%		–			

NOTES:

1. Supply current does not include current drawn through internal pull-up resistors and LCD voltage dividing resistors.
2. Data includes the power consumption for sub-system clock oscillation.

Table 17-3. Main System Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

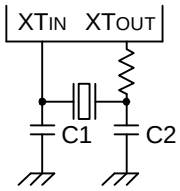
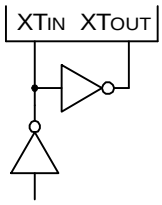
Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6	MHz
		Stabilization time (2)	Stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6	MHz
		Stabilization time (2)	V_{DD} = 4.5 V to 5.5 V	–	–	10	ms
			V_{DD} = 1.8 V to 4.5 V	–	–	30	
External Clock		X_{IN} input frequency (1)	–	0.4	–	6	MHz
		X_{IN} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	–	ns

NOTES:

1. Oscillation frequency and X_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillator stabilization after a power-on occurs, or when stop mode is terminated.

Table 17-4. Subsystem Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Crystal Oscillator		Oscillation frequency (1)	–	32	32.768	35	kHz
		Stabilization time (2)	V_{DD} = 2.7 V to 5.5 V	–	1.0	2	s
			V_{DD} = 1.8 V to 4.5 V	–	–	10	
External Clock		XT_{IN} input frequency (1)	–	32	–	100	kHz
		XT_{IN} input high and low level width (t_{XTL}, t_{XTH})	–	5	–	15	µs

NOTES:

1. Oscillation frequency and XT_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillator stabilization after a power-on occurs.

Table 17-5. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input capacitance	C_{IN}	f_{CLK} = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output capacitance	C_{OUT}		–	–	15	pF
I/O capacitance	C_{IO}		–	–	15	pF

Table 17-6. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction cycle time (1)	t_{CY}	V_{DD} = 2.7 V to 5.5 V	0.67	–	64	µs
		V_{DD} = 1.8 V to 5.5 V	1.3		64	
Interrupt input high, low width	t_{INTH}, t_{INTL}	INT0	(2)	–	–	µs
		INT1, INT2, INT4, KS0–KS2	10			
RESET and CE Input Low Width	t_{RSL}	Input	10	1	–	µs

NOTES:
1. Unless otherwise specified, Instruction Cycle Time condition values assume a main system clock/4 (fx/4) source.
2. Minimum value for INT0 is based on a clock of $2t_{CY}$ or 128/fxx as assigned by the IMOD0 register setting.

Table 17-6. A.C. Electrical Characteristics (Continued)

(T_A = – 10 °C to + 70 °C, V_{DD} = 3.5 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
A/D converting Resolution	–	–	–	8	–	bits
Absolute accuracy	–	–	–	–	± 2	LSB
AD conversion time	t_{CON}	–	17	34/fxx (note)	–	µs
Analog input voltage	V_{IAN}	–	V_{SS}	–	V_{DD}	V
Analog input impedance	R_{AN}	V_{DD} = 5 V	2	1000	–	MΩ

NOTE: fxx stands for the system clock (fx or fxt).

Table 17-6. A.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.5 V to 3.5 V or V_{DD} = 4.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VCOFM, VCOAM, FMIF and AMIF Input Voltage (Peak to Peak)	V_{IN}	Sine wave input	0.3	–	V_{DD}	V
Frequency	fV_{COAM}	VCOAM mode, sine wave input; V_{IN} = $0.3V_{P-P}$	0.5	–	30	MHz
	fV_{COFM}	VCOFM mode, sine wave input; V_{IN} = $0.3V_{P-P}$	30		150	
	f_{AMIF}	AMIF mode, sine wave input; V_{IN} = $0.3V_{P-P}$	0.1		1.0	
	f_{FMIF}	FMIF mode, sine wave input; V_{IN} = $0.3V_{P-P}$	5		15	

Table 17-6. A.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction cycle time (1)	t_{CY}	V_{DD} = 2.7 V to 5.5 V	0.67	–	64	µs
		V_{DD} = 1.8 V to 5.5 V	1.3	–	64	
		With subsystem clock (fxt)	114	122	125	
TCL0 input frequency	f_{TI}	V_{DD} = 2.7 V to 5.5 V	0	–	1.5	MHz
		V_{DD} = 1.8 V to 5.5 V			1	
TCL0 input high, low width	t_{TIH}, t_{TIL}	V_{DD} = 2.7. V to 5.5 V	0.48	–	–	µs
		V_{DD} = 1.8. V to 5.5 V	1.8			
SCK cycle time	t_{KCY}	V_{DD} = 2.7 V to 5.5 V External SCK source	800	–	–	ns
		Internal SCK source	650			
		V_{DD} = 1.8 V to 5.5 V External SCK source	3200			
		Internal SCK source	3800			
SCK high, low width	t_{KH}, t_{KL}	V_{DD} = 2.7 V to 5.5 V External SCK source	400	–	–	
		Internal SCK source	t_{KCY}/2- 50			
		V_{DD} = 1.8 V to 5.5 V External SCK source	1600			
		Internal SCK source	t_{KCY}/2-150			
SI setup time to SCK high	t_{SIK}	External SCK source	100	–	–	
		Internal SCK source	150			
SI hold time to SCK high	t_{KSI}	External SCK source	400	–	–	
		Internal SCK source	400			
Output delay for SCK to SO	t_{KSO}	V_{DD} = 2.7 V to 5.5 V External SCK source	–	–	300	
		Internal SCK source			250	
		V_{DD} = 1.8 V to 5.5 V External SCK source			1000	
		Internal SCK source			1000	

NOTE: Unless otherwise specified, Instruction Cycle Time condition values assume a main system clock/4 (fx/4) source.

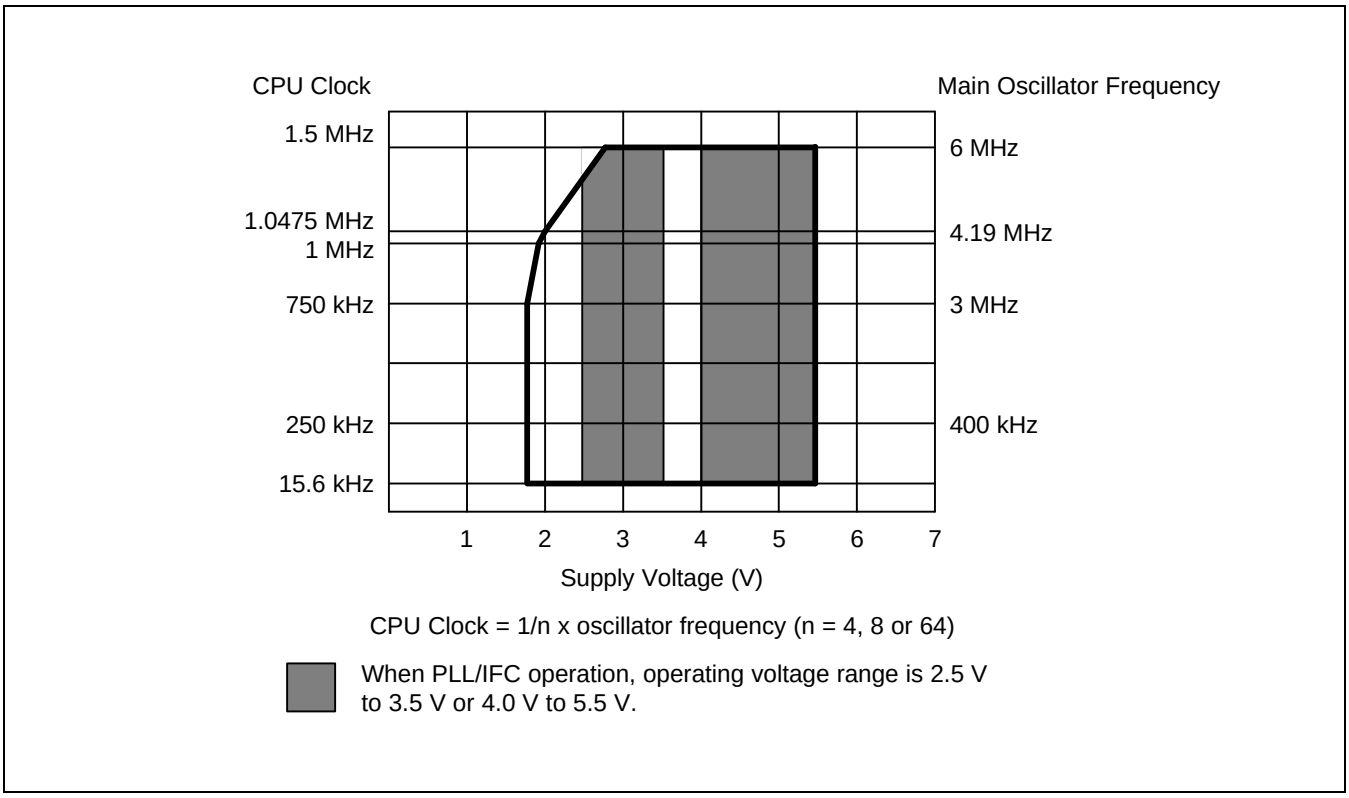


Figure 17-1. Standard Operating Voltage Range

Table 17-7. RAM Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	Normal operation	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V	–	0.1	1	µA

TIMING WAVEFORMS

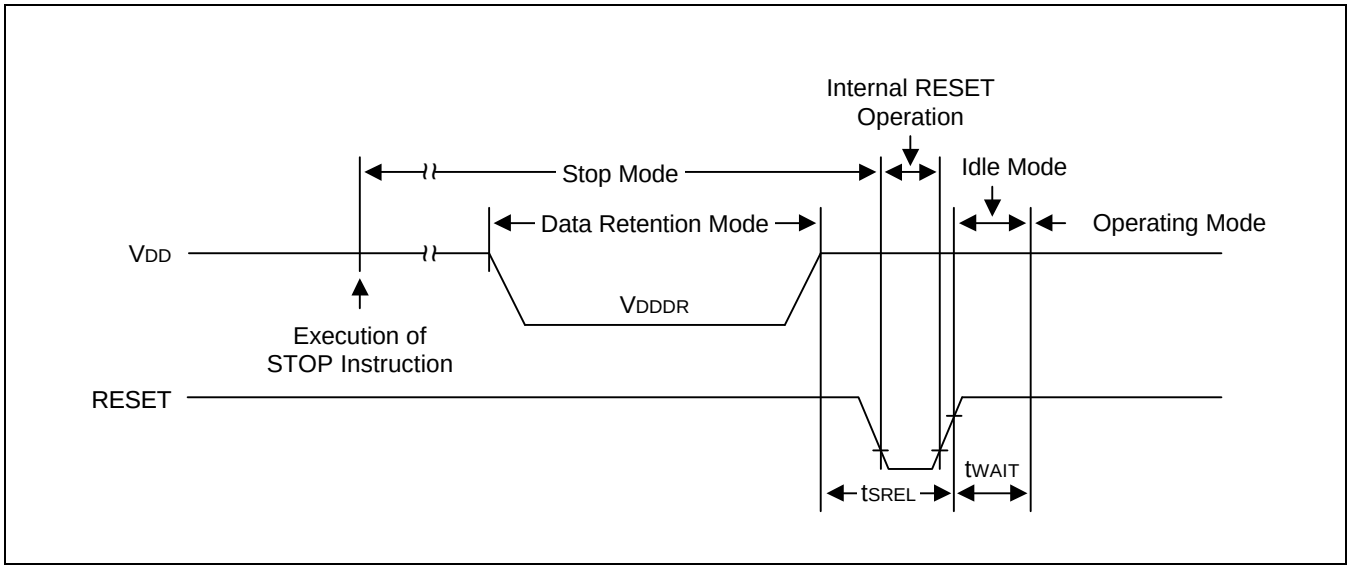


Figure 17-2. Stop Mode Release Timing When Initiated by RESET

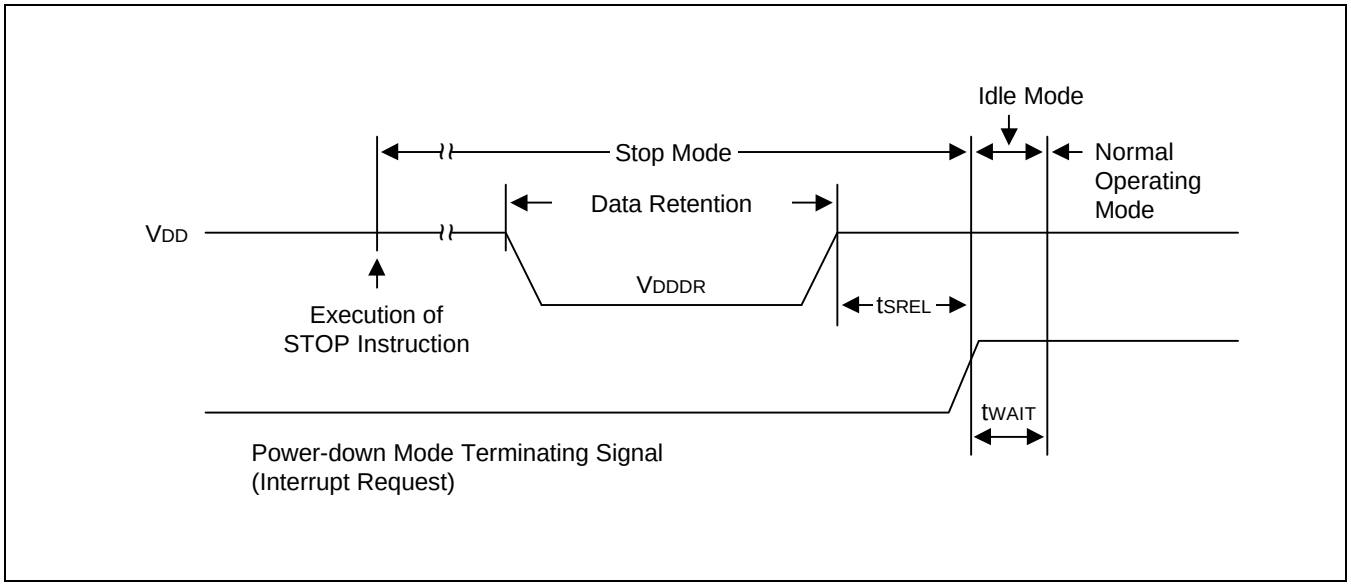


Figure 17-3. Stop Mode Release Timing When Initiated by an Interrupt Request

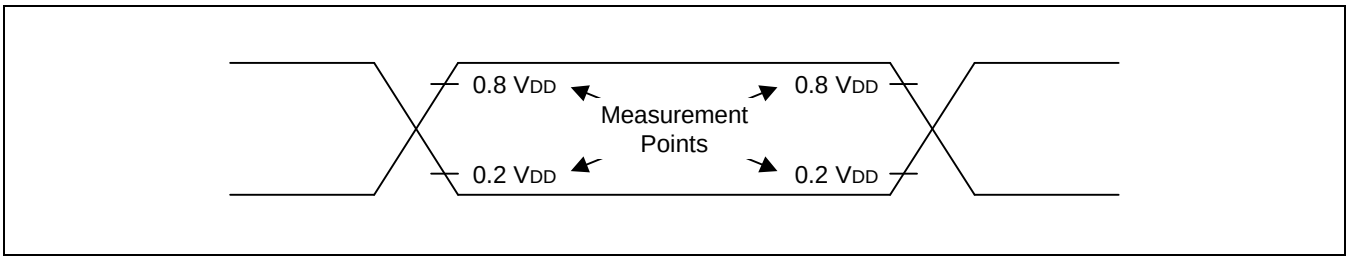


Figure 17-4. A.C. Timing Measurement Points (Except for X_{IN} and XT_{IN})

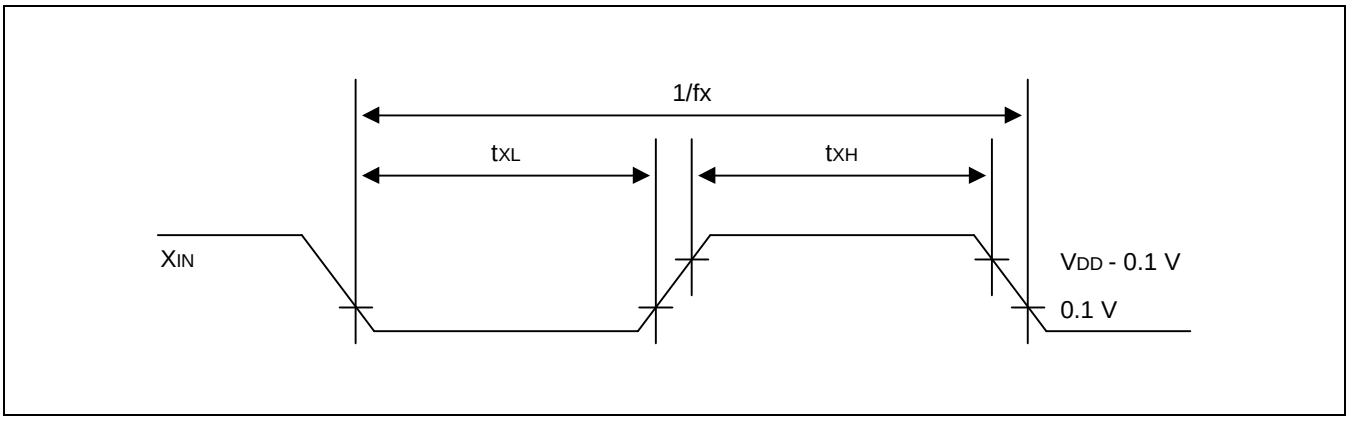


Figure 17-5. Clock Timing Measurement at X_{IN}

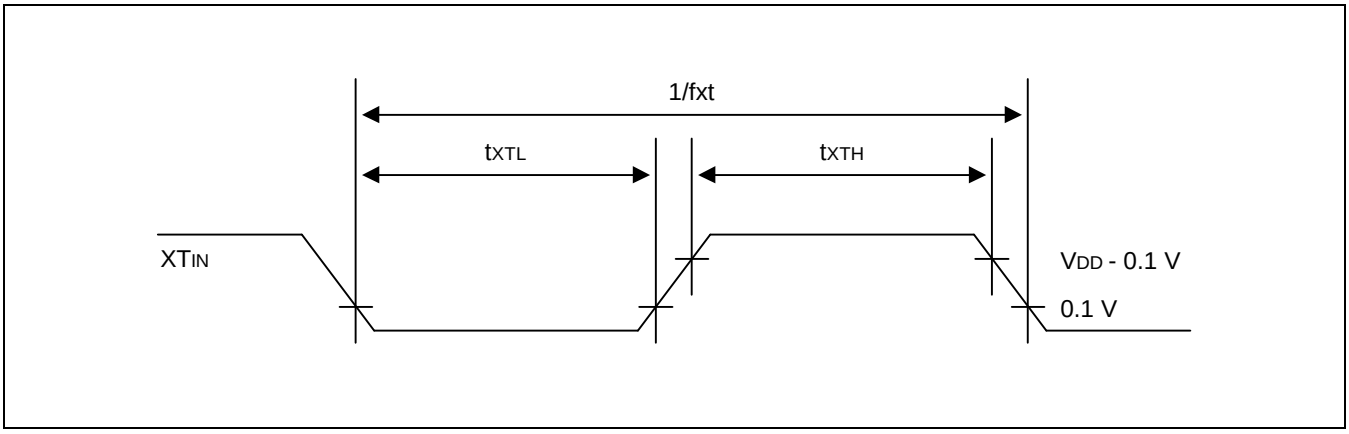


Figure 17-6. Clock Timing Measurement at XT_{IN}

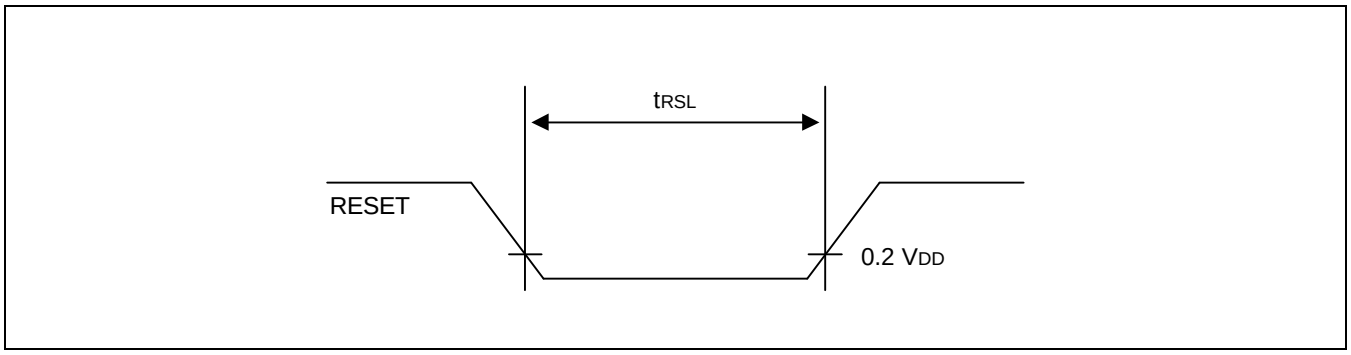


Figure 17-7. Input Timing for RESET Signal

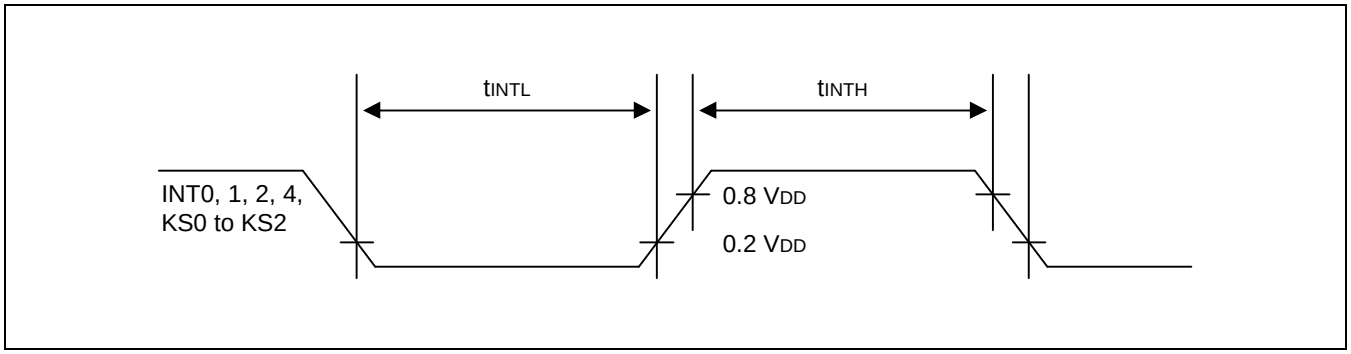


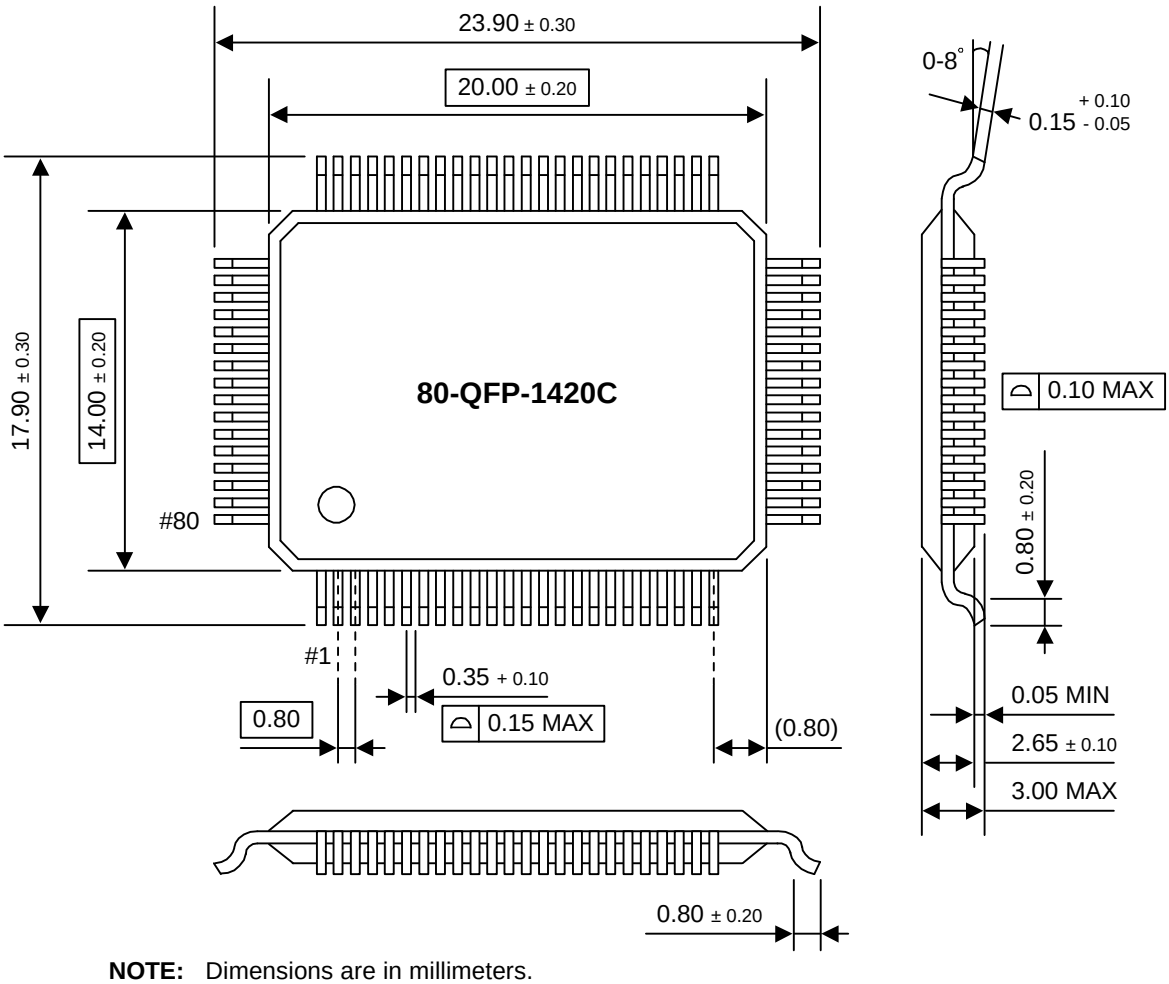
Figure 17-8. Input Timing for External Interrupts and Quasi-Interrupts

18 MECHANICAL DATA

OVERVIEW

This section contains the following information about the device package:

— Package dimensions in millimeters
— Pad diagram
— Pad/pin coordinate data table



NOTE: Dimensions are in millimeters.

Figure 18-1. 80-QFP-1420C Package Dimensions

19 S3P7335 OTP

OVERVIEW

The S3P7335 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C7335 microcontroller. It has an on-chip EPROM instead of masked ROM. The EPROM is accessed by a serial data format.

The S3P7335 is fully compatible with the S3C7335, both in function and in pin configuration. Because of its simple programming requirements, the S3P7335 is ideal for use as an evaluation chip for the S3C7335.

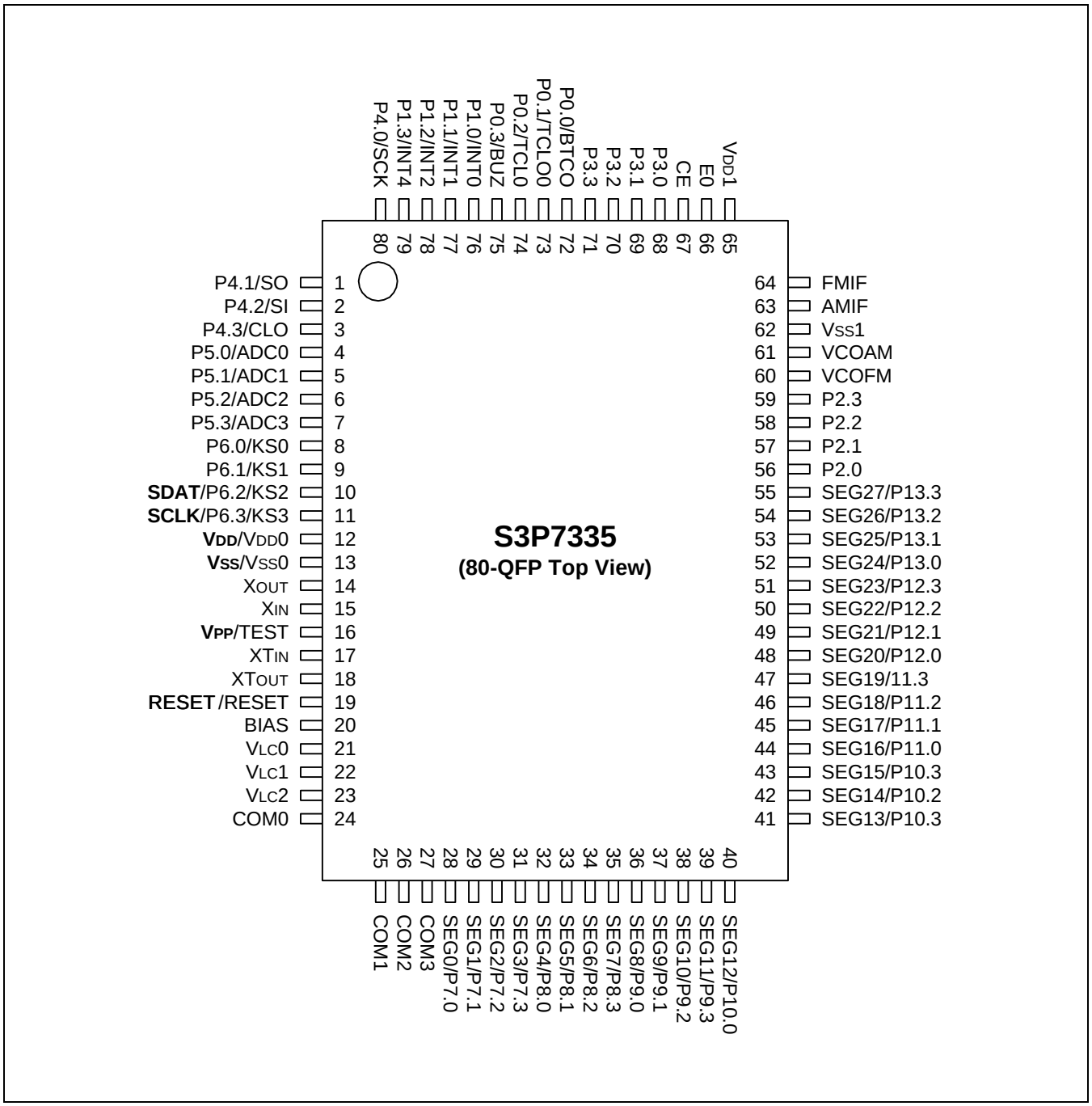


Figure 19-1. S3P7335 Pin Assignments (80-QFP)

Table 19-1. Pin Descriptions Used to Read/Write the EPROM

Main Chip	During Programming			
Pin Name	**Pin Name**	**Pin No.**	**I/O**	**Function**
P6.2	SDAT	10	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input or push-pull output port.
P6.3	SCLK	11	I/O	Serial clock pin. Input only pin.
TEST	**V_{PP} (TEST)**	16	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode.
RESET	RESET	19	I	Chip initialization
V_{DD} / V_{SS}	V_{DD} / V_{SS}	12/13	I	Logic power supply pin. V_{DD} should be tied to +5 V during programming.

Table 19-2. Comparison of S3P7335 and S3C7335 Features

Characteristic	S3P7335	S3C7335
Program Memory	16K bytes EPROM	16K bytes mask ROM
Operating Voltage (V_{DD})	1.8 V to 5.5 V 2.5 V to 3.5 V or 4.0 V to 5.5 V at PLL/IFC operation	1.8 V to 5.5 V 2.5 V to 3.5 V or 4.0 V to 5.5 V at PLL/IFC operation
OTP Programming Mode	V_{DD} = 5 V, V_{PP} (TEST) = 12.5 V	–
Pin Configuration	80 QFP	80 QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the Vpp (TEST) pin of the S3P7335, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 17-3 below.

Table 19-3. Operating Mode Selection Criteria

V_{DD}	Vpp(TEST)	REG/MEM	Address(A15-A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means low level; "1" means high level.

Table 19-4. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input high voltage	V_{IH1}	All input pins except those specified below	0.7 V_{DD}	–	V_{DD}	V
	V_{IH2}	P0.2, P1, P4.0, P4.2, P5, P6, CE and RESET	0.8 V_{DD}		V_{DD}	
	V_{IH3}	X_{IN}, X_{OUT}, XT_{IN}, and XT_{OUT}	V_{DD}–0.1		V_{DD}	
Input low voltage	V_{IL1}	All input pins except those specified below	–	–	0.3 V_{DD}	
	V_{IL2}	P0.2, P1, P4.0, P4.2, P5, P6, CE and RESET			0.2 V_{DD}	
	V_{IL3}	X_{IN}, X_{OUT}, XT_{IN}, and XT_{OUT}			0.1	
Output high voltage	V_{OH1}	V_{DD} = 4.5 V to 5.5 V, EO; I_{OH} = – 1 mA	V_{DD}–2.0	–	V_{DD}	
	V_{OH2}	V_{DD} = 4.5 V to 5.5 V; Other output ports; I_{OH} = – 1 mA	V_{DD}–1.0		V_{DD}	
Output low voltage	V_{OL1}	V_{DD} = 4.5 V to 5.5 V, EO; I_{OL} = 1 mA,	–	–	2.0	
	V_{OL2}	V_{DD} = 4.5 V to 5.5 V Other output ports; I_{OL} = 10 mA	–	–	2	
Input high leakage current(note)	I_{LIH}	V_{IN} = V_{DD} All input pins	–	–	3	µA
Input low leakage current(note)	I_{LIL}	V_{IN} = 0 V All input pins	–	–	– 3	
Output high leakage current(note)	I_{LOH}	V_{OUT} = V_{DD} All output pins	–	–	3	
Output low leakage current (note)	I_{LOL}	V_{OUT} = 0 V All output pins	–	–	– 3	

NOTE: Except for X_{IN}, X_{OUT}, XT_{IN}, and XT_{OUT}

Table 19-4. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
V_{LC0} output voltage	V_{LC0}	T_A = 25 °C	0.6 V_{DD}– 0.2	0.6 V_{DD}	0.6 V_{DD} + 0.2	V
V_{LC1} output voltage	V_{LC1}	T_A = 25 °C	0.4 V_{DD}– 0.2	0.4 V_{DD}	0.4 V_{DD} + 0.2	
V_{LC2} output voltage	V_{LC2}	T_A = 25 °C	0.2 V_{DD}– 0.2	0.2 V_{DD}	0.2 V_{DD} + 0.2	
COM output voltage deviation	V_{DC}	V_{DD} = 5V, (V_{LC0} - $COM_{i\ I = 0 - 3}$) IO = ± 15 µA (I = 0 - 3)	–	± 45	± 120	mV
SEG output voltage deviation	V_{DS}	V_{DD} = 5V, (V_{LC0} - $COM_{i\ I = 0 - 3}$) IO = ± 15 µA (I = 0 - 3)		± 45	± 120	
LCD output voltage deviation	R_{LCD}	T_A = 25 °C	70	100	150	kΩ
Oscillator feed back resistors	R_{OSC1}	V_{DD} = 5.0 V, T_A = 25 °C X_{IN} = V_{DD}, X_{OUT} = 0 V	300	600	1500	
	R_{OSC2}	V_{DD} = 5.0 V, T_A = 25 °C XT_{IN} = V_{DD}, XT_{OUT} = 0 V	1500	3000	4500	
Pull-down resistor	R_D	V_{DD} = 5.0 V, V_{IN} = V_{DD}; VCOFM, VCOAM, AMIF, and FMIF	15	30	45	
Pull-up resistor	R_{L1}	V_{IN} = 0 V; V_{DD} = 5 V Ports 1, 2, 3, 4, 5, and 6	25	47	100	
		V_{DD} = 3 V	50	95	200	
	R_{L2}	V_{IN} = 0 V; V_{DD} = 5 V RESET	100	220	400	
		V_{DD} = 3 V	200	450	800	

Table 19-4. D.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

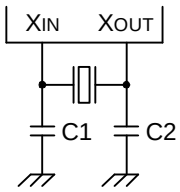
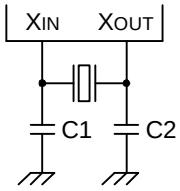
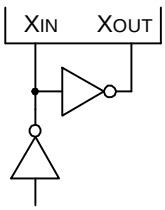
Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current(1)	I_{DD1} (2)	Main operating: PCON = 0011B, SCMOD = 0000B CE = V_{DD}; Crystal oscillator C1 = C2 = 22 pF V_{DD} = 5 V ± 10%	4.5 MHz	–	5.5	27	mA
	I_{DD2} (2)	CE Low mate: PCON = 0011B, SCMOD = 0000B CE = 0 V Crystal oscillator C1 = C2 = 22 pF V_{DD} = 5 V ± 10%	6.0 MHz	–	3.5	8	
			4.5 MHz		2.5	5.5	
		V_{DD} = 3 V ± 10%	6.0 MHz		1.6	4	
			4.5 MHz		1.2	3	
	I_{DD3} (2)	Main idle mode: PCON = 0111B, SCMOD =0000B Crystal oscillator C1 = C2 = 22 pF V_{DD} = 5 V ± 10%	6.0 MHz	–	1.0	2.5	
			4.5 MHz		0.9	2.0	
		V_{DD} = 3 V ± 10%	6.0 MHz		0.5	1.0	
			4.5MHz		0.4	0.8	
	I_{DD4}(2)	Sub operating mode: PCON = 0011B, SCMOD = 1001B CE = 0 V; V_{DD} = 3 V ± 10% 32 kHz crystal oscillator		–	15	30	uA
	I_{DD5} (2)	Sub idle mode: PCON = 0111B, SCMOD = 1001B CE = 0 V; V_{DD} = 3 V ± 10% 32 kHz crystal oscillator		–	6	15	
	IDD6(2)	Stop mode: CPU = fxt/4, SCMOD = 1101B CE = 0 V; V_{DD} = 5 V ± 10%		–	0.5	3	
	I_{DD7}(2)	Stop mode: CPU = fx/4, SCMOD = 0100B V_{DD} = 5 V ± 10%		–			

NOTES:

1. Supply current does not include current drawn through internal pull-up resistors and LCD voltage dividing resistors.
2. Data includes the power consumption for sub-system clock oscillation.

Table 19-5. Main System Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

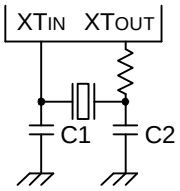
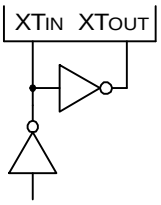
Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6	MHz
		Stabilization time (2)	Stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6	MHz
		Stabilization time (2)	V_{DD} = 4.5 V to 5.5 V	–	–	10	ms
			V_{DD} = 1.8 V to 4.5 V	–	–	30	
External Clock		X_{IN} input frequency (1)	–	0.4	–	6	MHz
		X_{IN} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	–	ns

NOTES:

1. Oscillation frequency and X_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillator stabilization after a power-on occurs, or when stop mode is terminated.

Table 19-6. Subsystem Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Crystal Oscillator		Oscillation frequency (1)	–	32	32.768	35	kHz
		Stabilization time (2)	V_{DD} = 2.7 V to 5.5 V	–	1.0	2	s
			V_{DD} = 1.8 V to 4.5 V	–	–	10	
External Clock		XT_{IN} input frequency (1)	–	32	–	100	kHz
		XT_{IN} input high and low level width (t_{XTL}, t_{XTH})	–	5	–	15	µs

NOTES:

1. Oscillation frequency and XT_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillator stabilization after a power-on occurs.

Table 19-7. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input capacitance	C_{IN}	f_{CLK} = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output capacitance	C_{OUT}		–	–	15	pF
I/O capacitance	C_{IO}		–	–	15	pF

Table 19-8. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction cycle time (1)	t_{CY}	V_{DD} = 2.7 V to 5.5 V	0.67	–	64	µs
		V_{DD} = 1.8 V to 5.5 V	1.3		64	
Interrupt input high, low width	t_{INTH}, t_{INTL}	INT0	(2)	–	–	µs
		INT1, INT2, INT4, KS0–KS2	10			
RESET and CE Input Low Width	t_{RSL}	Input	10	1	–	µs

NOTES:
1. Unless otherwise specified, Instruction Cycle Time condition values assume a main system clock/4 (fx/4) source.
2. Minimum value for INT0 is based on a clock of $2t_{CY}$ or 128/fxx as assigned by the IMOD0 register setting.

Table 19-8. A.C. Electrical Characteristics (continued)

(T_A = – 10 °C to + 70 °C, V_{DD} = 3.5 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
A/D converting Resolution	–	–	–	8	–	bits
Absolute accuracy	–	–	–	–	± 2	LSB
AD conversion time	t_{CON}	–	17	34/fxx (note)	–	µs
Analog input voltage	V_{IAN}	–	V_{SS}	–	V_{DD}	V
Analog input impedance	R_{AN}	V_{DD} = 5 V	2	1000	–	MΩ

NOTE: fxx stands for the system clock (fx or fxt).

Table 19-8. A.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.5 V to 3.5 V or V_{DD} = 4.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VCOFM, VCOAM, FMIF and AMIF Input Voltage (Peak to Peak)	V_{IN}	Sine wave input	0.3	–	V_{DD}	V
Frequency	fV_{COAM}	VCOAM mode, sine wave input; V_{IN} = $0.3V_{P-P}$	0.5	–	30	MHz
	fV_{COFM}	VCOFM mode, sine wave input; V_{IN} = $0.3V_{P-P}$	30		150	
	f_{AMIF}	AMIF mode, sine wave input; V_{IN} = $0.3V_{P-P}$	0.1		1.0	
	f_{FMIF}	FMIF mode, sine wave input; V_{IN} = $0.3V_{P-P}$	5		15	

Table 19-8. A.C. Electrical Characteristics (continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction cycle time (1)	t_{CY}	V_{DD} = 2.7 V to 5.5 V	0.67	–	64	µs
		V_{DD} = 1.8 V to 5.5 V	1.3	–	64	
		With subsystem clock (fxt)	114	122	125	
TCL0 input frequency	f_{TI}	V_{DD} = 2.7 V to 5.5 V	0	–	1.5	MHz
		V_{DD} = 1.8 V to 5.5 V			1	
TCL0 input high, low width	t_{TIH}, t_{TIL}	V_{DD} = 2.7. V to 5.5 V	0.48	–	–	µs
		V_{DD} = 1.8. V to 5.5 V	1.8			
SCK cycle time	t_{KCY}	V_{DD} = 2.7 V to 5.5 V External SCK source	800	–	–	ns
		Internal SCK source	650			
		V_{DD} = 1.8 V to 5.5 V External SCK source	3200			
		Internal SCK source	3800			
SCK high, low width	t_{KH}, t_{KL}	V_{DD} = 2.7 V to 5.5 V External SCK source	400	–	–	
		Internal SCK source	t_{KCY}/2- 50			
		V_{DD} = 1.8 V to 5.5 V External SCK source	1600			
		Internal SCK source	t_{KCY}/2-150			
SI setup time to SCK high	t_{SIK}	External SCK source	100	–	–	
		Internal SCK source	150			
SI hold time to SCK high	t_{KSI}	External SCK source	400	–	–	
		Internal SCK source	400			
Output delay for SCK to SO	t_{KSO}	V_{DD} = 2.7 V to 5.5 V External SCK source	–	–	300	
		Internal SCK source			250	
		V_{DD} = 1.8 V to 5.5 V External SCK source			1000	
		Internal SCK source			1000	

NOTE: Unless otherwise specified, Instruction Cycle Time condition values assume a main system clock/4 (fx/4) source.

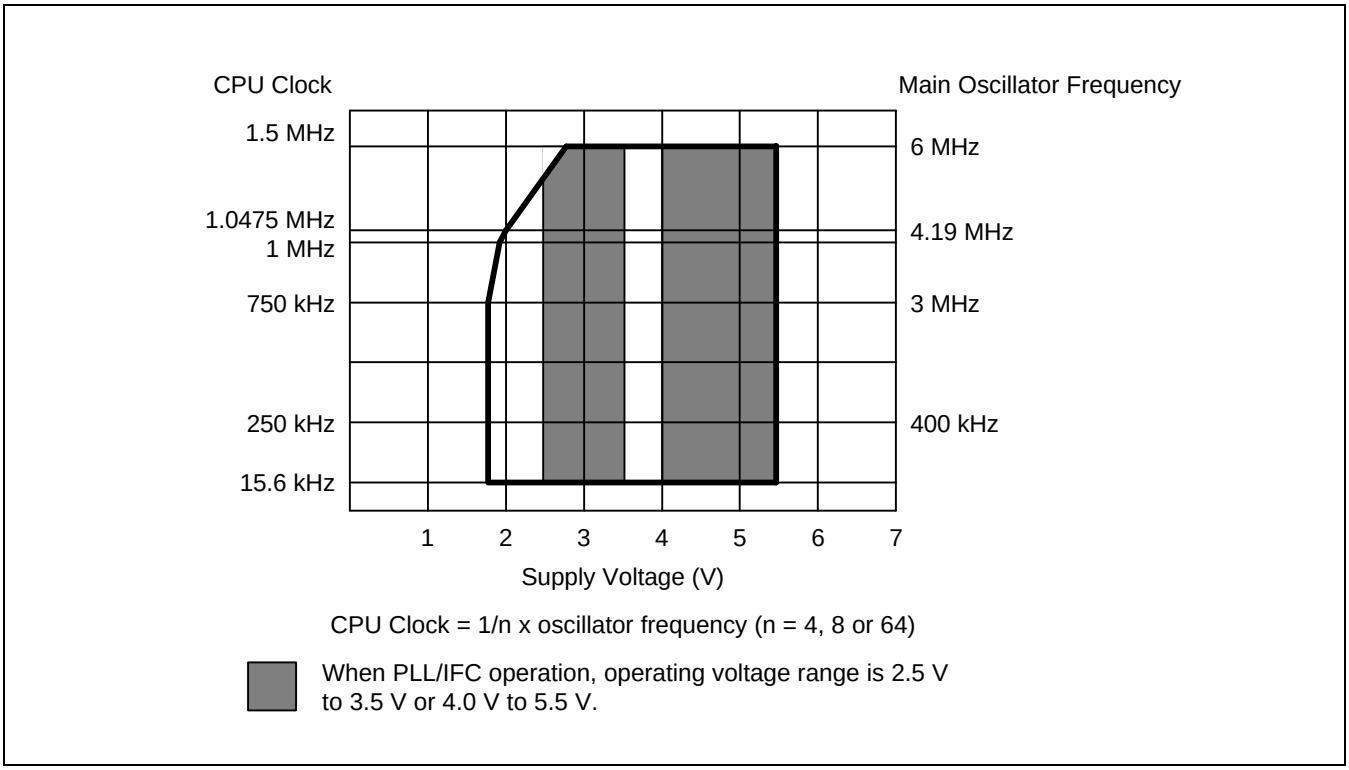


Figure 19-2. Standard Operating Voltage Range

Table 19-9. RAM Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	Normal operation	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V	–	0.1	1	µA

TIMING WAVEFORMS

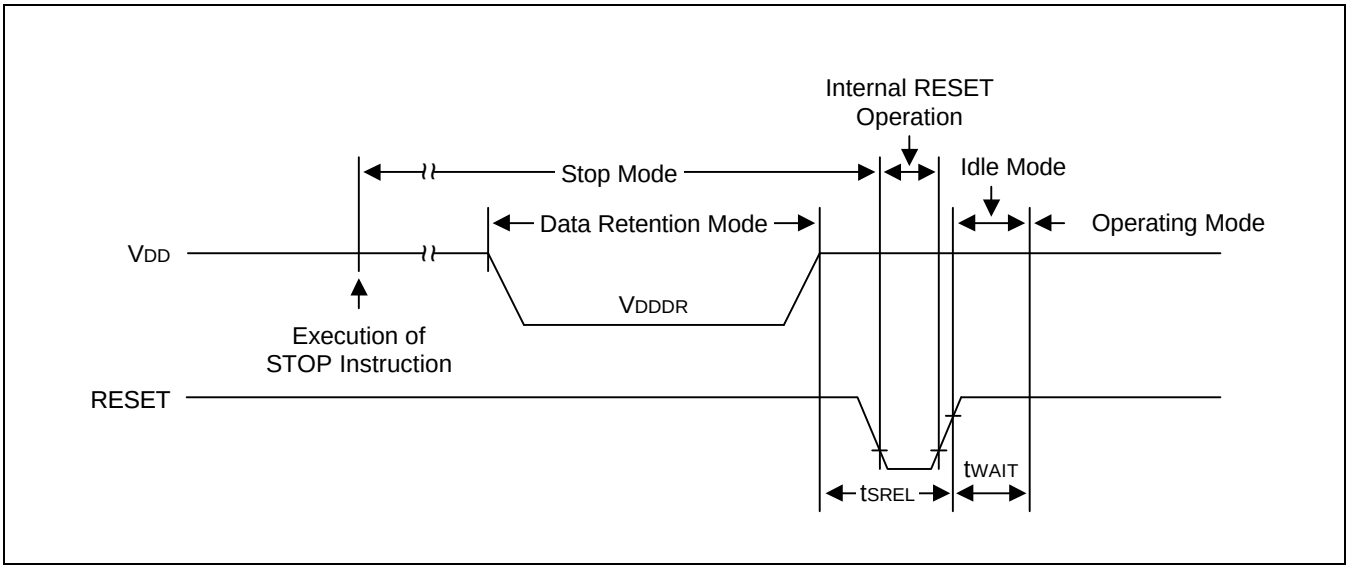


Figure 19-3. Stop Mode Release Timing When Initiated by RESET

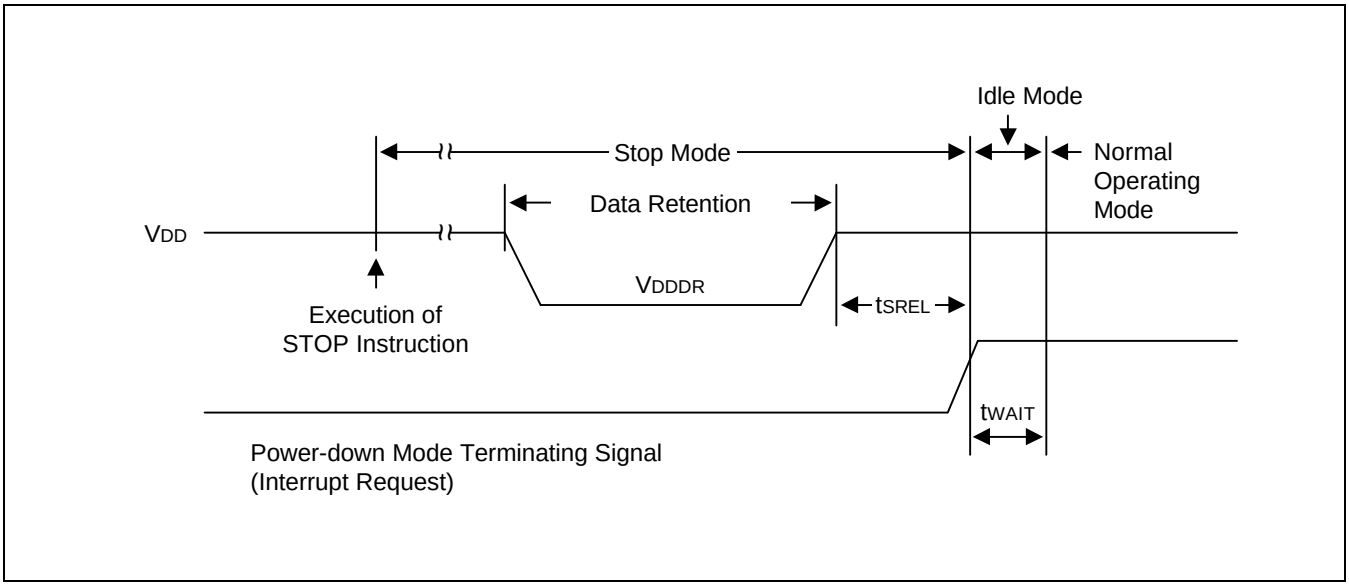


Figure 19-4. Stop Mode Release Timing When Initiated by an Interrupt Request

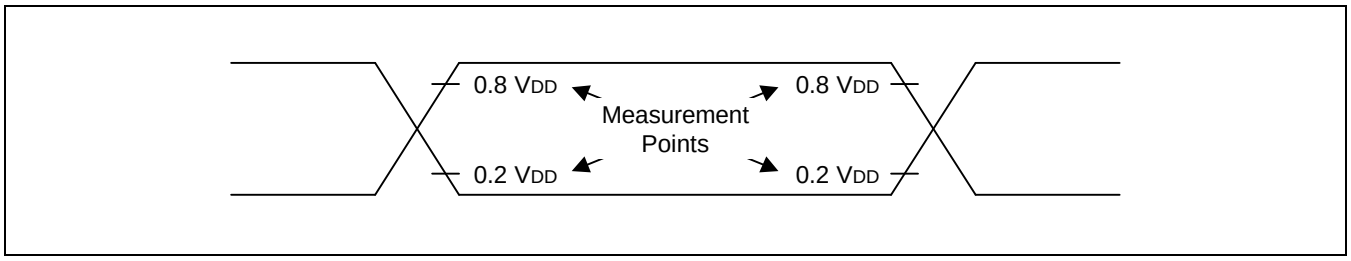


Figure 19-5. A.C. Timing Measurement Points (Except for X_{IN} and XT_{IN})

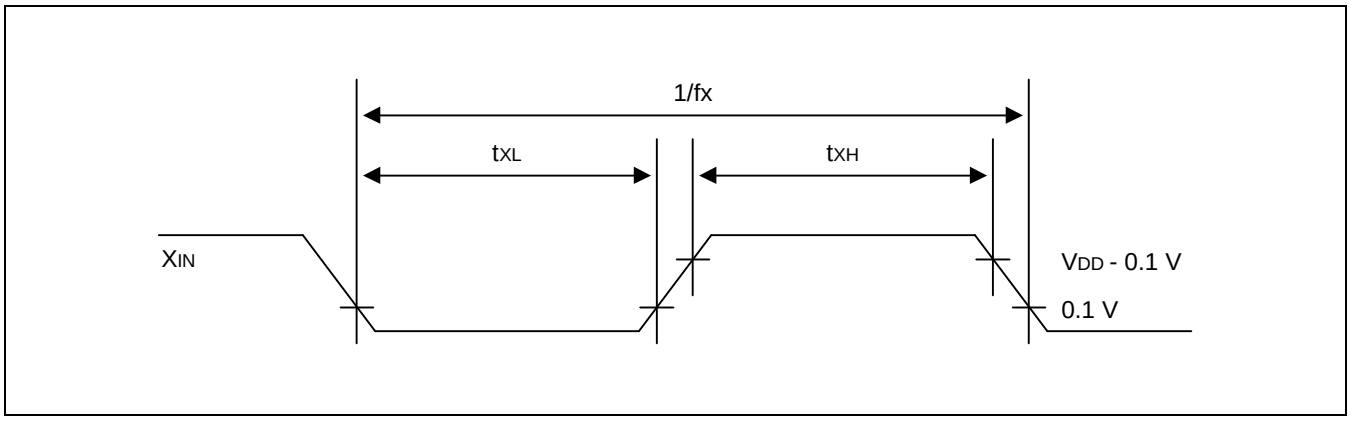


Figure 19-6. Clock Timing Measurement at X_{IN}

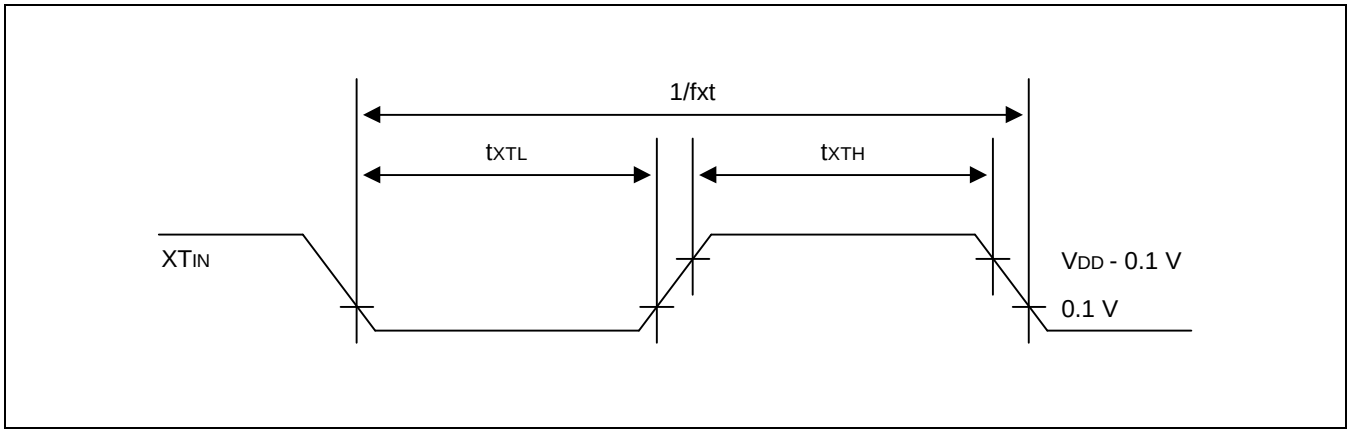


Figure 19-7. Clock Timing Measurement at XT_{IN}

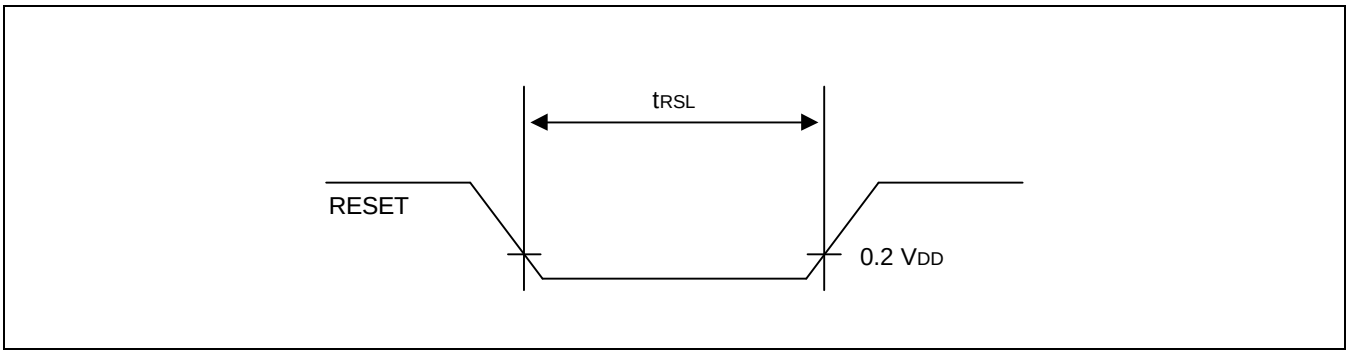


Figure 19-8. Input Timing for RESET Signal

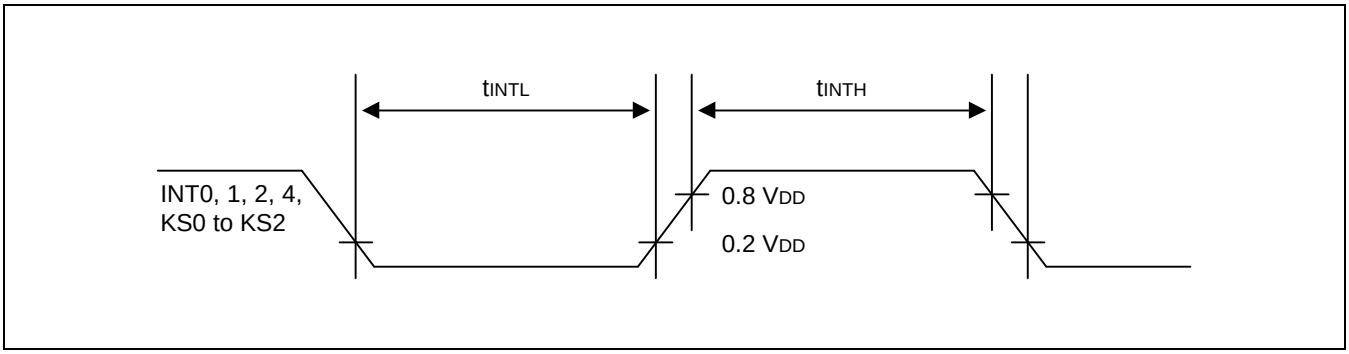


Figure 19-9. Input Timing for External Interrupts and Quasi-Interrupts