SIEMENS

Microcomputer Components

16-Bit CMOS Single-Chip Microcontroller

C163-L

Data Sheet 1998-08 Preliminary

C163-L **Revision History:**	**1998-08 Preliminary**
Previous Releases:	12.95 Advance Information
Page	**Subjects**
---	3 V specification introduced.
2	Ordering codes removed.
3	Pin description corrected (pin 16, 17, 21, 40).
24	SSCBR removed.
26, 27	Revised description of Absolute Maximum Ratings and Operating Conditions.
36	PLL description reworked.
39, 47	t_{22} updated.
55	t_{35}, t_{36}, t_{59} updated.
61	t_{200}, t_{203}, t_{204}, t_{209} updated.

Edition 1998-08

**Published by Siemens AG, Bereich Halbleiter,
Marketing-Kommunikation
Balanstraße 73, D-81541 München**

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SIEMENS

C166-Family of
High-Performance CMOS 16-Bit Microcontrollers

C163-L

Preliminary

C163-L 16-Bit Microcontroller

- High Performance 16-bit CPU with 4-Stage Pipeline
  - 80 ns Instruction Cycle Time at 25 MHz CPU Clock
  - 400 ns Multiplication (16 × 16 bit), 800 ns Division (32 / 16 bit)
  - Enhanced Boolean Bit Manipulation Facilities
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Single-Cycle Context Switching Support
  - 16 MBytes Total Linear Address Space for Code and Data
  - 1024 Bytes On-Chip Special Function Register Area
- 16-Priority-Level Interrupt System with 20 Sources, Sample-Rate down to 40 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- Clock Generation via on-chip PLL (1:1.5/2/2.5/3/4/5), via prescaler or via direct clock input
- On-Chip Memory Modules
  - 1 KBytes On-Chip Internal RAM (IRAM)
- On-Chip Peripheral Modules
  - Two Multi-Functional General Purpose Timer Units with 5 Timers
  - Two Serial Channels (Synchronous/Asynchronous and High-Speed-Synchronous)
- Up to 16 MBytes External Address Space for Code and Data
  - Programmable External Bus Characteristics for Different Address Ranges
  - Multiplexed or Demultiplexed External Address/Data Buses with 8-Bit or 16-Bit Data Bus Width
  - Five Programmable Chip-Select Signals
  - Hold- and Hold-Acknowledge Bus Arbitration Support
- Idle and Power Down Modes
- Programmable Watchdog Timer and Oscillator Watchdog
- Up to 77 General Purpose I/O Lines
- High Speed Operation with 5 V Supply up to 25 MHz
- Low Power Operation with 3 V Supply up to 12 MHz
- Supported by a Large Range of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- 100-Pin TQFP Package (Thin QFP)

This document describes the **SAB-C163-LF**, the **SAB-C163-L25F** and the **SAF-C163-L25F**.
For simplicity all versions are referred to by the term **C163-L** throughout this document.

Introduction

The C163-L is a derivative of the Siemens C166 family of 16-bit single-chip CMOS microcontrollers. It combines high CPU performance (up to 12.5 million instructions per second) with high peripheral functionality and enhanced IO-capabilities.

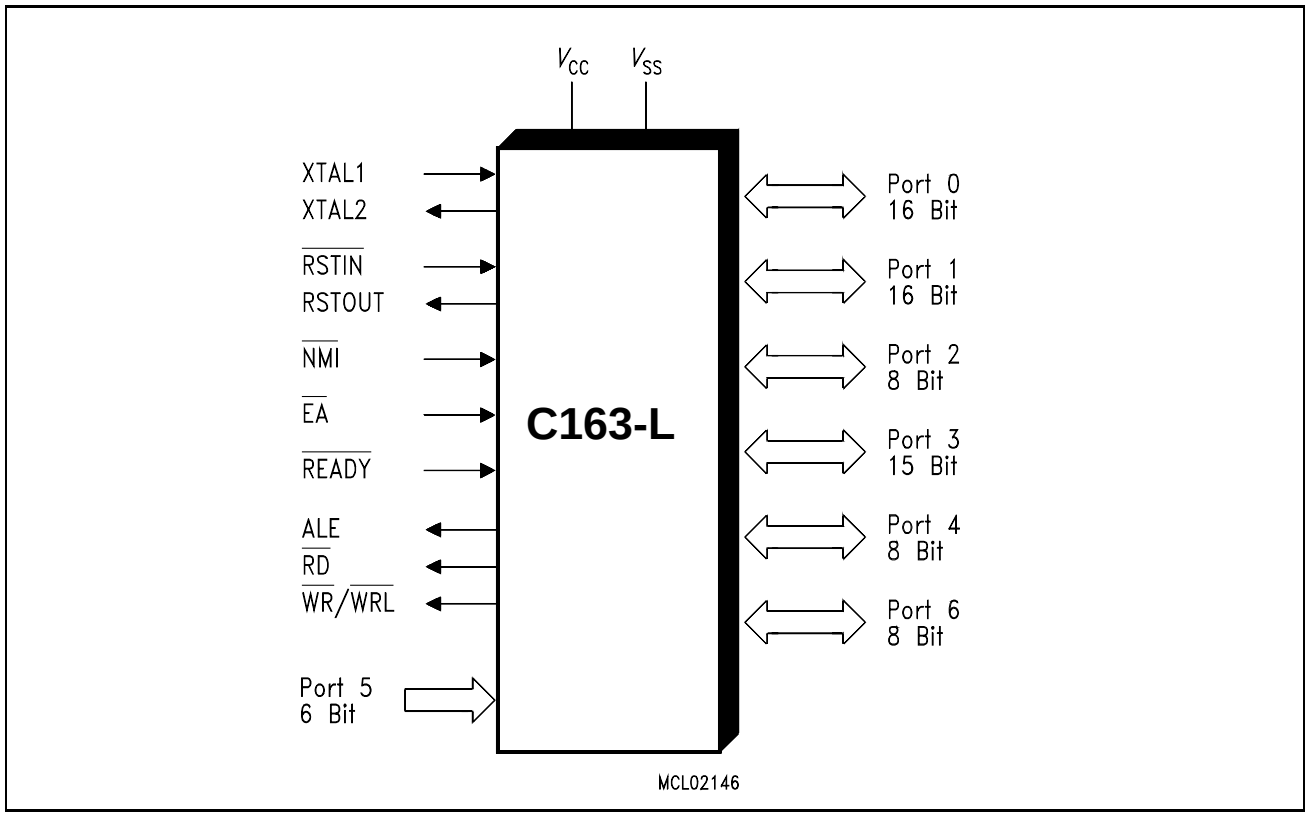


Figure 1
Logic Symbol

The C163-L can be operated from a 5 V power supply as well as from a 3 V power supply (25 MHz versions C163-L25F only). Within the standard supply voltage range of V_{DD} = 4.5 - 5.5 V it delivers its maximum performance at CPU clock frequencies of up to 25 MHz. Within the reduced supply voltage range of V_{DD} = 2.7 - 3.6 V it provides low power operation for energy sensitive applications at CPU clock frequencies of up to 12 MHz (PLL operation is not supported in this case).

Ordering Information

The ordering code for Siemens microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, ie. its function set
- the specified temperature range
- the package
- the type of delivery.

For the available ordering codes for the C163-L please refer to the
„**Product Information Microcontrollers**“, which summarizes all available microcontroller variants.

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.

Pin Configuration TQFP Package
(top view)

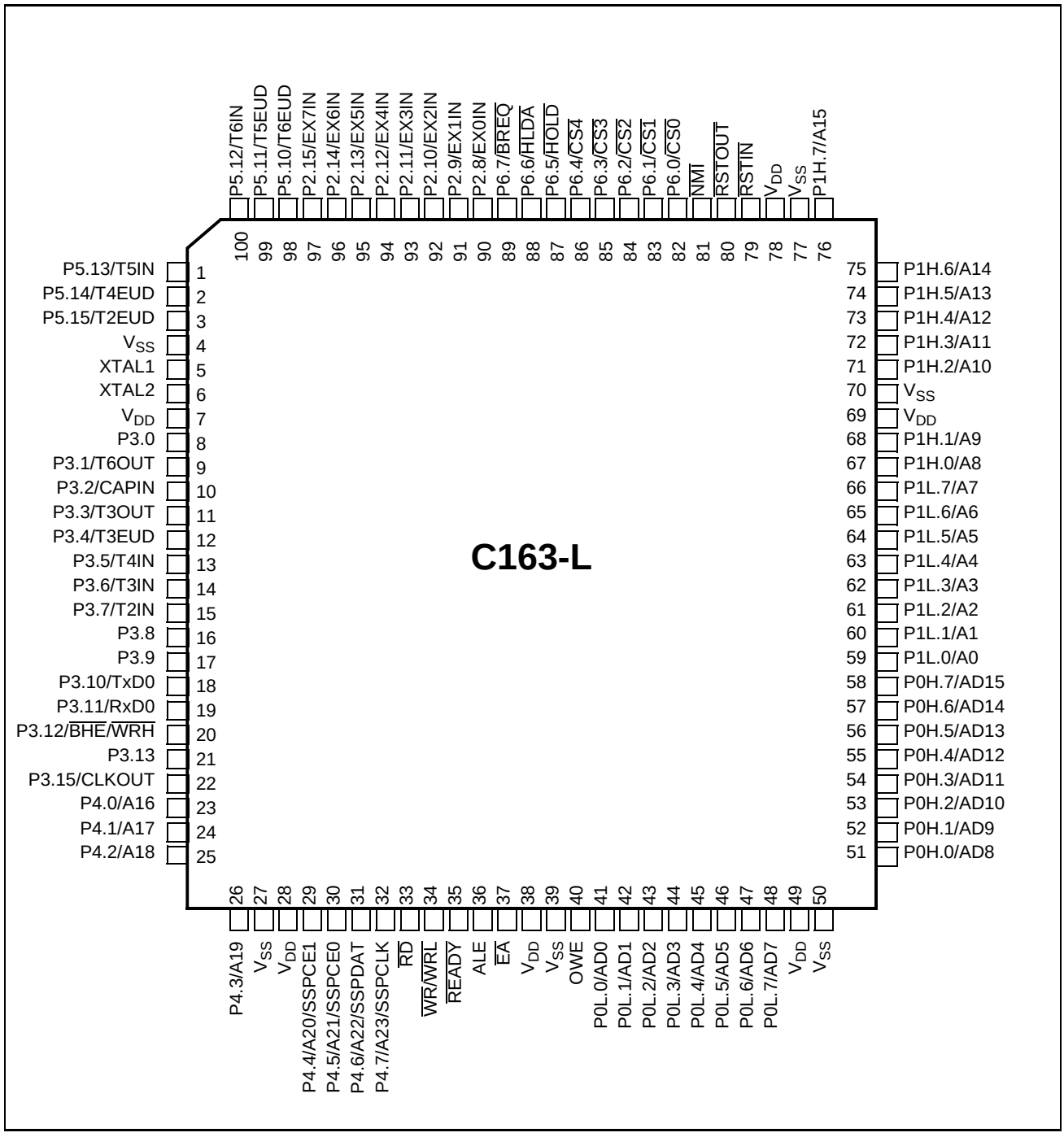


Figure 2

Pin Definitions and Functions

Symbol	Pin Numb. TQFP	Input Out-put	Function	
P5		I	Port 5 is a 6-bit input-only port with Schmitt-Trigger characteristics. The pins of Port 5 also serve as timer inputs:	
P5.10	98	I	T6EUD	GPT2 Timer T6 External Up/Down Control Input
P5.11	99	I	T5EUD	GPT2 Timer T5 External Up/Down Control Input
P5.12	100	I	T6IN	GPT2 Timer T6 Count Input
P5.13	1	I	T5IN	GPT2 Timer T5 Count Input
P5.14	2	I	T4EUD	GPT1 Timer T4 External Up/Down Control Input
P5.15	3	I	T2EUD	GPT1 Timer T2 External Up/Down Control Input
XTAL1	5	I	Input to the oscillator amplifier and input to the internal clock generator. Output of the oscillator amplifier circuit.	
XTAL2	6	O	To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.	
P3		IO	Port 3 is a 15-bit (P3.14 is missing) bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. Some Port 3 pins also serve for alternate functions:	
P3.0	8		-	
P3.1	9	O	T6OUT	GPT2 Timer T6 Toggle Latch Output
P3.2	10	I	CAPIN	GPT2 Register CAPREL Capture Input
P3.3	11	O	T3OUT	GPT1 Timer T3 Toggle Latch Output
P3.4	12	I	T3EUD	GPT1 Timer T3 Ext.Up/Down Ctrl.Input
P3.5	13	I	T4IN	GPT1 Timer T4 Input for Count/Gate/Reload/Capture
P3.6	14	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	15	I	T2IN	GPT1 Timer T2 Input for Count/Gate/Reload/Capture
P3.8	16		-	
P3.9	17		-	
P3.10	18	O	T×D0	ASC0 Clock/Data Output (Asyn./Syn.)
P3.11	19	IO	R×D0	ASC0 Data Input (Asyn.) or I/O (Syn.)
P3.12	20	O	$\overline{\text{BHE}}$	Ext. Memory High Byte Enable Signal,
		O	$\overline{\text{WRH}}$	Ext. Memory High Byte Write Strobe
P3.13	21		-	
P3.15	22	O	CLKOUT	System Clock Output (=CPU Clock)

Pin Definitions and Functions (cont'd)

Symbol	Pin Numb. TQFP	Input Out-put	Function	
P4		IO	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, Port 4 can be used to output the segment address lines and it provides the SSP interface lines:	
P4.0	23	O	A16	Least Significant Segment Address Line
P4.1	24	O	A17	Segment Address Line
P4.2	25	O	A18	Segment Address Line
P4.3	26	O	A19	Segment Address Line
P4.4	29	O	A20	Segment Address Line,
		O	SSPCE1	SSP Chip Enable Line 1
P4.5	30	O	A21	Segment Address Line,
		O	SSPCE0	SSP Chip Enable Line 0
P4.6	31	O	A22	Segment Address Line,
		IO	SSPDAT	SSP Data Input/Output Line
P4.7	32	O	A23	Most Significant Segment Addr. Line
		O	SSPCLK	SSP Clock Output Line
$\overline{RD}$	33	O	External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access.	
$\overline{WR}$/ $\overline{WRL}$	34	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See bit WRCFG in register SYSCON for mode selection.	
$\overline{READY}$	35	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to a low level.	
ALE	36	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.	
$\overline{EA}$	37	I	External Access Enable pin. A low level at this pin during and after Reset forces the C163-L to begin instruction execution out of external memory. A high level forces execution out of the internal ROM. The C163-L must have this pin tied to '0'.	

Pin Definitions and Functions (cont'd)

Symbol	Pin Numb. TQFP	Input Out-put	Function
PORT0 P0L.0-7 P0H.0-7	 41 - 48 51 - 58	IO	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: D0 – D7 D0 - D7 P0H.0 – P0H.7: I/O D8 - D15 **Multiplexed bus modes:** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: AD0 – AD7 AD0 - AD7 P0H.0 – P0H.7: A8 - A15 AD8 - AD15
PORT1 P1L.0-7 P1H.0-7	 59 - 66 67, 68, 71 - 76	IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode.
$\overline{\text{RSTIN}}$	79	I	Reset Input with Schmitt-Trigger characteristics. A low level at this pin for a minimum of 2 CPU clock cycles while the oscillator is running resets the C163-L. An internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}. **Note**: To let the reset configuration of PORT0 settle and to let the PLL lock a reset duration of ca. 1 ms is recommended.
$\overline{\text{RST}}$ $\overline{\text{OUT}}$	80	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.
$\overline{\text{NMI}}$	81	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the C163-L to go into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.

Pin Definitions and Functions (cont'd)

Symbol	Pin Numb. TQFP	Input Out-put	Function
P6		IO	Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The Port 6 pins also serve as bus interface signals:
P6.0	82	O	$\overline{CS0}$ Chip Select 0 Output
P6.1	83	O	$\overline{CS1}$ Chip Select 1 Output
P6.2	84	O	$\overline{CS2}$ Chip Select 2 Output
P6.3	85	O	$\overline{CS3}$ Chip Select 3 Output
P6.4	86	O	$\overline{CS4}$ Chip Select 4 Output
P6.5	87	I	$\overline{HOLD}$ External Master Hold Request Input
P6.6	88	I/O	$\overline{HLDA}$ Hold Acknowledge Output or Input (Master mode: O, Slave mode: I)
P6.7	89	O	$\overline{BREQ}$ Bus Request Output
P2		IO	Port 2 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The Port 2 pins also serve as fast external interrupt inputs:
P2.8	90	I	EX0IN Fast External Interrupt 0 Input
P2.9	91	I	EX1IN Fast External Interrupt 1 Input
P2.10	92	I	EX2IN Fast External Interrupt 2 Input
P2.11	93	I	EX3IN Fast External Interrupt 3 Input
P2.12	94	I	EX4IN Fast External Interrupt 4 Input
P2.13	95	I	EX5IN Fast External Interrupt 5 Input
P2.14	96	I	EX6IN Fast External Interrupt 6 Input
P2.15	97	I	EX7IN Fast External Interrupt 7 Input
OWE	40	I	Oscillator Watchdog Enable. This pin enables the PLL when high or disables it when low (e.g. to disable the OWD for testing purposes. An internal pullup device holds this input high if nothing is driving it. **Note**: The input voltage at pin OWE must not exceed 12.6 V. For 3 V operation pin OWE must be driven low.
V_{DD}	7, 28, 38, 49, 69, 78	-	Digital Supply Voltage: + 5 V or +3 V during normal operation and idle mode. ≥ 2.5 V during power down mode
V_{SS}	4, 27, 39, 50, 70, 77	-	Digital Ground.

Functional Description

The architecture of the C163-L combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the C163-L.

Note: All time specifications refer to a CPU clock of 25/12 MHz for 5/3 V operation (see definition in the AC Characteristics section).

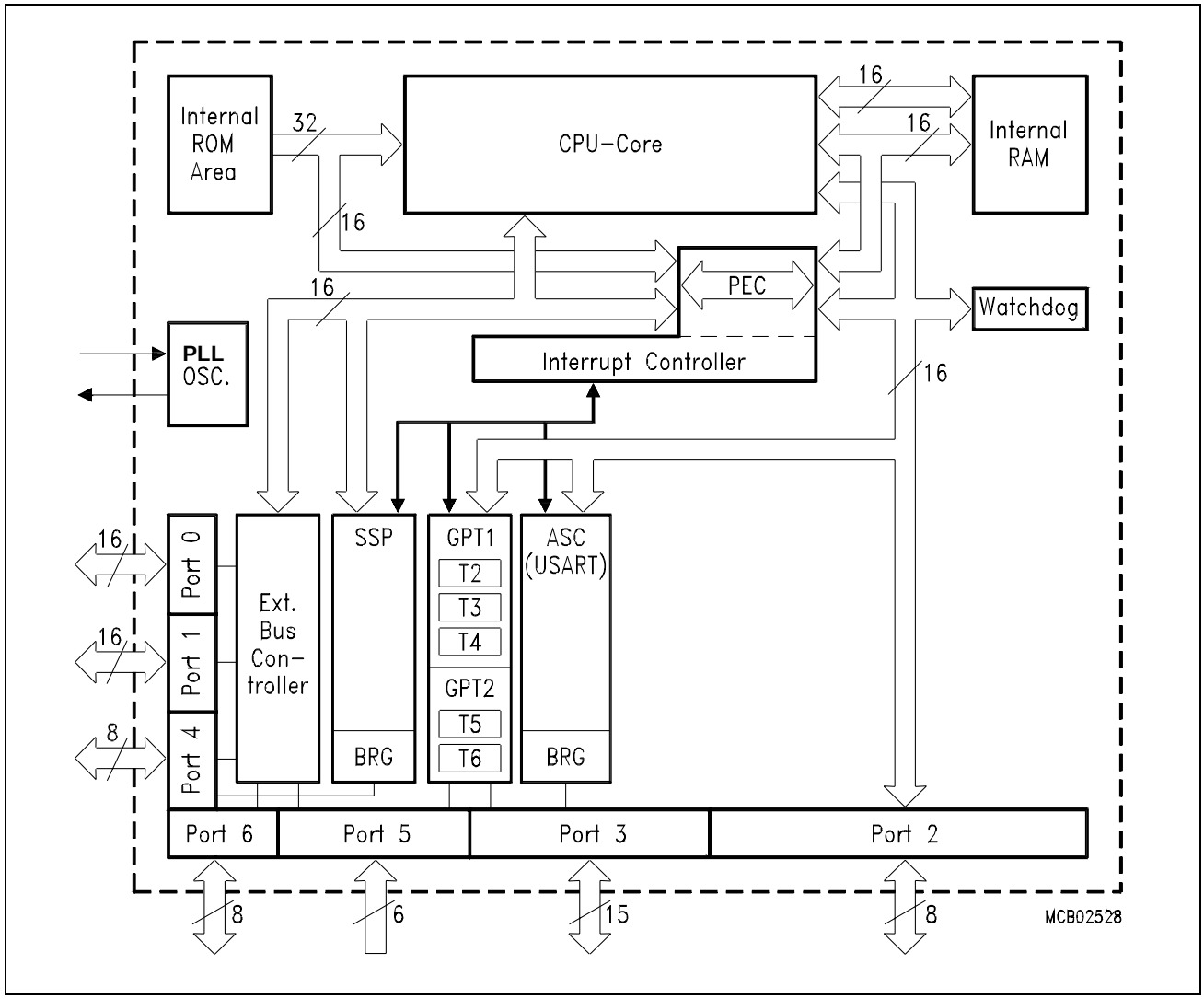


Figure 3
Block Diagram

Memory Organization

The memory space of the C163-L is configured in a Von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which includes 16 MBytes. The entire memory space can be accessed bytewise or wordwise. Particular portions of the on-chip memory have additionally been made directly bit addressable.

The C163-L is prepared to incorporate on-chip mask-programmable ROM, OTP or Flash memory for code or constant data. Currently no program memory is integrated.

1 KByte of on-chip RAM is provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, …, RL7, RH7) so-called General Purpose Registers (GPRs).

1024 bytes (2 * 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for other/future members of the C166 family.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 16 MBytes of external RAM and/or ROM can be connected to the microcontroller.

External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

– 16-/18-/20-/24-bit Addresses, 16-bit Data, Demultiplexed

– 16-/18-/20-/24-bit Addresses, 16-bit Data, Multiplexed

– 16-/18-/20-/24-bit Addresses, 8-bit Data, Multiplexed

– 16-/18-/20-/24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.
In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which allow to access different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.
Up to 5 external $\overline{CS}$ signals (4 windows plus default) can be generated in order to save external glue logic. Access to very slow memories is supported via a particular ‘Ready’ function.

A $\overline{HOLD}$/$\overline{HLDA}$ protocol is available for bus arbitration and allows to share external resources with other bus masters. The bus arbitration is enabled by setting bit HLDEN in register SYSCON. After setting HLDEN once, pins P6.7...P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{HLDA}$ pin is an output. By setting bit DP6.7 to ’1’ the Slave Mode is selected where pin $\overline{HLDA}$ is switched to input. This allows to directly connect the slave controller to another master controller without glue logic.

For applications which require less than 16 MBytes of external memory space, this address space can be restricted to 1 MByte, 256 KByte or to 64 KByte. In this case Port 4 outputs four, two or no address lines at all. It outputs all 8 address lines, if an address space of 16 MBytes is used.

Note: When the on-chip SSP Module is to be used the segment address output on Port 4 must be limited to 4 bits (ie. A19...A16) in order to enable the alternate function of the SSP interface pins.

Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the C163-L's instructions can be executed in just one machine cycle which requires 80 ns at 25-MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16 $\times$ 16 bit multiplication in 5 cycles and a 32-/16 bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.

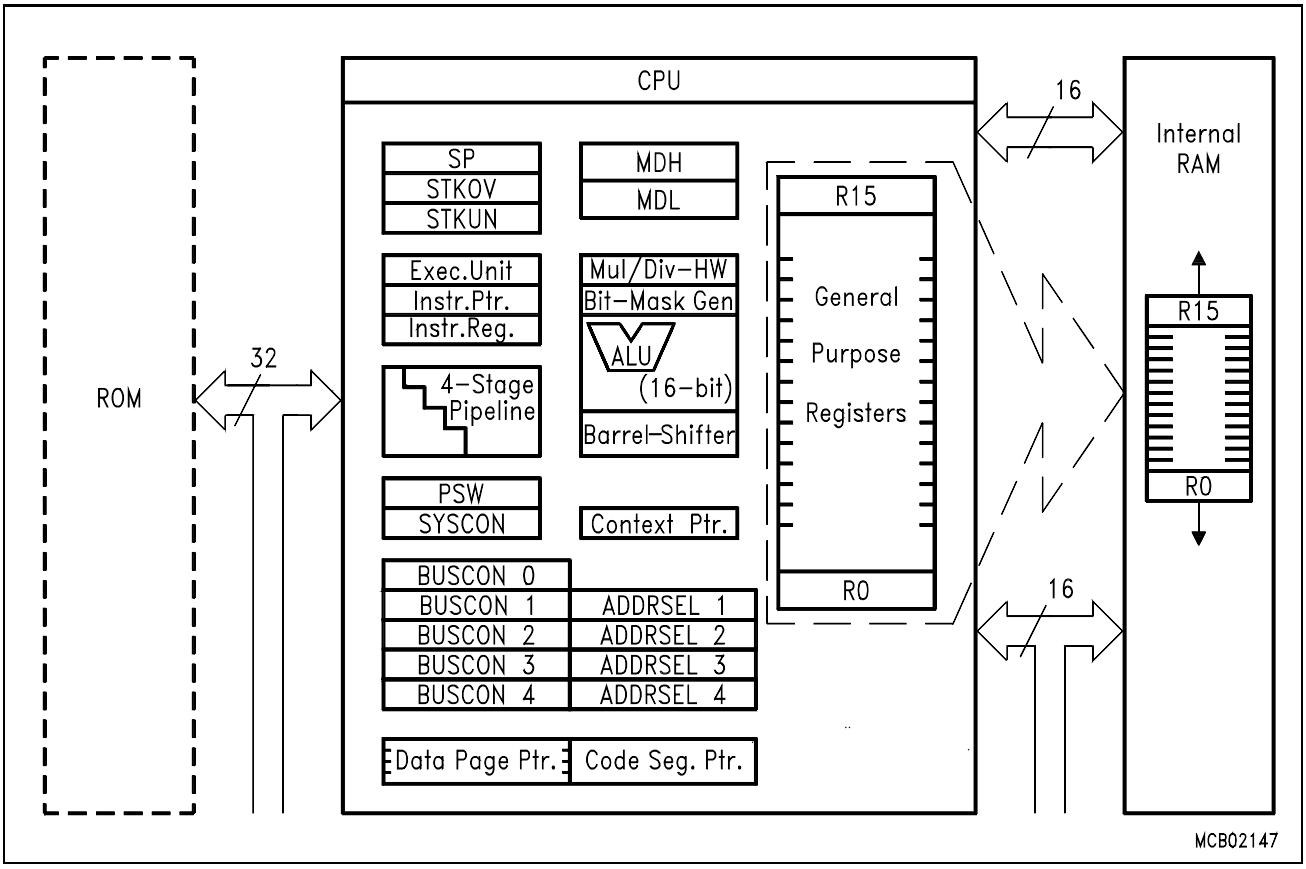


Figure 4
CPU Block Diagram

The CPU disposes of an actual register context consisting of up to 16 wordwide GPRs which are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at a time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 512 words is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient C163-L instruction set which includes the following instruction classes:

– Arithmetic Instructions
– Logical Instructions
– Boolean Bit Manipulation Instructions
– Compare and Loop Control Instructions
– Shift and Rotate Instructions
– Prioritize Instruction
– Data Movement Instructions
– System Stack Instructions
– Jump and Call Instructions
– Return Instructions
– System Control Instructions
– Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

Interrupt System

With an interrupt response time within a range from just 200 ns to 480 ns (in case of internal program execution), the C163-L is capable of reacting very fast to the occurence of non-deterministic events.

The architecture of the C163-L supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicity decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C163-L has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

The following table shows all of the possible C163-L interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers:

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
External Interrupt 0	CC8IR	CC8IE	CC8INT	$00'0060_H$	18_H
External Interrupt 1	CC9IR	CC9IE	CC9INT	$00'0064_H$	19_H
External Interrupt 2	CC10IR	CC10IE	CC10INT	$00'0068_H$	$1A_H$
External Interrupt 3	CC11IR	CC11IE	CC11INT	$00'006C_H$	$1B_H$
External Interrupt 4	CC12IR	CC12IE	CC12INT	$00'0070_H$	$1C_H$
External Interrupt 5	CC13IR	CC13IE	CC13INT	$00'0074_H$	$1D_H$
External Interrupt 6	CC14IR	CC14IE	CC14INT	$00'0078_H$	$1E_H$
External Interrupt 7	CC15IR	CC15IE	CC15INT	$00'007C_H$	$1F_H$
GPT1 Timer 2	T2IR	T2IE	T2INT	$00'0088_H$	22_H
GPT1 Timer 3	T3IR	T3IE	T3INT	$00'008C_H$	23_H
GPT1 Timer 4	T4IR	T4IE	T4INT	$00'0090_H$	24_H
GPT2 Timer 5	T5IR	T5IE	T5INT	$00'0094_H$	25_H
GPT2 Timer 6	T6IR	T6IE	T6INT	$00'0098_H$	26_H
GPT2 CAPREL Register	CRIR	CRIE	CRINT	$00'009C_H$	27_H
ASC0 Transmit	S0TIR	S0TIE	S0TINT	$00'00A8_H$	$2A_H$
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	$00'011C_H$	47_H
ASC0 Receive	S0RIR	S0RIE	S0RINT	$00'00AC_H$	$2B_H$
ASC0 Error	S0EIR	S0EIE	S0EINT	$00'00B0_H$	$2C_H$
SSP Interrupt	XP1IR	XP1IE	XP1INT	$00'0104_H$	41_H
PLL Unlock / OWD	XP3IR	XP3IE	XP3INT	$00'010C_H$	43_H

The C163-L also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

The following table shows all of the possible exceptions or error conditions that can arise during run-time:

Exception Condition	**Trap Flag**	**Trap Vector**	**Vector Location**	**Trap Number**	**Trap Priority**
Reset Functions:					
Hardware Reset		RESET	$00'0000_H$	00_H	III
Software Reset		RESET	$00'0000_H$	00_H	III
Watchdog Timer Overflow		RESET	$00'0000_H$	00_H	III
Class A Hardware Traps:					
Non-Maskable Interrupt	NMI	NMITRAP	$00'0008_H$	02_H	II
Stack Overflow	STKOF	STOTRAP	$00'0010_H$	04_H	II
Stack Underflow	STKUF	STUTRAP	$00'0018_H$	06_H	II
Class B Hardware Traps:					
Undefined Opcode	UNDOPC	BTRAP	$00'0028_H$	$0A_H$	I
Protected Instruction Fault	PRTFLT	BTRAP	$00'0028_H$	$0A_H$	I
Illegal Word Operand Access	ILLOPA	BTRAP	$00'0028_H$	$0A_H$	I
Illegal Instruction Access	ILLINA	BTRAP	$00'0028_H$	$0A_H$	I
Illegal External Bus Access	ILLBUS	BTRAP	$00'0028_H$	$0A_H$	I
Reserved			$[2C_H – 3C_H]$	$[0B_H – 0F_H]$	
Software Traps TRAP Instruction			Any $[00'0000_H – 00'01FC_H]$ in steps of 4_H	Any $[00_H – 7F_H]$	Current CPU Priority

General Purpose Timer (GPT) Unit

The GPT unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.
The GPT unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of three basic modes of operation, which are Timer, Gated Timer, and Counter Mode. In Timer Mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.
Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 320 ns (@ 25 MHz CPU clock).

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e. g. position tracking.

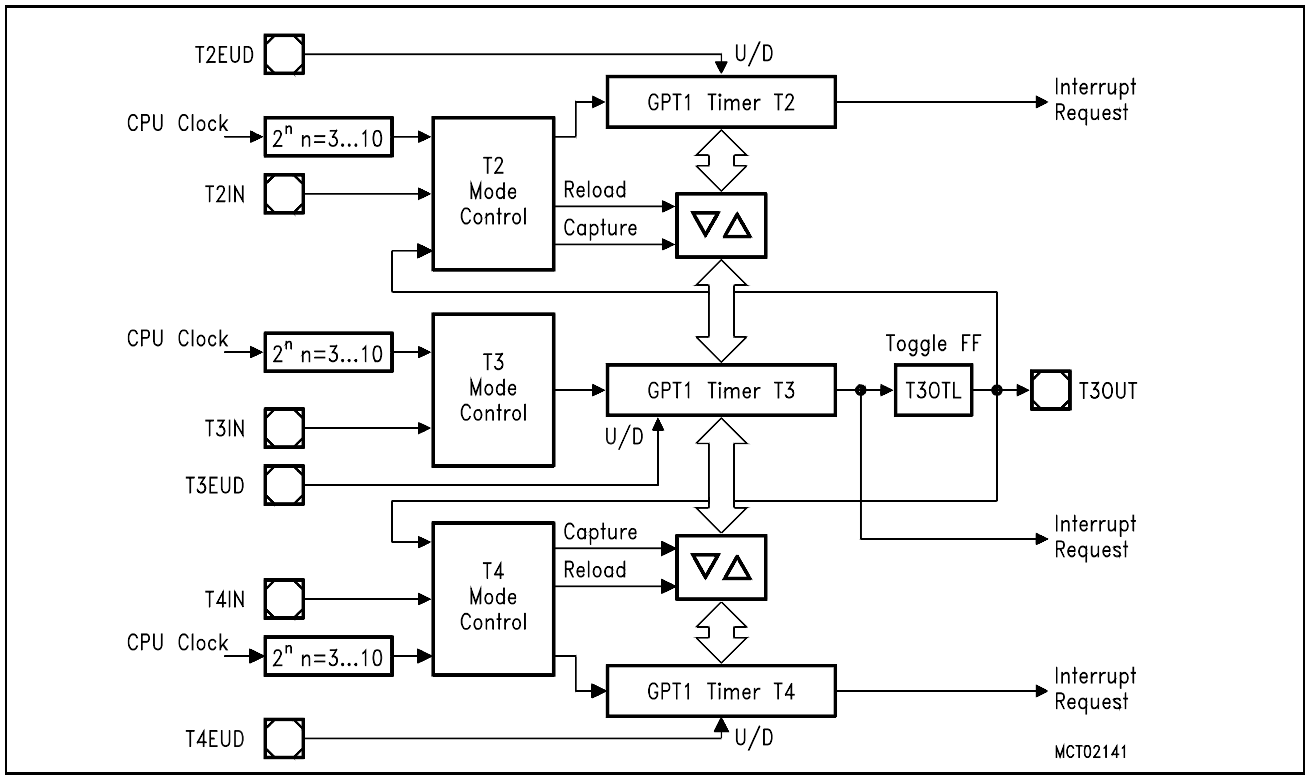


Figure 5
Block Diagram of GPT1

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer over-flow/ underflow. The state of this latch may be output on port a pin (T3OUT) e.g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

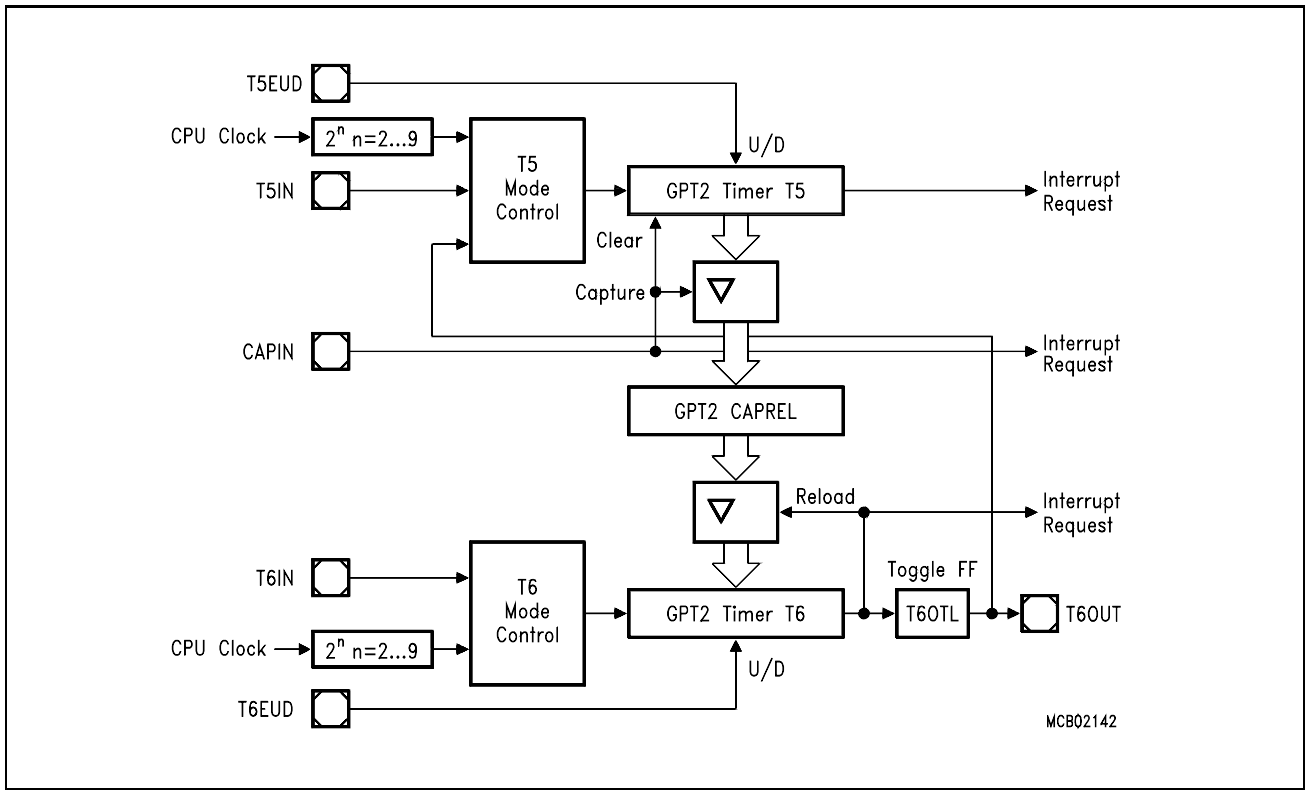


Figure 6
Block Diagram of GPT2

With its maximum resolution of 160 ns (@ 25 MHz), the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Timer T6 has an output toggle latch (T6OTL) which changes its state on each timer overflow/underflow. Concatenation of the timers is supported via T6OTL.

The state of this latch may be used to clock timer T5, or it may be output on a port pin (T6OUT). The overflows/underflows of timer T6 can additionally be used to cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows absolute time differences to be measured or pulse multiplication to be performed without software overhead.

Parallel Ports

The C163-L provides up to 77 I/O lines which are organized into six input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of three I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

All port lines have programmable alternate input or output functions associated with them. PORT0 and PORT1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A23/19/17...A16 in systems where segmentation is enabled to access more than 64 KBytes of memory. Port 6 provides optional bus arbitration signals ($\overline{\text{BREQ}}$, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$) and chip select signals. Port 3 includes alternate functions of timers, serial interfaces, the optional bus control signal $\overline{\text{BHE}}$ and the system clock output (CLKOUT). Port 5 is used for timer control signals. All port lines that are not used for these alternate functions may be used as general purpose I/O lines.

Serial Channels

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by two serial interfaces with different functionality, an Asynchronous/ Synchronous Serial Channel (ASC0) and a Synchronous Serial Port (SSP).

The ASC0 is upward compatible with the serial ports of the Siemens 8-bit microcontroller families and supports full-duplex asynchronous communication at up to 781 KBaud and half-duplex synchronous communication at up to 3.125 MBaud @ 25 MHz CPU clock.
A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling 4 separate interrupt vectors are provided. In asynchronous mode, 8- or 9-bit data frames are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data plus wake up bit mode).
In synchronous mode, the ASC0 transmits or receives bytes (8 bits) synchronously to a shift clock which is generated by the ASC0. The ASC0 always shifts the LSB first. A loop back option is available for testing purposes.
A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmission or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated, if the last character received has not been read out of the receive buffer register at the time the reception of a new character is complete.

The SSP transmits 1...3 bytes or receives 1 byte after sending 1...3 bytes synchronously to a shift clock which is generated by the SSP. The SSP can start shifting with the LSB or with the MSB and allows to select shifting and latching clock edges as well as the clock polarity. Up to two chip select lines may be activated in order to direct data transfers to one or both of two peripheral devices.
One general interrupt vector is provided for the SSP.

Watchdog Timer

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. Thus, the chip's start-up procedure is always monitored. The software has to be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset and pulls the $\overline{\text{RSTOUT}}$ pin low in order to allow external hardware components to be reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided either by 2 or by 128. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Thus, time intervals between 20 µs and 336 ms can be monitored (@ 25 MHz). The default Watchdog Timer interval after reset is 5.24 ms (@ 25 MHz).

Oscillator Watchdog

During direct drive or prescaler operation the Oscillator Watchdog (OWD) monitors the clock signal generated by the on-chip oscillator (either with a crystal or via external clock drive). For this operation the PLL provides a clock signal which is used to supervise transitions on the oscillator clock. This PLL clock is independent from the XTAL1 clock. When the expected oscillator clock transitions are missing the OWD activates the PLL Unlock / OWD interrupt node and supplies the CPU with the PLL clock signal. Under these circumstances the PLL will oscillate with its basic frequency.

A low level on pin OWE disables the PLL and the OWD's interrupt output so the clock signal is derived from the oscillator clock in any case.

Note: The CPU clock source is only switched back to the oscillator clock after a hardware reset.

For 3 V operation pin OWE must always be low (OWD disabled) as the PLL cannot deliver an appropriate clock signal in this case.

For 5 V operation pin OWE should only be pulled low (PLL disabled) if direct drive or prescaler operation is configured. All other configurations (PLL factors) result in direct drive operation.

Instruction Set Summary

The table below lists the instructions of the C163-L in a condensed way.
The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **“C16x Family Instruction Set Manual”**.

This document also provides a detailled description of each instruction.

Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16-16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise XOR, (word/byte operands)	2 / 4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL / SHR	Shift left/right direct word GPR	2
ROL / ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2

Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
MOV(B)	Move word (byte) data	2 / 4
MOVBS	Move byte operand to word operand with sign extension	2 / 4
MOVBZ	Move byte operand to word operand. with zero extension	2 / 4
JMPA, JMPI, JMPR	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
J(N)B	Jump relative if direct bit is (not) set	4
JBC	Jump relative and clear bit if direct bit is set	4
JNBS	Jump relative and set bit if direct bit is not set	4
CALLA, CALLI, CALLR	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH, POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack und update register with word operand	4
RET	Return from intra-segment subroutine	2
RETS	Return from inter-segment subroutine	2
RETP	Return from intra-segment subroutine and pop direct word register from system stack	2
RETI	Return from interrupt service subroutine	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$-pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT	Disable Watchdog Timer	4
EINIT	Signify End-of-Initialization on RSTOUT-pin	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4
NOP	Null operation	2

Special Function Registers Overview

The following table lists all SFRs which are implemented in the C163-L in alphabetical order. **Bit-addressable** SFRs are marked with the letter "**b**" in column "Name". SFRs within the **Extended SFR-Space** (ESFRs) are marked with the letter "**E**" in column "Physical Address". Registers within on-chip X-Peripherals (SSP) are marked with the letter "**X**" in column "Physical Address".

An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Special Function Registers Overview

Name	Physical Address	8-Bit Address	Description	Reset Value
ADDRSEL1	$FE18_H$	$0C_H$	Address Select Register 1	0000_H
ADDRSEL2	$FE1A_H$	$0D_H$	Address Select Register 2	0000_H
ADDRSEL3	$FE1C_H$	$0E_H$	Address Select Register 3	0000_H
ADDRSEL4	$FE1E_H$	$0F_H$	Address Select Register 4	0000_H
BUSCON0 b	$FF0C_H$	86_H	Bus Configuration Register 0	$0XX0_H$
BUSCON1 b	$FF14_H$	$8A_H$	Bus Configuration Register 1	0000_H
BUSCON2 b	$FF16_H$	$8B_H$	Bus Configuration Register 2	0000_H
BUSCON3 b	$FF18_H$	$8C_H$	Bus Configuration Register 3	0000_H
BUSCON4 b	$FF1A_H$	$8D_H$	Bus Configuration Register 4	0000_H
CAPREL	$FE4A_H$	25_H	GPT2 Capture/Reload Register	0000_H
CC8IC b	$FF88_H$	$C4_H$	EX0IN Interrupt Control Register	0000_H
CC9IC b	$FF8A_H$	$C5_H$	EX1IN Interrupt Control Register	0000_H
CC10IC b	$FF8C_H$	$C6_H$	EX2IN Interrupt Control Register	0000_H
CC11IC b	$FF8E_H$	$C7_H$	EX3IN Interrupt Control Register	0000_H
CC12IC b	$FF90_H$	$C8_H$	EX4IN Interrupt Control Register	0000_H
CC13IC b	$FF92_H$	$C9_H$	EX5IN Interrupt Control Register	0000_H
CC14IC b	$FF94_H$	CA_H	EX6IN Interrupt Control Register	0000_H
CC15IC b	$FF96_H$	CB_H	EX7IN Interrupt Control Register	0000_H
CP	$FE10_H$	08_H	CPU Context Pointer Register	$FC00_H$
CRIC b	$FF6A_H$	$B5_H$	GPT2 CAPREL Interrupt Control Register	0000_H
CSP	$FE08_H$	04_H	CPU Code Segment Pointer Register (read only)	0000_H

Special Function Registers Overview (cont'd)

Name		Physical Address		8-Bit Address	Description	Reset Value
DP0L	**b**	$F100_H$	**E**	80_H	P0L Direction Control Register	00_H
DP0H	**b**	$F102_H$	**E**	81_H	P0H Direction Control Register	00_H
DP1L	**b**	$F104_H$	**E**	82_H	P1L Direction Control Register	00_H
DP1H	**b**	$F106_H$	**E**	83_H	P1H Direction Control Register	00_H
DP2	**b**	$FFC2_H$		$E1_H$	Port 2 Direction Control Register	0000_H
DP3	**b**	$FFC6_H$		$E3_H$	Port 3 Direction Control Register	0000_H
DP4	**b**	$FFCA_H$		$E5_H$	Port 4 Direction Control Register	00_H
DP6	**b**	$FFCE_H$		$E7_H$	Port 6 Direction Control Register	00_H
DPP0		$FE00_H$		00_H	CPU Data Page Pointer 0 Register (10 bits)	0000_H
DPP1		$FE02_H$		01_H	CPU Data Page Pointer 1 Register (10 bits)	0001_H
DPP2		$FE04_H$		02_H	CPU Data Page Pointer 2 Register (10 bits)	0002_H
DPP3		$FE06_H$		03_H	CPU Data Page Pointer 3 Register (10 bits)	0003_H
EXICON	**b**	$F1C0_H$	**E**	$E0_H$	External Interrupt Control Register	0000_H
MDC	**b**	$FF0E_H$		87_H	CPU Multiply Divide Control Register	0000_H
MDH		$FE0C_H$		06_H	CPU Multiply Divide Register – High Word	0000_H
MDL		$FE0E_H$		07_H	CPU Multiply Divide Register – Low Word	0000_H
ODP2	**b**	$F1C2_H$	**E**	$E1_H$	Port 2 Open Drain Control Register	0000_H
ODP3	**b**	$F1C6_H$	**E**	$E3_H$	Port 3 Open Drain Control Register	0000_H
ODP6	**b**	$F1CE_H$	**E**	$E7_H$	Port 6 Open Drain Control Register	00_H
ONES		$FF1E_H$		$8F_H$	Constant Value 1's Register (read only)	$FFFF_H$
P0L	**b**	$FF00_H$		80_H	Port 0 Low Register (Lower half of PORT0)	00_H
P0H	**b**	$FF02_H$		81_H	Port 0 High Register (Upper half of PORT0)	00_H
P1L	**b**	$FF04_H$		82_H	Port 1 Low Register (Lower half of PORT1)	00_H
P1H	**b**	$FF06_H$		83_H	Port 1 High Register (Upper half of PORT1)	00_H
P2	**b**	$FFC0_H$		$E0_H$	Port 2 Register	0000_H
P3	**b**	$FFC4_H$		$E2_H$	Port 3 Register	0000_H
P4	**b**	$FFC8_H$		$E4_H$	Port 4 Register (8 bits)	00_H
P5	**b**	$FFA2_H$		$D1_H$	Port 5 Register (read only)	$XXXX_H$

Special Function Registers Overview (cont'd)

Name		Physical Address		8-Bit Address	Description	Reset Value
P6	**b**	$FFCC_H$		$E6_H$	Port 6 Register (8 bits)	00_H
PECC0		$FEC0_H$		60_H	PEC Channel 0 Control Register	0000_H
PECC1		$FEC2_H$		61_H	PEC Channel 1 Control Register	0000_H
PECC2		$FEC4_H$		62_H	PEC Channel 2 Control Register	0000_H
PECC3		$FEC6_H$		63_H	PEC Channel 3 Control Register	0000_H
PECC4		$FEC8_H$		64_H	PEC Channel 4 Control Register	0000_H
PECC5		$FECA_H$		65_H	PEC Channel 5 Control Register	0000_H
PECC6		$FECC_H$		66_H	PEC Channel 6 Control Register	0000_H
PECC7		$FECE_H$		67_H	PEC Channel 7 Control Register	0000_H
PSW	**b**	$FF10_H$		88_H	CPU Program Status Word	0000_H
RP0H	**b**	$F108_H$	**E**	84_H	System Startup Configuration Register (Rd. only)	XX_H
S0BG		$FEB4_H$		$5A_H$	Serial Channel 0 Baud Rate Generator Reload Register	0000_H
S0CON	**b**	$FFB0_H$		$D8_H$	Serial Channel 0 Control Register	0000_H
S0EIC	**b**	$FF70_H$		$B8_H$	Serial Channel 0 Error Interrupt Control Register	0000_H
S0RBUF		$FEB2_H$		59_H	Serial Channel 0 Receive Buffer Register (read only)	XX_H
S0RIC	**b**	$FF6E_H$		$B7_H$	Serial Channel 0 Receive Interrupt Control Register	0000_H
S0TBIC	**b**	$F19C_H$	**E**	CE_H	Serial Channel 0 Transmit Buffer Interrupt Control Register	0000_H
S0TBUF		$FEB0_H$		58_H	Serial Channel 0 Transmit Buffer Register (write only)	00_H
S0TIC	**b**	$FF6C_H$		$B6_H$	Serial Channel 0 Transmit Interrupt Control Register	0000_H
SP		$FE12_H$		09_H	CPU System Stack Pointer Register	$FC00_H$
SSPCON0		$EF00_H$	**X**	---	SSP Control Register 0	0000_H
SSPCON1		$EF02_H$	**X**	---	SSP Control Register 1	0000_H
SSPRTB		$EF04_H$	**X**	---	SSP Receive/Transmit Buffer	$XXXX_H$
SSPTBH		$EF06_H$	**X**	---	SSP Transmit Buffer High	$XXXX_H$
STKOV		$FE14_H$		$0A_H$	CPU Stack Overflow Pointer Register	$FA00_H$

Special Function Registers Overview (cont'd)

Name		Physical Address	8-Bit Address	Description	Reset Value
STKUN		$FE16_H$	$0B_H$	CPU Stack Underflow Pointer Register	$FC00_H$
SYSCON	**b**	$FF12_H$	89_H	CPU System Configuration Register	$0XX0_H$ [1]
T2		$FE40_H$	20_H	GPT1 Timer 2 Register	0000_H
T2CON	**b**	$FF40_H$	$A0_H$	GPT1 Timer 2 Control Register	0000_H
T2IC	**b**	$FF60_H$	$B0_H$	GPT1 Timer 2 Interrupt Control Register	0000_H
T3		$FE42_H$	21_H	GPT1 Timer 3 Register	0000_H
T3CON	**b**	$FF42_H$	$A1_H$	GPT1 Timer 3 Control Register	0000_H
T3IC	**b**	$FF62_H$	$B1_H$	GPT1 Timer 3 Interrupt Control Register	0000_H
T4		$FE44_H$	22_H	GPT1 Timer 4 Register	0000_H
T4CON	**b**	$FF44_H$	$A2_H$	GPT1 Timer 4 Control Register	0000_H
T4IC	**b**	$FF64_H$	$B2_H$	GPT1 Timer 4 Interrupt Control Register	0000_H
T5		$FE46_H$	23_H	GPT2 Timer 5 Register	0000_H
T5CON	**b**	$FF46_H$	$A3_H$	GPT2 Timer 5 Control Register	0000_H
T5IC	**b**	$FF66_H$	$B3_H$	GPT2 Timer 5 Interrupt Control Register	0000_H
T6		$FE48_H$	24_H	GPT2 Timer 6 Register	0000_H
T6CON	**b**	$FF48_H$	$A4_H$	GPT2 Timer 6 Control Register	0000_H
T6IC	**b**	$FF68_H$	$B4_H$	GPT2 Timer 6 Interrupt Control Register	0000_H
TFR	**b**	$FFAC_H$	$D6_H$	Trap Flag Register	0000_H
WDT		$FEAE_H$	57_H	Watchdog Timer Register (read only)	0000_H
WDTCON		$FFAE_H$	$D7_H$	Watchdog Timer Control Register	$000X_H$ [2]
XP1IC	**b**	$F18E_H$ **E**	$C7_H$	SSP Interrupt Control Register	0000_H
XP3IC	**b**	$F19E_H$ **E**	CF_H	PLL/OWD Interrupt Control Register	0000_H
ZEROS	**b**	$FF1C_H$	$8E_H$	Constant Value 0's Register (read only)	0000_H

1) The system configuration is selected during reset.

2) Bit WDTR indicates a watchdog timer triggered reset.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	T_{ST}	-65	150	°C	
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	-0.5	6.5	V	
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	V_{DD}+0.5	V	
Input current on any pin during overload condition		-10	10	mA	
Absolute sum of all input currents during overload condition		-	|100|	mA	
Power dissipation	P_{DISS}	-	1.5	W	

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN}>V_{DD}$ or $V_{IN}<V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the C163-L. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Digital supply voltage	V_{DD}	4.5	5.5	V	Active mode, f_{CPUmax} = 25 MHz
		2.5	5.5	V	PowerDown mode
Reduced digital supply voltage	V_{DD}	2.7	3.6	V	Active mode, f_{CPUmax} = 12 MHz
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	-	±5	mA	Per pin 1) 2)
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	-	50	mA	
Ambient temperature	T_A	0	70	°C	SAB-C163-L...
		-40	85	°C	SAF-C163-L...

1) Overload conditions occur if the standard operatings conditions are exceeded, ie. the voltage on any pin exceeds the specified range (ie. $V_{OV} > V_{DD}$+0.5V, except pin OWE, or $V_{OV} < V_{SS}$-0.5V). The absolute sum of input overload currents on all port pins may not exceed **50 mA**. The supply voltage must remain within the specified limits.

2) Not 100% tested, guaranteed by design characterization.

Note: Operation at reduced supply voltage is defined for the 25 MHz devices (SA*-C163L25F) only.

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C163-L and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the C163-L will provide signals with the respective timing characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the respective timing characteristics to the C163-L.

DC Characteristics (Standard Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Input low voltage	V_{IL}	SR	– 0.5	0.2 V_{DD} – 0.1	V	–
Input high voltage (all except $\overline{RSTIN}$ and XTAL1)	V_{IH}	SR	0.2 V_{DD} + 0.9	V_{DD} + 0.5	V	–
Input high voltage $\overline{RSTIN}$	V_{IH1}	SR	0.6 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage XTAL1	V_{IH2}	SR	0.7 V_{DD}	V_{DD} + 0.5	V	–
Output low voltage (PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	V_{OL}	CC	–	0.45	V	I_{OL} = 2.4 mA
Output low voltage (all other outputs)	V_{OL1}	CC	–	0.45	V	I_{OL1} = 1.6 mA
Output high voltage (PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	V_{OH}	CC	0.9 V_{DD} 2.4	– –	V V	I_{OH} = – 500 µA I_{OH} = – 2.4 mA
Output high voltage [1] (all other outputs)	V_{OH1}	CC	0.9 V_{DD} 2.4	–	V V	I_{OH} = – 250 µA I_{OH} = – 1.6 mA
Input leakage current (Port 5)	I_{OZ1}	CC	–	±200	nA	0.45 V < V_{IN} < V_{DD}
Input leakage current (all other)	I_{OZ2}	CC	–	±500	nA	0.45 V < V_{IN} < V_{DD}
$\overline{RSTIN}$ pullup resistor	R_{RST}	CC	50	250	kΩ	–
Read/Write inactive current [2]	I_{RWH}	[3]	–	-40	µA	V_{OUT} = 2.4 V
Read/Write active current [2]	I_{RWL}	[4]	-500	–	µA	V_{OUT} = V_{OLmax}
ALE inactive current [2]	I_{ALEL}	[3]	–	40	µA	V_{OUT} = V_{OLmax}
ALE active current [2]	I_{ALEH}	[4]	500	–	µA	V_{OUT} = 2.4 V
Port 6 inactive current [2]	I_{P6H}	[3]	–	-40	µA	V_{OUT} = 2.4 V
Port 6 active current [2]	I_{P6L}	[4]	-500	–	µA	V_{OUT} = V_{OL1max}
PORT0 configuration current [2]	I_{P0H}	[3]	–	-10	µA	V_{IN} = V_{IHmin}
	I_{P0L}	[4]	-100	–	µA	V_{IN} = V_{ILmax}
XTAL1 input current	I_{IL}	CC	–	±20	µA	0 V < V_{IN} < V_{DD}
Pin capacitance [5] (digital inputs/outputs)	C_{IO}	CC	–	10	pF	f = 1 MHz T_A = 25 °C
Power supply current (at 5 V supply voltage)	I_{DD5}		–	10 + 3.5 * f_{CPU}	mA	$\overline{RSTIN}$ = V_{IL2} f_{CPU} in [MHz] [6]

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Idle mode supply current (at 5 V supply voltage)	I_{ID5}	–	2 + 1.1 * f_{CPU}	mA	$\overline{RSTIN}$ = V_{IH1} f_{CPU} in [MHz] 6)
Power-down mode supply current (at 5 V supply voltage)	I_{PD5}	–	50	µA	V_{DD} = V_{DDmax} 7)

1) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

2) This specification is only valid during Reset, or during Hold- or Adapt-mode. Port 6 pins are only affected, if they are used for $\overline{CS}$ output and the open drain function is not enabled.

3) The maximum current may be drawn while the respective signal line remains inactive.

4) The minimum current must be drawn in order to drive the respective signal line active.

5) Not 100% tested, guaranteed by design characterization.

6) The supply current is a function of the operating frequency. This dependency is illustrated in the figure below. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

7) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} – 0.1 V to V_{DD}, V_{REF} = 0 V, all outputs (including pins configured as outputs) disconnected.

DC Characteristics (Reduced Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Input low voltage	V_{IL}	SR	– 0.5	0.8	V	–
Input high voltage (all except $\overline{RSTIN}$ and XTAL1)	V_{IH}	SR	1.8	V_{DD} + 0.5	V	–
Input high voltage $\overline{RSTIN}$	V_{IH1}	SR	0.6 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage XTAL1	V_{IH2}	SR	0.7 V_{DD}	V_{DD} + 0.5	V	–
Output low voltage (PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	V_{OL}	CC	–	0.45	V	I_{OL} = 1.6 mA
Output low voltage (all other outputs)	V_{OL1}	CC	–	0.45	V	I_{OL1} = 1.0 mA
Output high voltage (PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	V_{OH}	CC	0.9 V_{DD}	–	V	I_{OH} = – 500 µA
Output high voltage [1] (all other outputs)	V_{OH1}	CC	0.9 V_{DD}	–	V	I_{OH} = – 250 µA
Input leakage current (Port 5)	I_{OZ1}	CC	–	±200	nA	0.45 V < V_{IN} < V_{DD}
Input leakage current (all other)	I_{OZ2}	CC	–	±500	nA	0.45 V < V_{IN} < V_{DD}
$\overline{RSTIN}$ pullup resistor	R_{RST}	CC	50	250	kΩ	–
Read/Write inactive current [2]	I_{RWH}	[3]	–	-10	µA	V_{OUT} = 2.4 V
Read/Write active current [2]	I_{RWL}	[4]	-500	–	µA	V_{OUT} = V_{OLmax}
ALE inactive current [2]	I_{ALEL}	[3]	–	20	µA	V_{OUT} = V_{OLmax}
ALE active current [2]	I_{ALEH}	[4]	500	–	µA	V_{OUT} = 2.4 V
Port 6 inactive current [2]	I_{P6H}	[3]	–	-10	µA	V_{OUT} = 2.4 V
Port 6 active current [2]	I_{P6L}	[4]	-500	–	µA	V_{OUT} = V_{OL1max}
PORT0 configuration current [2]	I_{P0H}	[3]	–	-5	µA	V_{IN} = V_{IHmin}
	I_{P0L}	[4]	-100	–	µA	V_{IN} = V_{ILmax}
XTAL1 input current	I_{IL}	CC	–	±20	µA	0 V < V_{IN} < V_{DD}
Pin capacitance [5] (digital inputs/outputs)	C_{IO}	CC	–	10	pF	f = 1 MHz T_A = 25 °C
Power supply current (at 3 V supply voltage)	I_{DD3}		–	10 + 1.5 * f_{CPU}	mA	$\overline{RSTIN}$ = V_{IL2} f_{CPU} in [MHz] [6]

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Idle mode supply current (at 3 V supply voltage)	I_{ID3}	–	2 + 0.7 * f_{CPU}	mA	$\overline{RSTIN}$ = V_{IH1} f_{CPU} in [MHz] 6)
Power-down mode supply current (at 3 V supply voltage)	I_{PD3}	–	30	µA	V_{DD} = V_{DDmax} 7)

1) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

2) This specification is only valid during Reset, or during Hold- or Adapt-mode. Port 6 pins are only affected, if they are used for $\overline{CS}$ output and the open drain function is not enabled.

3) The maximum current may be drawn while the respective signal line remains inactive.

4) The minimum current must be drawn in order to drive the respective signal line active.

5) Not 100% tested, guaranteed by design characterization.

6) The supply current is a function of the operating frequency. This dependency is illustrated in the figure below. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

7) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} – 0.1 V to V_{DD}, V_{REF} = 0 V, all outputs (including pins configured as outputs) disconnected.

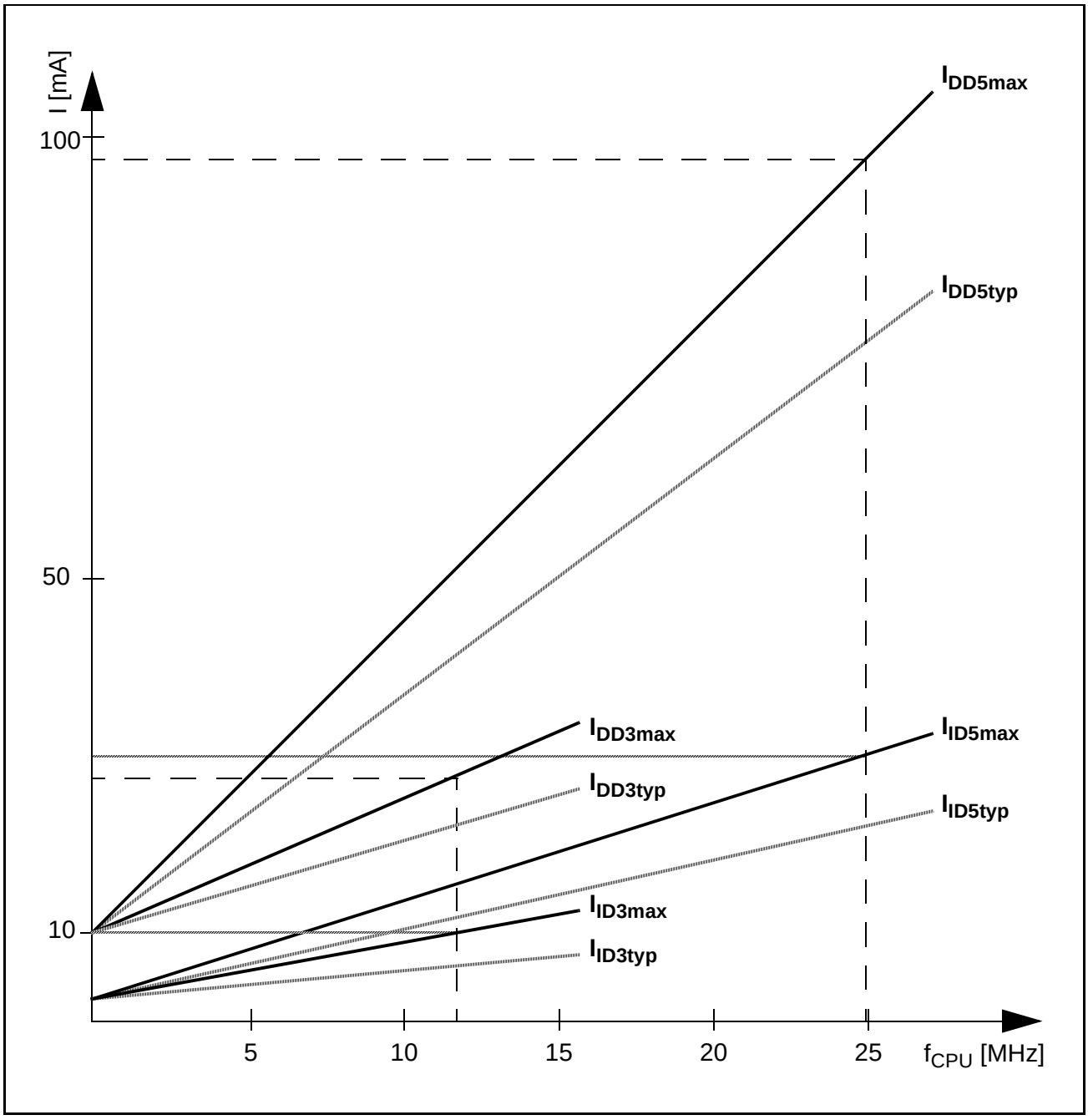
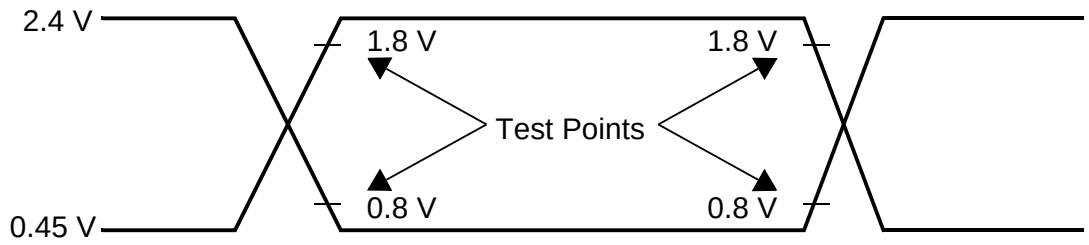


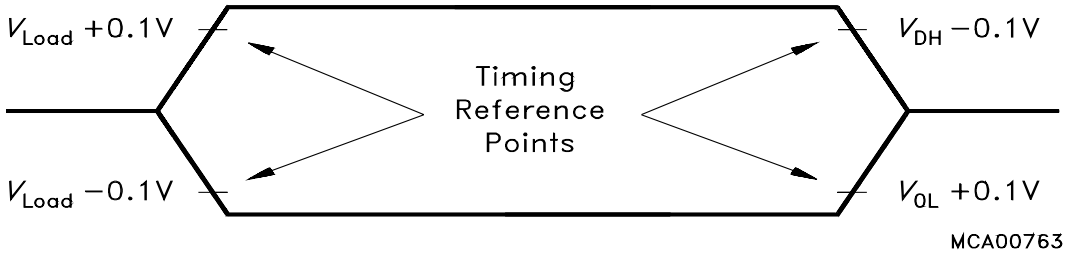
Figure 7
Supply/Idle Current as a Function of Operating Frequency

Testing Waveforms



AC inputs during testing are driven at 2.4 V for a logic ‘1’ and 0.45 V for a logic ‘0’.
Timing measurements are made at V_{IH} min for a logic ‘1’ and V_{IL} max for a logic ‘0’.

Figure 8
Input Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20 mA).

Figure 9
Float Waveforms

AC Characteristics
Definition of Internal Timing

The internal operation of the C163-L is controlled by the internal CPU clock f_{CPU}. Both edges of the CPU clock can trigger internal (eg. pipeline) or external (eg. bus cycles) operations.

The specification of the external timing (AC Characteristics) therefore depends on the time between two consecutive edges of the CPU clock, called “TCL” (see figure below).

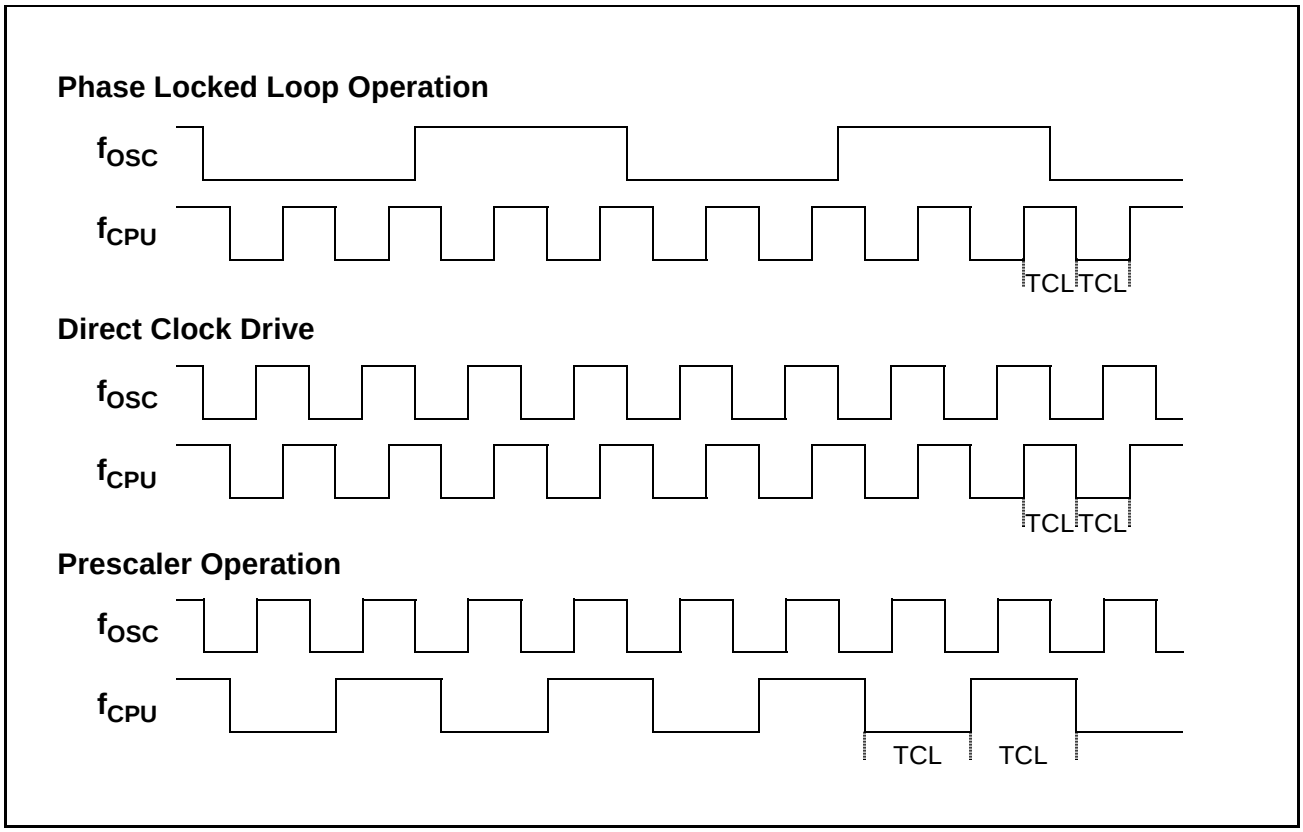


Figure 10
Generation Mechanisms for the CPU Clock

The CPU clock signal can be generated via different mechanisms. The duration of TCLs and their variation (and also the derived external timing) depends on the used mechanism to generate f_{CPU}. This influence must be regarded when calculating the timings for the C163-L.

Note: The example for PLL operation shown in the figure above refers to a PLL factor of 4.

The used mechanism to generate the CPU clock is selected during reset via the logic levels on pins P0.15-13 (P0H.7-5).

The table below associates the combinations of these three bits with the respective clock generation mode.

C163-L Clock Generation Modes

P0.15-13 (P0H.7-5)			CPU Frequency $f_{CPU} = f_{OSC} * F$	External Clock Input Range [1]	Notes
1	1	1	f_{osc} * 4	2.5 to 6.25 MHz	Default configuration
1	1	0	f_{osc} * 3	3.33 to 8.33 MHz	
1	0	1	f_{osc} * 2	5 to 12.5 MHz	
1	0	0	f_{osc} * 5	2 to 5 MHz	
0	1	1	f_{osc} * 1	1 to 25 MHz	Direct drive [2]
0	1	0	f_{osc} * 1.5	6.66 to 16.6 MHz	
0	0	1	f_{osc} / 2	2 to 50 MHz	CPU clock via prescaler
0	0	0	f_{osc} * 2.5	4 to 10 MHz	

1) The external clock input range refers to a CPU clock range of 10...25 MHz.

2) The maximum frequency depends on the duty cycle of the external clock signal.
Direct drive is also selected instead of PLL operation if pin OWE = ’0’ in such a case.

Prescaler Operation

When pins P0.15-13 (P0H.7-5) equal ’001’ during reset the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.
The frequency of f_{CPU} is half the frequency of f_{OSC} and the high and low time of f_{CPU} (ie. the duration of an individual TCL) is defined by the period of the input clock f_{OSC}.

The timings listed in the AC Characteristics that refer to TCLs therefore can be calculated using the period of f_{OSC} for any TCL.

Direct Drive

When pins P0.15-13 (P0H.7-5) equal ’011’ during reset the on-chip phase locked loop is disabled and the CPU clock is directly driven from the internal oscillator with the input clock signal.
The frequency of f_{CPU} directly follows the frequency of f_{OSC} so the high and low time of f_{CPU} (ie. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{OSC}.

The timings listed below that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances. This minimum value can be calculated via the following formula:

$$TCL_{min} = 1/f_{OSC} * DC_{min} \qquad \text{(DC = duty cycle)}$$

For two consecutive TCLs the deviation caused by the duty cycle of f_{OSC} is compensated so the duration of 2TCL is always $1/f_{OSC}$. The minimum value TCL_{min} therefore has to be used only once for timings that require an odd number of TCLs (1,3,...). Timings that require an even number of TCLs (2,4,...) may use the formula $2TCL = 1/f_{OSC}$.

Note: The address float timings in Multiplexed bus mode (t_{11} and t_{45}) use the maximum duration of TCL ($TCL_{max} = 1/f_{OSC} * DC_{max}$) instead of TCL_{min}.

Phase Locked Loop

For all other combinations of pins P0.15-13 (P0H.7-5) during reset the on-chip phase locked loop is enabled and provides the CPU clock (see table above). The PLL multiplies the input frequency by the factor **F** which is selected via the combination of pins P0.15-13 (i.e. $f_{CPU} = f_{OSC} * \mathbf{F}$). With every **F**'th transition of f_{OSC} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothely, i.e. the CPU clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{OSC}. The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCLs.

The timings listed in the AC Characteristics that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances.

The actual minimum value for TCL depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCL is lower than for one single TCL (see formula and figure below).
For a period of $\boldsymbol{N} * TCL$ the minimum value is computed using the corresponding deviation $D_{\boldsymbol{N}}$:

$(\boldsymbol{N} * TCL)_{min} = \boldsymbol{N} * TCL_{NOM} - D_{\boldsymbol{N}}$ $\quad D_{\boldsymbol{N}}\,[ns] = \pm(13.3 + \boldsymbol{N}*6.3) / f_{CPU}\,[MHz]$,
where $\boldsymbol{N}$ = number of consecutive TCLs and $1 \le \boldsymbol{N} \le 40$.

So for a period of 3 TCLs @ 25 MHz (i.e. $\boldsymbol{N} = 3$): $D_{\boldsymbol{3}} = (13.3 + \boldsymbol{3} * 6.3) / 25 = 1.288$ ns,
and $(3TCL)_{min} = 3TCL_{NOM} - 1.288$ ns = 58.7 ns (@ f_{CPU} = 25 MHz).

This is especially important for bus cycles using waitstates and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is neglectible.

Note: For all periods longer than 40 TCL the N=40 value can be used (see figure below).

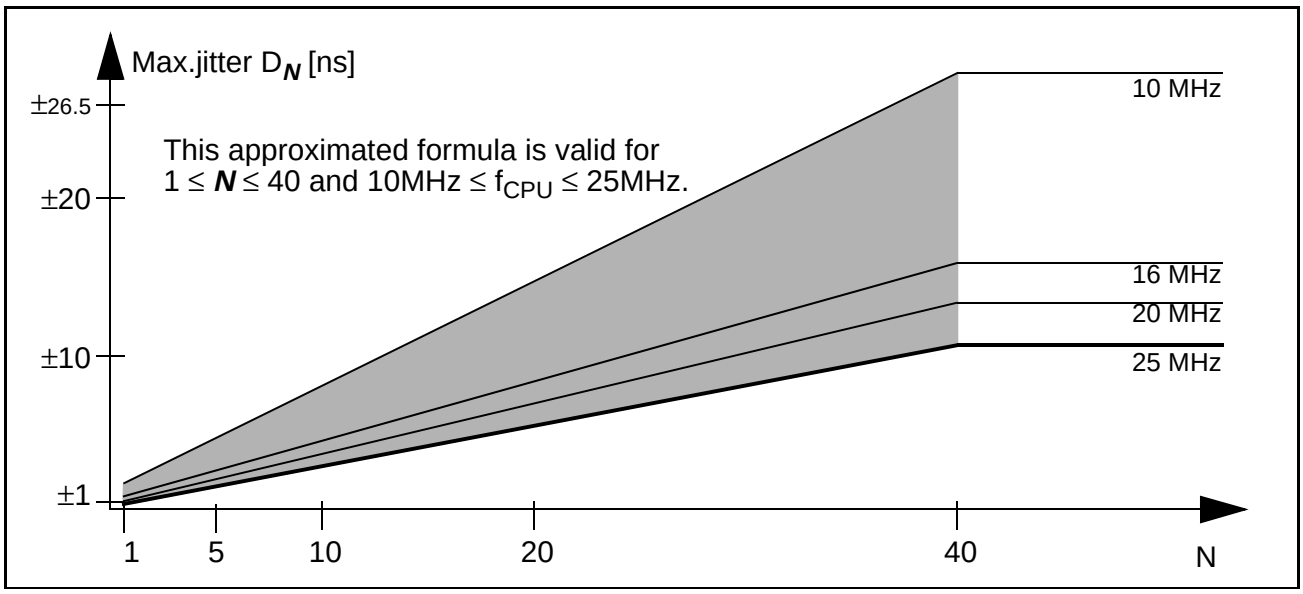


Figure 11
Approximated Maximum Accumulated PLL Jitter

Note: The PLL only operates within the standard supply voltage range of V_{DD} = 4.5 - 5.5 V.

AC Characteristics
External Clock Drive XTAL1 (Standard Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol		Direct Drive 1:1		Prescaler 2:1		PLL 1:N		Unit
			min.	max.	min.	max.	min.	max.	
Oscillator period	t_{OSC}	SR	40	1000	20	500	60 [1]	500 [1]	ns
High time	t_1	SR	18 [2]	–	6 [2]	–	10 [2]	–	ns
Low time	t_2	SR	18 [2]	–	6 [2]	–	10 [2]	–	ns
Rise time	t_3	SR	–	10 [2]	–	6 [2]	–	10 [2]	ns
Fall time	t_4	SR	–	10 [2]	–	6 [2]	–	10 [2]	ns

1) The minimum and maximum oscillator periods for PLL operation depend on the selected CPU clock generation mode. Please see respective table above.

2) The clock input signal must reach the defined levels V_{IL} and V_{IH2}.

AC Characteristics
External Clock Drive XTAL1 (Reduced Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol		Direct Drive 1:1		Prescaler 2:1		PLL 1:N		Unit
			min.	max.	min.	max.	min.	max.	
Oscillator period	t_{OSC}	SR	83	1000	42	500	–	–	ns
High time	t_1	SR	36[1]	–	10 [1]	–	–	–	ns
Low time	t_2	SR	36 [1]	–	10 [1]	–	–	–	ns
Rise time	t_3	SR	–	10 [1]	–	6 [1]	–	–	ns
Fall time	t_4	SR	–	10 [1]	–	6 [1]	–	–	ns

1) The clock input signal must reach the defined levels V_{IL} and V_{IH2}.

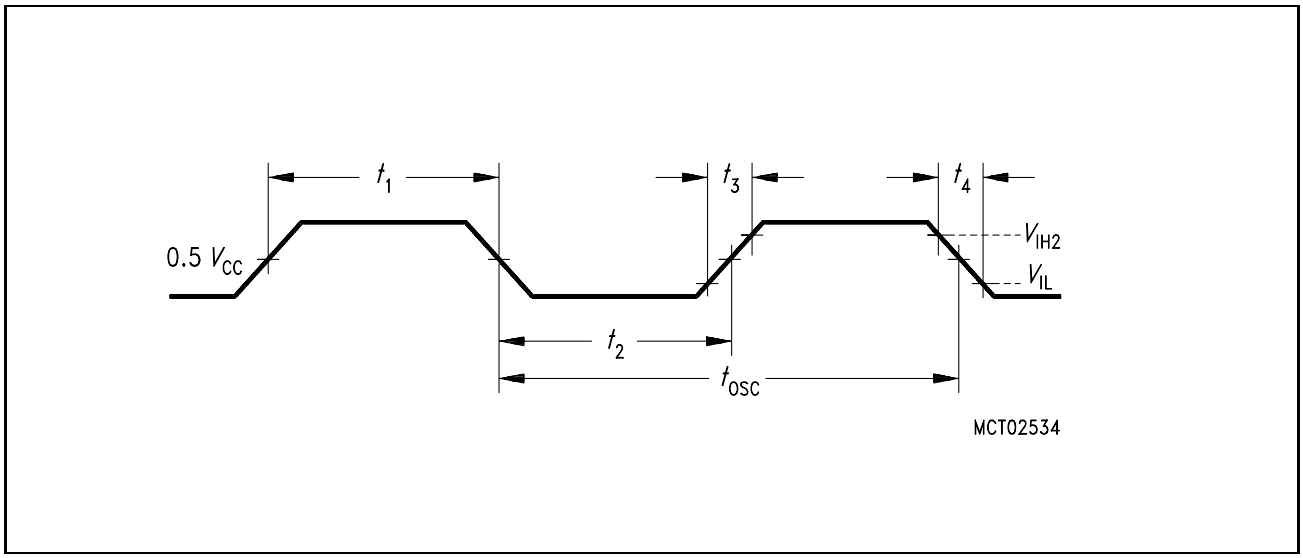


Figure 12
External Clock Drive XTAL1

Memory Cycle Variables

The timing tables below use three variables which are derived from the BUSCONx registers and represent the special characteristics of the programmed memory cycle. The following table describes, how these variables are to be computed.

Description	Symbol	Values
ALE Extension	t_A	TCL * <ALECTL>
Memory Cycle Time Waitstates	t_C	2TCL * (15 - <MCTC>)
Memory Tristate Time	t_F	2TCL * (1 - <MTTC>)

AC Characteristics
Multiplexed Bus (Standard Supply Voltage Range)

(Operating Conditions apply, C_L = 100 pF)
ALE cycle time = 6 TCL + 2t_A + t_C + t_F (120 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
Address setup to ALE	t_6	CC	4 + t_A	–	TCL - 16 + t_A	–	ns
Address hold after ALE	t_7	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	-10 + t_A	–	-10 + t_A	–	ns
Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_{10}	CC	–	6	–	6	ns
Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_{11}	CC	–	26	–	TCL + 6	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	20 + t_C	–	2TCL - 20 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	40 + t_C	–	3TCL - 20 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	50 + 2t_A + t_C	–	4TCL - 30 + 2t_A + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$	t_{19}	SR	–	26 + t_F	–	2TCL - 14 + t_F	ns
Data valid to $\overline{WR}$	t_{22}	CC	20 + t_C	–	2TCL - 20 + t_C	–	ns
Data hold after $\overline{WR}$	t_{23}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{25}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
Address hold after $\overline{RD}$, $\overline{WR}$	t_{27}	CC	26 + t_F	–	2TCL - 14 + t_F	–	ns
ALE falling edge to $\overline{CS}$	t_{38}	CC	-4 - t_A	10 - t_A	-4 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In	t_{39}	SR	–	40 + t_C + 2t_A	–	3TCL - 20 + t_C + 2t_A	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	t_{40}	CC	46 + t_F	–	3TCL - 14 + t_F	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{42}	CC	16 + t_A	–	TCL - 4 + t_A	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{43}	CC	-4 + t_A	–	-4 + t_A	–	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{44}	CC	–	0	–	0	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{45}	CC	–	20	–	TCL	ns
$\overline{RdCS}$ to Valid Data In (with RW delay)	t_{46}	SR	–	16 + t_C	–	2TCL - 24 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW delay)	t_{47}	SR	–	36 + t_C	–	3TCL - 24 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW delay)	t_{48}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW delay)	t_{49}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
Data valid to $\overline{WrCS}$	t_{50}	CC	26 + t_C	–	2TCL - 14 + t_C	–	ns
Data hold after $\overline{RdCS}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{RdCS}$	t_{52}	SR	–	20 + t_F	–	2TCL - 20 + t_F	ns
Address hold after $\overline{RdCS}$, $\overline{WrCS}$	t_{54}	CC	20 + t_F	–	2TCL - 20 + t_F	–	ns
Data hold after $\overline{WrCS}$	t_{56}	CC	20 + t_F	–	2TCL - 20 + t_F	–	ns

AC Characteristics
Multiplexed Bus (Reduced Supply Voltage Range)

(Operating Conditions apply, C_L = 100 pF)
ALE cycle time = 6 TCL + 2t_A + t_C + t_F (250 ns at 12 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 12 MHz		Variable CPU Clock 1 / 2TCL = 1 to 12 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	22 + t_A	–	TCL - 20 + t_A	–	ns
Address setup to ALE	t_6	CC	12 + t_A	–	TCL - 30 + t_A	–	ns
Address hold after ALE	t_7	CC	32 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	32 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	-10 + t_A	–	-10 + t_A	–	ns
Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_{10}	CC	–	6	–	6	ns
Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_{11}	CC	–	48	–	TCL + 6	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	63 + t_C	–	2TCL - 20 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	105 + t_C	–	3TCL - 20 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	49 + t_C	–	2TCL - 34 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	91 + t_C	–	3TCL - 34 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	93 + t_A + t_C	–	3TCL - 32 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	115 + 2t_A + t_C	–	4TCL - 52 + 2t_A + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$	t_{19}	SR	–	69 + t_F	–	2TCL - 14 + t_F	ns
Data valid to $\overline{WR}$	t_{22}	CC	47 + t_C	–	2TCL - 36 + t_C	–	ns
Data hold after $\overline{WR}$	t_{23}	CC	69 + t_F	–	2TCL - 14 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{25}	CC	69 + t_F	–	2TCL - 14 + t_F	–	ns

Parameter	Symbol		Max. CPU Clock = 12 MHz		Variable CPU Clock 1 / 2TCL = 1 to 12 MHz		Unit
			min.	max.	min.	max.	
Address hold after $\overline{RD}$, $\overline{WR}$	t_{27}	CC	69 + t_F	–	2TCL - 14 + t_F	–	ns
ALE falling edge to $\overline{CS}$	t_{38}	CC	-10 - t_A	10 - t_A	-10 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In	t_{39}	SR	–	89 + t_C + 2t_A	–	3TCL - 36 + t_C+2t_A	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	t_{40}	CC	105 + t_F	–	3TCL - 20 + t_F	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{42}	CC	36 + t_A	–	TCL - 6 + t_A	–	ns
ALE fall. edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{43}	CC	-6 + t_A	–	-6 + t_A	–	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (with RW delay)	t_{44}	CC	–	0	–	0	ns
Address float after $\overline{RdCS}$, $\overline{WrCS}$ (no RW delay)	t_{45}	CC	–	42	–	TCL	ns
$\overline{RdCS}$ to Valid Data In (with RW delay)	t46	SR	–	45 + tC	–	2TCL - 38 + tC	ns
$\overline{RdCS}$ to Valid Data In (no RW delay)	t47	SR	–	87 + tC	–	3TCL - 38 + tC	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW delay)	t_{48}	CC	69 + t_C	–	2TCL - 14 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW delay)	t_{49}	CC	111 + t_C	–	3TCL - 14 + t_C	–	ns
Data valid to $\overline{WrCS}$	t_{50}	CC	53 + t_C	–	2TCL - 30 + t_C	–	ns
Data hold after $\overline{RdCS}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{RdCS}$	t_{52}	SR	–	63 + t_F	–	2TCL - 20 + t_F	ns
Address hold after $\overline{RdCS}$, $\overline{WrCS}$	t_{54}	CC	63 + t_F	–	2TCL - 20 + t_F	–	ns
Data hold after $\overline{WrCS}$	t_{56}	CC	63 + t_F	–	2TCL - 20 + t_F	–	ns

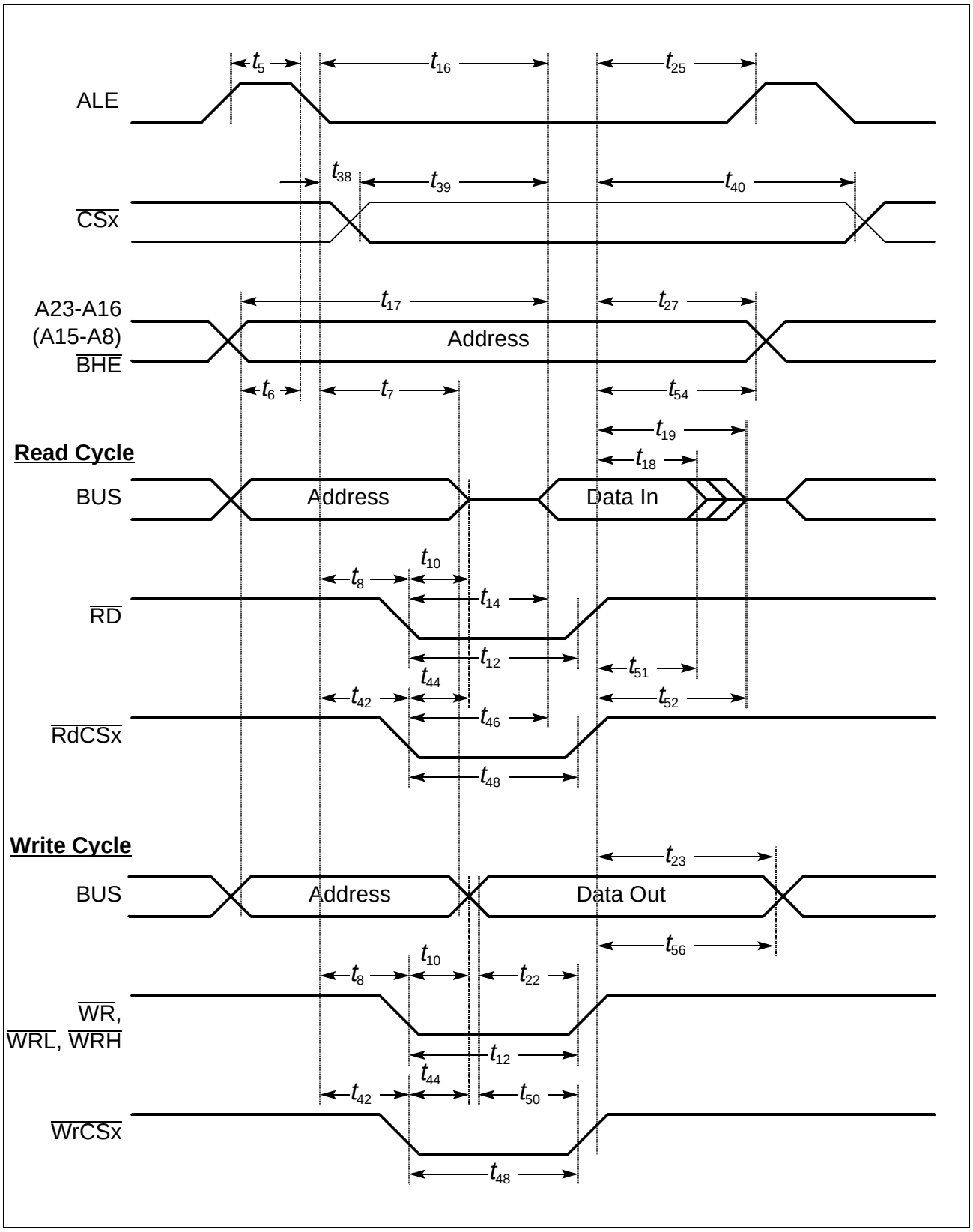


Figure 13-1
External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Normal ALE

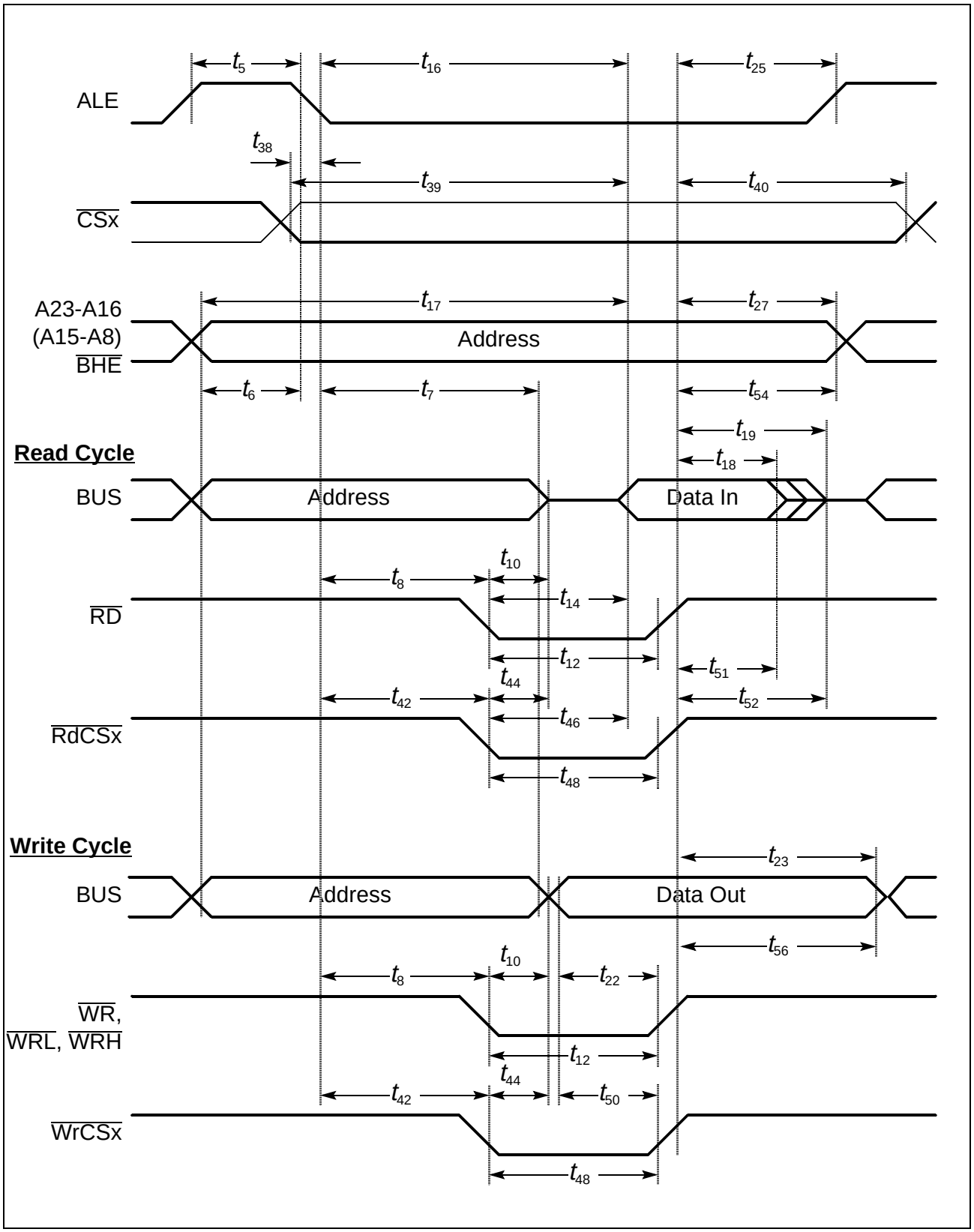


Figure 13-2
External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Extended ALE

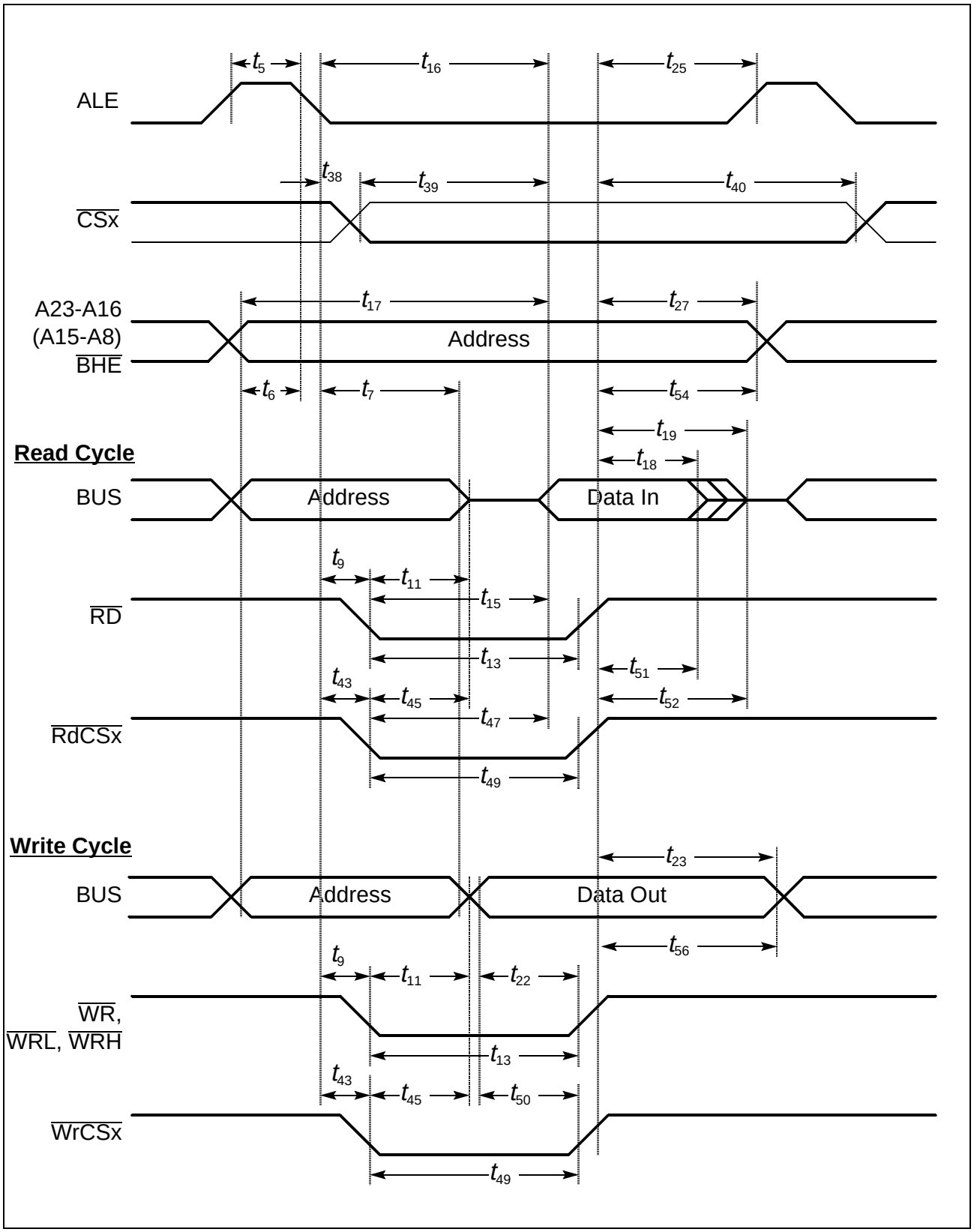


Figure 13-3
External Memory Cycle: Multiplexed Bus, No Read/Write Delay, Normal ALE

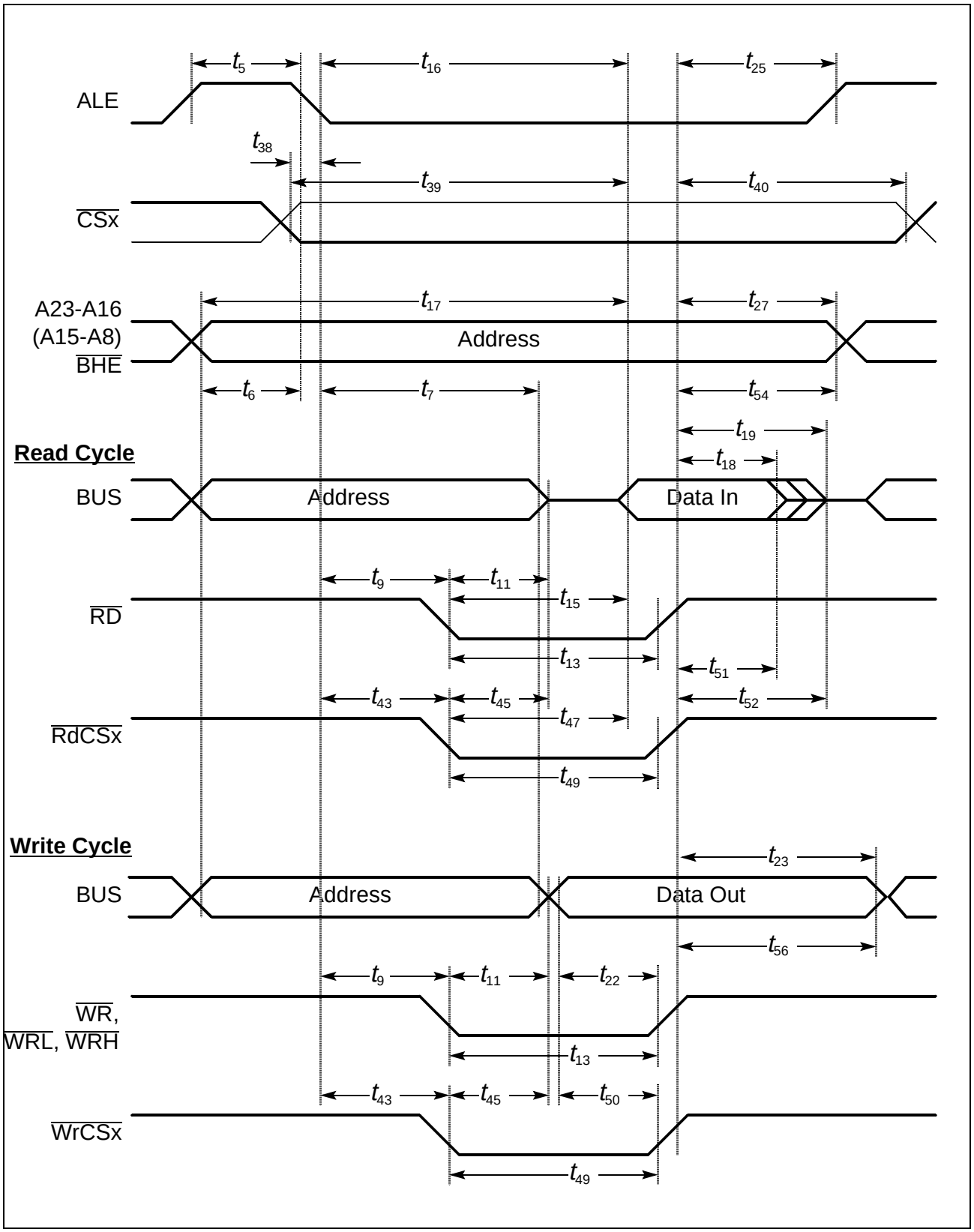


Figure 13-4
External Memory Cycle: Multiplexed Bus, No Read/Write Delay, Extended ALE

AC Characteristics
Demultiplexed Bus (Standard Supply Voltage Range)

(Operating Conditions apply, C_L = 100 pF)
ALE cycle time = 4 TCL + 2t_A + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
Address setup to ALE	t_6	CC	4 + t_A	–	TCL - 16 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	10 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	-10 + t_A	–	-10 + t_A	–	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	20 + t_C	–	2TCL - 20 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	40 + t_C	–	3TCL - 20 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	40 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	50 + 2t_A + t_C	–	4TCL - 30 + 2t_A + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$ rising edge (with RW-delay [1])	t_{20}	SR	–	26 + t_F	–	2TCL - 14 + 2t_A + t_F [1]	ns
Data float after $\overline{RD}$ rising edge (no RW-delay [1])	t_{21}	SR	–	10 + t_F	–	TCL - 10 + 2t_A + t_F [1]	ns
Data valid to $\overline{WR}$	t_{22}	CC	20 + t_C	–	2TCL - 20 + t_C	–	ns
Data hold after $\overline{WR}$	t_{24}	CC	10 + t_F	–	TCL - 10 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{26}	CC	-10 + t_F	–	-10 + t_F	–	ns
Address hold after $\overline{WR}$ [2]	t_{28}	CC	0 + t_F	–	0 + t_F	–	ns
ALE falling edge to $\overline{CS}$	t_{38}	CC	-4 - t_A	10 - t_A	-4 - t_A	10 - t_A	ns

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
$\overline{CS}$ low to Valid Data In	t_{39}	SR	–	40 + t_C + 2t_A	–	3TCL - 20 + t_C+2t_A	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	t_{41}	CC	6 + t_F	–	TCL - 14 + t_F	–	ns
ALE falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW-delay)	t_{42}	CC	16 + t_A	–	TCL - 4 + t_A	–	ns
ALE falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW-delay)	t_{43}	CC	-4 + t_A	–	-4 + t_A	–	ns
$\overline{RdCS}$ to Valid Data In (with RW-delay)	t_{46}	SR	–	16 + t_C	–	2TCL - 24 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW-delay)	t_{47}	SR	–	36 + t_C	–	3TCL - 24 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW-delay)	t_{48}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW-delay)	t_{49}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
Data valid to $\overline{WrCS}$	t_{50}	CC	26 + t_C	–	2TCL - 14 + t_C	–	ns
Data hold after $\overline{RdCS}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{RdCS}$ (with RW-delay)	t_{53}	SR	–	20 + t_F	–	2TCL - 20 + t_F	ns
Data float after $\overline{RdCS}$ (no RW-delay)	t_{68}	SR	–	0 + t_F	–	TCL - 20 + t_F	ns
Address hold after $\overline{RdCS}$, $\overline{WrCS}$	t_{55}	CC	-6 + t_F	–	-6 + t_F	–	ns
Data hold after $\overline{WrCS}$	t_{57}	CC	6 + t_F	–	TCL - 14 + t_F	–	ns

1) RW-delay and t_A refer to the next following bus cycle.

2) Read data are latched with the same clock edge that triggers the address change and the rising $\overline{RD}$ edge. Therefore address changes before the end of $\overline{RD}$ have no impact on read cycles.

AC Characteristics
Demultiplexed Bus (Reduced Supply Voltage Range)

(Operating Conditions apply, C_L = 100 pF)
ALE cycle time = 4 TCL + 2t_A + t_C + t_F (166.7 ns at 12 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 12 MHz		Variable CPU Clock 1 / 2TCL = 1 to 12 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	22 + t_A	–	TCL - 20 + t_A	–	ns
Address setup to ALE	t_6	CC	12 + t_A	–	TCL - 30 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	32 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	-10 + t_A	–	-10 + t_A	–	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	63 + t_C	–	2TCL - 20 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	105 + t_C	–	3TCL - 20 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	49 + tC	–	2TCL - 34 + tC	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	91 + tC	–	3TCL - 34 + tC	ns
ALE low to valid data in	t_{16}	SR	–	93 + tA + tC	–	3TCL - 32 + tA + tC	ns
Address to valid data in	t_{17}	SR	–	115 + 2tA + tC	–	4TCL - 52 + 2tA + tC	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$ rising edge (with RW-delay [1])	t_{20}	SR	–	69 + t_F	–	2TCL - 14 + 2t_A + t_F [1]	ns
Data float after $\overline{RD}$ rising edge (no RW-delay [1])	t_{21}	SR	–	32 + t_F	–	TCL - 10 + 2t_A + t_F [1]	ns
Data valid to $\overline{WR}$	t_{22}	CC	47 + t_C	–	2TCL - 36 + t_C	–	ns
Data hold after $\overline{WR}$	t_{24}	CC	32 + t_F	–	TCL - 10 + t_F	–	ns
ALE rising edge after $\overline{RD}$, $\overline{WR}$	t_{26}	CC	-12 + tF	–	-12 + tF	–	ns
Address hold after $\overline{WR}$ [2]	t_{28}	CC	0 + tF	–	0 + tF	–	ns
ALE falling edge to $\overline{CS}$	t_{38}	CC	-10 - t_A	10 - t_A *)	-10 - t_A	10 - t_A *)	ns

Parameter	Symbol		Max. CPU Clock = 12 MHz		Variable CPU Clock 1 / 2TCL = 1 to 12 MHz		Unit
			min.	max.	min.	max.	
$\overline{CS}$ low to Valid Data In	t_{39}	SR	–	89 + t_C + 2t_A	–	3TCL - 36 + t_C+2t_A	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	t_{41}	CC	22 + t_F	–	TCL - 20 + t_F	–	ns
ALE falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW-delay)	t_{42}	CC	36 + t_A	–	TCL - 6 + t_A	–	ns
ALE falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW-delay)	t_{43}	CC	-6 + t_A	–	-6 + t_A	–	ns
$\overline{RdCS}$ to Valid Data In (with RW-delay)	t_{46}	SR	–	45 + t_C	–	2TCL - 38 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW-delay)	t_{47}	SR	–	87 + t_C	–	3TCL - 38 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW-delay)	t_{48}	CC	69 + t_C	–	2TCL - 14 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW-delay)	t_{49}	CC	111 + t_C	–	3TCL - 14 + t_C	–	ns
Data valid to $\overline{WrCS}$	t_{50}	CC	53 + t_C	–	2TCL - 30 + t_C	–	ns
Data hold after $\overline{RdCS}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{RdCS}$ (with RW-delay)	t_{53}	SR	–	63 + t_F	–	2TCL - 20 + t_F	ns
Data float after $\overline{RdCS}$ (no RW-delay)	t_{68}	SR	–	22 + t_F	–	TCL - 20 + t_F	ns
Address hold after $\overline{RdCS}$, $\overline{WrCS}$	t_{55}	CC	-20 + t_F	–	-20 + t_F	–	ns
Data hold after $\overline{WrCS}$	t_{57}	CC	26 + t_F	–	TCL - 16 + t_F	–	ns

1) RW-delay and t_A refer to the next following bus cycle.

2) Read data are latched with the same clock edge that triggers the address change and the rising $\overline{RD}$ edge. Therefore address changes before the end of $\overline{RD}$ have no impact on read cycles.

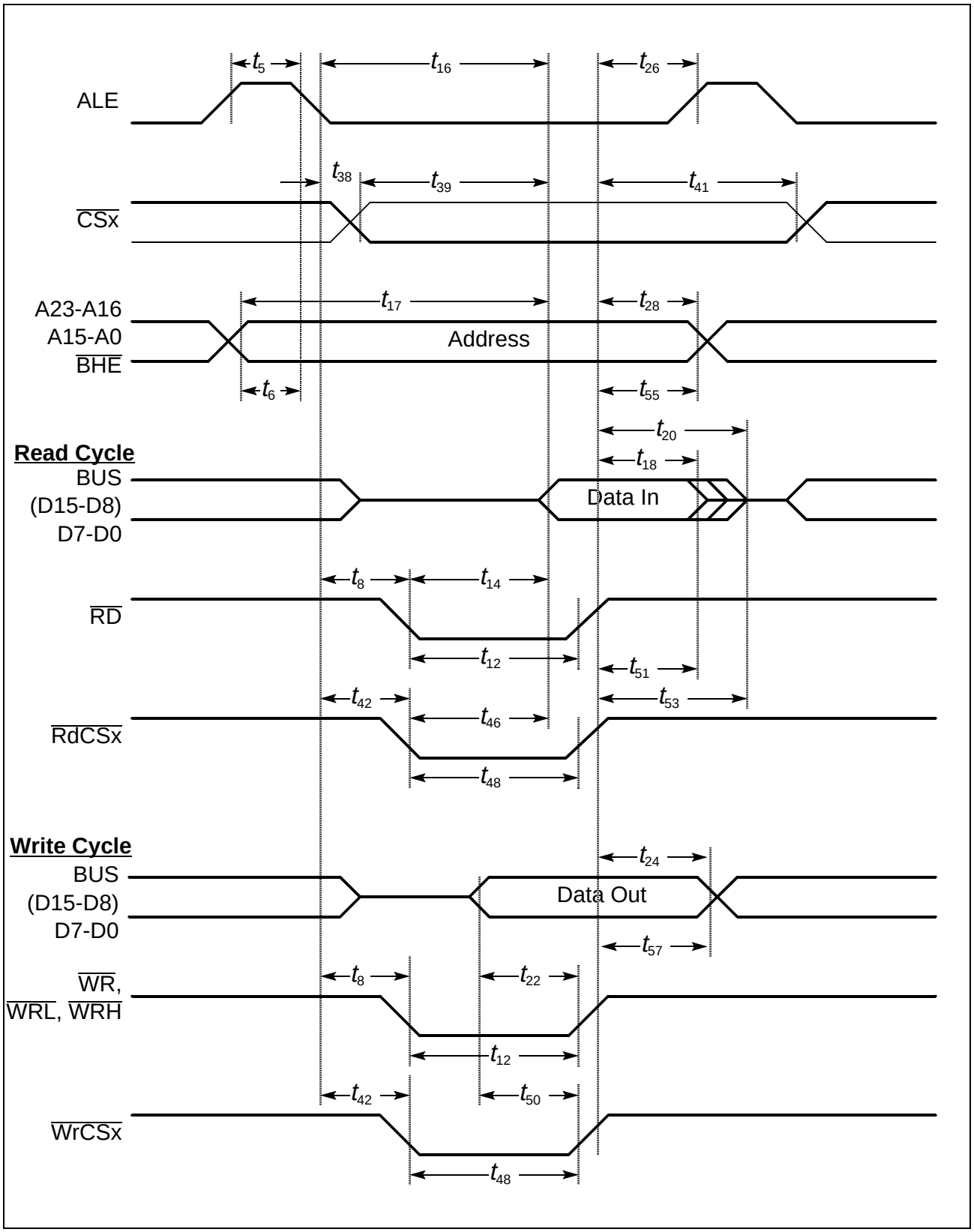


Figure 14-1
External Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Normal ALE

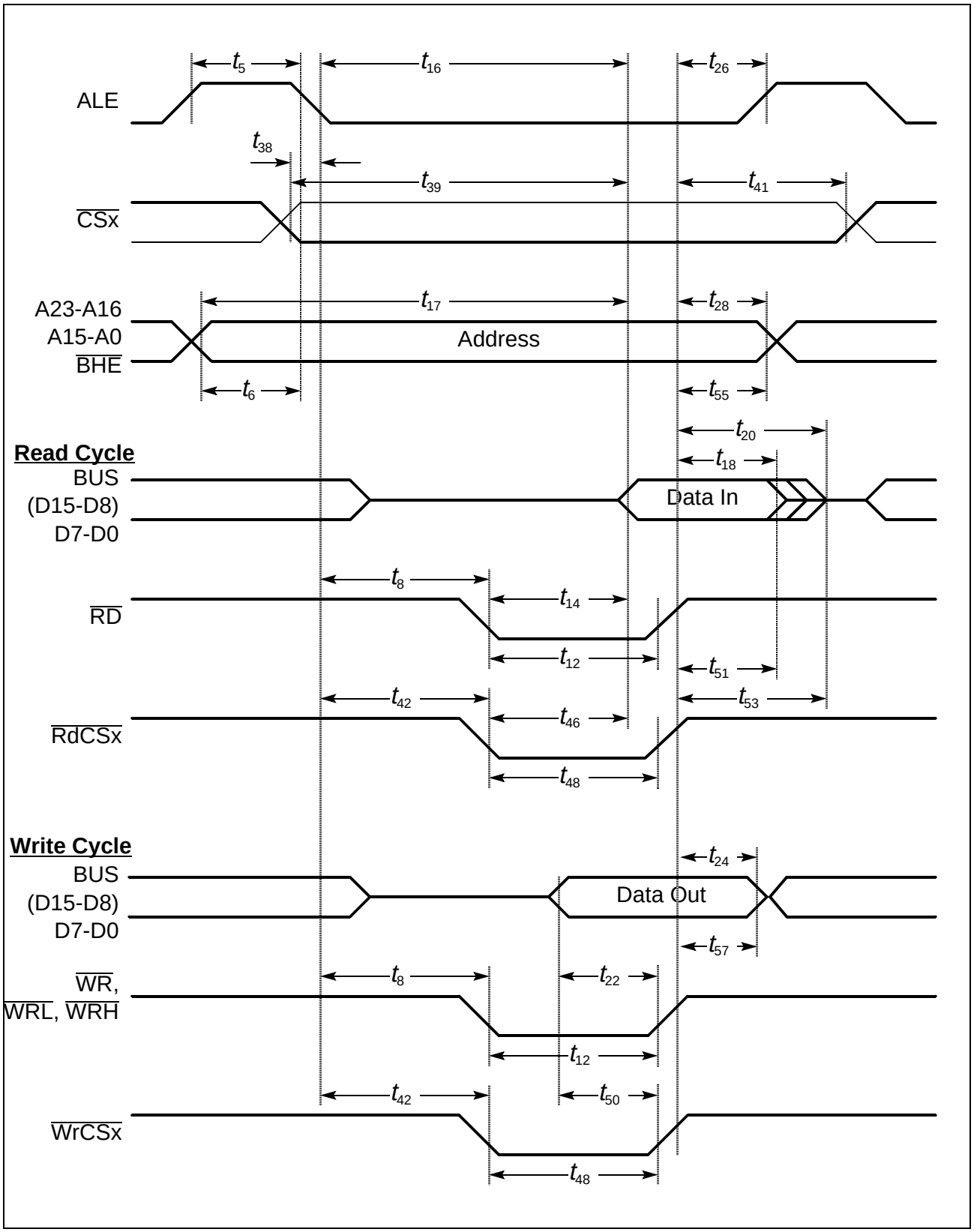


Figure 14-2
External Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Extended ALE

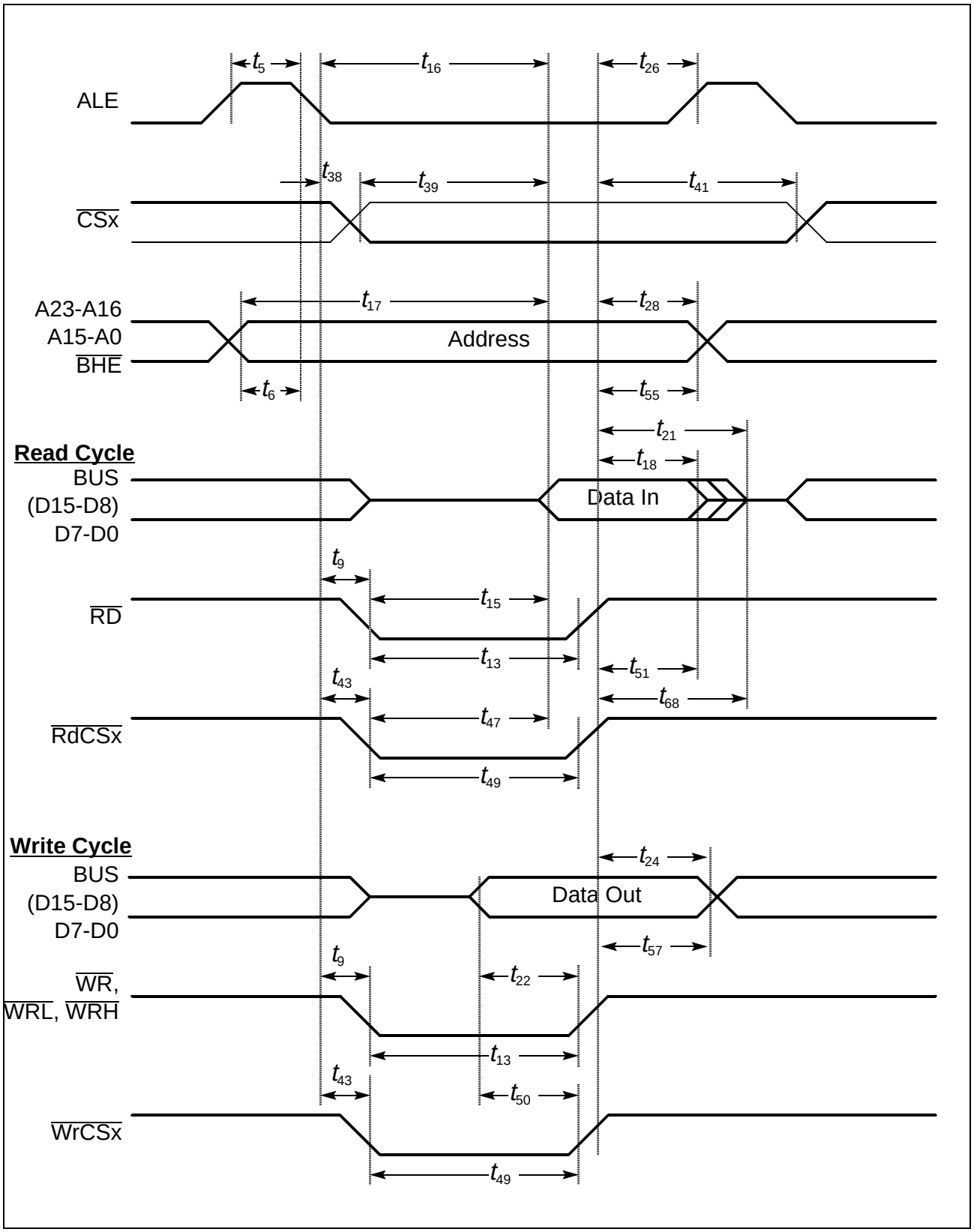


Figure 14-3
External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Normal ALE

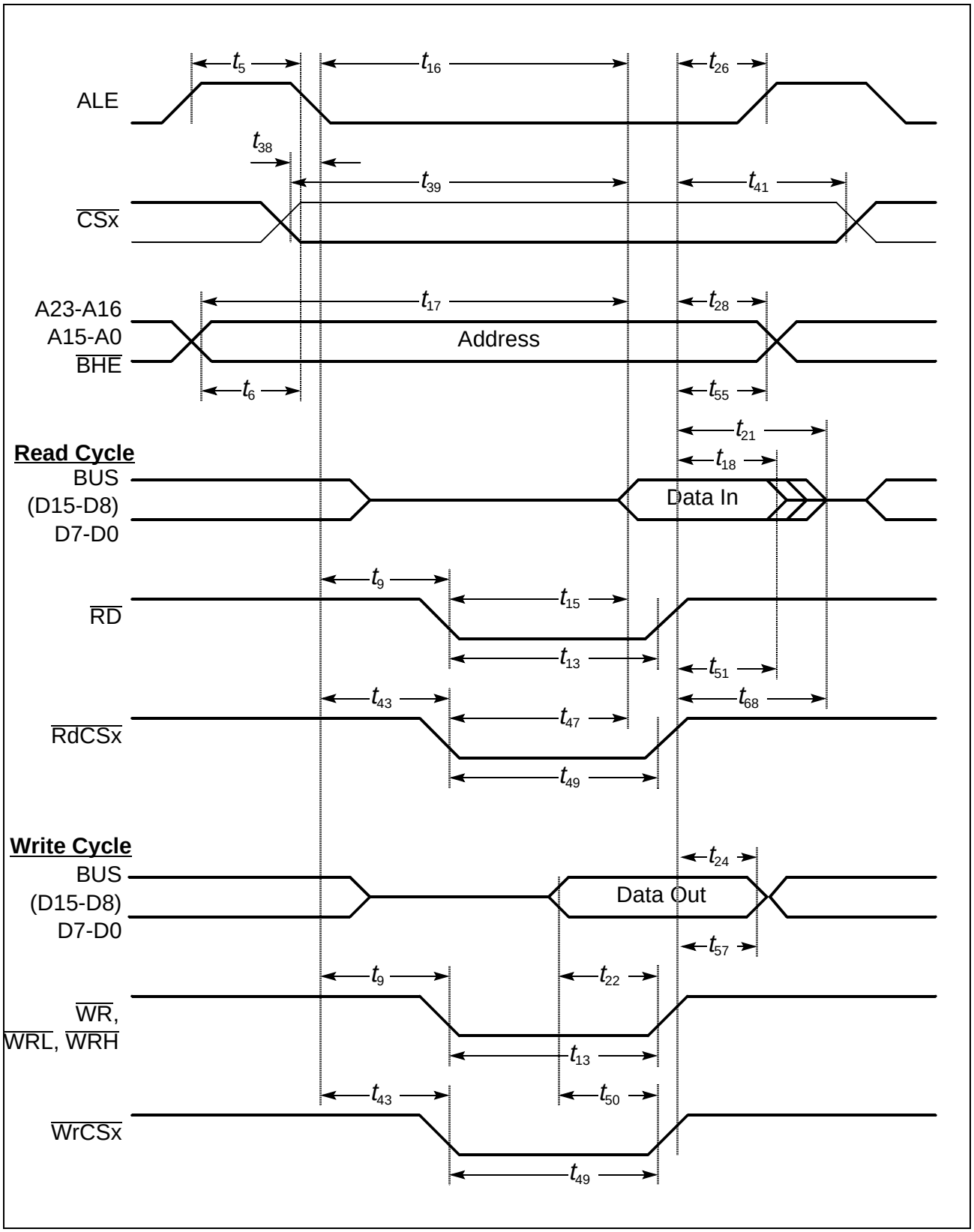


Figure 14-4
External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Extended ALE

AC Characteristics

CLKOUT and $\overline{\text{READY}}$ (Standard Supply Voltage Range)

(Operating Conditions apply, C_L = 100 pF)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
CLKOUT cycle time	t_{29}	CC	40	40	2TCL	2TCL	ns
CLKOUT high time	t_{30}	CC	14	–	TCL – 6	–	ns
CLKOUT low time	t_{31}	CC	10	–	TCL – 10	–	ns
CLKOUT rise time	t_{32}	CC	–	4	–	4	ns
CLKOUT fall time	t_{33}	CC	–	4	–	4	ns
CLKOUT rising edge to ALE falling edge	t_{34}	CC	0 + t_A	10 + t_A	0 + t_A	10 + t_A	ns
Synchronous $\overline{\text{READY}}$ setup time to CLKOUT	t_{35}	SR	14	–	14	–	ns
Synchronous $\overline{\text{READY}}$ hold time after CLKOUT	t_{36}	SR	4	–	4	–	ns
Asynchronous $\overline{\text{READY}}$ low time	t_{37}	SR	54	–	2TCL + 14	–	ns
Asynchronous $\overline{\text{READY}}$ setup time [1]	t_{58}	SR	14	–	14	–	ns
Asynchronous $\overline{\text{READY}}$ hold time [1]	t_{59}	SR	4	–	4	–	ns
Async. $\overline{\text{READY}}$ hold time after $\overline{\text{RD}}$, $\overline{\text{WR}}$ high (Demultiplexed Bus) [2]	t_{60}	SR	0	0 + $2t_A$ + t_C + t_F [2]	0	TCL - 20 + $2t_A$ + t_C + t_F [2]	ns

1) These timings are given for test purposes only, in order to assure recognition at a specific clock edge.

2) Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating $\overline{\text{READY}}$.
The $2t_A$ and t_C refer to the next following bus cycle, t_F refers to the current bus cycle.

AC Characteristics
CLKOUT and $\overline{\text{READY}}$ (Reduced Supply Voltage Range)

(Operating Conditions apply, C_L = 100 pF)

Parameter	Symbol		Max. CPU Clock = 12 MHz		Variable CPU Clock 1 / 2TCL = 1 to 12 MHz		Unit
			min.	max.	min.	max.	
CLKOUT cycle time	t_{29}	CC	83	83	2TCL	2TCL	ns
CLKOUT high time	t_{30}	CC	22	–	TCL – 20	–	ns
CLKOUT low time	t_{31}	CC	26	–	TCL – 16	–	ns
CLKOUT rise time	t_{32}	CC	–	16	–	16	ns
CLKOUT fall time	t_{33}	CC	–	10	–	10	ns
CLKOUT rising edge to ALE falling edge	t_{34}	CC	-6 + t_A	6 + t_A	-6 + t_A	6 + t_A	ns
Synchronous $\overline{\text{READY}}$ setup time to CLKOUT	t_{35}	SR	20	–	20	–	ns
Synchronous $\overline{\text{READY}}$ hold time after CLKOUT	t_{36}	SR	0	–	0	–	ns
Asynchronous $\overline{\text{READY}}$ low time	t_{37}	SR	103	–	2TCL + 20	–	ns
Asynchronous $\overline{\text{READY}}$ setup time [1]	t_{58}	SR	20	–	20	–	ns
Asynchronous $\overline{\text{READY}}$ hold time [1]	t_{59}	SR	0	–	0	–	ns
Async. $\overline{\text{READY}}$ hold time after $\overline{\text{RD}}$, $\overline{\text{WR}}$ high (Demultiplexed Bus) [2]	t_{60}	SR	0	16 + $2t_A$ + t_C + t_F [2]	0	TCL - 26 + $2t_A$ + t_C + t_F [2]	ns

1) These timings are given for test purposes only, in order to assure recognition at a specific clock edge.

2) Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating $\overline{\text{READY}}$.
The $2t_A$ and t_C refer to the next following bus cycle, t_F refers to the current bus cycle.

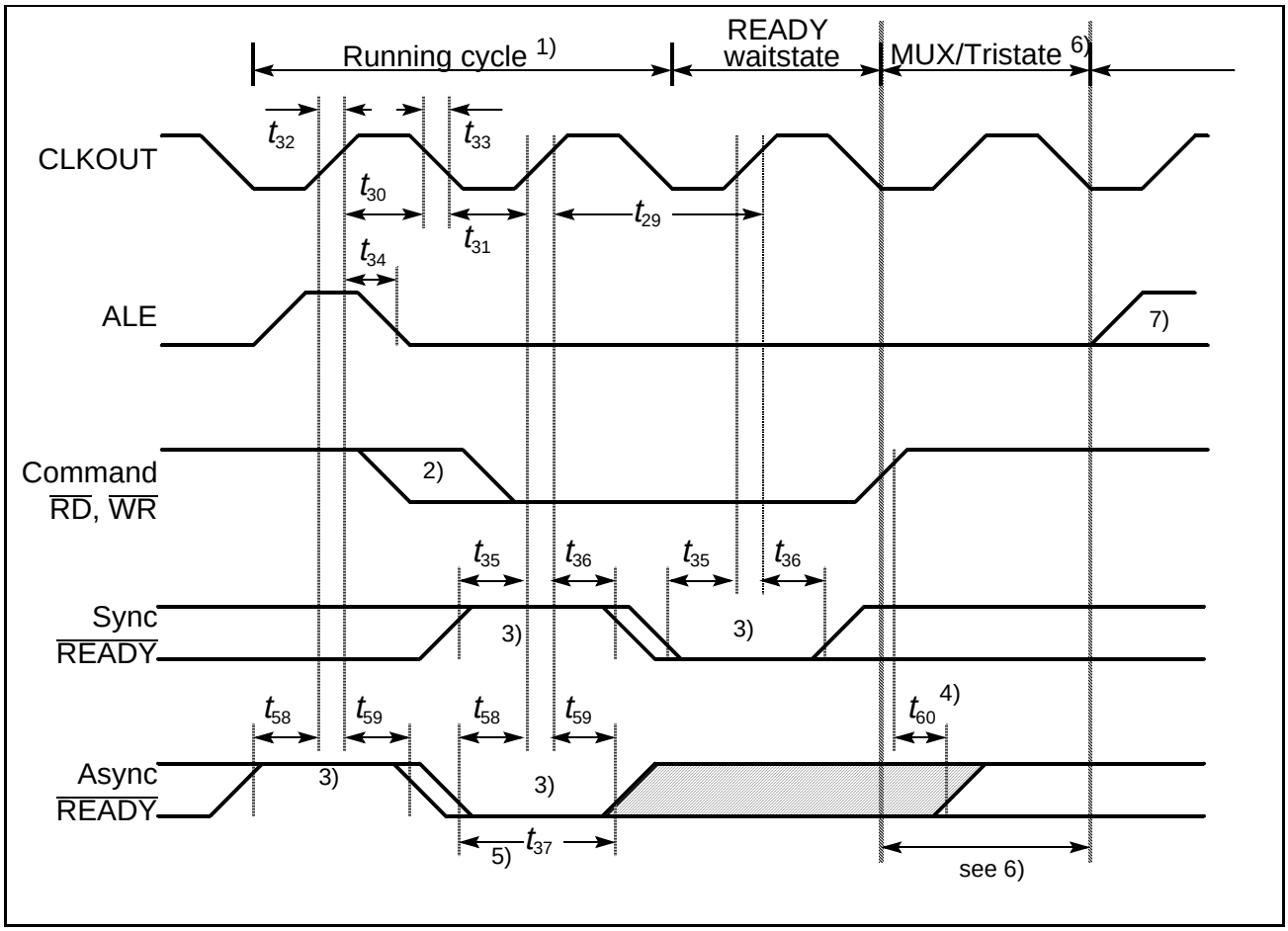


Figure 15
CLKOUT and $\overline{\text{READY}}$

Notes

1) Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).

2) The leading edge of the respective command depends on RW-delay.

3) $\overline{\text{READY}}$ sampled HIGH at this sampling point generates a READY controlled waitstate,
$\overline{\text{READY}}$ sampled LOW at this sampling point terminates the currently running bus cycle.

4) $\overline{\text{READY}}$ may be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).

5) If the Asynchronous $\overline{\text{READY}}$ signal does not fulfill the indicated setup and hold times with respect to CLKOUT (eg. because CLKOUT is not enabled), it must fulfill t_{37} in order to be safely synchronized. This is guaranteed, if $\overline{\text{READY}}$ is removed in reponse to the command (see Note 4)).

6) Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here.
For a multiplexed bus with MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus without MTTC waitstate this delay is zero.

7) The next external bus cycle may start here.

AC Characteristics
External Bus Arbitration (Standard Supply Voltage Range)

(Operating Conditions apply, C_L = 100 pF)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
$\overline{\text{HOLD}}$ input setup time to CLKOUT	t_{61}	SR	20	–	20	–	ns
CLKOUT to $\overline{\text{HLDA}}$ high or $\overline{\text{BREQ}}$ low delay	t_{62}	CC	–	20	–	20	ns
CLKOUT to $\overline{\text{HLDA}}$ low or $\overline{\text{BREQ}}$ high delay	t_{63}	CC	–	20	–	20	ns
$\overline{\text{CSx}}$ release	t_{64}	CC	–	20	–	20	ns
$\overline{\text{CSx}}$ drive	t_{65}	CC	-4	24	-4	24	ns
Other signals release	t_{66}	CC	–	20	–	20	ns
Other signals drive	t_{67}	CC	-4	24	-4	24	ns

AC Characteristics
External Bus Arbitration (Reduced Supply Voltage Range)

(Operating Conditions apply, C_L = 100 pF)

Parameter	Symbol		Max. CPU Clock = 12 MHz		Variable CPU Clock 1 / 2TCL = 1 to 12 MHz		Unit
			min.	max.	min.	max.	
$\overline{\text{HOLD}}$ input setup time to CLKOUT	t_{61}	SR	34	–	34	–	ns
CLKOUT to $\overline{\text{HLDA}}$ high or $\overline{\text{BREQ}}$ low delay	t_{62}	CC	–	24	–	24	ns
CLKOUT to $\overline{\text{HLDA}}$ low or $\overline{\text{BREQ}}$ high delay	t_{63}	CC	–	24	–	24	ns
$\overline{\text{CSx}}$ release	t_{64}	CC	–	20	–	20	ns
$\overline{\text{CSx}}$ drive	t_{65}	CC	-6	30	-6	30	ns
Other signals release	t_{66}	CC	–	20	–	20	ns
Other signals drive	t_{67}	CC	-6	30	-6	30	ns

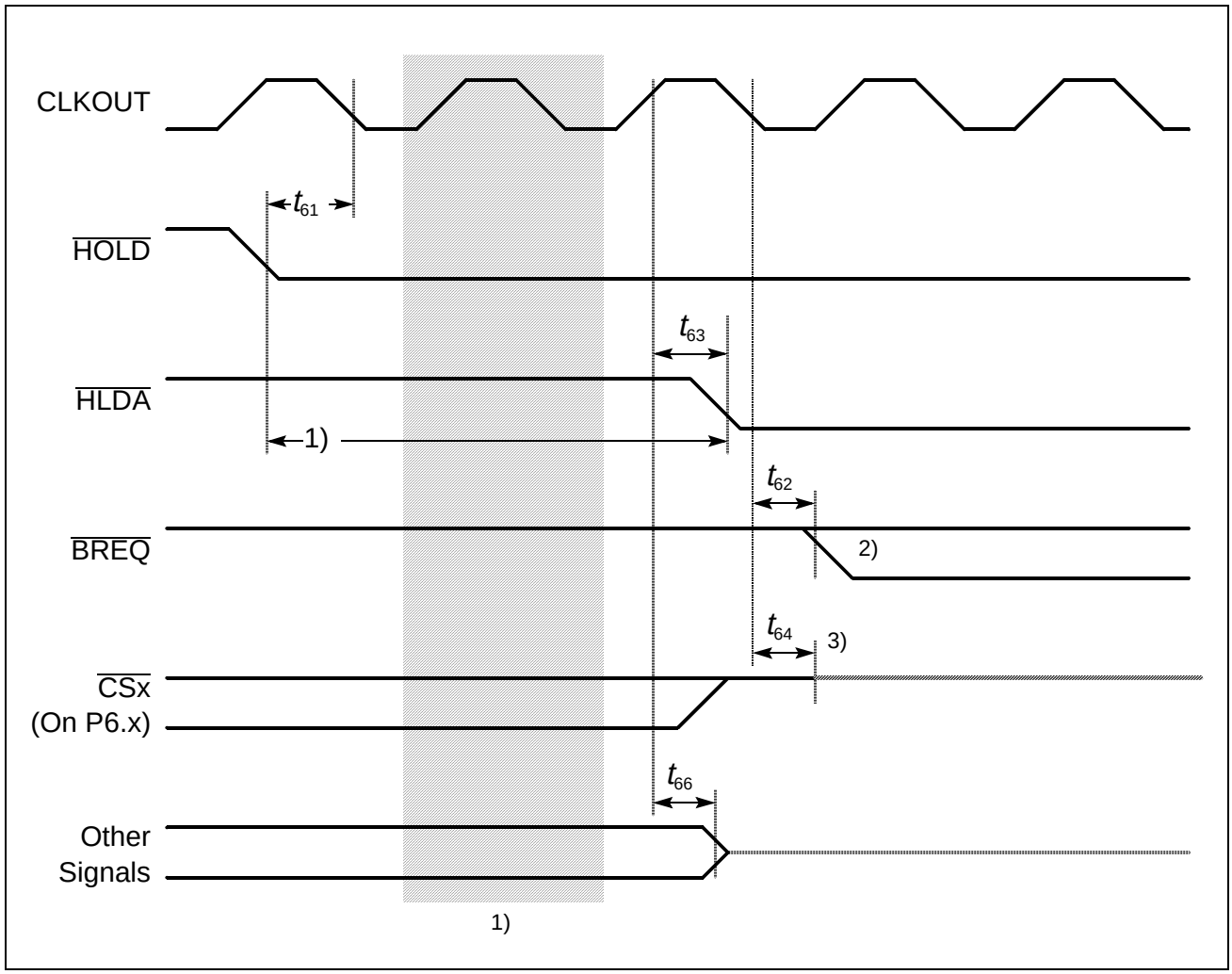


Figure 16
External Bus Arbitration, Releasing the Bus

Notes

1) The C163-L will complete the currently running bus cycle before granting bus access.

2) This is the first possibility for $\overline{\text{BREQ}}$ to get active.

3) The $\overline{\text{CS}}$ outputs will be resistive high (pullup) after t_{64}.

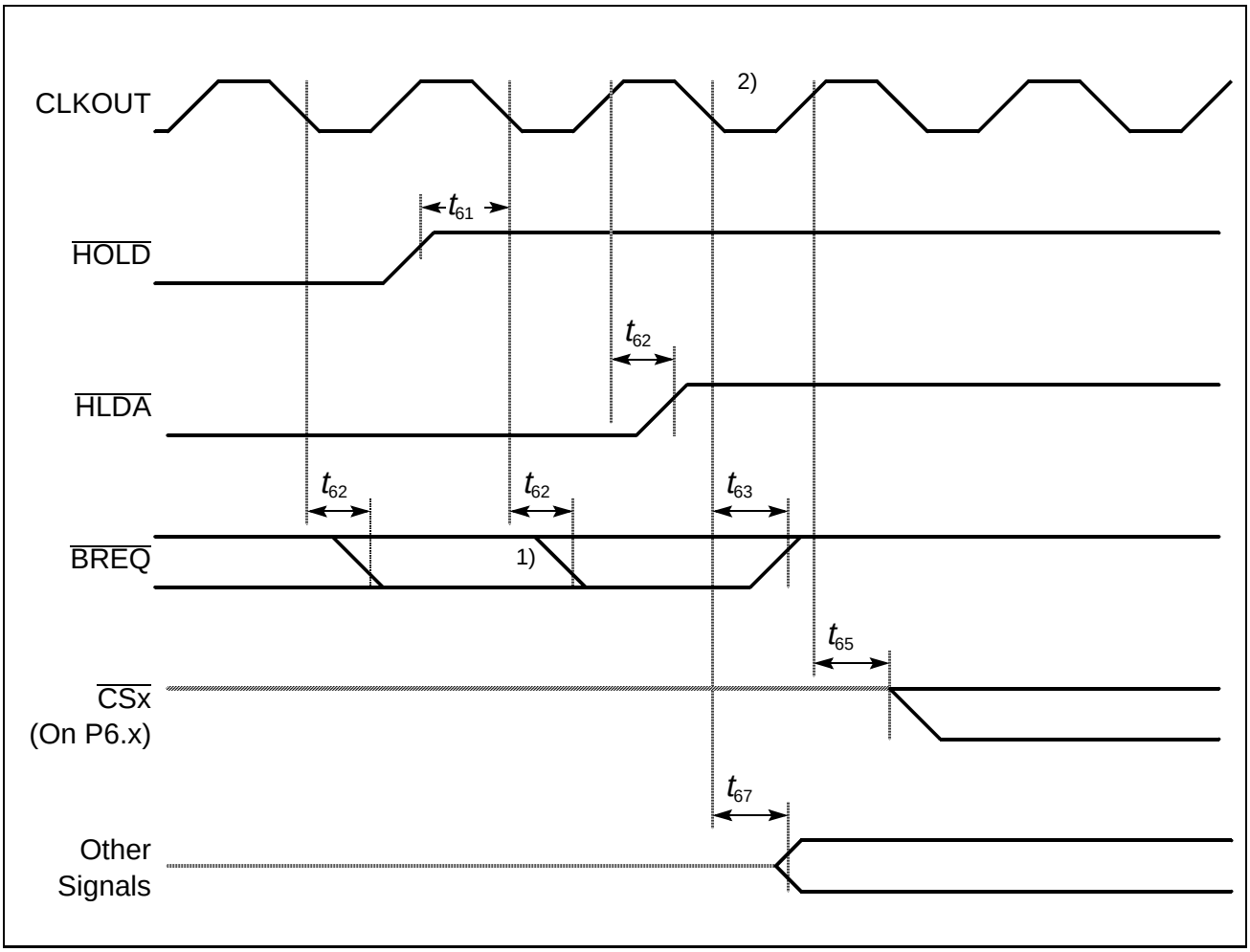


Figure 17
External Bus Arbitration, (Regaining the Bus)

Notes

1) This is the last chance for $\overline{\text{BREQ}}$ to trigger the indicated regain-sequence.
Even if $\overline{\text{BREQ}}$ is activated earlier, the regain-sequence is initiated by $\overline{\text{HOLD}}$ going high.
Please note that $\overline{\text{HOLD}}$ may also be deactivated without the C163-L requesting the bus.

2) The next C163-L driven bus cycle may start here.

AC Characteristics

Synchronous Serial Port Timing (Standard Supply Voltage Range)

(Operating Conditions apply, C_L = 100 pF)

Parameter	Symbol		Max. Baudrate = 12.5 / 10 MBd		Variable Baudrate = 0.5 to 12.5 MBd		Unit
			min.	max.	min.	max.	
SSP clock cycle time	t_{200}	CC	80 / 100	80 / 100	4 TCL	512 TCL	ns
SSP clock high time	t_{201}	CC	30 / 40	– / –	t_{200}/2 - 10	–	ns
SSP clock low time	t_{202}	CC	30 / 40	– / –	t_{200}/2 - 10	–	ns
SSP clock rise time	t_{203}	CC	– / –	6 / 6	–	6	ns
SSP clock fall time	t_{204}	CC	– / –	6 / 6	–	6	ns
CE active before shift edge	t_{205}	CC	30 / 40	– / –	t_{200}/2 - 10	–	ns
CE inactive after latch edge	t_{206}	CC	70 / 90	90 / 110	t_{200} - 10	t_{200} + 10	ns
Write data valid after shift edge	t_{207}	CC	– / –	10 / 10	–	10	ns
Write data hold after shift edge	t_{208}	CC	0 / 0	– / –	0	–	ns
Write data hold after latch edge	t_{209}	CC	34 / 44	46 / 56	t_{200}/2 - 6	t_{200}/2 + 6	ns
Read data active after latch edge	t_{210}	SR	50 / 60	– / –	t_{200}/2 + 10	–	ns
Read data setup time before latch edge	t_{211}	SR	20 / 20	– / –	20	–	ns
Read data hold time after latch edge	t_{212}	SR	0 / 0	– / –	0	–	ns

AC Characteristics

Synchronous Serial Port Timing (Reduced Supply Voltage Range)

(Operating Conditions apply, C_L = 100 pF)

Parameter	Symbol		Max. Baudrate = 6 MBd		Variable Baudrate = 0.5 to 6 MBd		Unit
			min.	max.	min.	max.	
SSP clock cycle time	t_{200}	CC	167	167	4 TCL	512 TCL	ns
SSP clock high time	t_{201}	CC	63	–	t_{200}/2 - 20	–	ns
SSP clock low time	t_{202}	CC	73	–	t_{200}/2 - 10	–	ns
SSP clock rise time	t_{203}	CC	–	14	–	14	ns
SSP clock fall time	t_{204}	CC	–	10	–	10	ns
CE active before shift edge	t_{205}	CC	73	– / –	t_{200}/2 - 10	–	ns
CE inactive after latch edge	t_{206}	CC	147	187	t_{200} - 20	t_{200} + 20	ns
Write data valid after shift edge	t_{207}	CC	– / –	20	–	20	ns
Write data hold after shift edge	t_{208}	CC	-6	–	-6	–	ns
Write data hold after latch edge	t_{209}	CC	63	103	t_{200}/2 - 20	t_{200}/2 + 20	ns
Read data active after latch edge	t_{210}	SR	93	–	t_{200}/2 + 10	–	ns
Read data setup time before latch edge	t_{211}	SR	30	–	30	–	ns
Read data hold time after latch edge	t_{212}	SR	0	–	0	–	ns

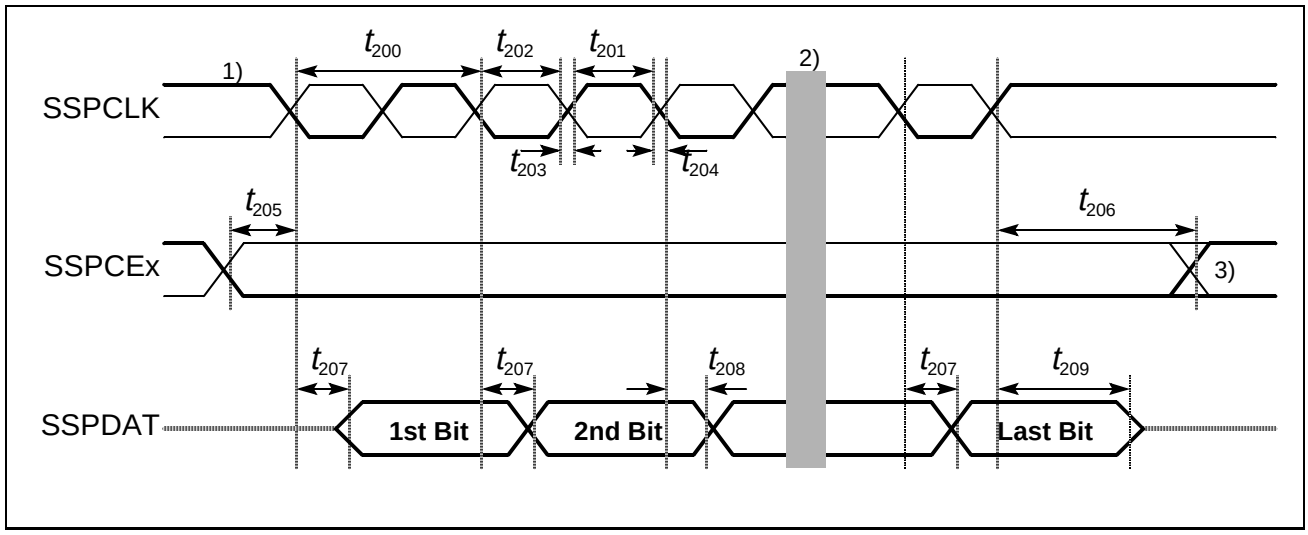


Figure 18
SSP Write Timing

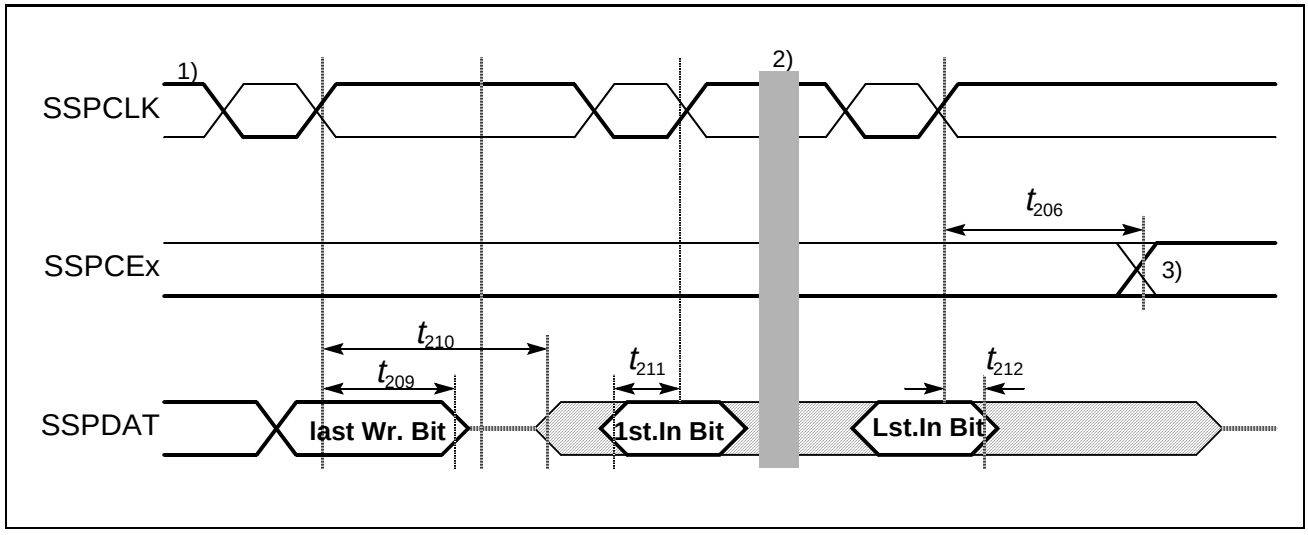


Figure 19
SSP Read Timing

Notes

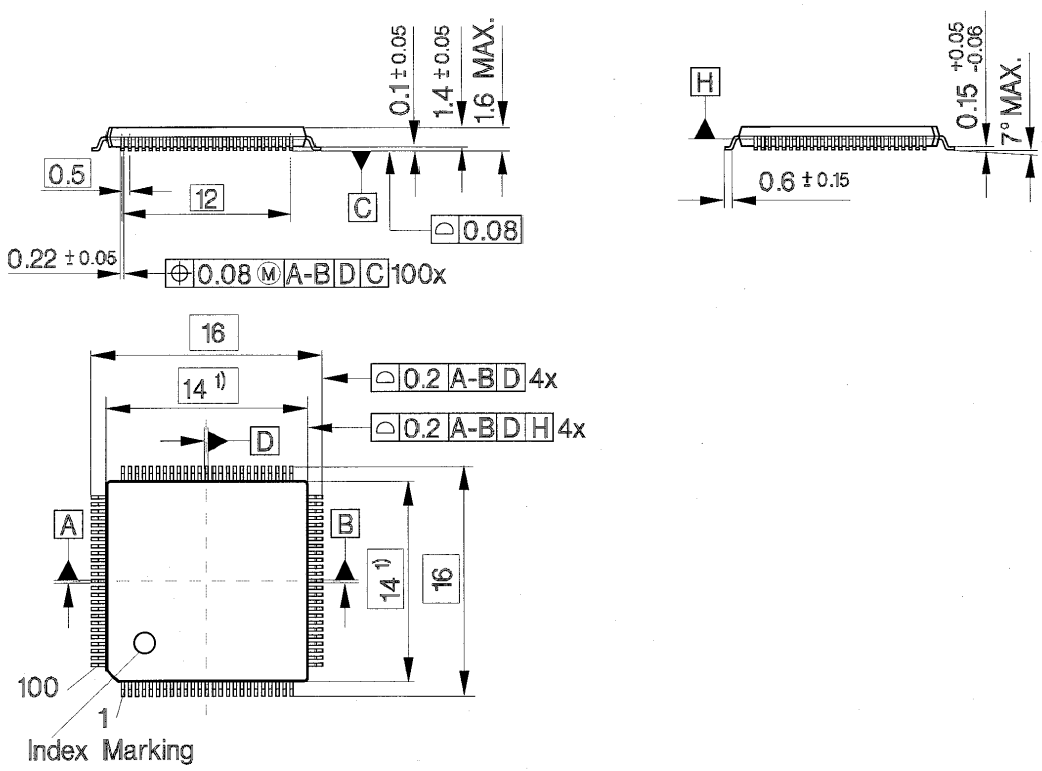
1) The transition of shift and latch edge of SSPCLK is programmable. This figure uses the falling edge as shift edge (drawn bold).

2) The bit timing is repeated for all bits to be transmitted or received.

3) The active level of the chip enable lines is programmable. This figure uses an active low CE (drawn bold). At the end of a transmission or reception the CE signal is disabled in single transfer mode. In continuous transfer mode it remains active.

Package Outlines

Plastic Package, P-TQFP-100-3 (SMD)
(Plastic Thin Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Figure 20

Sorts of Packing

Package outlines for tubes, trays, etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device Dimensions in mm

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