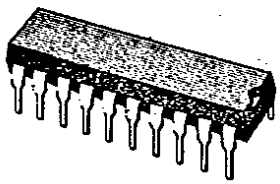
SGS-THOMSON MICROELECTRONICS

T-46-07-11

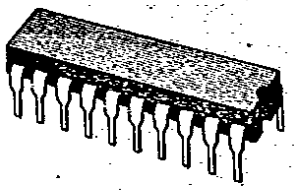
T74LS374

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

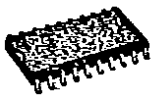
- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERED POSITIVE EDGE-TRIGGERED CLOCK
- 3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS
- HYSTERESIS ON OUTPUT ENABLE INPUT TO IMPROVE NOISE MARGIN
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)



M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS374 D1
T74LS374 B1
T74LS374 C1
T74LS374 M1

DESCRIPTION

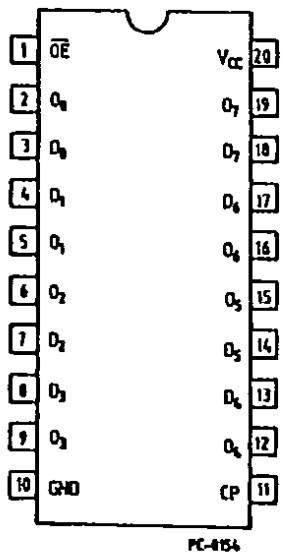
The T74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

PIN NAMES

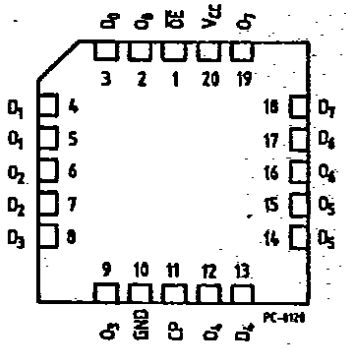
D_0-D_7	DATA INPUTS
$\overline{CP}$	CLOCK (active HIGH going edge) INPUT
$\overline{OE}$	OUTPUT ENABLE (active LOW) INPUT
O_0-O_7	OUTPUTS

PIN CONNECTION (top view)

DUAL IN LINE

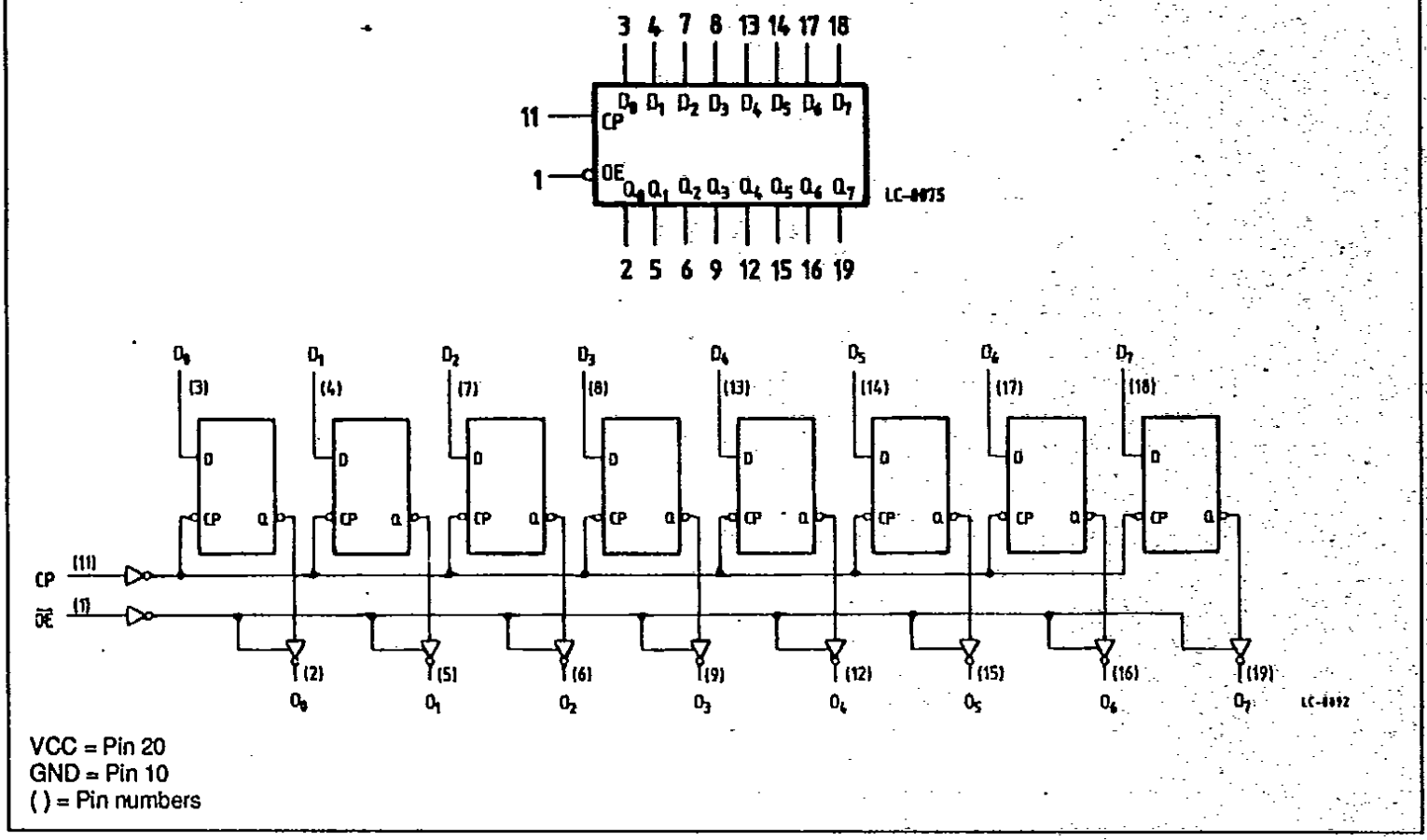


CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM



VCC = Pin 20
GND = Pin 10
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to + 7	V
V_I	Input Voltage, Applied to Input	− 0.5 to + 15	V
V_O	Output Voltage, Applied to Output	− 0.5 to + 10	V
I_I	Input Current, Into Inputs	− 30 to + 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS374XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

TRUTH TABLE

D_n	CP	$\overline{OE}$	Q_n
H	I	L	H
L	I	L	L
X	X	H	Z*

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High impedance

* Note : Contents of flip-flops unaffected by the state of the Output Enable Input ($\overline{OE}$).

FUNCTIONAL DESCRIPTION

The LS374 consist of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The Clock and Output Enable are common. The eight flip-flops will store the state of their individual D inputs that meet the set-up and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are refected on the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the OE input does not affect the state of the flip-flops.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.4	3.1		V_{CC} = MIN, I_{OH} = - 2.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 24 mA		V
I_{OZH}	Output Off Current HIGH			20	V_{CC} = MAX, V_{OUT} = 2.7 V V_E = 2.0 V		µA
I_{OZL}	Output Off Current LOW			- 20	V_{CC} = MAX, V_{OUT} = 0.4 V V_E = 2.0 V		µA
I_{IH}	Input HIGH Current			20	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	Input HIGH Current at MAX Input Voltage			0.1	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 30		- 130	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current Output Off		27	45	V_{CC} = MAX, V_{IN} = 0 V V_E = 4.5 V		mA

Notes : 1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions (note 1)		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, CP to Output		15 19	28 28	fig. 1	C_L = 45 pF R_L = 667 Ω	ns
t_{PZH}	Output Enable Time to HIGH Level		20	28	figs. 3, 4		ns
t_{PZL}	Output Enable Time to LOW Level		21	28	figs. 2, 4		ns
t_{PLZ}	Output Disable Time from LOW Level		12	20	figs. 2, 4	C_L = 5.0 pF R_L = 667 Ω	ns
t_{PHZ}	Output Disable Time from HIGH Level		15	25	figs. 3, 4		ns
f_{MAX}	Maximum Input Frequency	35	50		fig. 1		MHz

AC SET-UP REQUIREMENTS : T_A = 25 °C

Symbol	Parameter	Limit			Test Conditions		Unit
		Min.	Typ.	Max.			
t_wCP	Minimum Clock Pulse Width HIGH or LOW	13	10		fig. 1	V_{CC} = 5.0 V	ns
t_s	Minimum Set-up Time, Data to CP	20	15				ns
t_h	Minimum Hold Time, Data to CP	0	− 3				ns

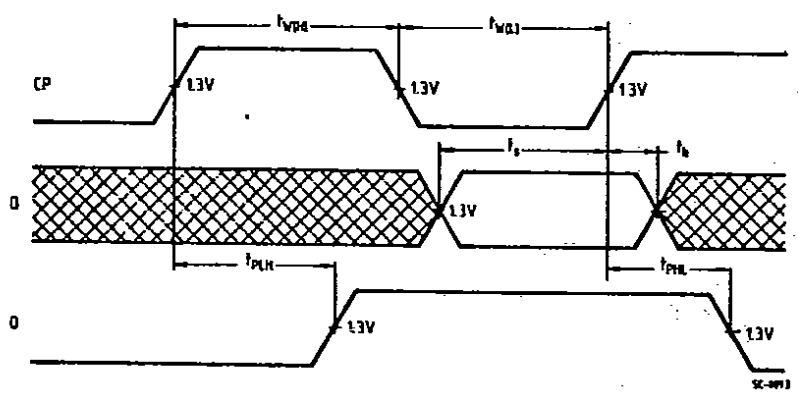
DEFINITION OF TERMS :

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

AC WAVEFORMS AND LOAD CIRCUIT

Figure 1.



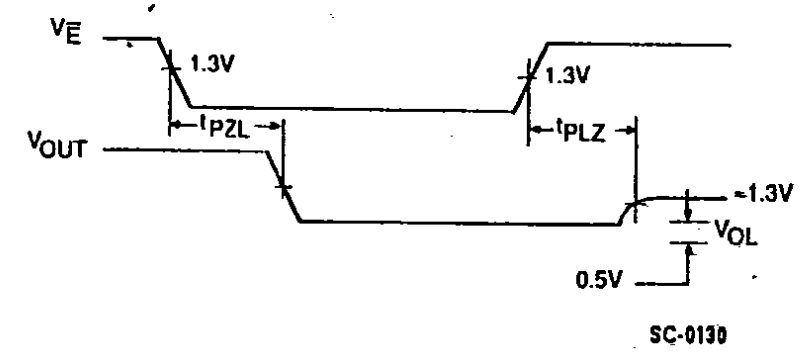


Figure 3.

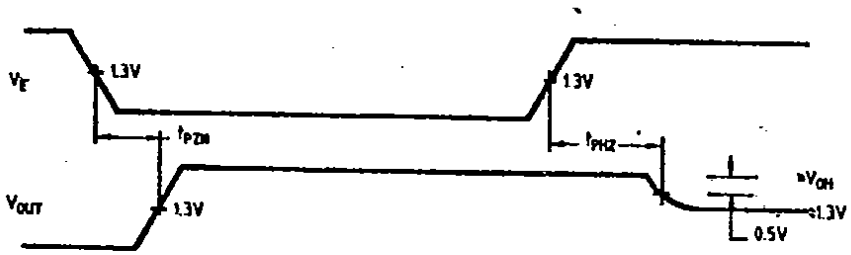


Figure 4.