HN1B01FDW1T1

Complementary Dual General Purpose Amplifier Transistor

PNP and NPN Surface Mount

- High Voltage and High Current: V_{CEO} = 50 V, I_C = 200 mA
- High h_{FE}: h_{FE} = 200 ~ 400
- Moisture Sensitivity Level: 1
- ESD Rating – Human Body Model: 3A
  – Machine Model: C

MAXIMUM RATINGS (T_A = 25°C)

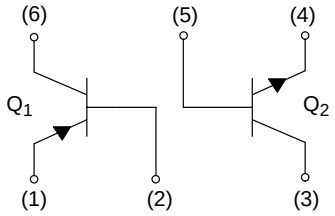
Rating	Symbol	Value	Unit
Collector–Base Voltage	$V_{(BR)CBO}$	60	Vdc
Collector–Emitter Voltage	$V_{(BR)CEO}$	50	Vdc
Emitter–Base Voltage	$V_{(BR)EBO}$	7.0	Vdc
Collector Current – Continuous	I_C	200	mAdc

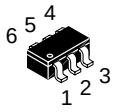
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Power Dissipation	P_D	380	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

ON Semiconductor™

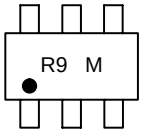
http://onsemi.com





SC–74
CASE 318F
STYLE 3

MARKING DIAGRAM



R9 = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device †	Package	Shipping
HN1B01FDW1T1	SC–74	3000/Tape & Reel

†The “T1” suffix refers to a 7 inch reel.

March, 2002 – Rev. 0

Publication Order Number:
HN1B01FDW1T1/D

Q1: PNP

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Breakdown Voltage (I_C = 2.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	–50	–	Vdc
Collector–Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	–60	–	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	–7.0	–	Vdc
Collector–Base Cutoff Current (V_{CB} = 45 Vdc, I_E = 0)	I_{CBO}	–	–0.1	μAdc
Collector–Emitter Cutoff Current (V_{CE} = 10 Vdc, I_B = 0) (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 30 Vdc, I_B = 0, T_A = 80°C)	I_{CEO}	 – – –	 –0.1 –2.0 –1.0	 μAdc nAdc mAdc
DC Current Gain (Note 1) (V_{CE} = 6.0 Vdc, I_C = 2.0 mAdc)	h_{FE}	 –200	 –400	–
Collector–Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$	–0.15	–0.3	Vdc

Q2: NPN

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Breakdown Voltage (I_C = 2.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	50	–	Vdc
Collector–Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	60	–	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	7.0	–	Vdc
Collector–Base Cutoff Current (V_{CB} = 45 Vdc, I_E = 0)	I_{CBO}	–	0.1	μAdc
Collector–Emitter Cutoff Current (V_{CE} = 10 Vdc, I_B = 0) (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 30 Vdc, I_B = 0, T_A = 80°C)	I_{CEO}	 – – –	 0.1 2.0 1.0	 μAdc nAdc mAdc
DC Current Gain (Note 1) (V_{CE} = 6.0 Vdc, I_C = 2.0 mAdc)	h_{FE}	 200	 400	–
Collector–Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$	0.15	0.25	Vdc

1. Pulse Test: Pulse Width ≤ 300 μs, D.C. ≤ 2%.

Typical Electrical Characteristics: PNP Transistor

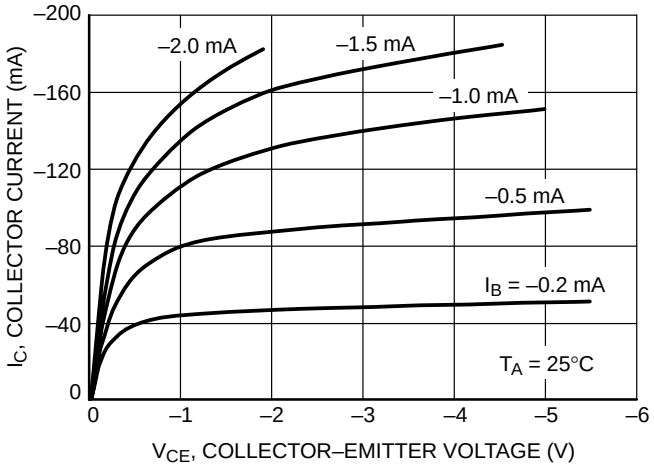


Figure 1. Collector Saturation Region

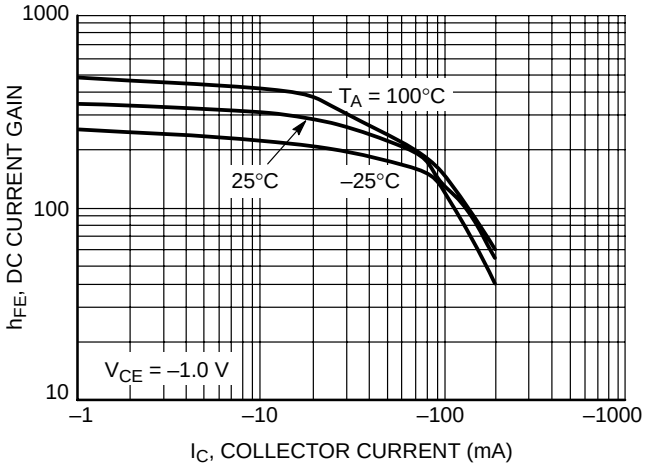


Figure 2. DC Current Gain

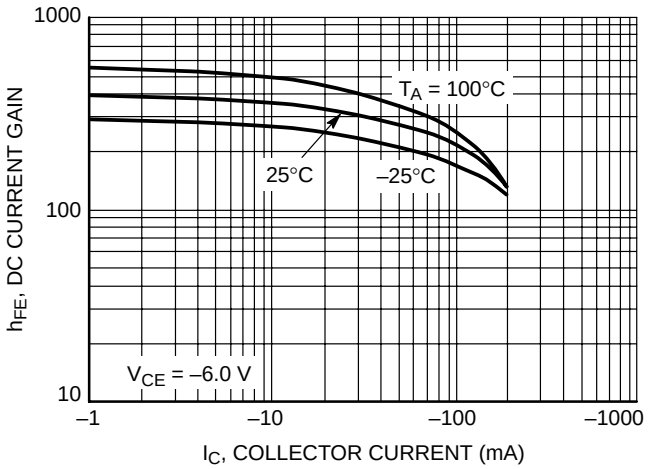


Figure 3. DC Current Gain

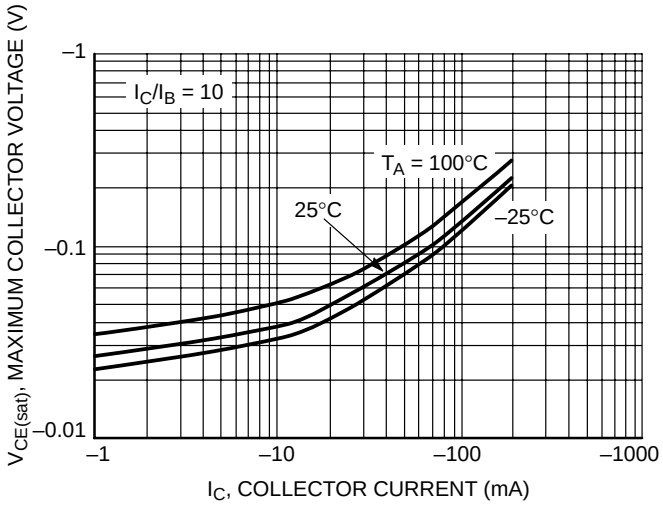


Figure 4. $V_{CE(sat)}$ versus I_C

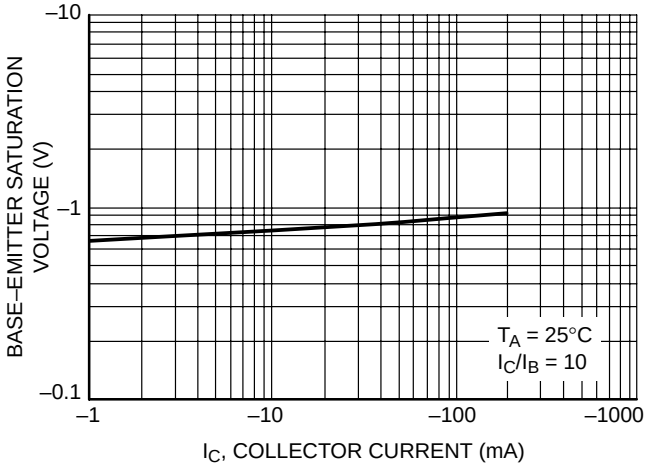


Figure 5. $V_{BE(sat)}$ versus I_C

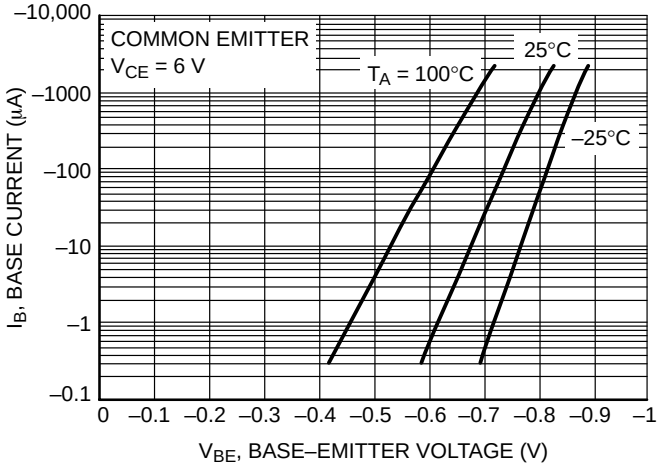


Figure 6. Base–Emitter Voltage

Typical Electrical Characteristics: NPN Transistor

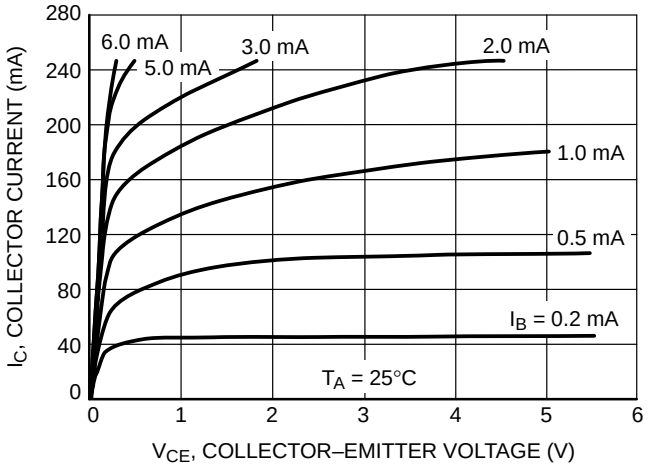


Figure 7. Collector Saturation Voltage

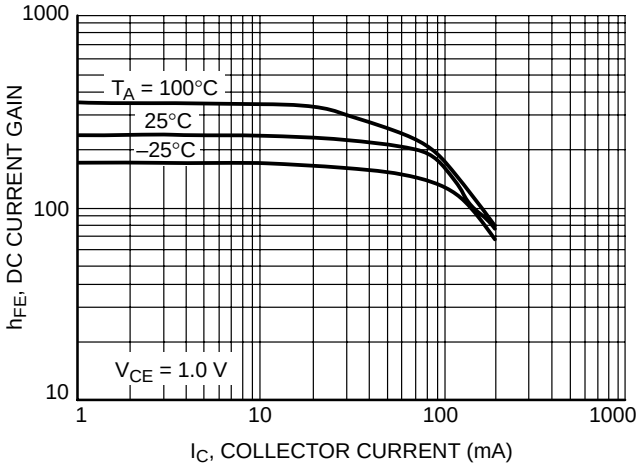


Figure 8. DC Current Gain

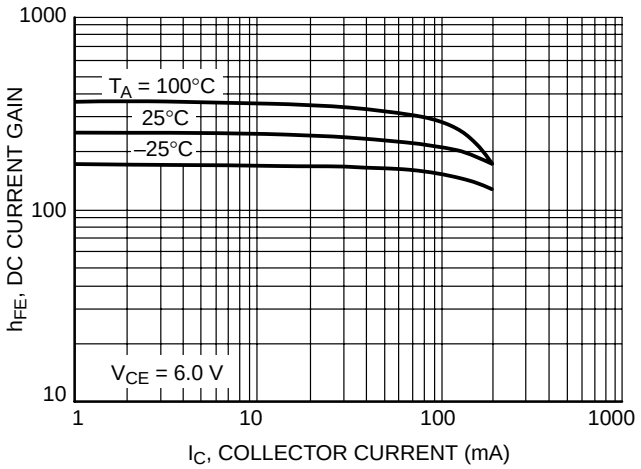


Figure 9. DC Current Gain

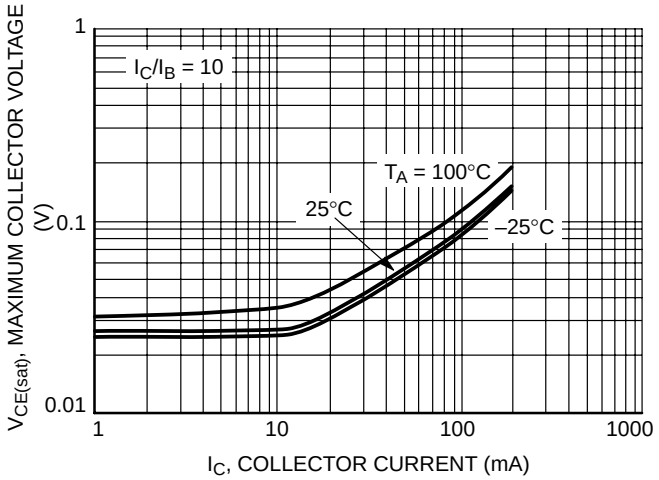


Figure 10. $V_{CE(sat)}$ versus I_C

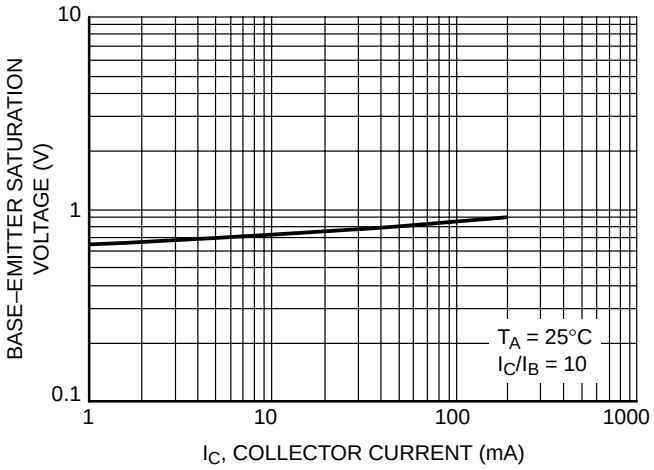


Figure 11. $V_{BE(sat)}$ versus I_C

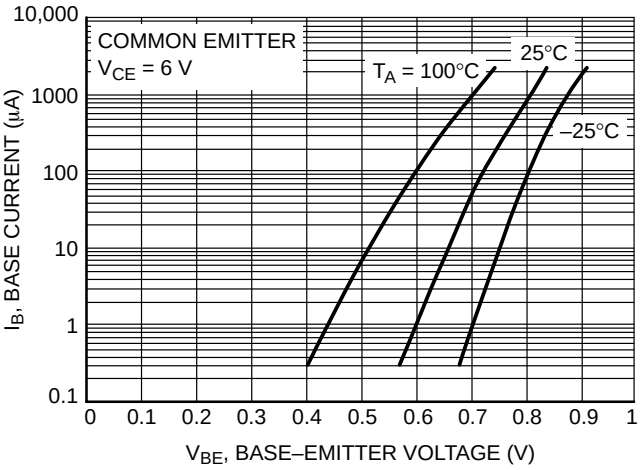
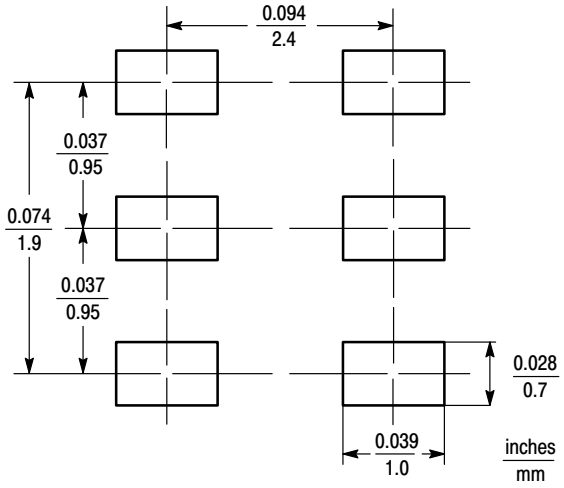


Figure 12. Base–Emitter Voltage

INFORMATION FOR USING THE SC-74 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self-align when subjected to a solder reflow process.



SC-74

SC-74 POWER DISSIPATION

The power dissipation of the SC-74 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SC-74 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 380 milliwatts.

$$P_D = \frac{150°C - 25°C}{329°C/W} = 380 \text{ milliwatts}$$

The 329°C/W for the SC-74 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 380 milliwatts. There are other alternatives to achieving higher power dissipation from the SC-74 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC-59, SC-74, SC-70/SOT-323, SOD-123, SOT-23, SOT-143, SOT-223, SO-8, SO-14, SO-16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used since the use of forced cooling will increase the temperature gradient and will result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 13 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

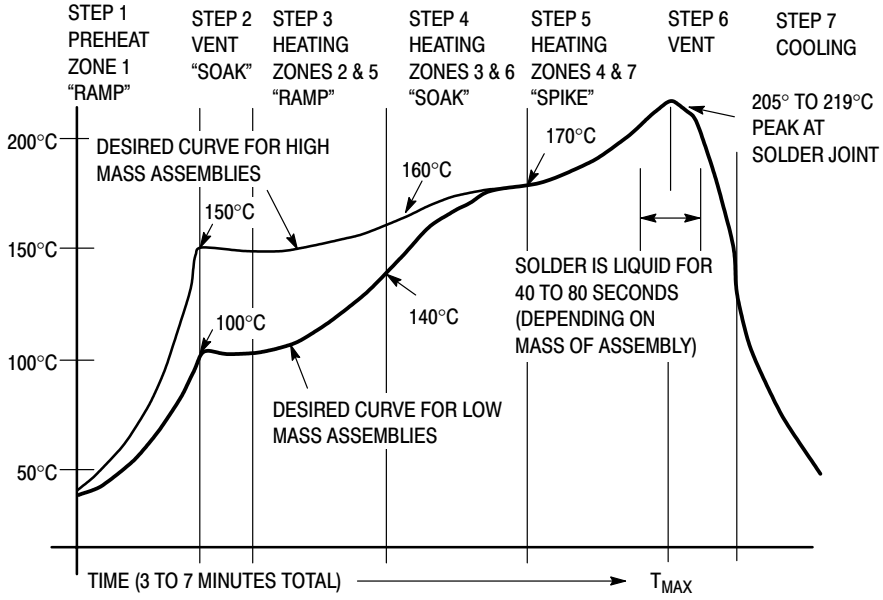
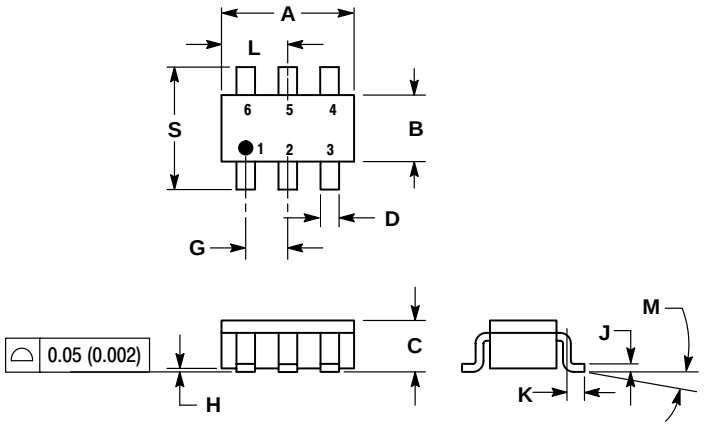


Figure 13. Typical Solder Heating Profile

PACKAGE DIMENSIONS

SC−74
CASE 318F−03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F−01 AND −02 OBSOLETE. NEW STANDARD 318F−03.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1142	0.1220	2.90	3.10
B	0.0512	0.0669	1.30	1.70
C	0.0354	0.0433	0.90	1.10
D	0.0098	0.0197	0.25	0.50
G	0.0335	0.0413	0.85	1.05
H	0.0005	0.0040	0.013	0.100
J	0.0040	0.0102	0.10	0.26
K	0.0079	0.0236	0.20	0.60
L	0.0493	0.0649	1.25	1.65
M	0 °	10 °	0 °	10 °
S	0.0985	0.1181	2.50	3.00

STYLE 3:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

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PUBLICATION ORDERING INFORMATION

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Email: ONlit@hibbertco.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

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ON Semiconductor Website: http://onsemi.com

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Sales Representative.