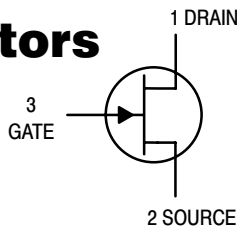


# JFET Chopper Transistors

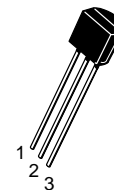
## N-Channel — Depletion



**J111**  
**J112**  
**J113**

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Gate Voltage	$V_{DG}$	–35	Vdc
Gate–Source Voltage	$V_{GS}$	–35	Vdc
Gate Current	$I_G$	50	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	350 2.8	mW mW/ $^\circ\text{C}$
Lead Temperature	$T_L$	300	$^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150	$^\circ\text{C}$



**CASE 29–11, STYLE 5**  
**TO–92 (TO–226AA)**

### ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

#### OFF CHARACTERISTICS

Gate–Source Breakdown Voltage ( $I_G = -1.0 \mu\text{Adc}$ )	$V_{(BR)GSS}$	35	—	Vdc
Gate Reverse Current ( $V_{GS} = -15 \text{Vdc}$ )	$I_{GSS}$	—	–1.0	nAdc
Gate Source Cutoff Voltage ( $V_{DS} = 5.0 \text{Vdc}, I_D = 1.0 \mu\text{Adc}$ )	$V_{GS(off)}$	J111 –3.0 J112 –1.0 J113 –0.5	–10 –5.0 –3.0	Vdc
Drain–Cutoff Current ( $V_{DS} = 5.0 \text{Vdc}, V_{GS} = -10 \text{Vdc}$ )	$I_{D(off)}$	—	1.0	nAdc

#### ON CHARACTERISTICS

Zero–Gate–Voltage Drain Current <sup>(1)</sup> ( $V_{DS} = 15 \text{Vdc}$ )	$I_{DSS}$	J111 20 J112 5.0 J113 2.0	— — —	mAdc
Static Drain–Source On Resistance ( $V_{DS} = 0.1 \text{Vdc}$ )	$r_{DS(on)}$	J111 — J112 — J113 —	30 50 100	$\Omega$
Drain Gate and Source Gate On–Capacitance ( $V_{DS} = V_{GS} = 0, f = 1.0 \text{MHz}$ )	$C_{dg(on)}$ + $C_{sg(on)}$	—	28	pF
Drain Gate Off–Capacitance ( $V_{GS} = -10 \text{Vdc}, f = 1.0 \text{MHz}$ )	$C_{dg(off)}$	—	5.0	pF
Source Gate Off–Capacitance ( $V_{GS} = -10 \text{Vdc}, f = 1.0 \text{MHz}$ )	$C_{sg(off)}$	—	5.0	pF

1. Pulse Width = 300  $\mu\text{s}$ , Duty Cycle = 3.0%.

TYPICAL SWITCHING CHARACTERISTICS

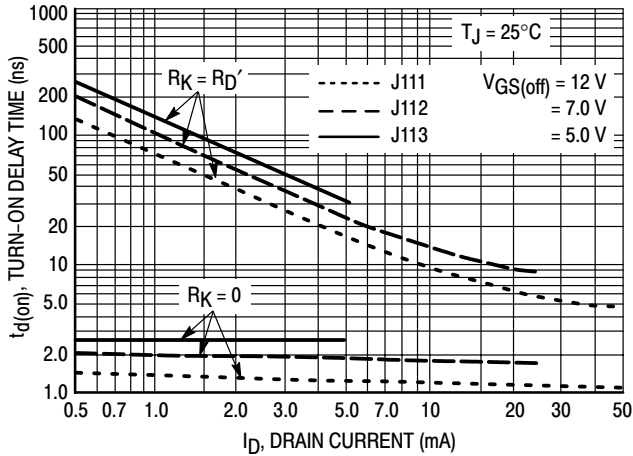


Figure 1. Turn-On Delay Time

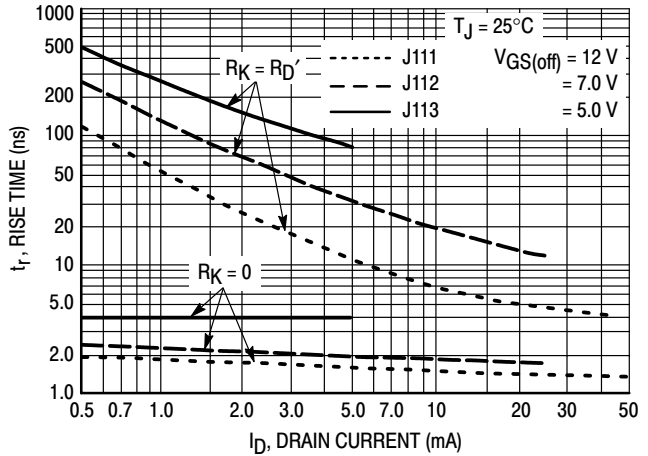


Figure 2. Rise Time

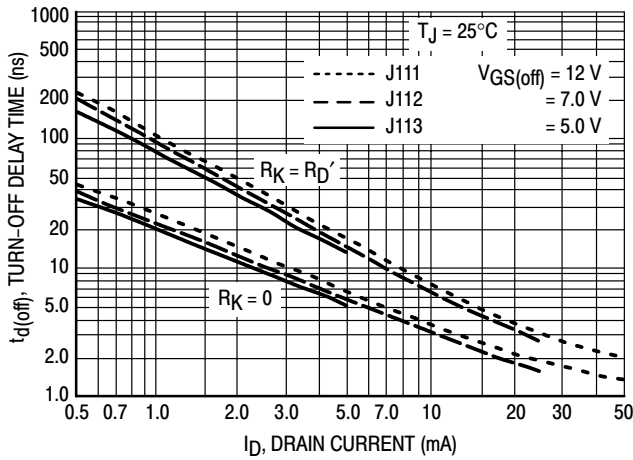


Figure 3. Turn-Off Delay Time

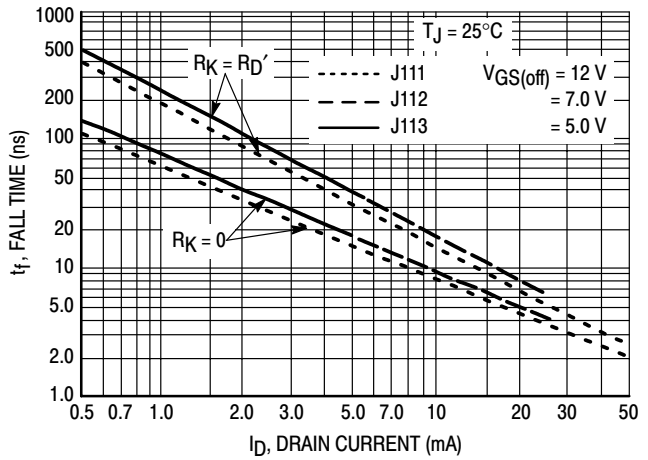


Figure 4. Fall Time

NOTE 1

The switching characteristics shown above were measured using a test circuit similar to Figure 5. At the beginning of the switching interval, the gate voltage is at Gate Supply Voltage ( $-V_{GG}$ ). The Drain-Source Voltage ( $V_{DS}$ ) is slightly lower than Drain Supply Voltage ( $V_{DD}$ ) due to the voltage divider. Thus Reverse Transfer Capacitance ( $C_{RSS}$ ) or Gate-Drain Capacitance ( $C_{gd}$ ) is charged to  $V_{GG} + V_{DS}$ .

During the turn-on interval, Gate-Source Capacitance ( $C_{gs}$ ) discharges through the series combination of  $R_{Gen}$  and  $R_K$ .  $C_{gd}$  must discharge to  $V_{DS(on)}$  through  $R_G$  and  $R_K$  in series with the parallel combination of effective load impedance ( $R'_D$ ) and Drain-Source Resistance ( $r_{ds}$ ). During the turn-off, this charge flow is reversed.

Predicting turn-on time is somewhat difficult as the channel resistance  $r_{ds}$  is a function of the gate-source voltage. While  $C_{gs}$  discharges,  $V_{GS}$  approaches zero and  $r_{ds}$  decreases. Since  $C_{gd}$  discharges through  $r_{ds}$ , turn-on time is non-linear. During turn-off, the situation is reversed with  $r_{ds}$  increasing as  $C_{gd}$  charges.

The above switching curves show two impedance conditions; 1)  $R_K$  is equal to  $R_D$ , which simulates the switching behavior of cascaded stages where the driving source impedance is normally the load impedance of the previous stage, and 2)  $R_K = 0$  (low impedance) the driving source impedance is that of the generator.

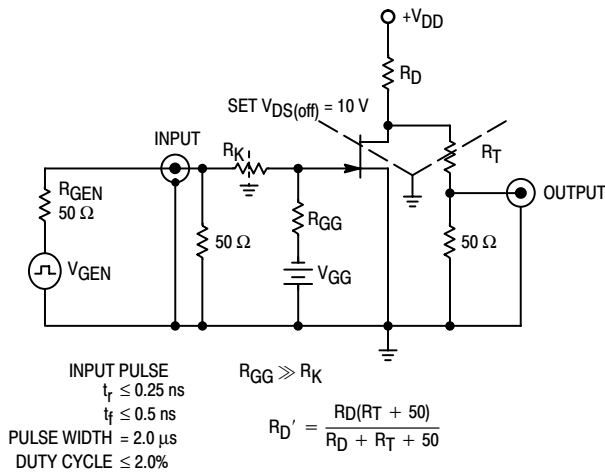


Figure 5. Switching Time Test Circuit

# J111 J112 J113

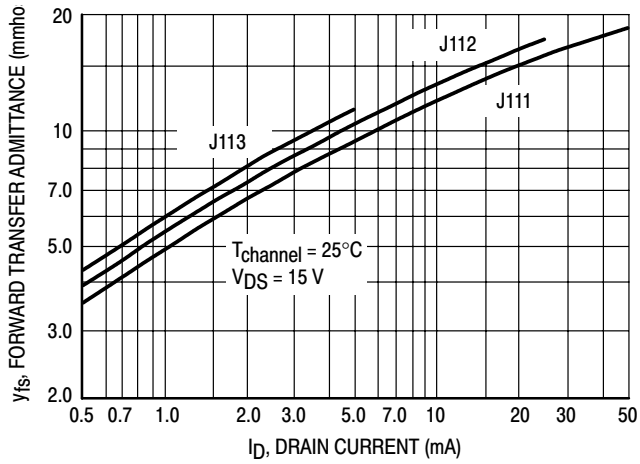


Figure 6. Typical Forward Transfer Admittance

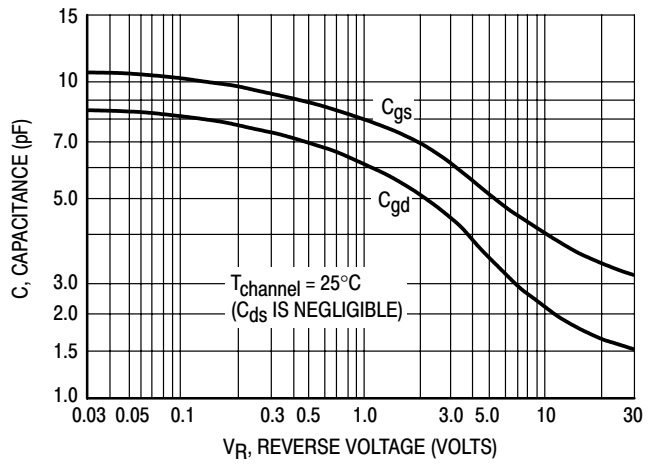


Figure 7. Typical Capacitance

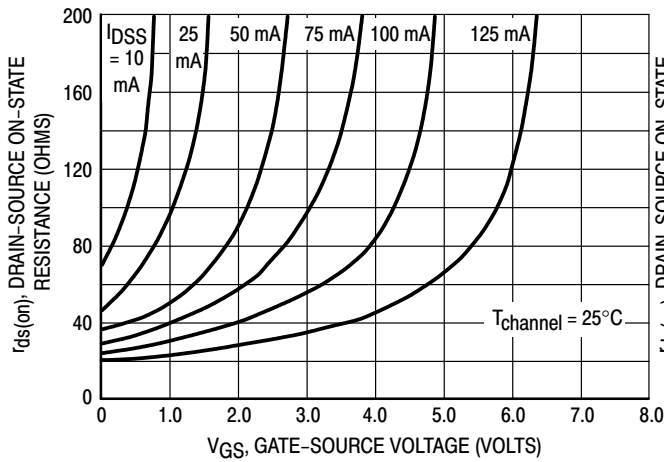


Figure 8. Effect of Gate-Source Voltage On Drain-Source Resistance

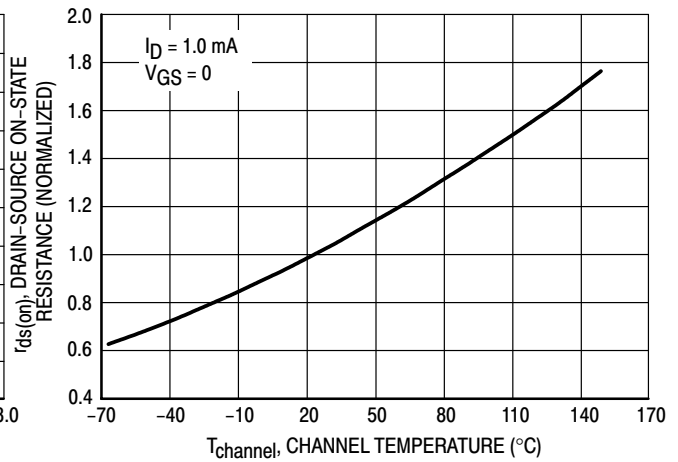


Figure 9. Effect of Temperature On Drain-Source On-State Resistance

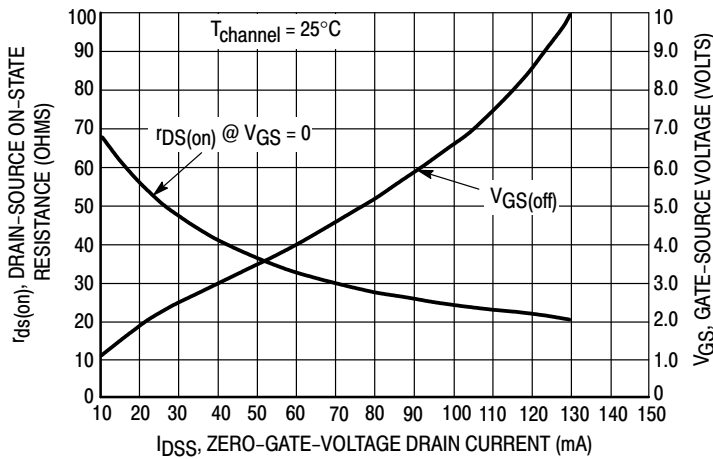


Figure 10. Effect of  $I_{DSS}$  On Drain-Source Resistance and Gate-Source Voltage

## NOTE 2

The Zero-Gate-Voltage Drain Current ( $I_{DSS}$ ), is the principle determinant of other J-FET characteristics. Figure 10 shows the relationship of Gate-Source Off Voltage ( $V_{GS(off)}$ ) and Drain-Source On Resistance ( $r_{ds(on)}$ ) to  $I_{DSS}$ . Most of the devices will be within  $\pm 10\%$  of the values shown in Figure 10. This data will be useful in predicting the characteristic variations for a given part number.

For example:

Unknown

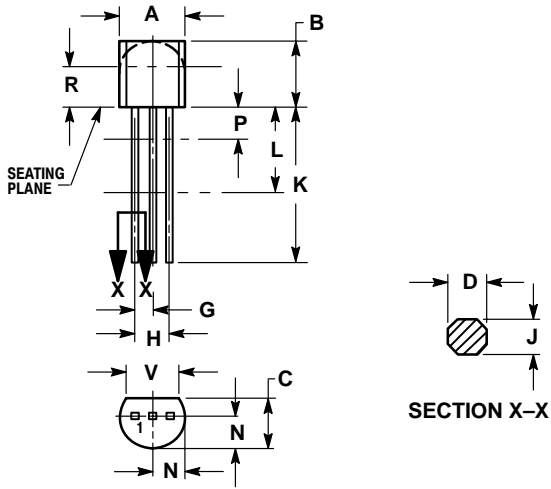
$r_{ds(on)}$  and  $V_{GS}$  range for an J112

The electrical characteristics table indicates that an J112 has an  $I_{DSS}$  range of 25 to 75 mA. Figure 10, shows  $r_{ds(on)} = 52$  Ohms for  $I_{DSS} = 25$  mA and 30 Ohms for  $I_{DSS} = 75$  mA. The corresponding  $V_{GS}$  values are 2.2 volts and 4.8 volts.

# J111 J112 J113

## PACKAGE DIMENSIONS

### TO-92 (TO-226) CASE 29-11 ISSUE AL




#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

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