

NEC**MOS INTEGRATED CIRCUIT**
 μ PD161660**POWER SUPPLY FOR TFT-LCD DRIVER****DESCRIPTION**

The μ PD161660 is a power supply IC for TFT-LCD driver. This ICs can generate the levels which TFT-LCD driver need, from 2.7 V.

FEATURES

- To generate 3 levels from single voltage input
- To integrate regulator circuit for source and gate driver

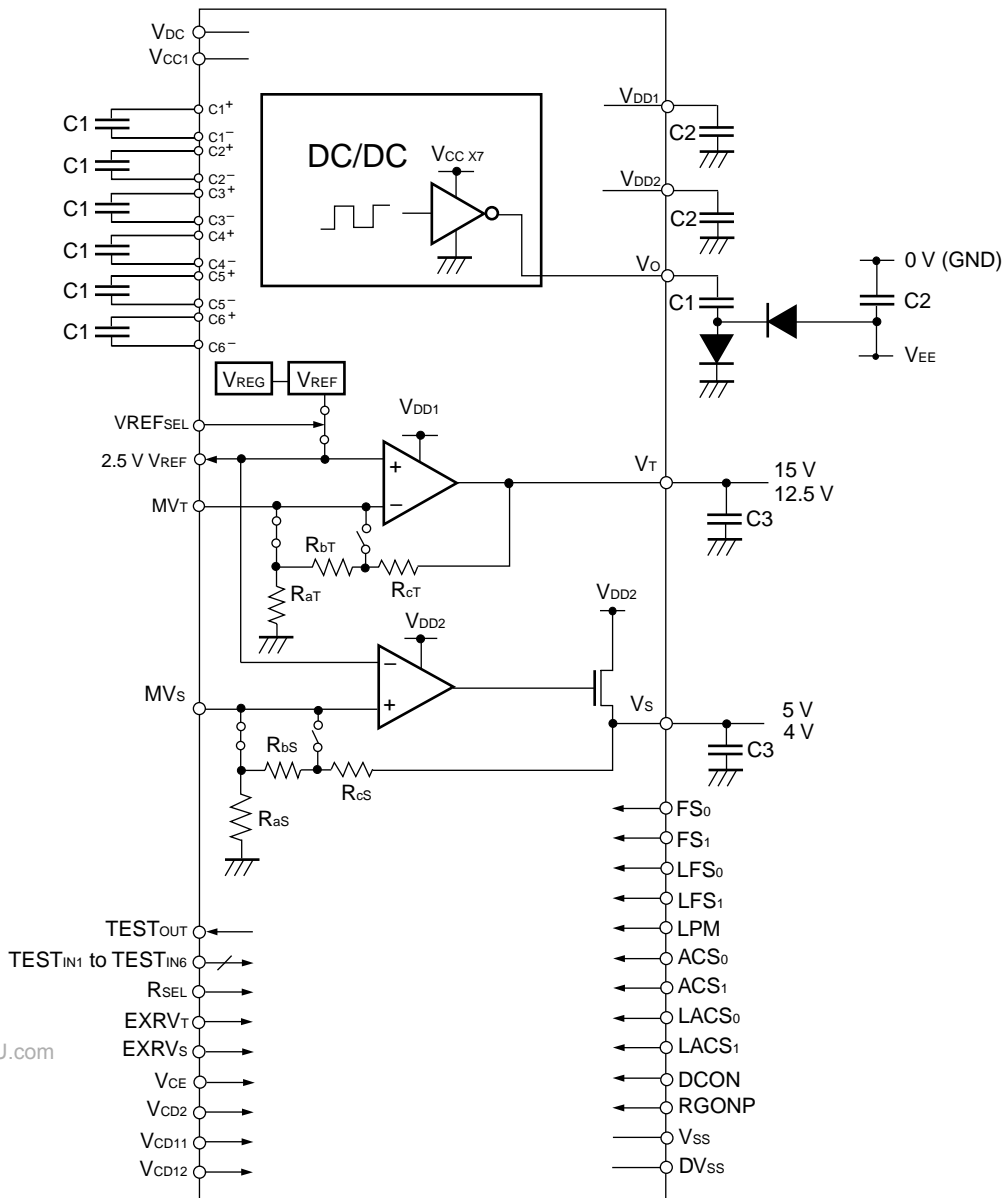
ORDERING INFORMATION

	Part number	Package
★	μ PD161660P	Chip

Remark Purchasing the above chip entails the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representative.

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

1. BLOCK DIAGRAM/SYSTEM DIAGRAM



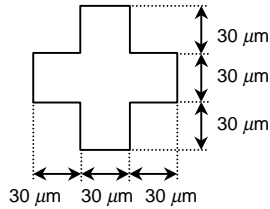
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2. PIN CONFIGURATION (Pad Layout)

Chip size: X = 4.20 mm, Y = 4.35 mm

Pad size : 100 x 100 μm²

(1) Alignment mark



(2) Arrangement

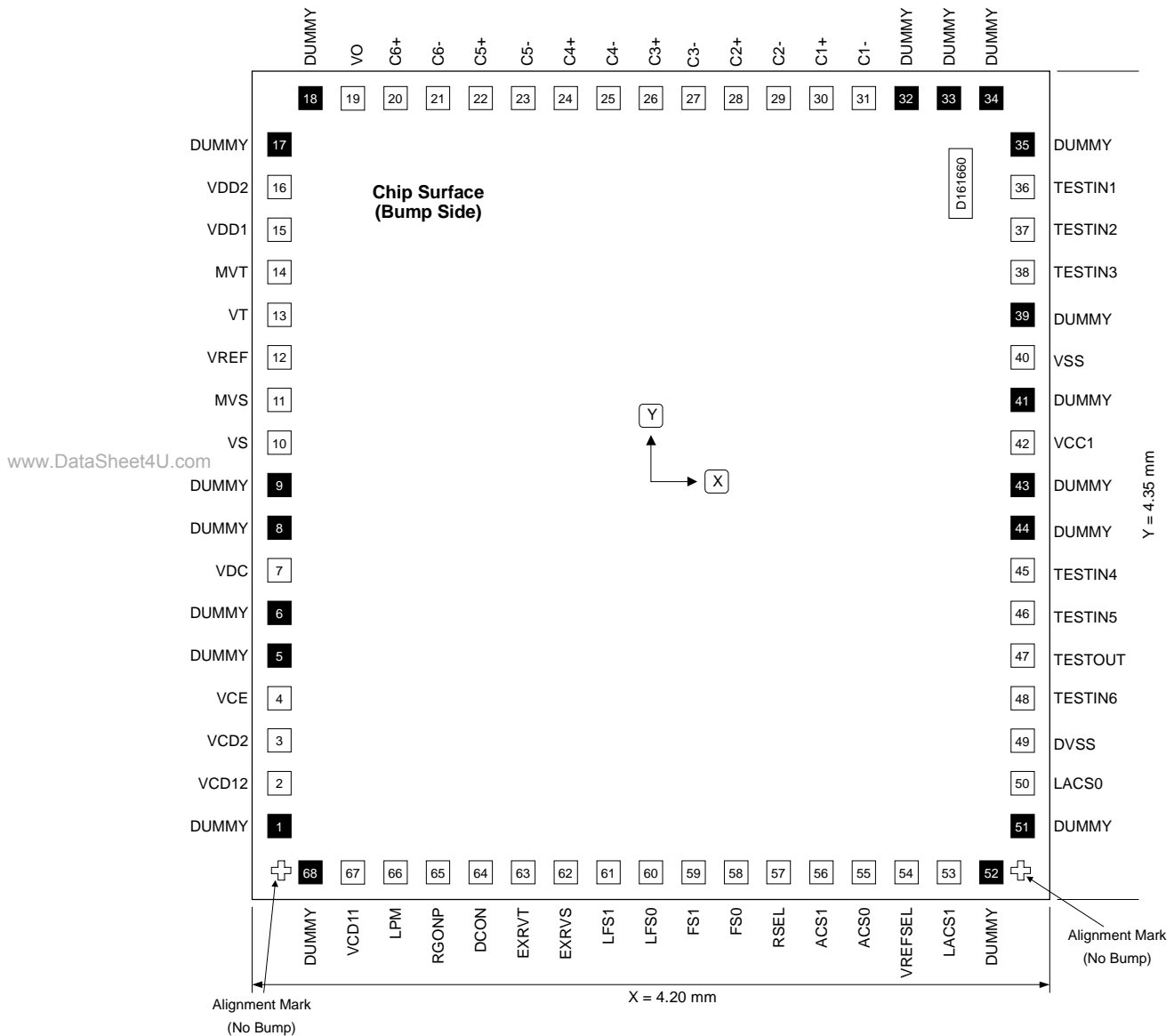


Table 2-1. Pad Layout

Pad No.	Pad name	X[mm]	Y[mm]
1	DUMMY	-1950	-1800
2	V _{CD12}	-1950	-1575
3	V _{CD2}	-1950	-1350
4	V _{CE}	-1950	-1125
5	DUMMY	-1950	-900
6	DUMMY	-1950	-675
7	V _{DC}	-1950	-450
8	DUMMY	-1950	-225
9	DUMMY	-1950	0
10	V _S	-1950	225
11	MV _S	-1950	450
12	V _{REF}	-1950	675
13	V _T	-1950	900
14	MV _T	-1950	1125
15	V _{DD1}	-1950	1350
16	V _{DD2}	-1950	1575
17	DUMMY	-1950	1800
18	DUMMY	-1800	2025
19	V _O	-1575	2025
20	C ₆ ⁺	-1350	2025
21	C ₆ ⁻	-1125	2025
22	C ₅ ⁺	-900	2025
23	C ₅ ⁻	-675	2025
24	C ₄ ⁺	-450	2025
25	C ₄ ⁻	-225	2025
26	C ₃ ⁺	0	2025
27	C ₃ ⁻	225	2025
28	C ₂ ⁺	450	2025
29	C ₂ ⁻	675	2025
30	C ₁ ⁺	900	2025
31	C ₁ ⁻	1125	2025
32	DUMMY	1350	2025
33	DUMMY	1575	2025
34	DUMMY	1800	2025
35	DUMMY	1950	1800
36	TEST _{IN1}	1950	1575
37	TEST _{IN2}	1950	1350
38	TEST _{IN3}	1950	1125
39	DUMMY	1950	900
40	V _{SS}	1950	675

Pad No.	Pad name	X[mm]	Y[mm]
41	DUMMY	1950	450
42	V _{CC1}	1950	225
43	DUMMY	1950	0
44	DUMMY	1950	-225
45	TEST _{IN4}	1950	-450
46	TEST _{IN5}	1950	-675
47	TEST _{OUT}	1950	-900
48	TEST _{IN6}	1950	-1125
49	DV _{SS}	1950	-1350
50	LACS ₀	1950	-1575
51	DUMMY	1950	-1800
52	DUMMY	1800	-2025
53	LACS ₁	1575	-2025
54	V _{REFSEL}	1350	-2025
55	ACS ₀	1125	-2025
56	ACS ₁	900	-2025
57	R _{SEL}	675	-2025
58	FS ₀	450	-2025
59	FS ₁	225	-2025
60	LFS ₀	0	-2025
61	LFS ₁	-225	-2025
62	EXRVS	-450	-2025
63	EXRVT	-675	-2025
64	D _{CON}	-900	-2025
65	R _{GONP}	-1125	-2025
66	L _{PM}	-1350	-2025
67	V _{CD11}	-1575	-2025
68	DUMMY	-1800	-2025
	Alignment mark	-1950	-2025
	Alignment mark	1950	-2025

3. PIN FUNCTIONS

(1/2)

Symbol	Pin Name	Pad No.	I/O	Description
V _{DC}	Power supply	7	–	Power supply for DC/DC converter.
V _{CC1}	Power supply	42	–	Power supply for logic circuit.
V _{SS}	Ground	40	–	Ground.
DV _{SS}	Ground	49	–	Ground (for control pin pull-down)
V _{DD1}	DC/DC converter output	15	–	Boost voltage of DC/DC converter (x4, x5, x6 or x7). The capacitors required for each boost level are shown below. <ul style="list-style-type: none"> • x4 boost: C1, C2, C6 (C3, C4, and C5 are not required) • x5 boost: C1, C2, C3, C6 (C4, and C5 are not required) • x6 boost: C1, C2, C3, C4, C6 (C5 is not required) • x7 boost: C1, C2, C3, C4, C5, C6
V _{DD2}	DC/DC converter output	16	–	Boost voltage of DC/DC converter (x2 or x3). The boost steps for V _{DD2} is selected by V _{CD2} pin. The capacitors required for each boost level are shown below. <ul style="list-style-type: none"> • x2 boost: C1 • x3 boost: C1, C2,
V _O	Rectangle signal output for negative boost	19	–	Rectangle signal output for negative boost. The V _O voltage range is selected by V _{CE} pin. The capacitors required for each boost level are shown below. <V _{CE} = L> <ul style="list-style-type: none"> • x3 boost: C1, C2 • x4 boost: C1, C2, C3 • x5 boost: C1, C2, C3, C4 • x6 boost: C1, C2, C3, C4, C5 <V _{CE} = H> <ul style="list-style-type: none"> • x4 boost: C1, C2, C6 • x5 boost: C1, C2, C3, C6 • x6 boost: C1, C2, C3, C4, C6 • x7 boost: C1, C2, C3, C4, C5, C6
V _T	Regulator output	13	–	15 V/12.5 V regulator output for gate driver.
V _S	Regulator output	10	–	5 V/4 V regulator output for source driver.
V _{REF}	Reference voltage input/output	12	I/O	The gate driver includes reference voltage for V _B regulator. When V _{REFSEL} = H, external reference voltage can be input. Reference voltage input/output pin of V _T , V _S regulator.
DCON	DC/DC converter control	64	I	DC/DC converter ON/OFF control. Connect to DCON pin of source driver.
RGONP	Regulator control	65	I	Regulator ON/OFF control. Connect to RGONP pin of source driver.
EXRV _T	V _T regulating resistor selection	63	I	To select internal/external resistor for V _T regulator.
EXRV _S	V _S regulating resistor selection	62	I	To select internal/external resistor for V _S regulator.

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Symbol	Pin Name	Pad No.	I/O	Description
V _{CD11}	V _{DD1} booster selection	67	I	To select x4/x5/x6/x7 boost for V _{DD1} . Connect to V _{CD11} pin of source driver.
V _{CD12}	V _{DD1} booster selection	2	I	To select x4/x5/x6/x7 boost for V _{DD1} . Connect to V _{CD12} pin of source driver.
V _{CD2}	V _{DD2} booster selection	3	I	To select x2/x3 boost for V _{DD2} . Connect to V _{CD2} pin of source driver.
V _{CE}	V _O level selection	4	I	To select x3/x4/x5/x6/x7 boost for V _O top voltage level. Connect to V _{CE} pin of source driver.
LPM	Low power mode signal	66	I	Control signal for low power mode. When this pin is high level, it comes to be low power mode. LPM = H: LACS ₀ , LACS ₁ , LFS ₀ , LFS ₁ are enabled. LPM = L: ACS ₀ , ACS ₁ , FS ₀ , FS ₁ are enabled. Connect to LPMP pin of source driver.
ACS ₀ , ACS ₁	Amp. current selection	55, 56	I	To select Amp. current when in scanning.
LACS ₀ , LACS ₁	Amp. current selection	50, 53	I	To select Amp. current in low power mode.
MV _T	V _T regulator input	14	–	EXRV _T = H: Connect to external resistor. EXRV _T = L: Leave it open.
MV _S	V _S regulator input	11	–	EXRV _S = H: Connect to external resistor. EXRV _S = L: Leave it open.
TEST _{IN1} - TEST _{IN6}	Test	36-38, 45, 46, 48	I	Test pins. Normally leave it open.
TEST _{OUT}	Test output	47	O	Test pin. Normally leave them open.
FS ₀ , FS ₁	OSC frequency selection	58, 59	I	To select OSC frequency for DC/DC converter when in scanning.
LFS ₀ , LFS ₁	OSC frequency selection	60, 61	I	To select OSC frequency for DC/DC capacitor when in scanning.
R _{SEL}	Internal resistor selection for regulator	57	I	To select internal resistor for regulator.
VREF _{SEL}	Regulator reference voltage input selection	54	I	To select external or internal reference voltage of V _T , V _S regulator.
C ₁ ⁺ , C ₁ ⁻ C ₂ ⁺ , C ₂ ⁻ C ₃ ⁺ , C ₃ ⁻ C ₄ ⁺ , C ₄ ⁻ C ₅ ⁺ , C ₅ ⁻ C ₆ ⁺ , C ₆ ⁻	Capacitor connect pin for boost	30, 31 28, 29 26, 27 24, 25 22, 23 20, 21	–	To connect external capacitor for DC/DC converter. The capacitance and tolerance of each capacitor are shown below. Capacitance : 1 μF Withstanding voltage: 10 V

4. MODE DESCRIPTION

(1) DC/DC converter control

DCON	H	DC/DC converter ON
	L	DC/DC converter OFF

(2) Regulator control

RGONP	H	Regulator ON
	L	Regulator OFF (V_T , V_S = High impedance)

(3) V_T regulating resistor

EXRV _T	H	External resistor
	L	Internal resistor

(4) V_S regulating resistor

EXRV _S	H	External resistor
	L	Internal resistor

(5) V_{DD2} booster selection

V _{CD2}	H	x3 booster
	L	x2 booster

(6) V_T , V_S regulator selection

		V_T	V_S
R _{SEL}	H	15.0 V	5.0 V
	L	12.5 V	4.0 V

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(7) Regulator reference voltage input selection

VREF _{SEL}	H	V _{REF} : External reference voltage input
	L	V _{REF} : Internal reference voltage output

(8) V_{DD1} and V_o high-level booster selection

V _{CD12}	V _{CD11}	V _{CE}	V _{DD1} booster	V _o high level
H	H	H	x7 V _{DC}	x7 V _{DC}
H	H	L	x7 V _{DC}	x6 V _{DC}
H	L	H	x6 V _{DC}	x6 V _{DC}
H	L	L	x6 V _{DC}	x5 V _{DC}
L	H	H	x5 V _{DC}	x5 V _{DC}
L	H	L	x5 V _{DC}	x4 V _{DC}
L	L	H	x4 V _{DC}	x4 V _{DC}
L	L	L	x4 V _{DC}	x3 V _{DC}

(9) Amp. current selection

		V _T			V _s		
ACS ₀ ^{Note} (LACS ₀)	ACS ₁ ^{Note} (LACS ₁)	Source current	Sink current	Amp. current	Source current	Sink current	Amp. current
L	L	1 mA >	0.5 μA	1 μA	3 mA >	0.5 μA	1 μA
L	H	1 mA >	1 μA	2 μA	3 mA >	1 μA	2 μA
H	L	1 mA >	2.5 μA	5 μA	3 mA >	2.5 μA	5 μA
H	H	1 mA >	5 μA	10 μA	3 mA >	5 μA	10 μA

Note ACS₀, ACS₁ : Current selection in scanning time

LACS₀, LACS₁: Current selection in low power mode

(10) OSC frequency selection

FS ₁ , LFS ₁ ^{Note}	FS ₀ , LFS ₀ ^{Note}	OSC
L	L	f _{osc} /8
L	H	f _{osc} /2
H	L	f _{osc} /32
H	H	f _{osc} /256

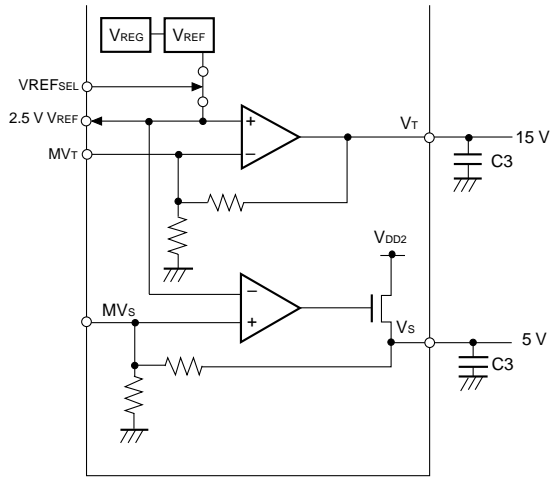
Note FS₀, FS₁ : Current selection when in scanning

LFS₀, LFS₁: Current selection in low power mode

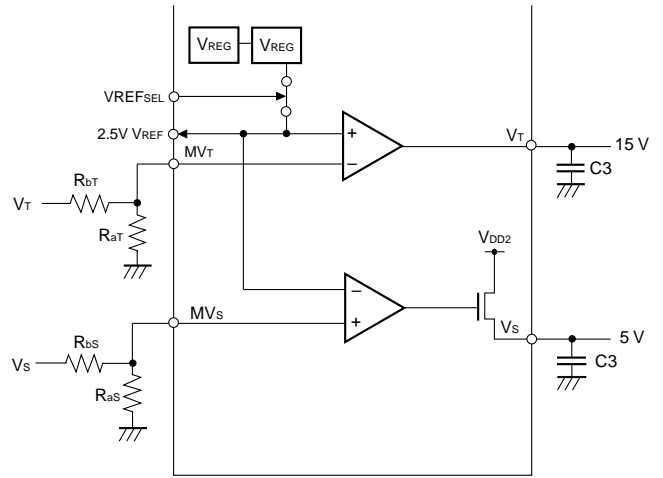
(11) Low power mode selection

LPM	H	Low power mode LACS ₀ , LACS ₁ , LFS ₀ , LFS ₁ are enable.
	L	Normal mode ACS ₀ , ACS ₁ , FS ₀ , FS ₁ are enable.

Figure 4-1. Example of Internal/External resistor for the regulator



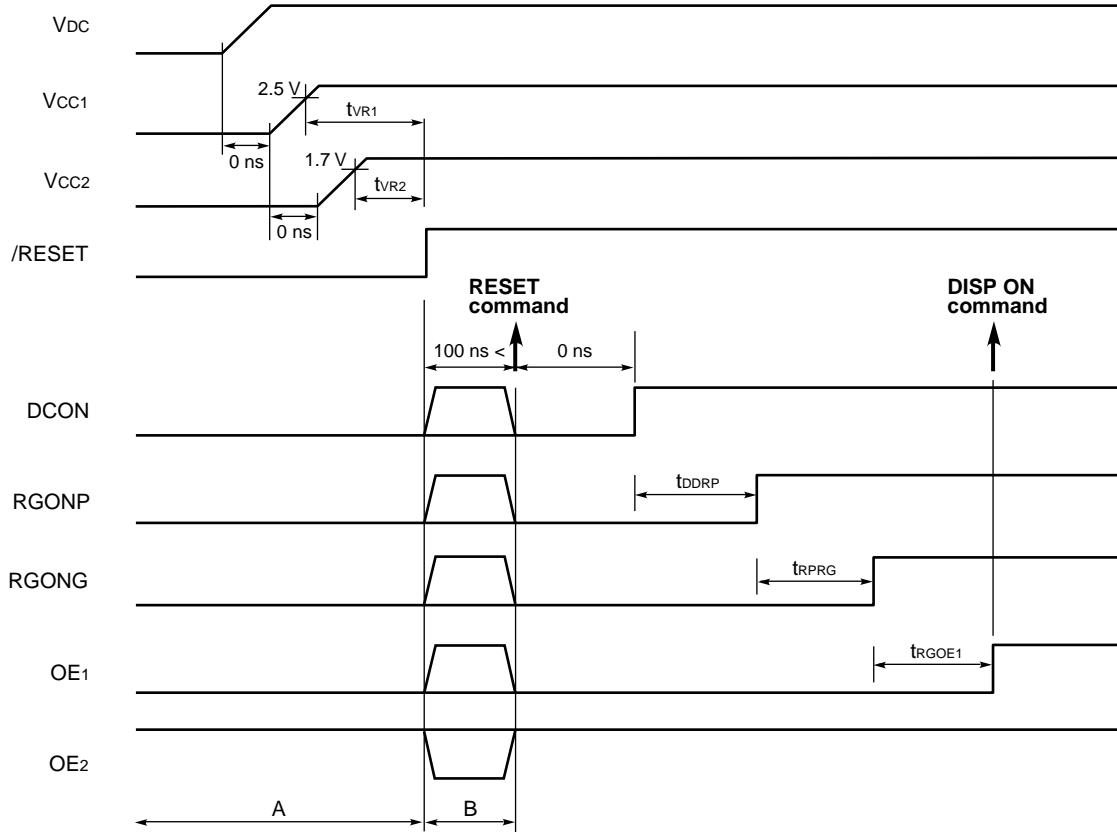
Internal Resistor Mode
 EXRV_T = L
 EXRV_S = L



External Resistor Mode
 EXRV_T = H
 EXRV_S = H
 $V_T = (1 + \frac{R_{bT}}{R_{aT}}) V_{REF}$
 $V_S = (1 + \frac{R_{bS}}{R_{aS}}) V_{REF}$

5. POWER ON/OFF SEQUENCE

5.1 Power ON sequence



tVR1, tVR2 = 100 ns MIN.

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Remarks 1. /xxx indicates active low signal.

2. OE1, OE2, /RESET, RGONG, RGONP, VCC2 are signals from source driver.

- ① All three power supplies, VDC, VCC1, and VCC2, can be on at the same time.
- ② The pins are fixed to the following levels by the source driver during the period of /RESET = L (A period).
 Note that the gate output is fixed to the VB level, and the DC/DC converter and the regulators are off.
 DCON, RGONG, RGONP, OE1: L (low level)
 OE2: H (high level)
- ③ The /RESET pin can be made high at the end of both tVR1, which starts from the rising edge of VCC1, and tVR2, which starts from the rising edge of VCC2.
- ④ The wait time between when the /RESET signal rises and when the RESET command is acknowledged must be at least 100 ns.
- ⑤ The logical status of the DCON, RGONG, RGONP, OE1, and OE2 pins in the period between when the /RESET signal rises and when the RESET command (↑part) is acknowledged (B period) is undefined. Be aware, therefore,

that the gate output may be undefined and the DC/DC converter and the regulators may be on. If the B period is sufficiently short however, it is unlikely that the display will be affected. Note that the gate output MAX value in the B period must be determined separately as a specification of the LCD module.

The pins are re-fixed to the following levels by the source driver when the RESET command is input.

Note that the gate output is fixed to the V_B level, and the DC/DC converter and the regulators are off.

DCON, RGONG, RGONP, OE₁: L (low level)

OE₂: H (high level)

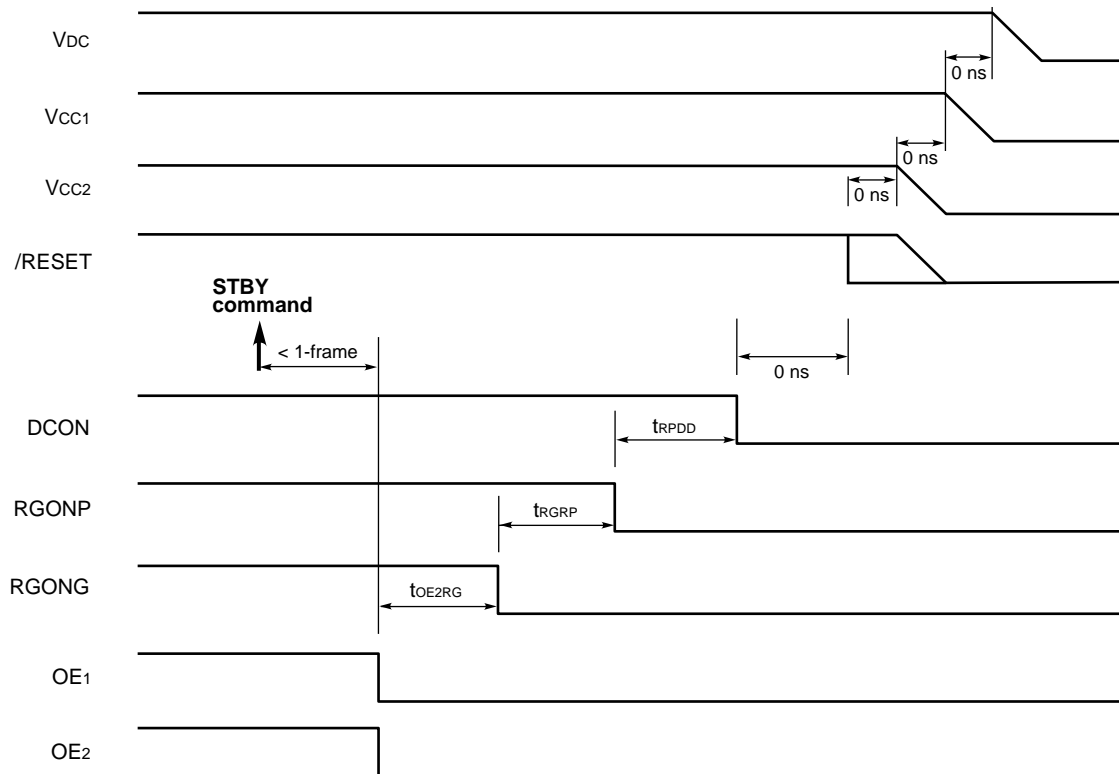
- ⑦ Set a timing that ensures the DCON, RGONP, and RGONG pins are shifted to high level in that order after the RESET command is input. At this time, the DC/DC converter and the regulators are on. Before that, the booster level must have been set up (by BGRS, V_{CE} , V_{CD2} , PVCOM of R32 register and R34 register of the μPD161620). Note that the target timing of t_{DDRP} and t_{RPRG} (while the DC/DC converter output and regulator output is stable) is t_{DDRP} = approx. 50 ms and t_{RPRG} = approx. 20 ms, but users are requested to set the final timing after sufficiently evaluating the μPD161660 in the LCD module.

- ⑧ Input the DISPON command (↑part) after ensuring that all the power supplies are high level.

The source driver will start display with OE₁ = H.

The target is t_{RGOE1} = approx. 1 ms, but users are requested to set the final timing after sufficiently evaluating the μPD161660 in the LCD module.

5.2 Power OFF sequence



Remark OE₁, OE₂, /RESET, RGONG, RGONP, V_{CC2} are the signals from driver.

① Input the STBY command (↑part).

The source driver sets the status of the OE₁ and OE₂ pins to low level within one frame.

The gate output is fixed to V_T.

② Set a timing that ensures the RGONG, RGONP, and DCON pins are shifted to low level in that order after the panel load has been sufficiently discharged (t_{OE2RG} timing; Secure an amount of time equivalent to one frame after executing the standby command). At this time, the DC/DC converter and the regulators are off.

Note that a timing of 0 ns for t_{RGRP} and t_{RPDD} causes no problems on the device side, but users are requested to set the final timing after sufficiently evaluating the μPD161660 in the LCD module.

③ Although it is unnecessary to input the RESET command to the source driver, for designs in which the system is reset when the power supply is turned off, make settings that ensure /RESET = L at DCON = L and subsequent timings.

④ All three power supplies, V_{DC}, V_{CC1}, and V_{CC2}, can be off at the same time.

6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Supply voltage	V _{CC1}	-0.5 to +6.0	V
Supply voltage	V _{DC}	-0.5 to +6.0	V
Input voltage	V _I	-0.5 to V _{CC1} + 0.5	V
Input current	I _I	±10	mA
Output voltage	V _{DD1}	-0.5 to +40	V
Output current	I _O	±10	mA
Output current	I _{O2}	±10	mA
Operating ambient temperature	T _A	-40 to +85	°C
Storage temperature	T _{stg}	-55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (T_A = -40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{CC1}	2.5	2.7	3.6	V
Supply voltage	V _{DC}	2.5		3.6	V
Input voltage	V _I	0		V _{CC1}	V

Electrical Characteristics (Unless otherwise specified, T_A = -40 to +85°C, V_{CC1} = 2.5 to 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High level input voltage	V _{IH}		0.8 V _{CC1}			V
Low level input voltage	V _{IL}				0.2 V _{CC1}	V
Boost voltage	V _{DD1}	I _{DD1} = 300 μA, 7 x Boost	6 V _{DC}		7 V _{DC}	V
Boost voltage	V _{DD1}	I _{DD1} = 300 μA, 6 x Boost	5 V _{DC}		6 V _{DC}	V
Boost voltage	V _{DD1}	I _{DD1} = 300 μA, 5 x Boost	4 V _{DC}		5 V _{DC}	V
Boost voltage	V _{DD1}	I _{DD1} = 300 μA, 4 x Boost	3 V _{DC}		4 V _{DC}	V
Boost voltage	V _{DD2}	V _{CD2} = L, I _{DD2} = 1 mA	1.8 V _{DC}		2 V _{DC}	V
Boost voltage	V _{DD2}	V _{CD2} = H, I _{DD2} = 1 mA	2.7 V _{DC}		3 V _{DC}	V
Output voltage	V _T	R _{SEL} = H	13.5	15	16.5	V
Output voltage	V _T	R _{SEL} = L	11.25	12.5	13.75	V
Output voltage	V _S	R _{SEL} = H	4.5	5	5.5	V
Output voltage	V _S	R _{SEL} = L	3.6	4	4.4	V
★ V _{CC1} static current	I _{VCC1d}	V _{CC1} = 2.7 V, DCON, RGONG, RGONP = L			5	μA
★ V _{DC} static current	I _{VDCd}	V _{DC} = 2.5 V, DCON, RGONG, RGONP = L			5	μA
V _{REF} voltage			2.25	2.5	2.75	V

[MEMO]

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NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.