A Typical Microprocessor System
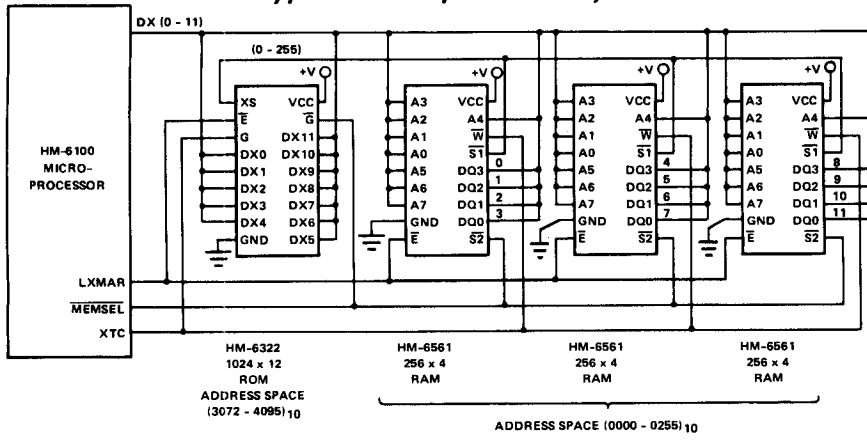

HM-6100 MICRO-PROCESSOR

DX (0 - 11)

(0 - 255)

HM-6322	HM-6561	HM-6561	HM-6561
1024 x 12	256 x 4	256 x 4	256 x 4
ROM	RAM	RAM	RAM
ADDRESS SPACE			
(3072 - 4095)$_{10}$			

ADDRESS SPACE (0000 - 0255)$_{10}$

3

Table 1 – CMOS Microprocessor Products

HARRIS PART NUMBER	DESCRIPTION	PAGE NUMBER
CPU/Controller Group		
HM-6100	12- Bit PDP -8/E* Microprocessor (CPU)	5-7
HD-6101	Peripheral Interface Element (PIE)	5-29

Table 2 – 6100 Compatible CMOS Memory Products

HARRIS PART NUMBER	DESCRIPTION	PAGE NUMBER
Read Only Memory		
HM-6322	1024 x 12 ROM	3-4
HM-6661	256 x 4 PROM	3-112
Random Access Memory	RAM	
HM-6512	64 x 12	3-42
HM-6561	256 x 4	3-78
HM-6518	1024 x 1	3-66

Table 3 – CMOS Interface Products

HARRIS PART NUMBER	DESCRIPTION	PAGE NUMBER
Communication Group		
HD-6402	Universal Asynchronous Receiver/Transmitter (UART)	4-7
HD-4702	Programmable Bit Rate Generator (BRG)	4-3
HD-6408	Asynchronous Serial Manchester Adapter	4-12
Bus Driver Group		
HD-6431	Hex Latched Bus Driver	4-28
HD-6432	Hex Bi-Directional Bus Driver	4-31
HD-6433	Quad Bus Separator/Driver	4-34
HD-6434	Octal Resettable Latched Bus Driver	4-37
HD-6435	Hex Resettable Latched Bus Driver	4-40
HD-6436	Octal Bus Buffer/Driver	4-43
HD-6440	One-of-Eight Latched Decoder/Driver	4-46
HD-6495	Hex Bus Buffer/Driver	4-50

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Table 4 – Microprocessor Support Systems

HARRIS PART NUMBER	DESCRIPTION	PAGE NUMBER
HB-61000	MICRO-12 Evaluation Board	6-4
HB-61001	4K by 12 Memory Board	6-8

*Digital Equipment Corp

General Purpose Registers Located in Memory — The first 128 words of each memory field (page 0, or the Register Page) can be used as general purpose registers. Since they are located in memory, the MRIs are used to manipulate them rather than a separate set of "register instructions".

Auto Increment Registers — When locations $10\text{-}17_8$ of the register page are used as operand addresses they are automatically incremented prior to each use.

IOTs — There is an entire class of Input/Output transfer instructions. Hardware interfacing of the CPU to the various peripherals is simple and straight forward.

Microcode — Accumulator operations can be microcoded to tailor the instruction set to a particular application.

Execution Times — Since the HM-6100 is a static device which can be operated at clock frequencies from 0 to 8MHz, the number of states required to execute each instruction is given.

Control Panel Memory — This has been included in the HM-6100 to simplify implementation of the control panel function in microcomputer systems. Its use is not, however, limited to that function in that the control panel interrupt request is a true non-maskable interrupt which accesses a program stored in Control Panel (CP) memory. As such, CP memory is valuable for functions such as system debug, system diagnostic programs, non-maskable interrupt routines, resident storage of frequently used for software, etc. It is in no way limited to "Control Panel Functions". The HM-6100 will execute programs in Control Panel Memory or Main Memory or a combination of both.

NOTE: In HM-6100 literature bit 0 refers to the MSB, bit 11 refers to the LSB. Data is represented in Two's Complement Integer notation. In this system, the negative of a number is formed by complementing each bit in the data word and adding "1" to the complemented number. The sign is indicated by the most significant bit. In the 12-bit word used by the HM-6100, when bit 0 is a "0", it denotes a positive number and when bit 0 is a "1", it denotes a negative number. The maximum number ranges for this system are 3777_8 (+2047) and 4000_8 (-2048).

System Flexibility

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Using the HM-6100 family, the designer has access to a comprehensive product line dedicated to satisfy his particular system requirements. He also has a very low cost reproduction of the PDP-8/E minicomputer whose existence is justified by a large product market base and a wealth of existing software. The wide range of CMOS memory products enable partitioning of the memory system in blocks from 64 to 4096 words of RAM and from 256 to 1024 words of ROM or PROM.
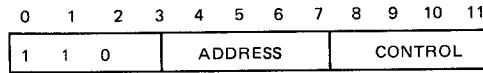
DEVELOPMENT SUPPORT

The 6100 CPU family is supported by the Harris, single-board, CMOS MICRO-12 microcomputer and by existing PDP-8 minicomputers and their low cost operating systems.

The HM-6100 communicates with the PIE and with peripherals through the PIE via IOT commands. During the IOTA cycle an instruction of the form 6XXX is loaded into all PIE instruction registers. The bits are interpreted as shown below.

The 5 address bits (3-7) are compared with the pin programmable select inputs SEL3, SEL4, SEL5, SEL6, SEL7 to address 1 of 31 possible PIEs. Address zero is reserved for IOT's internal to the HM-6100. The four control bits are decoded by the PIE to select one of 16 instructions which are described below.

PIE INSTRUCTION FORMAT

0	1	2	3	4	5	6	7	8	9	10	11
1	1	0	ADDRESS					CONTROL			

CONTROL	MNEMONICS	ACTION
0000 1000	READ1 READ2	The READ instructions generate a pulse on the appropriate read outputs. This signal is used by the peripheral device to gate onto the DX bus to be "OR'ed" with the HM-6100 accumulator data. The HM-6100 accumulator is cleared prior to reading peripheral data when $\overline{CO}$ is asserted low.
0001 1001	WRITE1 WRITE2	The WRITE instructions generate a pulse on the appropriate write output. This signal is used by peripherals to load the HM-6100 accumulator data on the DX lines into peripheral data registers. The HM-6100 AC is cleared after the write operation when the $\overline{CO}$ input is asserted low.
0010 0011 1010 1011	SKIP1 SKIP2 SKIP3 SKIP4	The SKIP instructions test the state of the sense flip flops. If the input conditions have set the sense flip flop, the PIE will assert the $\overline{SKP/INT}$ output causing the HM-6100 to skip the next program instruction. The sense flip flop is then cleared. If the sense flip flop is not set, the PIE not assert the $\overline{SKP/INT}$ output and the HM-6100 will execute the next instruction.
0100	RCRA	The Read Control Register A instruction gates the contents of CRA onto the DX lines during time 4 to be "OR" transferred to the HM-6100 AC.
0101 1101 1100	WCRA WCRB WVR	The Write Control Register A, Write Control Register B and Write Vector Register instructions transfer HM-6100 AC data on the DX lines during time 5 of IOTA into the appropriate register.
0110 1110	SFLAG1 SFLAG3	The SET FLAG instructions set the bits FL1 and FL3 in control register A to a high level. PIE outputs FLAG1 and FLAG3 follow the data stored in bits FL1 and FL3 of CRA.
0111 1111	CFLAG1 CFLAG3	The CLEAR FLAG instructions clear the bits FL1 and FL3 in control register A to a low level.
$(6007)_8$	CAF	HM-6100 internal IOT instruction CLEAR ALL FLAGS clears the interrupt requests by clearing the sense flip flops.

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Programmable Outputs

FLAGs (1-4) - The FLAGs are general purpose outputs that can be set and cleared under program control. GLAG1 follows bit FL1 in Control Register A and etc. FLAGs can be changed by loading new data into CRA via the WCRA commands. In addition, FLAG1 and FLAG3 can be set and cleared directly by the commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.

CONTROL REGISTER A (CRA)

The CRA can be read and written by the HM-6100 via the RCRA and WCRA commands.

The format and meaning of control bits are shown below.

FL (1-4) — Data on FLAG outputs corresponds to data in FL (1-4). Changing the FL bits under software control changes the corresponding FLAG outputs.

IE (1-4) — A high level on INTERRUPT ENABLE enables interrupts for the SENSE inputs.

Otherwise these inputs provide conditional skip testing as defined by the SKIP1-4 instructions.

WP (1-2) — A high level on WRITE POLARITY bits causes positive pulses at the WRITE outputs.

0	1	2	3	4	5	6	7	8	9	10	11
FL4	FL3	FL2	FL1	WP2	*	WP1	*	IE4	IE3	IE2	IE1
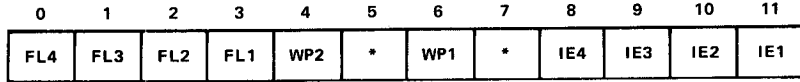
* = Don't Care

CONTROL REGISTER B (CRB)

The CRB can be written by the HM-6100 via the WCRB instruction. It has no read back capability. The format and meaning of control bits are shown.

SL (1-4) — A high level on the SENSE LEVEL bits causes the SENSE inputs to be level sensitive. A low level in the SL bits causes the SENSE inputs to be edge sensitive. An interrupt request is generated only if a sense line is set up to be edge sensitive and interrupts are enabled via the IE bits of CRA.

SP (1-4) — A high level on the SENSE POLARITY bits causes the flip flop to be set by high level or positive going edge. A low level causes the flip flop to be set by a low level or negative going edge.

0	1	2	3	4	5	6	7	8	9	10	11
SL4	SL3	SL2	SL1	SP4	SP3	SP2	SP1	*	*	*	*
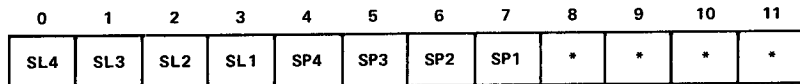
* = Don't Care

VECTOR REGISTER

A hardware priority network uniquely selects a PIE to provide a vectored address. The first IOT command of any type, after the HM-6100 signal INTERRUPT GRANT goes high, resets the INTGNT line to a low level. The INTGNT signal is used to freeze the priority network and enable vector generation. The highest priority PIE has PIN tied to V$_{CC}$. The lowest priority PIE is the last one on the chain. Within the PIE, SENSE1 has the highest priority and SENSE 4 has the lowest. The vector address generated by the PIE consists of 10 bits from the vector register and two bits that indicate the sense input within the highest priority PIE that generated the interrupt. If PIN is tied to GND, then the PIE will respond as a non-vectored interrupt device.

0	1	2	3	4	5	6	7	8	9	10	11
			VECTOR REGISTER							VPRI	
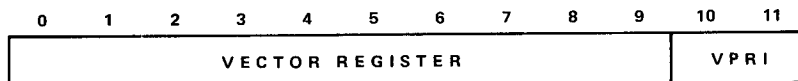
VPRI	CONDITIONS
00	SENSE 1
01	SENSE 2
10	SENSE 3
11	SENSE 4

IOT Considerations

The HM-6100 communicates with peripherals via input/output transfers (IOT) instructions. The first three bits, 0-2 are always set to 6_8 (110) to specify an IOT instruction. The next 9 bits, 3-11, are user definable and can provide a minimal implementation when each bit controls one operation. When following PDP-8/E format, the next six bits, 3-8, contain the device selection code that determines the specific I/O device for which the IOT instruction is intended and, therefore, permits interfaces with up to 63 I/O devices. The last three bits, 9-11, contain the operation specification code that determines the specific operation to be performed. The HD-6102 MEDIC utilizes the PDP-8/E format. When using the HD-6101 PIE and the HD-6103 PIO, bits 3-7 perform the device selection function and bits 8-11 provide the operation specification code.

IOT INSTRUCTION FORMAT

0	1	2	3	4	5	6	7	8	9	10	11
1	1	0	USER DEFINABLE BITS								
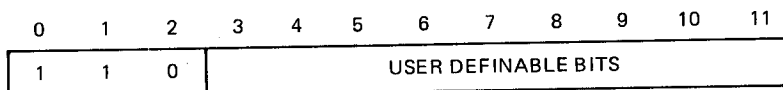
Basic IOT Instruction: 6XXX₈

0	1	2	3	4	5	6	7	8	9	10	11
1	1	0	DEVICE SELECTION						CONTROL		

PDP-8/E Format: 6NNX₈

0	1	2	3	4	5	6	7	8	9	10	11
1	1	0	DEVICE SELECTION					CONTROL			
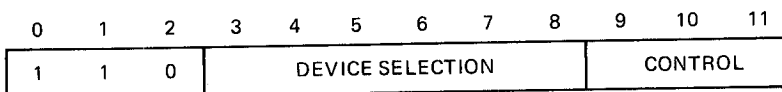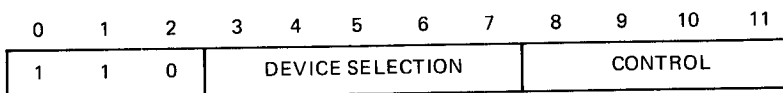
PIE and PIO Format

Care must be taken when building a system which uses all three peripheral interface devices from Harris to avoid conflicts with the device selection codes. Care also must be used when utilizing DEC compatible teletype and high speed reader interfaces in a system which includes PIE's and PIO's. The following table will assist in the assignment of device selection codes.

HM-6100 Microprocessor

The HM-6100 CMOS Microprocessor is a single address, fixed word length, parallel transfer 12 bit microprocessor. It is a member of a broad based CMOS product line which comprises 6100 peripheral devices, RAMs, PROMs, ROMS and a full logic family. The processor recognizes the PDP-8* instruction set and utilizes two's complement arithmetic logic. The device is completely static and may be operated from DC to its rated frequency. No external clock generators or controllers are required.

The support chips, Peripheral Interface Element (PIE), Universal Asynchronous Receiver Transmitter (UART), Bit Rate Generator, Read Only Memories (ROM), Random Access Memories (RAM) and Programmable Read Only Memories (PROM) are completely compatible with the microprocessor. All devices are available in either an industrial or a military temperature range.

* Trademark of Digital Equipment Corp., Maynard Ma.

Table of Instruction Set

BASIC INSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION
AND	0XXX	Logical AND
TAD	1XXX	Binary ADD
ISZ	2XXX	Increment, and skip if zero
DCA	3XXX	Deposit and clear AC
JMS	4XXX	Jump to subroutine
JMP	5XXX	Jump
IOT	6XXX	In/out transfer
OPR	7XXX	Operate

GROUP 1 OPERATE MICROINSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION	LOG SEQ
NOP	7000	No operation	1
IAC	7001	Increment accumulator	3
RAL	7004	Rotate accumulator left	4
RTL	7006	Rotate two left	4
RAR	7010	Rotate accumulator right	4
RTR	7012	Rotate two right	4
BSW	7002	Byte swap	4
CML	7020	Complement link	2
CMA	7040	Complement accumulator	2
CIA	7041	Complement and increment accum.	2,3
CLL	7100	Clear link	1
CLL RAL	7104	Clear link–rotate accum. left	1,4
CLL RTL	7106	Clear link–rotate two left	1,4
CLL RAR	7110	Clear link–rotate accum. right	1,4
CLL RTR	7112	Clear link–rotate two right	1,4
STL	7120	Set the link	1,2
CLA	7200	Clear accumulator	1
CLA IAC	7201	Clear accum. –increment accum.	1,3
GLK	7204	Get the link	1,4
CLA CLL	7300	Clear accumulator–clear link	1
STA	7240	Set the accumulator	1,2

GROUP 2 OPERATE MICROINSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION	LOG SEQ
NOP	7400	No operation	1
HLT	7402	Halt	3
OSR	7404	Or with switch register	3
SKP	7410	Skip	1
SNL	7420	Skip on non-zero link	1
SZL	7430	Skp on zero link	1
SZA	7440	Skip on zero accumulator	1
SNA	7450	Skip on non-zero accumulator	1
SZA SNL	7460	Skip on zero accum, or skip on non-zero link, or both	1
SNA SZL	7470	Skip on non-zero accum. and skip on zero link	1
SMA	7500	Skip on minus accumulator	1
SPA	7510	Skip on positive accumulator	1
SMA SNL	7520	Skip on minus accum, or skip on non-zero link or both	1
SPA SZL	7530	Skip on positive accum. and skip on zero link	1
SMA SZA	7540	Skip on minus accum. or skip on zero accum. or both	1
SPA SNA	7550	Skip on positive accum. and skip on non-zero accum.	1
SMA SZA SNL	7560	Skip on minus accum. or skip on zero accum. or skip on non-zero link or all	1
SPA SNA SZL	7570	Skip on positive accum. and skip on non-zero accum. and skip on zero link	1
CLA	7600	Clear accumulator	2
LAS	7604	Load accum. with switch register	1,3
SZA CLA	7640	Skip on zero accum. then clear accum.	1,2
SNA CLA	7650	Skip on non-zero accum. then clear accum.	1,2
SMA CLA	7700	Skip on minus accum. then clear accum.	1,2
SPA CLA	7710	Skip on positive accum. then clear accum.	1,2

GROUP 3 OPERATE MICROINSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION	LOG SEQ
NOP	7401	No operation	3
MQL	7421	MQ register load	2
MQA	7501	MQ register into accumulator	2
SWP	7521	Swap accum. and MQ register	3
CLA	7601	Clear accumulator	1
CAM	7621	Clear accum. and MQ register	3
ACL	7701	Clear accum. and load MQ register into accumulator	3
CLA SWP	7721	Clear accum. and swap accum. and MQ register	3

PROCESSOR IOT INSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION
SKON	6000	Skip if interruption on
ION	6001	Interrupt turn on
IOF	6002	Interrupt turn off
SRQ	6003	Skip If INT request
GTF	6004	Get flags
RTF	6005	Return flags
SGT	6006	Operation is determined by external devices, if any
CAF	6007	Clear all flags

Bit Assignments

MEMORY REFERENCE INSTRUCTION FORMAT

0	1	2	3	4	5	6	7	8	9	10	11
OP CODE 0-5				IA	IMP		ADDRESS				

PAGE
RELATIVE ADDRESS
INDIRECT ADDRESSING
0 = DIRECT
1 = INDIRECT
MEMORY PAGE
0 = PAGE 0
1 = CURRENT PAGE

GROUP 1

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	0	CLA	CLL	CMA	CML	RAR RTR	RAL RTL	0 1	IAC

LOGICAL SEQUENCES: 1 – CLA CLL
2 – CMA CML
3 – IAC
4 – RAR RAL RTR RTL BSW

BSW IF BITS 8 & 9
ARE 0 AND
BIT 10 IS 1

GROUP 2

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	1	CLA	SMA SPA	SZA SNA	SNL SZL	0 1	OSR	HLT	0

LOGICAL SEQUENCES: 1(Bit 8 is Zero) – SMA or SZA or SNL
(Bit 8 is One) – SPA and SNA and SZL
2 – CLA
3 – OSR HLT

GROUP 3

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	1	CLA	MQA	*	MQL	*	*	*	1

LOGICAL SEQUENCES: 1 – CLA
2 – MQA MQL
3 – ALL OTHERS

* DON'T CARE

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Specifications

CENTRAL PROCESSOR

HM-6100

- Crystal Controlled 2.45MHz
- Single Power Supply . . . . +5 Volts
- CMOS . . . . TTL Compatible

MEMORY

ROM — 1K x 12 Bits Monitor (Resident in control panel memory does not use user address space.)

RAM — 256 x 12 Bits (Expandable to 1K words.)

INTERFACES

SERIAL I/O: 20mA Current Loop TTY
RS-232 (Jumper Selectable)
Baud Rate 50 thru 9600 (Jumper Selectable)

BUS: CMOS Compatible (Dual 22 Pin Connector Provided)

PARALLEL I/O: 12 Bit Input (Optional)
12 Bit Output (Optional)
Large User Wirewrap Area Provided for Additional I/O

SOFTWARE

System monitor provided in ROM with resident keyboard, display and serial output control. Allows user to load, dump and display programs.

LITERATURE (Provided with Micro–12)

- Micro-12 User Manual
- Microprocessor Systems Design Manual
- Introduction to Programming
- Assembly Language Reference Card
- Introduction to DECUS

PHYSICAL CHARACTERISTICS

- Height . . . . 8.4 Inches
- Width . . . . 11.6 Inches
- Depth . . . . 0.75 Inches
- Weight . . . . 14 Oz.

ELECTRICAL CHARACTERISTICS

- V_{CC} = ... (+)5 Volts ±10%
- V_{TTY} = ... (-)12 Volts ±20%, 30mA
(Req. only if TTY is connected.)
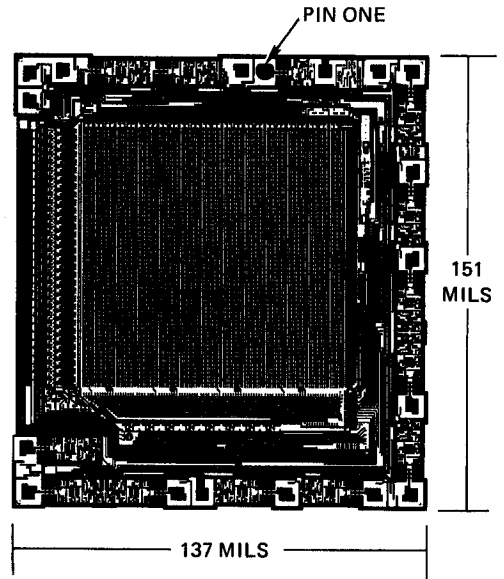- I_{CC} = ...40mA (System), 160mA (Display)

OPTIONS:

- 1K Memory
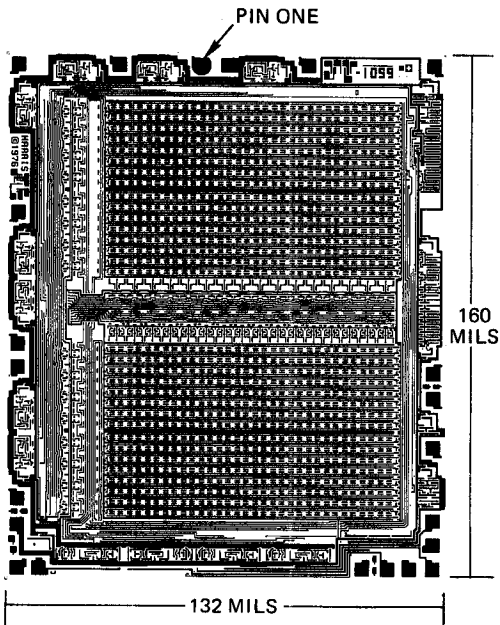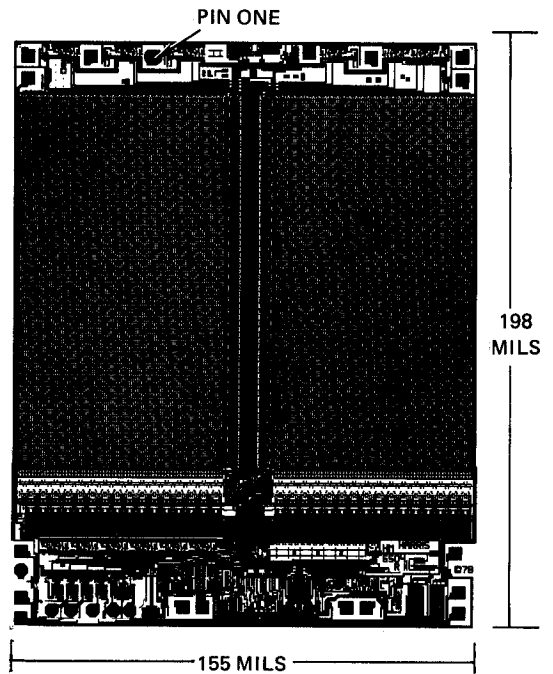- 4K Memory
- Parallel I/O
- Downloader Software

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18 HM-6100

PIN ONE

200 MILS

219 MILS

19 HM-6322

PIN ONE

151 MILS

137 MILS

20 HM-6501

PIN ONE

160 MILS

132 MILS

21 HM-6503, HM-6504

PIN ONE

198 MILS

155 MILS
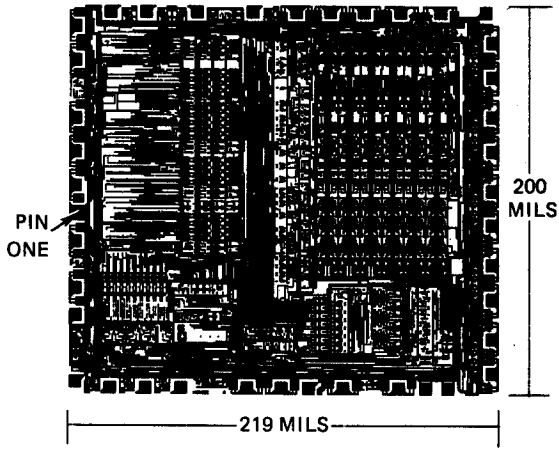
NOTE: OCTAGONAL PADS ARE NOT FOR BONDING.

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