Document order number: MC33480
Rev 2.0, 1/2006

Smart Front Corner Light Switch (Triple 10 mΩ and Dual 35 mΩ)

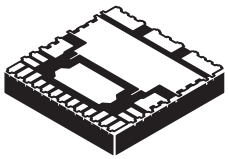
33480

HIGH-SIDE SWITCH

The 33480 is designed for low-voltage automotive and industrial lighting applications. Its five low $R_{DS(ON)}$ MOSFETs (three 10 mΩ, two 35 mΩ) can control the high sides of five separate resistive loads (bulbs).

Programming, control, and diagnostics are accomplished using a 16-bit SPI interface. Each output has its own PWM control via SPI. The 33480 has highly sophisticated failure mode handling to provide high availability of the outputs. Its multiphase control and output edge shaping improves electromagnetic compatibility (EMC) behavior.

The 33480 is packaged in a power-enhanced 12 x 12 nonleaded Power QFN package with exposed tabs.



Bottom View

PNASUFFIX
98ARL10596D
24-TERMINAL PQFN

Features

- Triple 10 mΩ and Dual 35 mΩ High-Side Switches
- 16-bit SPI Communication Interface with Daisy Chain Capability
- Current Sense Output with SPI-Programmable Multiplex Switch
- Digital Diagnosis Feature
- PWM Module with Multiphase Feature
- Fully Protected Switches
- Overcurrent Shutdown detection
- Power Net and Reverse Polarity Protection
- Low-Power Mode
- Fail Mode Functions including Autorestart feature
- External smart power switch control including current recopy

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
PC33480PNA/R2	-40°C to 125°C	24 PQFN

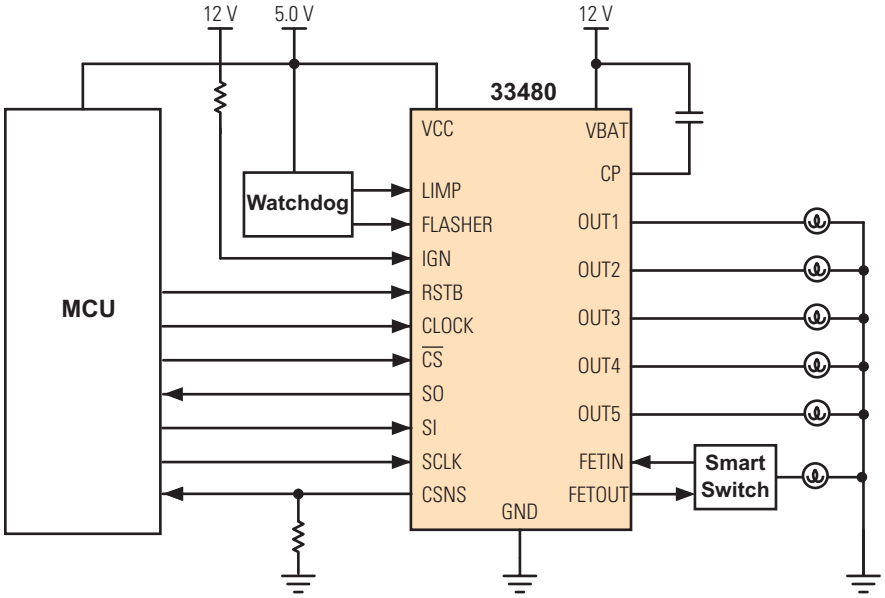


Figure 1. 33480 Simplified Application DiagraM

* This document contains information on a product under development.
Freescale reserves the right to change or discontinue this product without notice.

INTERNAL BLOCK DIAGRAM

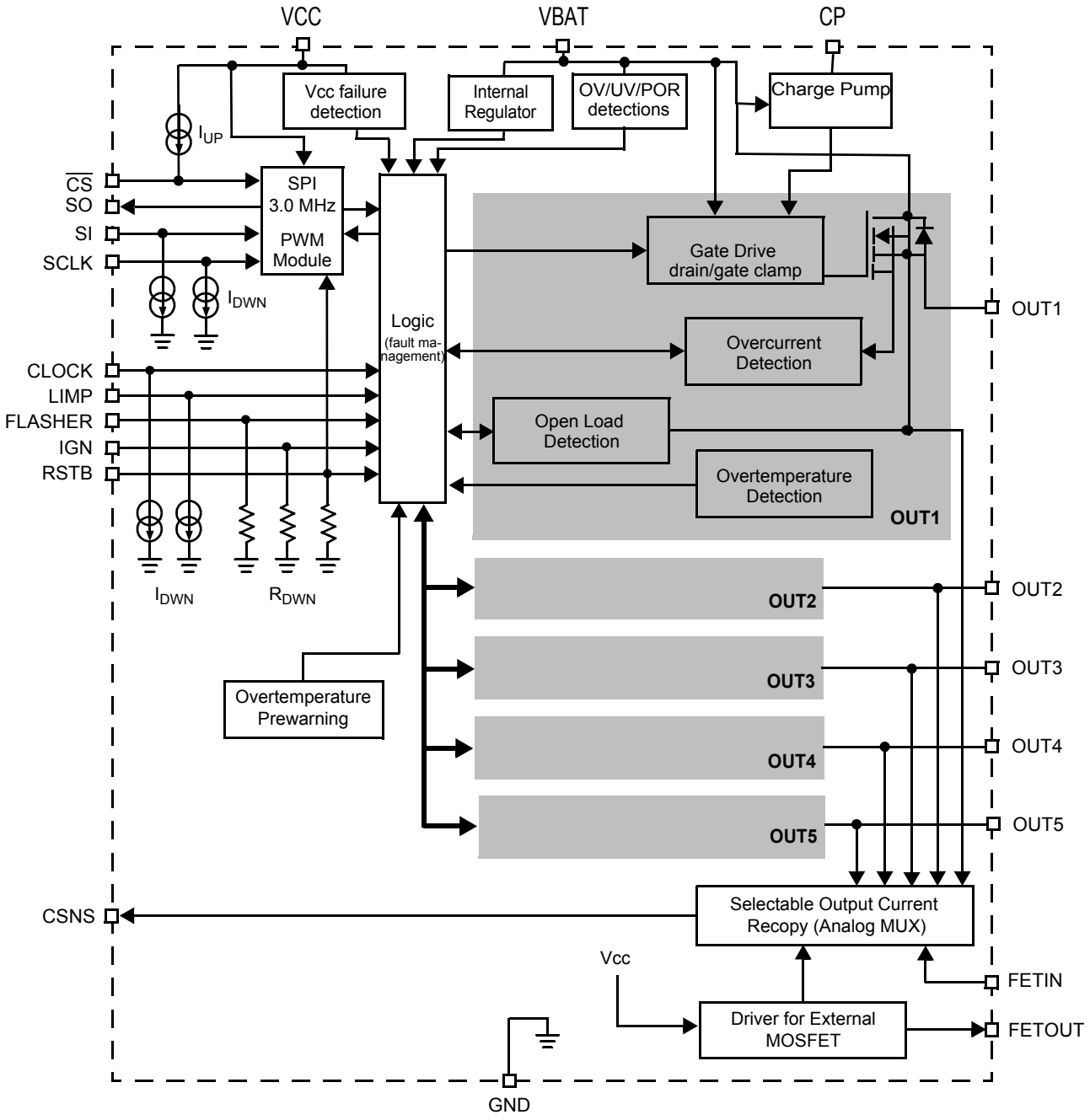


Figure 2. 33480 Simplified Internal Block Diagram

TERMINAL CONNECTIONS

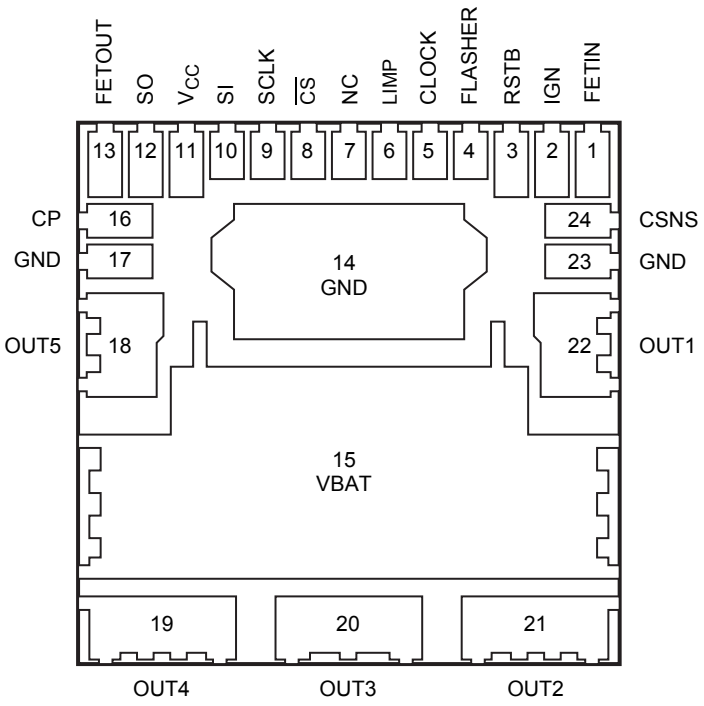


Figure 3. 33480 Terminal Connections (Transparent Top View Of Package)

Table 1. 33480 Terminal Definitions

A functional description of each terminal can be found in the Functional Terminal Description section beginning on Page 17.

Terminal Number	Terminal Name	Terminal Function	Formal Name	Definition
1	FETIN	Input	External FET Input	This terminal is the current sense recopy of the external SMART MOSFET.
2	IGN	Input	Ignition Input (Active High)	This input wakes the device. It also controls the Outputs 1 and 2 in case of Fail mode activation. This terminal has a passive internal pulldown.
3	RSTB	Input	Reset	This input wakes the device. It is also used to initialize the device configuration and fault registers through SPI. This digital terminal has a passive internal pulldown.
4	FLASHER	Input	Flasher Input (Active High)	This input wakes the device. The Fail mode can be activated by this digital input. This terminal has a passive internal pulldown.
5	CLOCK	Input	Clock Input	The PWM frequency and timing are generated from this digital clock input by the PWM module. This terminal has an active internal pulldown current source.
6	LIMP	Input	Limp Home Input (Active High)	The Fail mode can be activated by this digital input. This terminal has an active internal pulldown current source.
7	NC	NC	No Connect	No internal connection to this terminal.
8	$\overline{CS}$	Input	Chip Select (Active Low)	When this digital signal is high, SPI signals are ignored. Asserting this terminal low starts an SPI transaction. The transaction is signaled as completed when this signal returns high. This terminal has an active internal pullup current source.
9	SCLK	Input	SPI Clock Input	This digital input terminal is connected to the master microcontroller providing the required bit shift clock for SPI communication. This terminal has an active internal pulldown current source.

Table 1. 33480 Terminal Definitions (continued)

A functional description of each terminal can be found in the Functional Terminal Description section beginning on Page 17.

Terminal Number	Terminal Name	Terminal Function	Formal Name	Definition
10	SI	Input	Master-Out Slave-In	This data input is sampled on the positive edge of the SCLK. This terminal has an active internal pulldown current source.
11	VCC	Power	Logic Supply	SPI Logic power supply.
12	SO	Output	Master-In Slave-Out	SPI data is sent to the MCU by this terminal. This data output changes on the negative edge of SCLK and when $\overline{CS}$ is high, this terminal is high impedance.
13	FETOUT	Output	External FET Gate	This terminal controls an external SMART MOSFET by logic level. This output is also called OUT6.
14,17,23	GND	Ground	Ground	This terminal is the ground for the logic and analog circuitry of the device(1).
15	VBAT	Power	Battery Input	Power supply terminal.
16	CP	Output	Charge Pump	This terminal is the connection for an external tank capacitor (for internal use only).
18 22	OUT1 OUT5	Output	Output 1 Output 5	Protected 35 mΩ high-side power output to the load.
19 20 21	OUT2 OUT3 OUT4	Output	Output 2 Output 3 Output 4	Protected 10 mΩ high-side power output to the load.
24	CSNS	Output	Current Sense Output	This terminal is used to output a current proportional to OUT1:OUT5, FETin current, and it is used externally to generate a ground-referenced voltage for the microcontroller to monitor output current. OUT1:OUT5 and FETin choice is SPI programmable.

Notes

1. The pins 14, 17 and 23 must be shorted on the board.

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Overvoltage Test Range (all OUT[1:5] ON with nominal DC current) 2.0 Hours @ 25°C 1.0 Min @ 25°C Load Dump (400 ms) @ 25°C	V_{BAT}	 20 27 40	V
Reverse Polarity Voltage Range (all OUT[1:5] ON with nominal DC current) 2.0 Min @ 25°C	V_{BAT}	 -15	V
V_{CC} Supply Voltage	V_{CC}	-0.3 to 5.5	V
OUT[1:5] Voltage Positive Negative (ground disconnected)	V_{OUT}	 40 -16	V
Digital Input Current in Clamping Mode (SI, SCLK, $\overline{CS}$, IGN, FLASHER, LIMP)	I_{IN}	5.0	mA
SO and FETOUT Outputs Voltage	V_{SO}	-0.3 to V_{CC}+0.3	V
FETin Input Current	I_{FETin}	10	mA
Outputs clamp energy using single pulse method (L=2mH; R=0; Vbat=14V @150°C initial) OUT[1,5] OUT[2:4]	 $E_{1,5}$ $E_{2,3,4}$	 85 300	mJ
ESD Voltage (2) Human Body Model (HBM) Human Body Model (HBM) OUT [1:5] Charge Device Model (CDM)	V_{ESD}	 ±2kV ±8kV TBD	V
THERMAL RATINGS			
Operating Temperature Ambient Junction	 T_A T_J	 -40 to 125 -40 to 150	°C
Peak Terminal Re-flow Temperature During Solder Mounting (3)	T_{SOLDER}	260	°C
Storage Temperature	T_{STG}	-55 to 150	°C
THERMAL RESISTANCE			
Thermal Resistance, Junction to Case (4)	$R_{\theta JC}$	1.0	°K/W

Notes

2. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω) and the Charge Device Model.
3. Terminal soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device. If the qualification fails, T_{SOLDER} will be changed for 240°C.
4. Typical value guaranteed per design.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUTS (VBAT, VCC)					
Battery Supply Voltage Range	V_{BAT}				V
Full Performance & Short Circuit		7.0	–	18.0	
Extended Voltage Range (5)		6.0	–	20.0	
Battery Supply Undervoltage (UV flag is set ON)	V_{BATUV}	5.0	5.3	6.0	V
Battery Voltage Clamp (OV flaf is set ON)	$V_{BATCLAMP}$	41.0	47.0	53.0	V
Battery Supply Power on Reset (If Vbat < 5.5V, Vbat = Vcc)	V_{BATPOR}	–	4.2	5.0	V
V_{BAT} Supply Current @ 25°C and V_{BAT} = 12 V and V_{CC} = 5 V					
Sleep State Current	$I_{BATSLEEP}$	–	0.5	5.0	µA
Normal Mode, IGN=5V, RSTB=5V, Outputs Open	I_{BAT}	–	10.0	20.0	mA
Digital Supply Voltage Range, Full Performance	V_{CC}	4.5	–	5.5	V
Digital Supply Undervoltage (VCC Failure)	V_{CCUV}	2.5	3.0	3.5	V
Standby Current Consumption on V_{CC} @ 25°C and V_{BAT} = 12 V	I_{QCC}				µA
Output OFF		–	TBD	5.0	
Supply Current Consumption on V_{CC} and V_{BAT} = 12 V	I_{CC}				mA
No SPI		–	–	1.0	
3.0 MHz SPI Communication		–	–	5.0	
LOGIC INPUT/OUTPUT (IGN, $\overline{CS}$, CSNS, SI, SCLK, CLOCK, SO, FLASHER, RSTB, LIMP)					
Input High Logic Level (6)	V_{IH}	0.7	–	–	Vcc
Input Low Logic Level (6)	V_{IL}	–	–	0.3	Vcc
Ignition Threshold Level (IGN)	V_{IGNth}	2.0	–	4.0	V
Input Clamp Voltage (IGN)	V_{IGNcl}				V
I_{IGN} < 2.5 mA		7.0	–	14.0	
Input Forward Voltage (IGN)	V_{IGNfr}				V
I_{IGN} = -2.5 mA		-2.0	–	-0.3	
Input Active Pulldown Current for LIMP, SI, SCLK and CLOCK inputs	I_{DWN}	5.0	–	20.0	µA
Input Active Pullup Current ($\overline{CS}$)	I_{UP}	5.0	–	20.0	µA
Input Passive Pulldown Resistance (7)	R_{DWN}	100	200	400	kΩ
SO High-State Output Voltage	V_{SOH}				
I_{OH} = 1.0 mA		0.8	TBD	–	Vcc
SO Low-State Output Voltage	V_{SOL}				V
I_{OL} = -1.6 mA		–	0.2	0.4	

Notes

5. In extended mode, the functionality is guaranteed but not the electrical parameters.
6. Valid for RSTB, SI, SCLK, CLOCK, FLASHER and LIMP terminals.
7. Valid for FLASHER, IGN and RSTB terminals.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INPUT/OUTPUT (IGN, $\overline{CS}$, CSNS) (CONTINUED)					
SO Tri-State Leakage Current $\overline{CS}$ ≥ 0.7 V_{CC}	I_{SOLEAK}	 -1.0	 0.0	 1.0	µA
Current Sense Output Clamp Voltage $I_{CSNS<10mA}$	V_{CSNS}	5.0	6.0	7.0	V
OUTPUTS (OUT 1-5)					
Output Negative Clamp Voltage I_{OUT} = - 500 mA, Outputs OFF	V_{OUT}	 -20.0	 –	 -16.0	V
Drain to Source Clamp Voltage I_{OUT} = + 500 mA, Outputs shorted to ground I_{OUT} =OCHI, this parameter is guaranteed by design	$V_{DSCLAMP}$	 41.0	 47.0	 53.0	V
Current Sense Output Precision (8) Full-Scale Range (FSR) 0.75 FSR 0.50 FSR 0.25 FSR 0.10 FSR	I_{CS}/I_{CS}	 – – – –	 TBD TBD TBD TBD	 TBD TBD TBD TBD	%
Temperature Drift of Current Sense Output (9) V_{BAT}=13.5V, $I_{OUT1,5}$=2.8 A, I_{OUT2-4}=5.5 A, reference taken at T_A=25°C	$\Delta I_{CS}/\Delta T$	–	TBD	±400	ppm/°C
Over Temperature Shutdown	T_{OTS}	160	175	190	°C
Thermal PreWarning	$T_{OTSWARN}$	110	125	140	°C
PARKING LIGHT OUT1					
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, T_A = 25°C) V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)}$	 – –	 – –	 35 55	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, V_{BAT} = 13.5 V, T_A = 150°C) (10)	$R_{DS(ON)}$	 –	 –	 59.5	mΩ
Reverse Output ON Resistance (I_{OUT} = -2.8 A, T_A = 25°C) (11) V_{BAT} = -12 V	$R_{SD(ON)}$	 –	 –	 70	mΩ
High Over Current Shutdown Threshold 1 (10) V_{BAT} = 16 V, T_A = -40°C V_{BAT} = 16 V, T_A = 25°C V_{BAT} = 16 V, T_A = 125°C	I_{OCHI1}	27.7 TBD TBD TBD	34.6 TBD 34.6 TBD	38.9 TBD TBD TBD	A

Notes

8. T_A = 25°C. $\delta I_{CS}/I_{CS=}$ (measured I_{CS} - targeted I_{CS})/ targeted I_{CS} with targeted I_{CS}=5mA
9. Based on statistical data. Not production tested. $\Delta I_{CS}/\Delta T_=$ [(measured I_{CS} at T_1 - measured I_{CS} at T_2) / measured I_{CS} at room] / (T_1 - T_2)
10. Parameter guaranteed by design; however, it is not production tested.
11. Source-to-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{BAT}.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
PARKING LIGHT OUT1(CONTINUED)					
High Over Current Shutdown Threshold 2	I_{OCHI2}	11.9	14.9	17.9	A
Low Over Current Shutdown Threshold	I_{OCLO}	5.6	6.7	7.7	A
Open Load Current Threshold in ON State (12)	I_{OL}	0.05	0.2	0.5	A
Open Load Current Threshold in ON State with LED (13) V_{OUT} = V_{BAT} - 0.5 V	I_{OLLED}	 5.0	 10.0	 20.0	mA
Current Sense Full-Scale Range (14)	$I_{CS\ FSR}$	–	6.0	–	A
Severe short-circuit impedance detection for Vbat=20V without artificial network (15)	$R_{SC1(OUT1)}$	TBD	–	–	mΩ
Severe short-circuit impedance detection for Vbat=20V with artificial network L=10µH, R=20mohm (15)	$R_{SC2(OUT1)}$	TBD	–	–	mΩ
LOW BEAM OUT2					
Output Drain-to-Source ON Resistance (I_{OUT} = 5.5 A, T_A = 25°C) V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)}$	 – –	 – –	 10 15	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, V_{BAT} = 13.5 V, T_A = 150°C) (15)	$R_{DS(ON)}$	 –	 –	 17.0	mΩ
Reverse Source-to-Drain ON Resistance (I_{OUT} = -2.8 A, T_A = 25°C) (16) V_{BAT} = -12 V	$R_{SD(ON)}$	 –	 –	 20	mΩ
High Over Current Shutdown Threshold 1(15) V_{BAT} = 16 V, T_A = -40°C V_{BAT} = 16 V, T_A = 25°C V_{BAT} = 16 V, T_A = 125°C	I_{OCHI1}	61.6 TBD TBD TBD	77.0 TBD 77.0 TBD	92.4 TBD TBD TBD	A
High Over Current Shutdown Threshold 2	I_{OCHI2}	26.5	33.2	39.8	A
Low Over Current Shutdown Threshold Optional Xenon Bulb Optional H7 Bulb	I_{OCLO}	 18.6 12.4	 22.2 14.8	 25.8 17.2	A
Open Load Current Threshold in ON State (17)	I_{OL}	0.1	0.4	1.0	A
Open Load Current Threshold in ON State with LED (18) V_{OL} = V_{BAT} - 0.5 V	I_{OLLED}	 5.0	 10.0	 20.0	mA
Current Sense Full-Scale Range(19) Optional Xenon Bulb Optional H7 Bulb	$I_{CS\ FSR}$	 – –	 20.0 13.3	 – –	A

Notes

12. OLLED1, bit D0 in SI data is set to [0].
13. OLLED1, bit D0 in SI data is set to [1].
14. For typical value of $I_{CS\ FSR}$, I_{CSNS} = 5.0 mA. If the range is exceeded, no current clamp and the precision is no more guaranteed.
15. Parameter guaranteed by design; however, it is not production tested.
16. Source-to-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{BAT}..
17. OLLED2, bit D1 in SI data is set to [0].
18. OLLED2, bit D1 in SI data is set to [1].
19. For typical value of $I_{CS\ FSR}$, I_{CSNS} = 5.0 mA. If the range is exceeded, no current clamp and the precision is no more guaranteed

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LOW BEAM OUT2 (continued)					
Severe short-circuit impedance detection for Vbat=20V without artificial network (20)	$R_{SC1(OUT2)}$	TBD	–	–	mΩ
Severe short-circuit impedance detection for Vbat=20V with artificial network L=10µH, R=20mohm (20)	$R_{SC2(OUT2)}$	TBD	–	–	mΩ
HIGH BEAM OUT3					
Output Drain-to-Source ON Resistance (I_{OUT} = 5.5 A, T_A = 25°C) V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25}$	 – –	 – –	 10 15	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, V_{BAT} = 13.5 V, T_A = 150°C) (20)	$R_{DS(ON)150}$	–	–	17.0	mΩ
Reverse Source-to-Drain ON Resistance (I_{OUT} = -2.8 A, T_A = 25°C) (21) V_{BAT} = -12 V	$R_{SD(ON)25}$	–	–	20	mΩ
High Over Current Shutdown Threshold 1 V_{BAT} = 16 V, T_A = -40°C V_{BAT} = 16 V, T_A = 25°C V_{BAT} = 16 V, T_A = 125°C	I_{OCHI1} I_{OCHI1_40} I_{OCHI1_25} I_{OCHI1_125}	61.6 TBD TBD TBD	77.0 TBD 77.0 TBD	92.4 TBD TBD TBD	A
High Over Current Shutdown Threshold 2	I_{OCHI2}	26.5	33.2	39.8	A
Low Over Current Shutdown Threshold	I_{OCLO}	12.4	14.8	17.2	A
Open Load Current Threshold in ON State (22)	I_{OL}	0.1	0.4	1.0	A
Open Load Current Threshold in ON State with LED (23) V_{OL} = V_{BAT} - 0.5 V	I_{OLLED}	5.0	10.0	20.0	mA
Current Sense Full-Scale Range (24)	$I_{CS\ FSR}$	–	13.3	–	A
Severe short-circuit impedance detection for Vbat=20V without artificial network (20)	$R_{SC1(OUT3)}$	TBD	–	–	mΩ
Severe short-circuit impedance detection for Vbat=20V with artificial network L=10µH, R=20mohm (20)	$R_{SC2(OUT3)}$	TBD	–	–	mΩ

Notes

20. Parameter guaranteed by design; however, it is not production tested.
21. Source-to-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{BAT}.
22. OLLED3, bit D2 in SI data is set to [0].
23. OLLED3, bit D2 in SI data is set to [1].
24. For typical value of $I_{CS\ FSR}$, I_{CSNS} = 5.0 mA. If the range is exceeded, no current clamp and the precision is no more guaranteed.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
FOG LIGHT OUT4					
Output Drain-to-Source ON Resistance (I_{OUT} = 5.5 A, T_A = 25°C) V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25}$	 – –	 – –	 10 15	mΩ
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, V_{BAT} = 13.5 V, T_A = 150°C) (25)	$R_{DS(ON)150}$	–	–	17.0	mΩ
Reverse Source-to-Drain ON Resistance (I_{OUT} = -2.8 A, T_A = 25°C) (26) V_{BAT} = -12 V	$R_{SD(ON)25}$	–	–	20	mΩ
High Over Current Shutdown Threshold 1 (25) V_{BAT} = 16 V, T_A = -40°C V_{BAT} = 16 V, T_A = 25°C V_{BAT} = 16 V, T_A = 125°C	I_{OCHI1} I_{OCHI1_40} I_{OCHI1_25} I_{OCHI1_125}	61.6 TBD TBD TBD	77.0 TBD 77.0 TBD	92.4 TBD TBD TBD	A
High Over Current Shutdown Threshold 2	I_{OCHI2}	26.5	33.2	39.8	A
Low Over Current Shutdown Threshold	I_{OCLO}	12.4	14.8	17.2	A
Open Load Current Threshold in ON State (27)	I_{OL}	0.1	0.4	1.0	A
Open Load Current Threshold in ON State with LED (28) V_{OL} = V_{BAT} - 0.5 V	I_{OLLED}	5.0	10.0	20.0	mA
Current Sense Full-Scale Range (29)	$I_{CS\ FSR}$	–	13.3	–	A
Severe short-circuit impedance detection for Vbat=20V without artificial network (25)	$R_{SC1(OUT4)}$	TBD	–	–	mΩ
Severe short-circuit impedance detection for Vbat=20V with artificial network L=10µH, R=20mohm (25)	$R_{SC2(OUT4)}$	TBD	–	–	mΩ
FLASHER OUT5					
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, T_A = 25°C) V_{BAT} = 13.5 V V_{BAT} = 7.0 V	$R_{DS(ON)25}$	 – –	 – –	 35 55	mΩ

Notes

25. Parameter guaranteed by design; however, it is not production tested.
26. Source-to-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{BAT}.
27. OLLED4, bit D3 in SI data is set to [0].
28. OLLED4, bit D3 in SI data is set to [1].
29. For typical value of $I_{CS\ FSR}$, I_{CSNS} = 5.0 mA. If the range is exceeded, no current clamp and the precision is no more guaranteed.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
FLASHER OUT5 (CONTINUED)					
Output Drain-to-Source ON Resistance (I_{OUT} = 2.8 A, V_{BAT} = 13.5 V, T_A = 150°C) (30)	$R_{DS(ON)150}$	–	–	59.5	mΩ
Reverse Source-to-Drain ON Resistance (I_{OUT} = -2.8 A, T_J = 25°C) (31) V_{BAT} = -12 V	$R_{SD(ON)25}$	–	–	70	mΩ
High Over Current Shutdown Threshold 1 (30) V_{BAT} = 16 V, T_A = -40°C V_{BAT} = 16 V, T_A = 25°C V_{BAT} = 16 V, T_A = 125°C	I_{OCHI1} I_{OCHI1_40} I_{OCHI1_25} I_{OCHI1_125}	27.7 TBD TBD TBD	34.6 TBD 34.6 TBD	38.9 TBD TBD TBD	A
High Over Current Shutdown Threshold 2	I_{OCHI2}	11.9	14.9	17.9	A
Low Over Current Shutdown Threshold	I_{OCLO}	5.6	6.7	7.7	A
Open Load Current Threshold in ON State (32)	I_{OL}	0.05	0.2	0.5	A
Open Load Current Threshold in ON State with LED (33) V_{OL} = V_{BAT} - 0.5 V	I_{OLLED}	5.0	10.0	20.0	mA
Current Sense Full-Scale Range (33)	$I_{CS\ FSR}$	–	6.0	–	A
Severe short-circuit impedance detection for Vbat=20V without artificial network (30)	$R_{SC1(OUT5)}$	TBD	–	–	mΩ
Severe short-circuit impedance detection for Vbat=20V with artificial network L=10µH, R=20mohm (30)	$R_{SC2(OUT5)}$	TBD	–	–	mΩ
SPARE FETOUT / FETIN					
FETout Output High Level @ I = 1.0 mA	$V_{H\ MAX}$	0.8	–	–	V_{CC}
FETout Output Low Level @ I = -1.0 mA	$V_{H\ MIN}$	–	0.2	0.4	V
FETin Input Full Scale Range Current	I_{FETin}	–	5.0	–	mA
FETin Input Clamp Voltage I_{FETin}= 5mA, CSNS open	V_{CLIN}	5.3	–	7.0	V
Drop Voltage on FETin (FETin - CSNS) I_{FETin}= 5mA, CSNS = 5V	V_{DRIN}	0.0	–	0.3	V

Notes

30. Parameter guaranteed by design; however, it is not production tested.
31. Source-to-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{BAT}.
32. OLLED5, bit D4 in SI data is set to [0].
33. OLLED5, bit D4 in SI data is set to [1].
34. For typical value of $I_{CS\ FSR}$, I_{CSNS} = 5.0 mA. If the range is exceeded, no current clamp and the precision is no more guaranteed.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUTS TIMING (OUT1 to OUT5)					
Current Sense rising and falling Settling Time on resistive load only (Maximum Value, 5%)	t_{R5} / t_{F5}	–	2	10	µs
Current Sense rising and falling Settling Time on resistive load only (Maximum Value, 1%)	t_{R1} / t_{R5}	–	TBD	TBD	µs
Driver Output Positive Slew Rate (30% to 70% @ V_{BAT} = 14 V) I_{OUT} = 2.8 A for OUT1 and OUT5 I_{OUT} = 5.5 A for OUT2, OUT3, and OUT4	SR_R	 0.2 0.2	 0.4 0.4	 0.8 0.8	V/µs
Driver Output Negative Slew Rate (70% to 30% @ V_{BAT} = 14 V) I_{OUT} = 2.8 A for OUT1 and OUT5 I_{OUT} = 5.5 A for OUT2, OUT3, and OUT4	SR_F	 0.2 0.2	 0.4 0.4	 0.8 0.8	V/µs
Driver Output Matching Slew Rate (SR_R /SR_F) (70% to 30% @ V_{BAT} = 14 V @25°C) I_{OUT} = 2.8 A for OUT1 and OUT5 I_{OUT} = 5.5 A for OUT2, OUT3, and OUT4	ΔSR	 0.8 0.8	 1.0 1.0	 1.2 1.2	
Driver Output Turn-ON Delay (SPI ON Command [No PWM, $\overline{CS}$ Positive Edge] to Output = 50% V_{BAT} @ V_{BAT} = 14 V) (I_{OUT} = 2.8 A for OUT1 and OUT5 I_{OUT} = 5.5 A for OUT2, OUT3, and OUT4	t_{DLYON}	 40 40	 80 80	 160 (TBC) 160 (TBC)	µs
Driver Output Turn-OFF Delay (SPI OFF command [$\overline{CS}$ Positive Edge] to Output = 50% V_{BAT} @ V_{BAT} = 14 V) (see Figure4, p14) I_{OUT} = 2.8 A for OUT1 and OUT5 I_{OUT} = 5.5 A for OUT2, OUT3, and OUT4	t_{DLYOFF}	 40 40	 80 80	 160 (TBC) 160 (TBC)	µs
Driver Output Matching Time ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$) @ Output = 50% V_{BAT} with V_{BAT} = 14 V, f_{PWM} = 240 Hz, δ_{PWM} = 50%, @25°C I_{OUT} = 2.8 A for OUT1 and OUT5 I_{OUT} = 5.5 A for OUT2, OUT3, and OUT4	Δt_{RF}	 -25 -25	 0 0	 25 25	µs
PWM MODULE					
PWM Frequency Range	f_{PWM}	60.0	–	240.0	Hz
Clock Input Frequency Range	f_{CLK}	7.68	–	30.72	kHz
Output PWM Duty Cycle maximum range for 11V<Vbat<18V (35)	PWM_MAX	4.0	–	96.0	%
Output PWM Duty Cycle linear range for 11V<Vbat<18V (36)	PWM_LIN	6.2 (TBC)	–	96.0 (TBC)	%
WATCHDOG TIMING					
Watchdog Timeout (SPI Failure)	t_{WDTO}	50	75	100	ms
I/O PLAUSIBILITY CHECK TIMING					
Fault Shutdown Delay Time (from Overtemperature or OCHI1 or OCHI2 or OCLO Fault Detection to Output = 50% V_{BAT} without round shaping feature for turn off)	t_{SD}	–	7	30	µs

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
I/O PLAUSIBILITY CHECK TIMING (CONTINUED)					
High Overcurrent Threshold Time 1 for OUT1 and OUT5 for OUT2:4	 t_{OUT1} t_{OUT2}	 7 14	 10 20	 13 26	ms
High Overcurrent Threshold Time 2 for OUT1 and OUT5 for OUT2:4	 t_{OUT1} t_{OUT2}	 52.5 105	 75 150	 97.5 195	ms
Autorestart Period for OUT1 and OUT5 for OUT2	 $t_{AUTORST-T1}$ $t_{AUTORST-T2}$	 52.5 105	 75 150	 97.5 195	ms
Autorestart Overcurrent Shutdown Delay Time for OUT1 and OUT5 for OUT2	 $t_{OCHIARS}$ $t_{OCHIARS}$	 3.5 7.0	 5.0 10.0	 6.5 13.0	ms
Limp Home Input pin Deglicher Time	t_{LIMP}	7.0	10.0	13.0	ms
Cyclic Open Load Detection Timing with LED (37)	t_{OLLED}	105	150	195	ms
Flasher Toggle Timeout	$t_{FLASHER}$	1.4	TBD	TBD	s
Ignition Toggle Timeout	$t_{IGNITION}$	1.4	TBD	TBD	s
Clock Input Low Frequency Detection Range	$f_{LCLK\ det}$	1.0	2.0	4.0	kHz
Clock Input High Frequency Detection Range	$f_{HCLK\ det}$	100	200	400	kHz

Notes

35. The PWM ratio is measured at Vout = 50% of V_{BAT} in nominal range of PWM frequency (from 60Hz to 200Hz). It is possible to put the device fully on (PWM duty cycle = 100%) and fully off (PWM duty cycle = 0%). Between 4%-96%, $OCHI_{1,2}$, OCLO and open load are available in ON state.See Figure 4, Input Timing Switching Characteristics
36. Linear range is defined by output duty cycle to SPI duty cycle configuration +/-1 LSB. For values outside linear duty cycle range, a calibration curve is available.
37. IOLLEDn bit (where “n” corresponds to respective outputs 1 through 5) in SI data is set to logic [1]. Refer to Table 8, Serial Input Address and Configuration Bit Map, page 28.

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 4.5 V ≤ V_{CC} ≤ 5.5 V, 7.0 V ≤ V_{BAT} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI INTERFACE CHARACTERISTICS					
Maximum Frequency of SPI Operation	f_{SPI}	–	–	3.0	MHz
Rising Edge of $\overline{CS}$ to Falling Edge of $\overline{CS}$ (Required Setup Time) (38)	$t_{\overline{CS}}$	–	–	300	ns
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (Required Setup Time) (38)	t_{LEAD}	–	50	167	ns
Required High State Duration of SCLK (Required Setup Time) (38)	t_{WSCLKh}	–	–	167	ns
Required Low State Duration of SCLK (Required Setup Time) (38)	t_{WSCLKl}	–	–	167	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ (Required Setup Time) (38)	t_{LAG}	–	50	167	ns
SI to Falling Edge of SCLK (Required Setup Time) (39)	$t_{SI(SU}$	–	25	83	ns
Falling Edge of SCLK to SI (Required Setup Time) (39)	t_{SIHOLD}	–	25	83	ns
SO Rise Time C_L = 200 pF	t_{RSO}	–	25	50	ns
SO Fall Time C_L = 200 pF	t_{FSO}	–	25	50	ns
SI, $\overline{CS}$, SCLK, Incoming Signal Rise Time (39)	t_{RSI}	–	–	50	ns
SI, $\overline{CS}$, SCLK, Incoming Signal Fall Time (39)	t_{FSI}	–	–	50	ns
Time from Falling Edge of $\overline{CS}$ to SO Low Impedance (40)	$t_{SO(EN)}$	–	–	145	ns
Time from Rising Edge of $\overline{CS}$ to SO High Impedance (41)	$t_{SO(DIS)}$	–	65	145	ns
Time from Rising Edge of SCLK to SO Data Valid (42) 0.2 V_{cc} ≤ SO ≥ 0.7 V_{cc}, C_L = 200 pF	t_{VALID}	–	65	105	ns

Notes

38. Maximum setup time required for the 33480 is the minimum guaranteed time needed from the microcontroller.
39. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
40. Time required for output status data to be available for use at SO. 1.0 kΩ on pullup on $\overline{CS}$.
41. Time required for output status data to be terminated at SO. 1.0 kΩ on pullup on $\overline{CS}$.
42. Time required to obtain valid data out from SO following the rise of SCLK.

TIMING DIAGRAMS

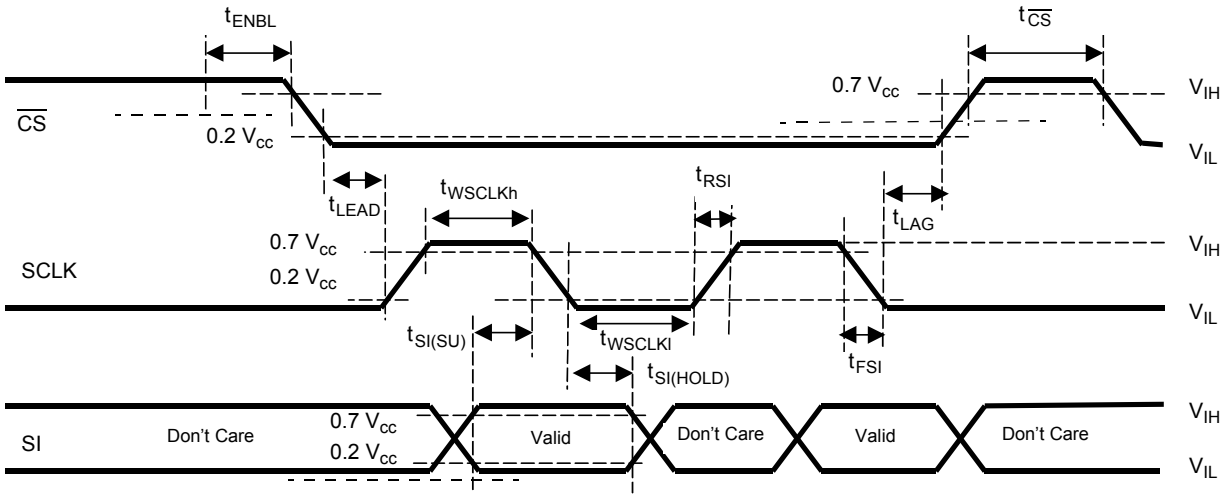


Figure 4. Input Timing Switching Characteristics

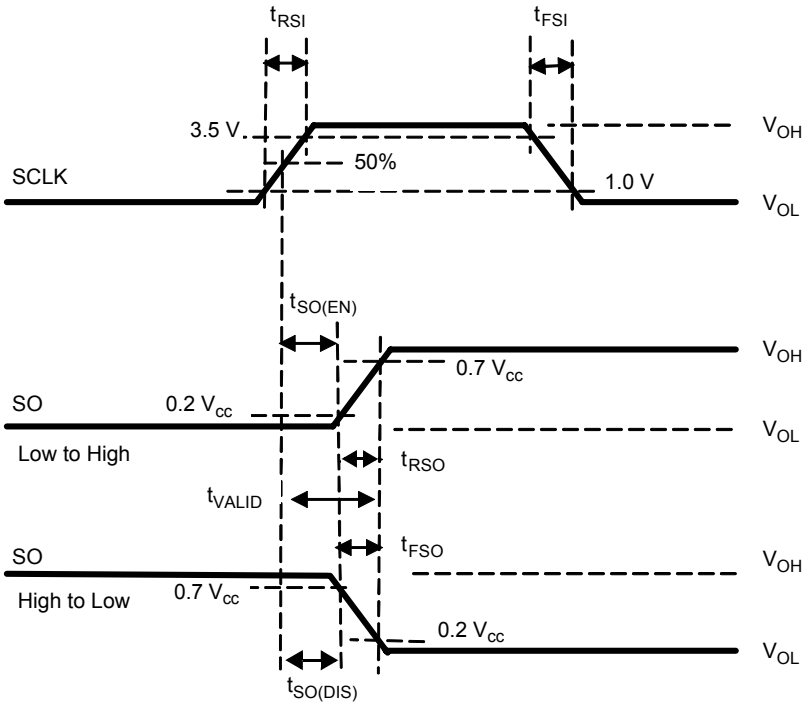


Figure 5. SCLK Waveform and Valid SO Data Delay Time

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33480 is designed for low-voltage automotive and industrial lighting applications. Its five low $R_{DS(ON)}$ MOSFETs (three 10 mΩ and two 35 mΩ) can control the high sides of five separate resistive loads (bulbs). Programming, control, and diagnostics are accomplished using a 16-bit SPI interface.

FUNCTIONAL TERMINAL DESCRIPTION

SUPPLY VOLTAGE (VBAT)

The VBAT terminal of the 33480 is the power supply of the device. In addition to its supply function, this tab contributes to the thermal behavior of the device by conducting the heat from the switching MOSFETs to the printed circuit board.

SUPPLY VOLTAGE (VCC)

This is an external voltage input terminal used to supply the SPI digital portion of the circuit and the gate driver of the external SMART MOSFET.

GROUND (GND)

This terminal is the ground of the device.

CLOCK INPUT (CLOCK)

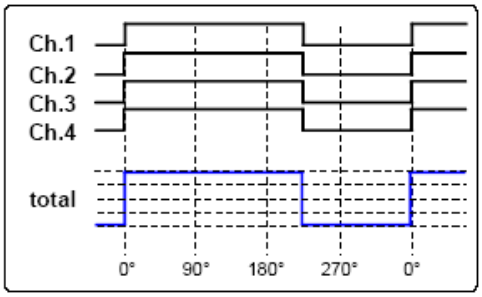
The PWM frequency and timing are generated from clock input by the PWM module. The clock input frequency is the factor 2^7 = 128 of the PWM frequency (60 Hz to 240 Hz). The OUT1:6 can be controlled in the range of 4% to 96% with a resolution of 7 bits of duty cycle (bits D[6:0]).

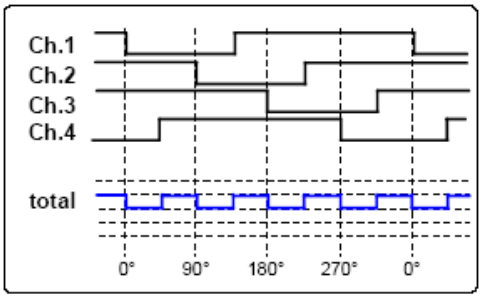
The following table describes the PWM resolution.

On/Off (Bit D7)	Duty cycle (7 bits resolution)	Output state
0	**X**	**OFF**
1	0000000	PWM (1/128 duty cycle)
1	0000001	PWM (2/128 duty cycle)
1	0000010	PWM (3/128 duty cycle)
1	1111111	fully ON

The timing includes four programmable PWM switching phases (0°, 90°, 180°, and 270°) to improve overall EMC behavior of the light module.

The amplitude of the input current is divided by four while the frequency is 4 times the original one. The two following pictures illustrate this behavior.





The synchronization of the switching phases between different corner light IC is provided by an SPI command in combination with the $\overline{CS}$ input. The bit in the SPI is called PWM sync (initialization register).

In Normal Mode, no PWM feature (100% duty cycle) is provided in the following instances:

- with the following SPI configuration: D7:D0=FF.
- In case of clock input signal failure (out of f_{PWM}), the outputs state depends of D7 bit value (D7=1=ON) in Normal Mode.

In Fail mode. The ouputs state depends of IGN and Flasher terminals.

LIMP HOME INPUT (LIMP)

The Fail mode of the component can be activated by this digital input port. The signal is “high active”, meaning the Fail mode can be activated by a logic high signal at the input.

IGNITION INPUT (IGN)

The ignition input wakes the device. It also controls the Fail mode activation. The signal is “high active”, meaning the component is active in case of a logic high at the input.

FLASHER INPUT (FLASHER)

The flasher input wakes the device. It also controls the Fail Mode activation. The signal is “high active”, meaning the component is active in case of a logic high at the input.

RESET INPUT (RSTB)

This input wakes the device when the RSTB terminal is at logic [1]. It is also used to initialize the device configuration and the SPI faults registers when the signal is low. All SI/SO registers described Table 8 and Table 11 are reset. The fault management is not affected by RSTB (see Figure 2).

CURRENT SENSE OUTPUT (CSNS)

The current sense output terminal is an analog current output. The routing to the external resistor is SPI programmable.

CHARGE PUMP (CP)

An external capacitor is connected between this terminal and V_{BAT} terminal. It is used as a tank for the internal charge pump. Its value is 100 nF ±20%, 25V maximum.

FETOUT OUTPUT (FETOUT)

This output terminal is used to control an external MOSFET (OUT6).

The high level of the FETout Output is Vcc if Vbat and Vcc are available in case of FETout is controlled ON.

FETout is not protected in case of short circuit or undervoltage on Vbat.

In case of reverse battery, OUT6 is OFF.

FETIN INPUT (FETIN)

This input terminal gives the current recopy of the external MOSFET. It can be routed on CSNS output by SPI command.

SPI PROTOCOL DESCRIPTION

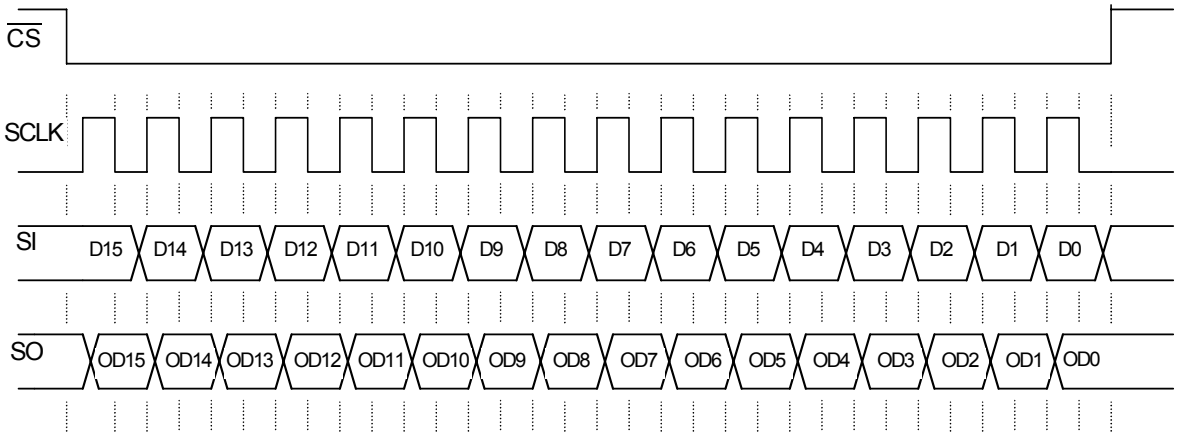
The SPI interface has a full-duplex, three-wire synchronous data transfer with four I/O lines associated with it: Serial Clock (SCLK), Serial Input (SI), Serial Output (SO), and Chip Select ($\overline{CS}$).

The SI/SO terminals of the 33480 device follow a first-in, first-out (D15 to D0) protocol, with both input and output words transferring the most significant bit (MSB) first. All inputs are compatible with 5.0 V CMOS logic levels, supplied by Vcc.

The SPI lines perform the following functions:

SERIAL CLOCK (SCLK)

The SCLK terminal clocks the internal shift registers of the 33480 device. The SI terminal accepts data into the input shift register on the falling edge of the SCLK signal, while the SO terminal shifts data information out of the SO line driver on the rising edge of the SCLK signal. It is important that the SCLK terminal be in a logic low state whenever $\overline{CS}$ makes any transition. For this reason, it is recommended the SCLK terminal be in a logic [0] whenever the device is not accessed ($\overline{CS}$ logic [1] state). SCLK has an internal pulldown, I_{DWN}. When $\overline{CS}$ is logic [1], signals at the SCLK and SI terminals are ignored and SO is tri-stated (high impedance) (see Figure 6).



NOTES: 1.
2.
3.

Notes
1. D15 : D0 relate to the most recent ordered entry of data into the device.
2. OD15 : OD0 relate to the first 16 bits of ordered fault and status data out of the device.

Figure 6. Single 16-Bit Word SPI Communication

SERIAL INPUT (SI)

The SI terminal is a serial interface command data input terminal. Each SI bit is read on the falling edge of SCLK. A 16-bit stream of serial data is required on the SI terminal, starting with D15 to D0. SI has an internal pulldown, Idown.

SERIAL OUTPUT (SO)

The SO data terminal is a tri-stateable output from the shift register. The SO terminal remains in a high-impedance state until the $\overline{CS}$ terminal is put into a logic [0] state. The SO data is capable of reporting the status of the output, the device configuration, and the state of the key inputs. The SO terminal changes state on the rising edge of SCLK and reads out on the falling edge of SCLK.

CHIP SELECT ($\overline{CS}$)

The $\overline{CS}$ terminal enables communication with the master device. When this terminal is in a logic [0] state, the device is capable of transferring information to, and receiving information from, the master device. The 33480 device latches in data from the Input Shift registers to the addressed registers on the rising edge of $\overline{CS}$. The device transfers status information from the power output to the Shift register on the falling edge of $\overline{CS}$. The SO output driver is enabled when $\overline{CS}$ is logic [0]. $\overline{CS}$ should transition from a logic [1] to a logic [0] state only when SCLK is a logic [0]. $\overline{CS}$ has an internal pullup, I_{UP}.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

SLEEP MODE

The Sleep mode is the default mode of the 33480. This is the state of the device after first applying battery voltage (V_{BAT}) and prior to any I/O transitions. This is also the state of the device when IGN, FLASHER, and RSTB are logic [0] (wake=0). In the Sleep mode, the outputs and all internal circuitry are OFF to minimize current draw. In addition, all SPI-configurable features of the device are reset. The 33480 will transit to two modes (Normal and Fail) depending on wake and fail signals (see Fig13).

The transition to the other modes is according following signals :

- Wake = IGN or IGN_ON or FLASHER or FLASHER_ON or RSTB
- Fail = VCC fail or SPI fail or External limp

NORMAL MODE

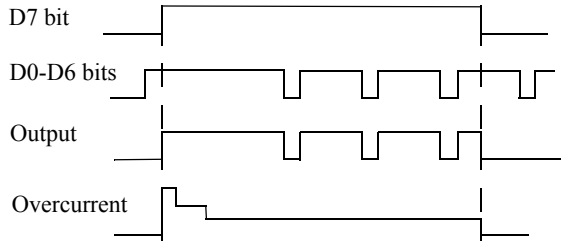
The 33480 is in Normal mode when:

- Wake = 1
- Fail = 0

In Normal operating mode the power outputs are under full control of the SPI as follows:

- The outputs 1 to 6, including multiphase timing, are controlled by the programmable PWM module.
- The outputs 1 to 5 are switched OFF in case of undervoltage on Vbat.
- The outputs 1 to 5 are protected by the overcurrent double window and overtemperature shutdown circuit.
- The digital diagnosis feature transfers status of the smart outputs via SPI.
- The analog current sense output (current recopy feature) can be routed by SPI.
- The SPI reports NM=1 in this mode.

The figure below describes the PWM, outputs and overcurrent behavior in Normal Mode.



FAIL MODE

The 33480 is in Fail mode when:

- Wake = 1
- Fail = 1.

In Fail mode :

- The outputs are under control of external terminals (see Table 5)
- The outputs are fully protected in case of overload, overtemperature and undervoltage (on Vbat or on Vcc).
- Neither digital diagnosis feature (SPI) nor analog current sense are available.
- Output 2 is configured in Xenon mode.
- In case of overload (OCHI2 or OCLO) conditions or undervoltage on Vbat, the outputs are under control of autorestart feature.
- In case of serious overload condition (OCHI1 or OT) the corresponding output is latched OFF until a new wake up event (wake=0 then 1).

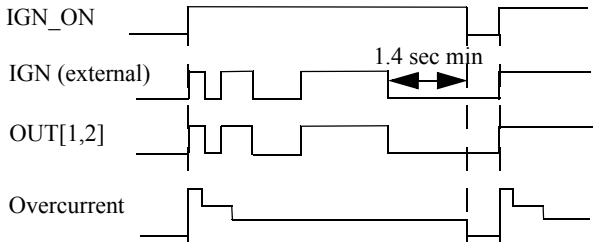


Table 5. Limp Home Output State

Output 1 Parking Light	Output 2 Low Beam	Output 3 High Beam	Output 4 Fog Light	Output 5 Flasher	External Switch Spare
IGN Terminal	IGN Terminal	OFF	OFF	FLASHER Terminal	OFF

AUTORESTART STRATEGY

The autorestart circuitry is used to supervise the outputs and reactivate high-side switches in case of overload or undervoltage failure conditions to provide a high availability of the outputs.

Autorestart feature is available in Fail mode when no supervising intelligence of the microcontroller is available. Autorestart is activated in case of overload condition (OCHI2 or OCLO) or undervoltage condition on VBat (see Fig10).

The autorestart switches ON the outputs. During ON state of the switch OCHI1 window is enable for tochi_Auto then after the output is protected by OCLO.

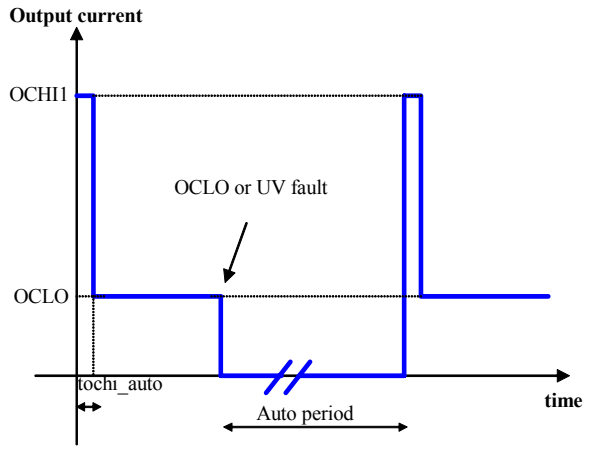


Figure 7. Overcurrent window in case of Autorestart

In case of OCHI1 or OT, the switch is latched OFF until wake up (wake=0 then1).

In case of OCLO or undervoltage, the output switch OFF and after autorestart period (150ms for 10mohm or 75ms for 35mhom) turn ON again.

In case of under voltage occurred in fail mode, it will be latched twice: one latch for outputs 1 and 5 and the second latch for output 2. That means the corresponding output is switched on only after its autorestart period ($t_{AUTORST-T1}$ or $t_{AUTORST-T2}$).

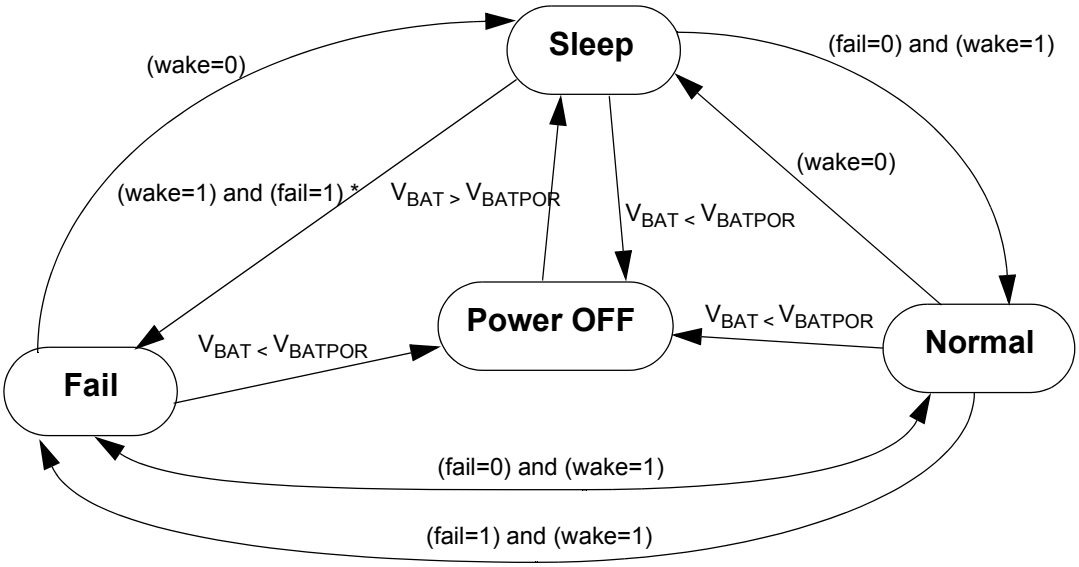
The Autorestart is not limited in time.

TRANSITION FAIL TO NORMAL MODE

To leave the fail mode, the fail condition must be removed (fail=0). The microcontroller has to send a SPI command with D10 must be to logic [1] to reset the watchdog bit ; the other bits are not considered. The previous latched faults are reset by the transition into Normal mode.

TRANSITION NORMAL TO FAIL MODE

To leave the Normal Mode, a fail condition must occur (fail=1). The previous latched faults are reset by the transition into Fail mode.



Notes:
* only available in case of Vcc fail condition
wake=(RSTB=1) OR (IGN_ON=1) OR (Flasher_ON=1)
fail=(Vcc_fail=1) OR (SPI_fail=1) OR (ext_limp=1)

Figure 8. Operating Modes State Machine

START-UP SEQUENCE

The 33480 enters in Normal Mode after start-up if following sequence is provided:

- Vbat and Vcc power supplies must be above their undervoltage thresholds (Sleep mode).
- generate wake up event (wake=1) from 0 to 1 on RSTB. The device switches to normal mode.
- apply PWM clock after maximum 200us (min 50us).
- send SPI command to the Device status register to clear the clock fail flag to enable the PWM module to start.

If the correct start-up sequence is not provided, the PWM function is not guaranteed.

The following figure describes the wake-up block diagram.

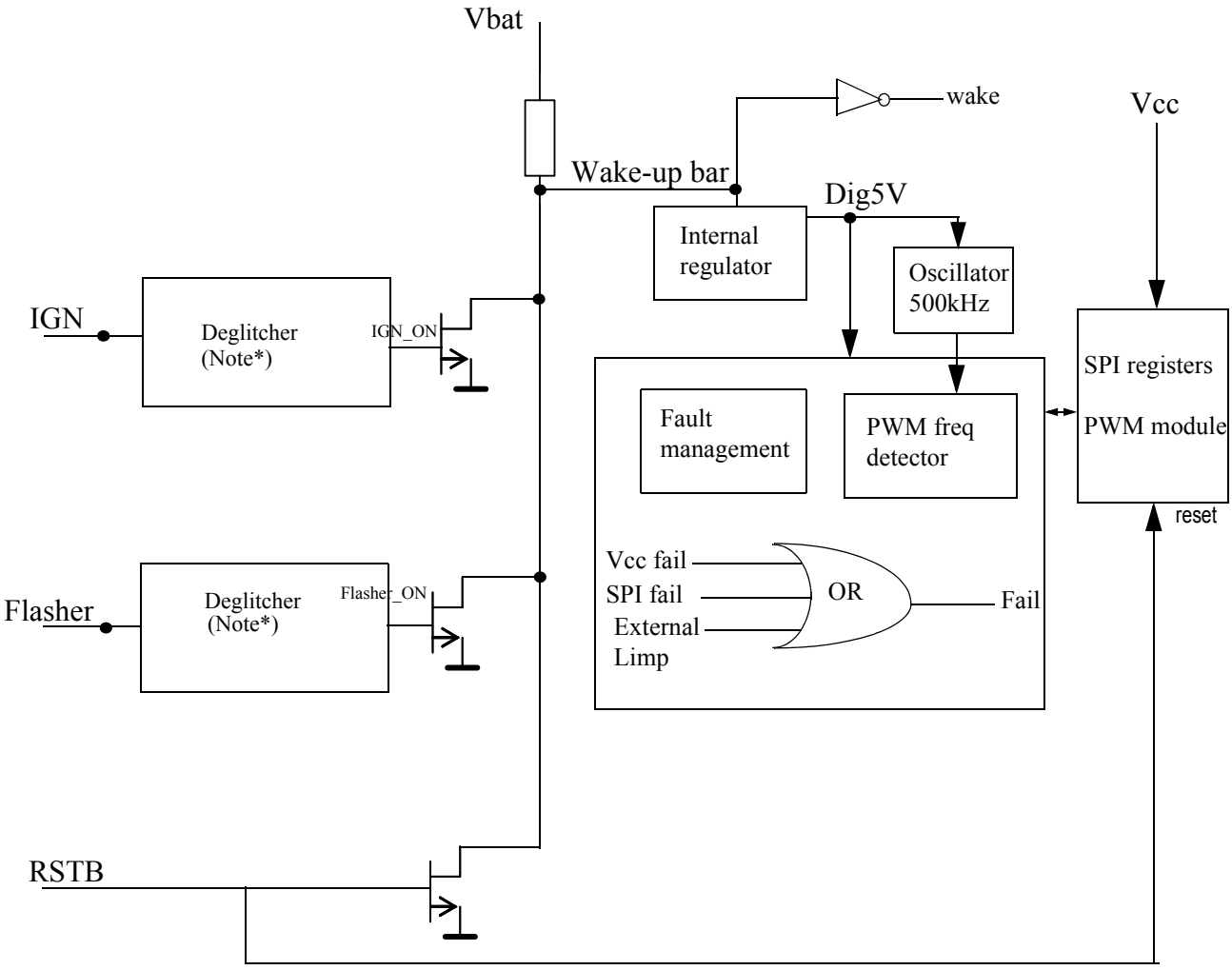
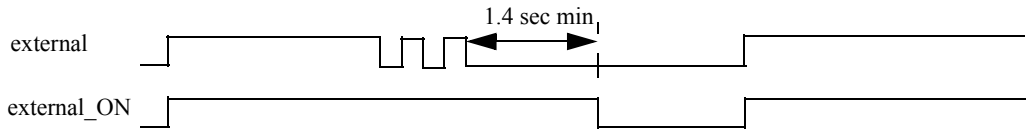


Figure 9. Wake-up block diagram

Note*:



external: IGN, Flasher
external_ON: IGN_ON, Flasher_ON

PROTECTION AND DIAGNOSIS FEATURES

Output Protection Features

The 33480 provides the following protection features:

- Protection against transients on V_{BAT} supply line (per ISO 7637)
- Active clamp, including protection against negative transients on output line
- Overtemperature
- Severe and resistive Overcurrent
- Open Load during ON state

These protections are provided for each output (OUT1:5).

Overtemperature detection

The 33480 provides overtemperature shutdown for each output (OUT1:OUT5). It can occur when the output terminal is in the ON or OFF state. An overtemperature fault condition results in turning OFF the corresponding output. The fault is latched and reported via SPI. To delatch the fault and be able to turn ON again the outputs, the failure condition must be removed (T< 175°C typically) and:

- if the device was in Normal Mode, the output corresponding register (bit D7) must be rewritten. Application of complete OCHI window (OCHI1+OCHI2 during t2) depends on toggling or not toggling D7 bit.
- if the device was in Fail Mode, the corresponding output is locked until restart of the device: wake up from Sleep Mode or V_{BATPOR}.

The SPI fault report (OTS bit) is removed after a read operation.

Overcurrent detections

The 33480 provides intelligent overcurrent shutdown (see Figure 10) in order to protect the internal power transistors and the harness in the event of overload (fuse characteristic).

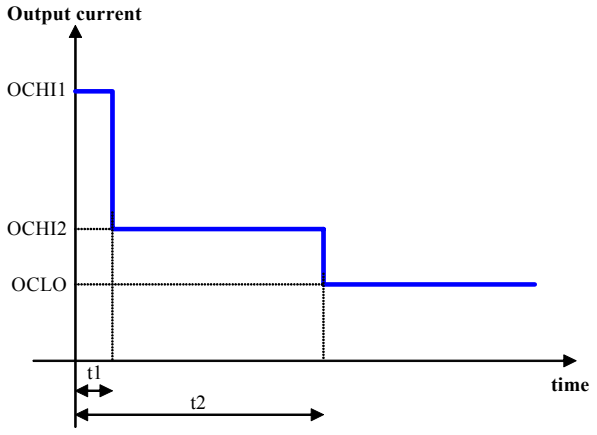


Figure 10. Double overcurrent window in Normal Mode

OCHI (I_{OCHI1} and then I_{OCHI2}) is only activated after toggling D7 bit in Normal Mode. In Fail Mode, the control of OCHI window is provided by the toggles: IGN_ON, Flasher_ON. The current thresholds (I_{OCHI1} , I_{OCHI2} and I_{OCLO}) and the time (t_1 and t_2) are fixed numbers for each driver. After t_2, OCLO current threshold is set to protect in steady state.

OUT2 is default loaded with the Xenon profile. The use of H7 bulbs at this output requires SPI programming (Xenon bit).

In case of overload (OCHI1 or OCHI2 or OCLO detection), the corresponding output is disabled immediately. The fault is latched and the status is reported via SPI. To delatch the fault, the failure condition must be removed and:

For OCHI1:

- if the device was in Normal Mode: the output corresponding register (bit D7) must be rewritten D7=1. Application of complete OCHI window depends on toggling or not toggling D7 bit.
- if the device was in Fail Mode, the failure is locked until restart of the device: wake up from Sleep Mode or V_{BATPOR}.

For OCHI2 and OCLO:

- if the device was in Normal Mode: the output corresponding register (bit D7) must be rewritten D7=1. Application of complete OCHI window depends on toggling or not toggling D7 bit.
- if the device was in Fail Mode, Autorestart is activated. The device Autorestart feature provides a fixed duty cycle and fixed period with OCHI1 window. Autorestart feature resets OCHI2 or OCLO fault after corresponding Autorestart period.

The SPI fault reports are removed after a read operation:

- OC bit=(OCHI1) or (OCHI2) fault
- OVL bit=(OCHI1) or (OCHI2) or (OCLO) fault

Overvoltage detection and active clamp

The 33480 provides an active gate clamp circuit in order to limit the maximum drain to source voltage.

In case of overload on an output the corresponding switch (OUT[1 to 5]) is turned off which leads to high voltage at Vbat with an inductive Vbat line. When Vbat voltage exceeds VBAT_CLAMP threshold, the fast turn-off on the corresponding output is deactivated and the drain to source voltage is limited by the active clamp circuit (VCLAMP_DS).

The following diagrams (9&10) describe the faults management in Normal Mode and Fail Mode .

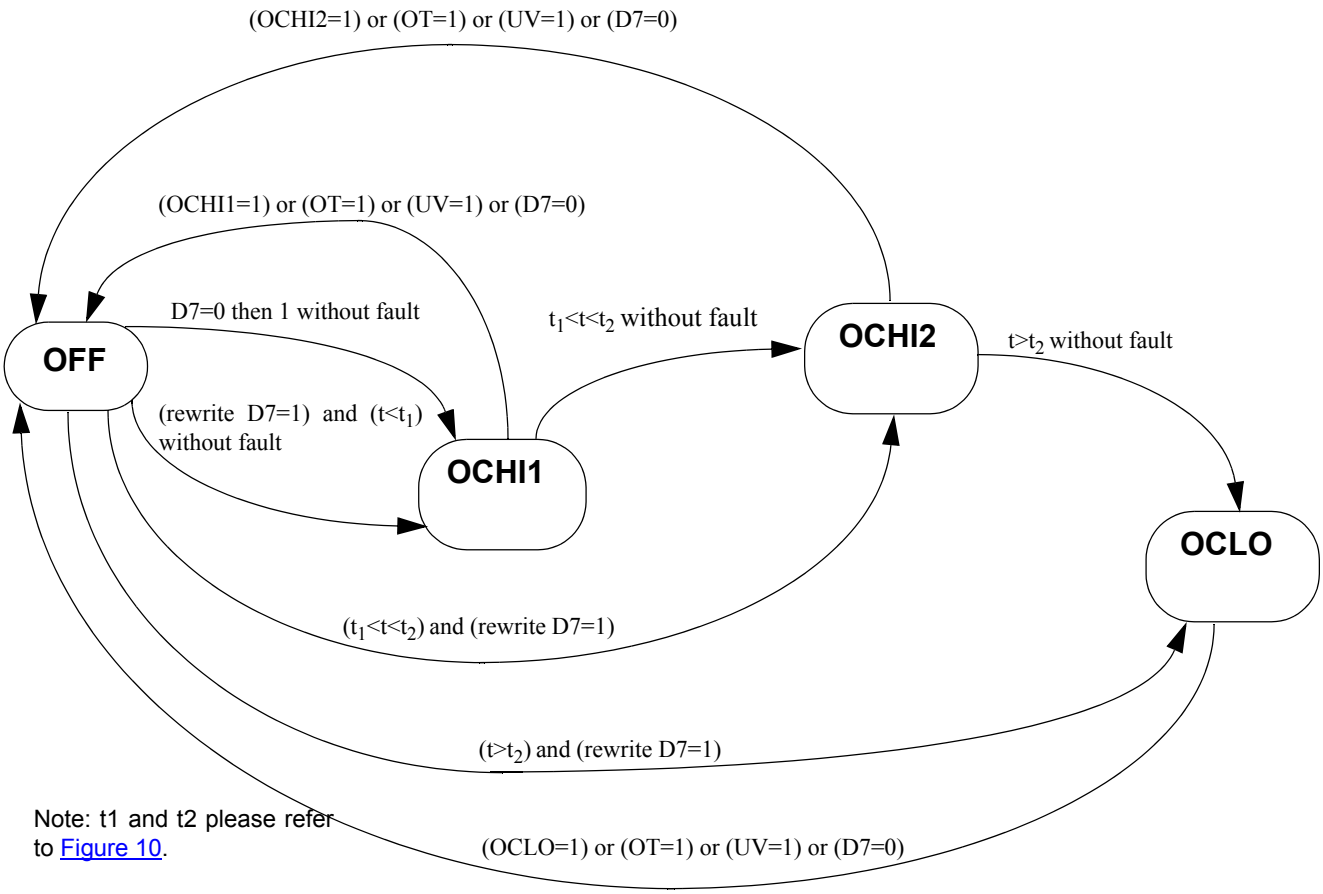
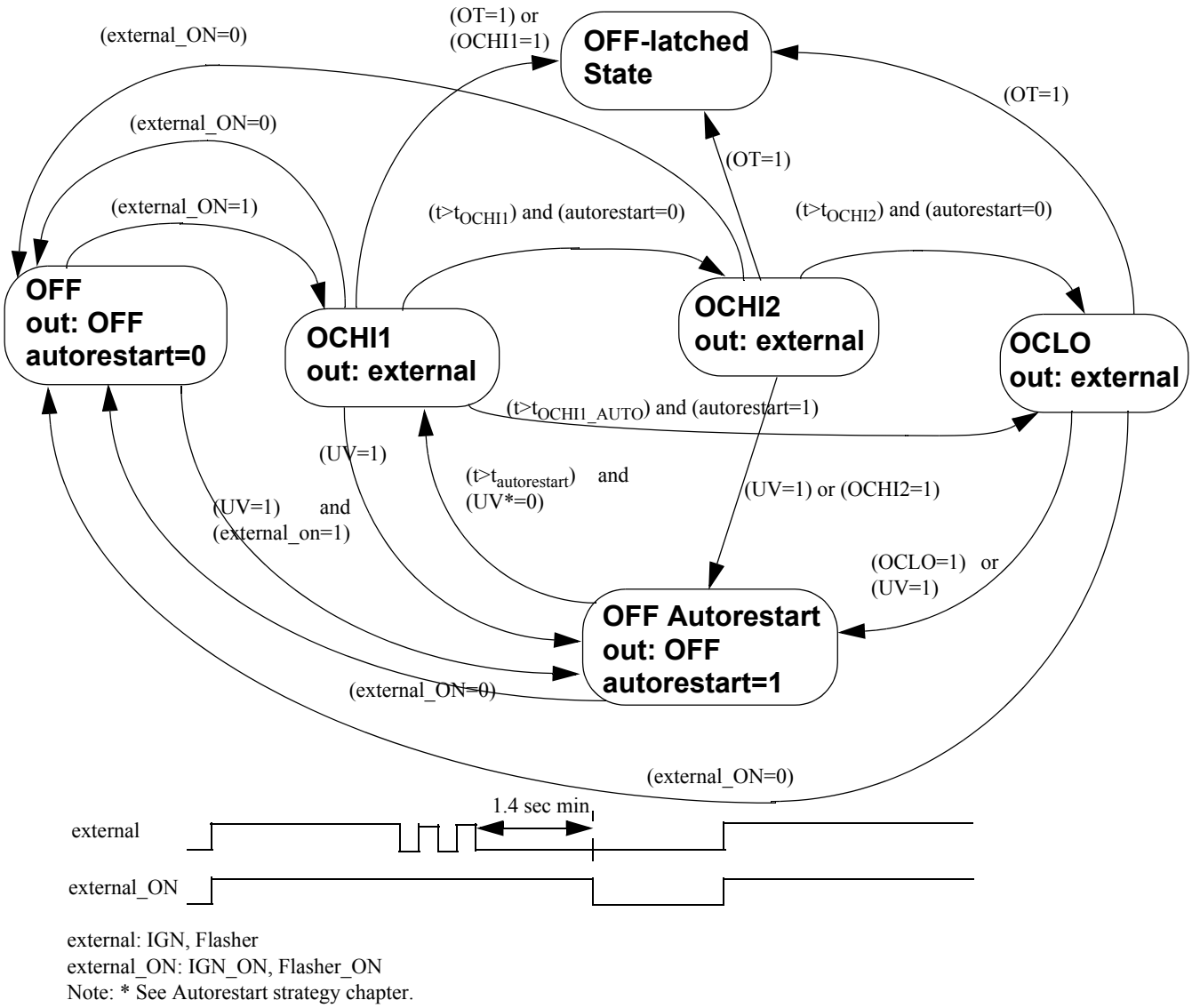


Figure 11. Faults management in Normal Mode (for OUT[1:5] only)



external: IGN, Flasher
external_ON: IGN_ON, Flasher_ON
Note: * See Autorestart strategy chapter.

Figure 12. Faults management in Fail Mode (for OUT[1:5] only)

Diagnosis

Open Load

The 33480 provides open load detection for each output (OUT1:OUT5) when the output terminal is in the ON state. Open load detection levels can be chosen by SPI to detect a standard bulb, a Xenon bulb for OUT2 only, or LEDs (OLLED bit). Open load for LEDs only is detected during each regular switch-off transition for minimum 200µs (PWM depending D[6:0] bits <> 7F) or periodically each t_{OLLED} (fully-on, D[6:0]=7F). To detect OLLED in fully on state, the output must be on at least t_{OLLED}. When an open load has been detected, the output stays ON.

To delatch the diagnosis, the condition should be removed and SPI read operation is needed (OL bit). In case of Power on Reset on Vbat, the fault will be reset.

Current Sense

The 33480 diagnosis for load current (OUT1:6) is done using the current sense (CSNS) terminal connected to an external resistor. The routing of the current sense sources is SPI programmable (MUX[2,0] bits).

The current recopy feature for OUT1:5 is disabled during high overcurrent shutdown phase (t_2) and is only enabled during low overcurrent shutdown threshold. The current recopy output delivers current only during ON time of the output switch without overshoot (aperiodic settling).

The current recopy is not active in Fail Mode.

TEMPERATURE PREWARNING

The 33480 provides a temperature prewarning reported via SPI (OTW bit) in Normal Mode. The information is latched. To delatch, a read SPI command is needed. In case of Power on Reset, the fault will be reset.

EXTERNAL TERMINAL STATUS

The 33480 provides the status of the FLASHER, IGN, and CLOCK terminals via SPI in real time and in Normal Mode.

FAILURE HANDLING STRATEGY

A highly sophisticated failure handling strategy enables light functionality even in case of failures inside the component or the light module. Components are protected against:

- Reverse Polarity
- Loss of Supply Lines
- Fatal Mistreatment of Logic I/O Terminals

REVERSE POLARITY PROTECTION ON VBAT

In case of permanently reverse polarity operation, the output transistors are turned ON (Rsd) to prevent thermal overload and no protections are available.

External diode on Vcc is necessary in order to not destroy the 33480 in case of reverse polarity.

In case of negative transients on the V_{BAT} line (per ISO 7637), the V_{CC} line is still operating, while the V_{BAT} line is negative. Therefore, the device is protected against latch-up.

LOSS OF SUPPLY LINES

The 33480 is protected against loss of any supply line. The detection of the supply line failure is provided inside the device itself.

LOSS OF VBAT

During undervoltage of V_{BAT} (V_{BATPOR}<V_{BAT}<V_{BATUV}) and with active device (wake=1), the outputs [1-5] are switched off and the external MOSFET remains in the previous state. No current path from Vbat to Vcc. The external MOSFET (OUT6) can be controlled by SPI if Vcc remains and is above to V_{CCUV}. The fault is reported to UVF bit (OD13). To delatch the fault, the undervoltage condition should be removed and:

- The bit D7 must be rewritten to logic [1] in Normal Mode. Application of OCHI window depends on toggling or not toggling D7 bit. When the fault is delatched, the 33480 returns in the configuration it was just before the failure.
- If the device was in Fail mode, the fault will be delatched by the Autorestart feature periodically.

In case of V_{BAT}<V_{BATPOR} (Power OFF state), all latched faults are reset if V_{CC} < V_{BAT}. In case of V_{BAT} is missing, all outputs (out[1:6]) are OFF and no current is conducted from Vcc to V_{BAT}.

LOSS OF V_{CC} (DIGITAL LOGIC SUPPLY LINE)

During loss of V_{CC} (V_{CC} < V_{CCUV}) and with wake=1, the 33480 is switched automatically into Fail mode (no deglich time). The external SMART MOSFET is OFF. All SPI registers are reset and must be reprogrammed when Vcc goes above V_{CCUV}.

LOSS OF GROUND (GND)

During loss of ground, the 33480 cannot operate the loads (the outputs (1:5) are switched OFF) but is not destroyed by the operating condition. Current limit resistors in the digital input lines protect the digital supply against excessive current (1kohm typical). The state of the external smart power switch controlled by FETout is not guaranteed and the state of external smart MOS is defined with external termination resistor.

FATAL MISTREATMENT OF LOGIC I/O TERMINALS

The digital I/Os are protected against fatal mistreatment by signal plausibility check according to Table 6.

Table 6. Logic I/O Plausibility Check

Input/Output	Signal Check Strategy
LIMP	Debounce for 10 ms
(PWM) CLOCK	Frequency range (bandpass filter)
SPI (MOSI, SCLK, $\overline{CS}$)	WD, D10 bit internal toggle

In case of LIMP input is set to logic [1] for a delay longer than 10ms typical, the 33480 is switched into Fail mode. In case of (PWM) Clock failure, no PWM feature is provided and

the bit D7 defines the outputs state. In case of SPI failure, the 33480 is switched into Fail mode (see Fig13).

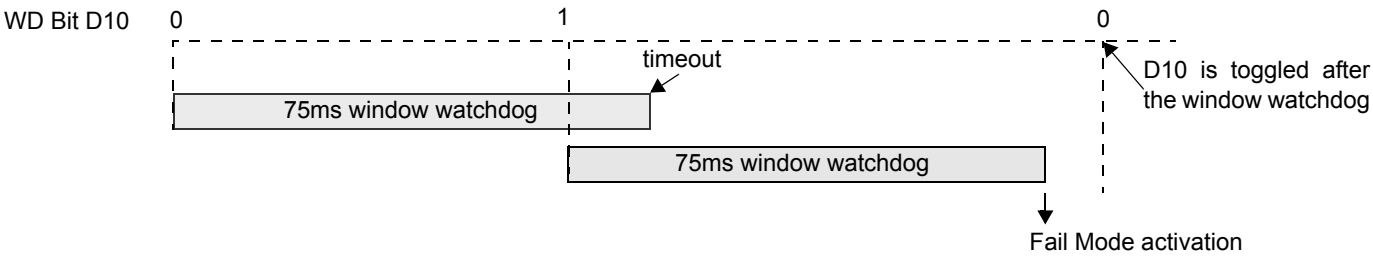


Figure 13. Watchdog window

FUNCTIONAL DESCRIPTION

SERIAL INPUT COMMUNICATION

SPI communication is accomplished using 16-bit messages. A message is transmitted by the master starting with the MSB, D15, and ending with the LSB, D0. Each incoming command message on the SI terminal can be interpreted using the bit assignment described in Table 7. The 5 bits D15:D11, called register address bits, are used to select the command register. Bit D10 is the watchdog bit. The remaining 10 bits, D9:D0, are used to configure and control the output and its protection features. Multiple messages can be transmitted in succession to accommodate those applications where daisy chaining is desirable or to confirm transmitted data as long as the messages are all multiples of 16 bits. Any attempt made to latch in a message that is not 16 bits will be ignored.

All SPI registers are reset (all bit equal 0) in case of RSTB equal 0 or fail mode (Fail=1).

Table 7. SI Message Bit Assignment

Bit Sig	SI Msg Bit	Message Bit Description
MSB	D15:D11	Register address bits.
	D10	Watchdog in: toggled to satisfy watchdog requirements.
LSB	D9:D0	Used to configure inputs, outputs, device protection features, and SO status content.

DEVICE REGISTER ADDRESSING

The register addresses (D15:D11) and the impact of the serial input registers on device operation are described in this section. Table 8 summarizes the SI registers.

Table 8. Serial Input Address and Configuration Bit Map

SI Register	SI Address					SI Data										
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Initialization	0	0	0	0	0	WD	0	0	0	PWM sync	$\overline{\text{Xenon}}$	MUX2	MUX1	MUX0	SOA1	SOA0
Config OL	0	0	0	0	1	WD	0	0	0	0	0	OLLED5	OLLED4	OLLED3	OLLED2	OLLED1
Unused	0	0	0	1	0	WD	0	0	0	0	0	0	0	0	0	0
Unused	0	0	0	1	1	WD	0	0	0	0	0	0	0	0	0	0
Control OUT1	0	1	0	0	1	WD	Phase2	Phase1	ONoff	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Control OUT2	0	1	0	1	0	WD	Phase2	Phase1	ONoff	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Control OUT3	0	1	0	1	1	WD	Phase2	Phase1	ONoff	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Control OUT4	0	1	1	0	0	WD	Phase2	Phase1	ONoff	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Control OUT5	0	1	1	0	1	WD	Phase2	Phase1	ONoff	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Control External Switch	0	1	1	1	0	WD	Phase2	Phase1	ONoff	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
RESET	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0

Note: testmode address used only by FSL is D[15:11]=01111 with RSTB voltage higher than 8V typ.

ADDRESS 00000—INITIALIZATION

The Initialization register is used to read the various statuses, choose one of the six outputs current recopy, load the H7 bulbs profile for OUT2 only, and synchronize the switching phases between different corner light devices. The register bits D1 and D0 determine the content of the 16 bits of the next SO data. (Refer to the section entitled Serial Output Communication (Device Status Return Data) beginning on page 30.) Table 9 describes the register of initialization.

The watchdog timeout is specified by t_{WDTO} parameter. As long as the WD bit (D10) of an incoming SPI message is toggled within the minimum watchdog timeout period (WDTO), the device will operate normally. If an internal watchdog timeout occurs before the WD bit is toggled, the device will revert to Fail mode. All registers are cleared. To exit the Fail mode, send valid SPI communication with WD bit = 1.

Table 9. Initialization Register

SI Address					SI Data										
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	WD	0	0	0	PWM sync	$\overline{\text{Xenon}}$	MUX2	MUX1	MUX0	SOA1	SOA0

x = Don't care

D6 (PWM sync) = 0, No synchronization

D6 (PWM sync) = 1, Synchronization on CSB positive edge

D5 ($\overline{\text{Xenon}}$) = 0, Xenon

D5 ($\overline{\text{Xenon}}$) = 1, H7 Bulb

D4, D3, D2 (MUX2, MUX1, MUX0) = 000, No current sense

D4, D3, D2 (MUX2, MUX1, MUX0) = 001, OUT1 current sense

D4, D3, D2 (MUX2, MUX1, MUX0) = 010, OUT2 current sense

D4, D3, D2 (MUX2, MUX1, MUX0) = 011, OUT3 current sense

D4, D3, D2 (MUX2, MUX1, MUX0) = 100, OUT4 current sense

D4, D3, D2 (MUX2, MUX1, MUX0) = 101, OUT5 current sense

D4, D3, D2 (MUX2, MUX1, MUX0) = 110, External Switch current sense

D4, D3, D2 (MUX2, MUX1, MUX0) = 111, No current sense

ADDRESS 00001—CONFIGURATION OL

The Configuration OL register is used to enable the open load detection for LEDs in Normal Mode (OLLEDn in Table 8, page 28). When bit D0 is set to logic [1], the open load detection circuit for LED is activated for output 1. When bit D0 is set to logic [0], open load detection circuit for standard bulbs is activated for output 1.

ADDRESS 00010

This register is not used.

ADDRESS 00011

This register is not used.

ADDRESS 01001—CONTROL OUT1

Bits D9 and D8 control the switching phases as shown in Table 10.

Table 10. Switching Phases

D9:D8	PWM Phase
00	0°
01	90°
10	180°
11	270°

Bit D7 at logic [1] turns ON OUT1. OUT1 is turned OFF with bit D7 at logic [0]. This register allows the master to control the duty cycle and the switching phases of OUT1. The duty cycle resolution is given by bits D6:D0.

D7 = 0, D6:D0 = XX output OFF.

D7 = 1, D6:D0 = 00 output ON during 1/128.

D7 = 1, D6:D0 = 1A output ON during 27/128 on PWM period.

D7 = 1, D6:D0 = 7F output continuous ON (no PWM).

ADDRESS 01010—CONTROL OUT2

Same description as OUT1.

ADDRESS 011111—CONTROL OUT3

Same description as OUT1.

ADDRESS 01100—CONTROL OUT4

Same description as OUT1.

ADDRESS 01101—CONTROL OUT5

Same description as OUT1.

ADDRESS 01110—CONTROL EXTERNAL SWITCH

Same description as OUT1.

ADDRESS 01111 —TEST MODE

This register is reserved for test and is not available with SPI during normal operation.

SERIAL OUTPUT COMMUNICATION (DEVICE STATUS RETURN DATA)

When the $\overline{CS}$ terminal is pulled low, the output register is loaded. Meanwhile, the data is clocked out MSB first as the new message data is clocked into the SI terminal. The first 16 bits of data clocking out of the SO, and following a $\overline{CS}$ transition, is dependant upon the previously written SPI word (SOA1 and SOA0 defined in the last SPI initialization word).

Any bits clocked out of the SO terminal after the first 16 will be representative of the initial message bits clocked into the SI terminal since the $\overline{CS}$ terminal first transitioned to a logic [0]. This feature is useful for daisy chaining devices.

A valid message length is determined following a $\overline{CS}$ transition of logic [0] to logic [1]. If the message length is valid, the data is latched into the appropriate registers. A valid message length is a multiple of 16 bits. At this time, the SO terminal is tri-stated and the fault status register is now able to accept new fault status information.

The output status register correctly reflects the status of the Initialization-selected register data at the time that the $\overline{CS}$ is pulled to a logic [0] during SPI communication and/or for the period of time since the last valid SPI communication, with the following exceptions:

- The previous SPI communication was determined to be invalid. In this case, the status will be reported as though the invalid SPI communication never occurred.
- Battery transients below 6.0 V, resulting in an under-voltage shutdown of the outputs, may result in incorrect data loaded into the status register.

SERIAL OUTPUT BIT ASSIGNMENT

The contents of bits OD15:OD0 depend on bits D1:D0 from the most recent initialization command SOA[1:0] (refer to Table 8, page 28), as explained in the paragraphs that follow.

The register bits are reset by a read operation and also if the fault is removed.

Table 11 summarizes the SO register content. Bit OD10 reflects Normal mode (NM).

Table 11. Serial Output Bit Map Description

Status/ Mode	Previous SI Data		SO Data															
	SOA1	SOA0	OD15	OD14	OD13	OD12	OD11	OD10	OD9	OD8	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
Output Status	0	0	0	0	UVF	OTW	OTS	NM	OL5	OVL5	OL4	OVL4	OL3	OVL3	OL2	OVL2	OL1	OVL1
Overload Status	0	1	0	1	UVF	OTW	OTS	NM	OC5	OTS5	OC4	OTS4	OC3	OTS3	OC2	OTS2	OC1	OTS1
Device Status	1	0	1	0	UVF	OTW	OTS	NM	0	OV	X	X	X	RC	0	FLASHER pin	IGN pin	CLOCK fail
Test Mode	1	1	1	1	UVF	OTW	OTS	NM	0	0	0	0	0	0	0	0	0	0
Reset	X	X	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

PREVIOUS ADDRESS SOA[1:0]=00

If the previous two LSBs are 00, bits OD15:OD0 reflect the output status (Table 12).

Table 12. Output Status

OD15	OD14	OD13	OD12	OD11	OD10	OD9	OD8	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
0	0	UVF	OTW	OTS	NM	OL5	OVL5	OL4	OVL4	OL3	OVL3	OL2	OVL2	OL1	OVL1

OD13 (UVF) = Undervoltage Flag on Vbat

OD12 (OTW) = Overtemperature Prewarning Flag

OD11 (OTS) = Overtemperature Flag for all outputs

OD10 (NM) = Normal mode

OD9, OD7, OD5, OD3, OD1 (OL5, OL4, OL3, OL2, OL1) = Open Load Flag at Outputs 5 through 1, respectively.

OD8, OD6, OD4, OD2, OD0 (OVL5, OVL4, OVL3, OVL2, OVL1) = Overload Flag for Outputs 5 through 1, respectively.This corresponds to overtemperature or OCHI or OCLO faults.

Note

A logic [1] at bits OD9:OD0 indicates a fault. If there is no fault, bits OD9:OD0 are logic [0].

OVL=OCHI1+OCHI2+OCLO

PREVIOUS ADDRESS SOA[1:0]=01

If the previous two LSBs are 01, bits OD15:OD0 reflect reflect the temperature status (Table 13).

Table 13. Overload Status

OD15	OD14	OD13	OD12	OD11	OD10	OD9	OD8	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
0	1	UVF	OTW	OTS	NM	OC5	OTS5	OC4	OTS4	OC3	OTS3	OC2	OTS2	OC1	OTS1

OD13 (UVF) = Undervoltage Flag on Vbat

OD12 (OTW) = Overtemperature Prewarning Flag

OD11 (OTS) = Overtemperature Flag for all outputs

OD10 (NM) = Normal mode

OD9, OD7, OD5, OD3, OD1 (OC5, OC4, OC3, OC2, OC1) = High Overcurrent Shutdown Flag for Outputs 5 through 1, respectively

OD8, OD6, OD4, OD2, OD0 (OTS5, OTS4, OTS3, OTS2, OTS1) = Overtemperature Flag for Outputs 5 through 1, respectively

Note

A logic [1] at bits OD9:OD0 indicates a fault. If there is no fault, bits OD9:OD0 are logic [0].

OC=OCHI1+OCHI2

PREVIOUS ADDRESS SOA[1:0]=10

If the previous two LSBs are 01, bits OD15:OD0 reflect the status of the 33480 (Table 14).

Table 14. Device Status

OD15	OD14	OD13	OD12	OD11	OD10	OD9	OD8	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
1	0	UVF	OTW	OTS	NM	0	0V	X	X	X	RC	0	FLASHER pin	IGN pin	CLOCK fail

OD13 (UVF) = Undervoltage Flag on Vbat

OD12 (OTW) = Overtemperature Prewarning Flag

OD11 (OTS) = Overtemperature Flag for all outputs

OD10 (NM) = Normal mode

OD4 (RC) = Logic [0] indicates a Front Corner Light Switch. Logic [1] indicates a Rear Corner Light Switch

OD2 (FLASHER pin) = Indicates the FLASHER terminal state in real time

OD1 (IGN pin) = Indicates the IGN terminal state in real time

OD0 (CLOCK fail) = Logic [1], which indicates a clock failure

OD8 (Overvoltage) = Overvoltage Flag on Vbat in real time

PREVIOUS ADDRESS SOA[1:0]=11

Null Data. No previous register Read Back command received, so bits OD9:OD0 are null.

TYPICAL APPLICATION

Figure 14 below shows full vehicle light functionality, including fog lights, battery redundancy concept, light substitution mode, and Fail mode.

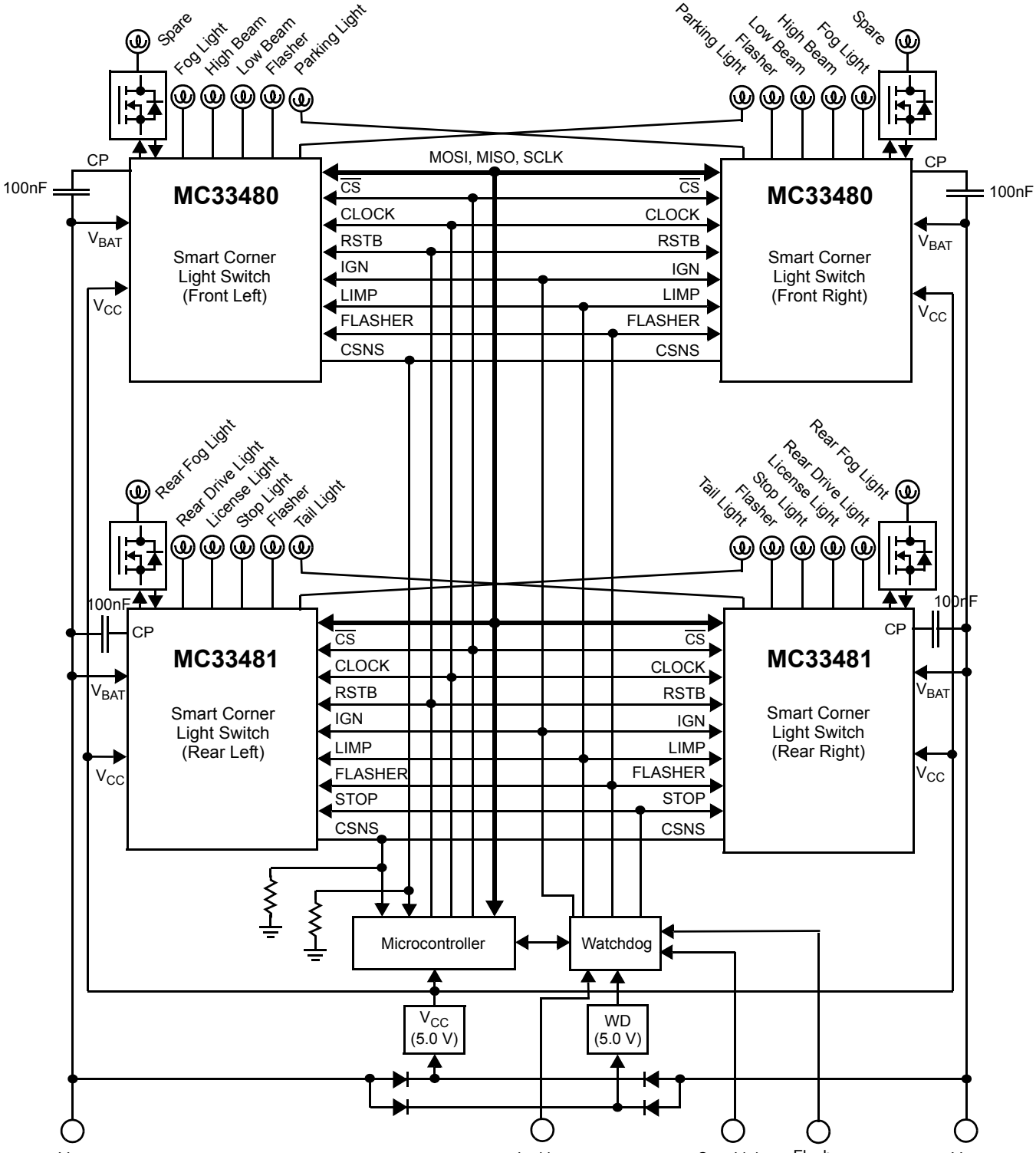


Figure 14. Typical Application

EMC & EMI PERFORMANCES

The 33480 must pass successfully the Class5 of the norm CISPR25.

The evaluation will be done on the Freescale board rev1.1.

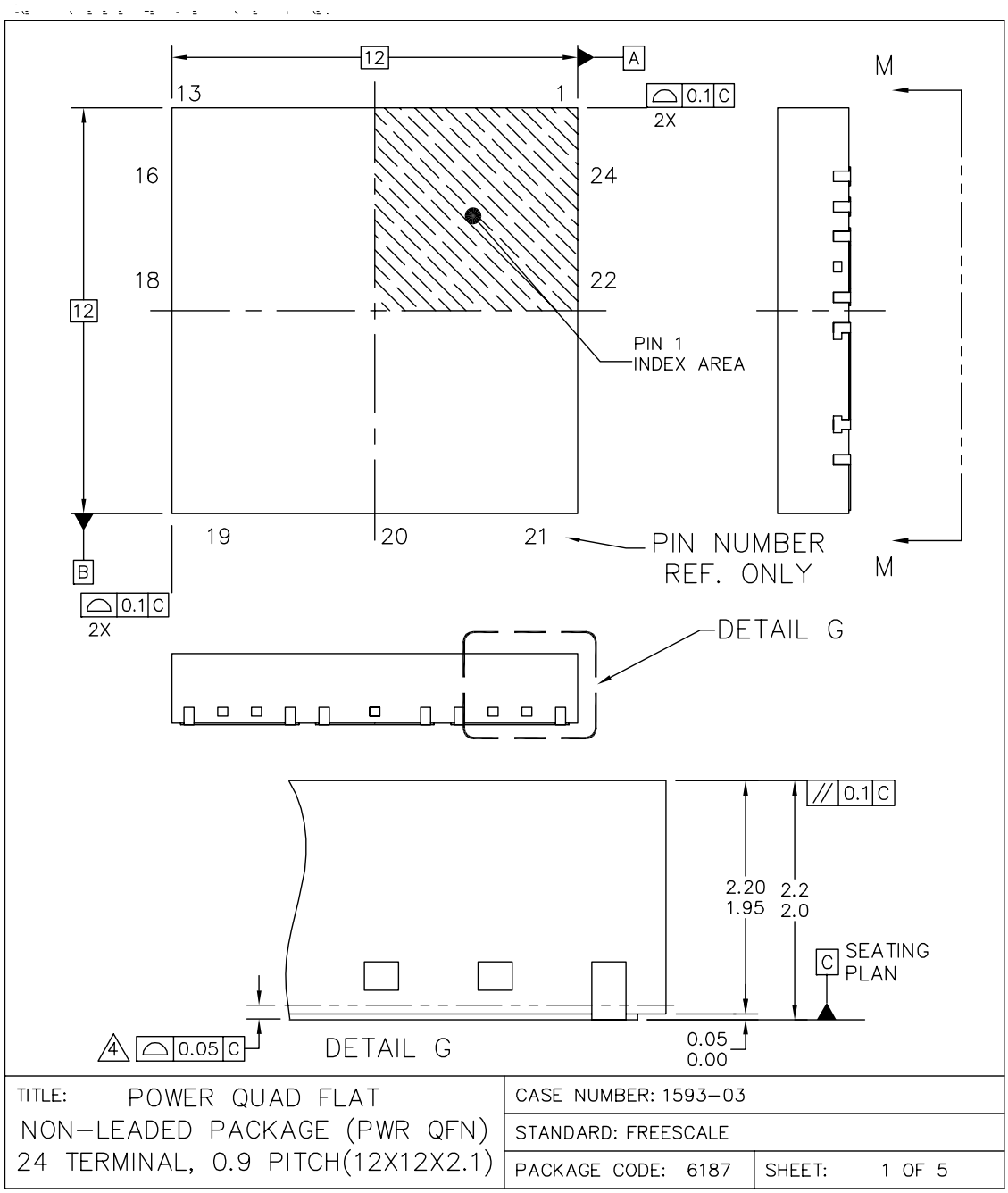
Conditions to be defined.

RELIABILITY TESTS

See document SCLS_reliability test spec_V22.doc, RevisionV2.2, Date September,23rd,2005.

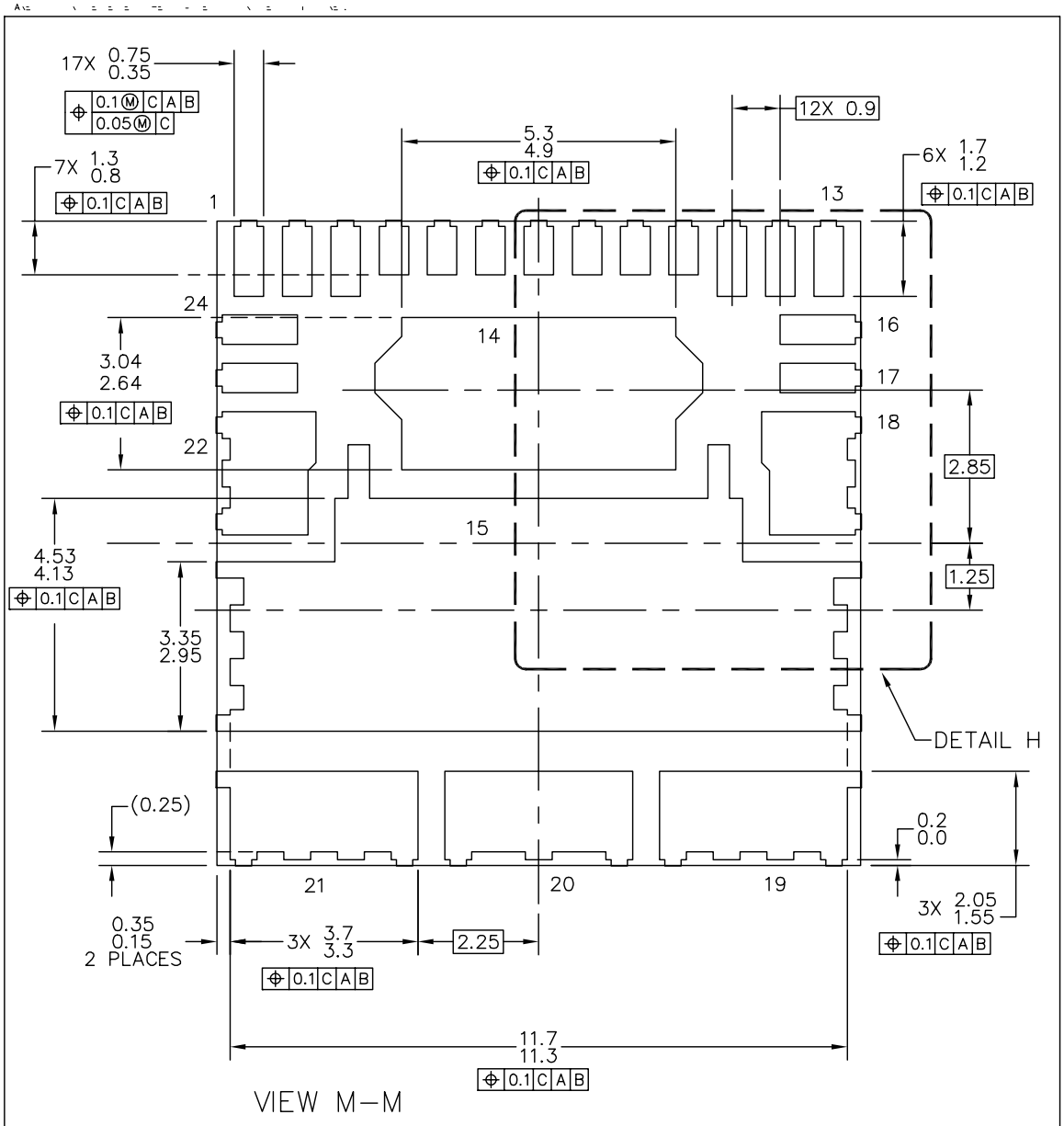
PACKAGING

PACKAGING DIMENSIONS

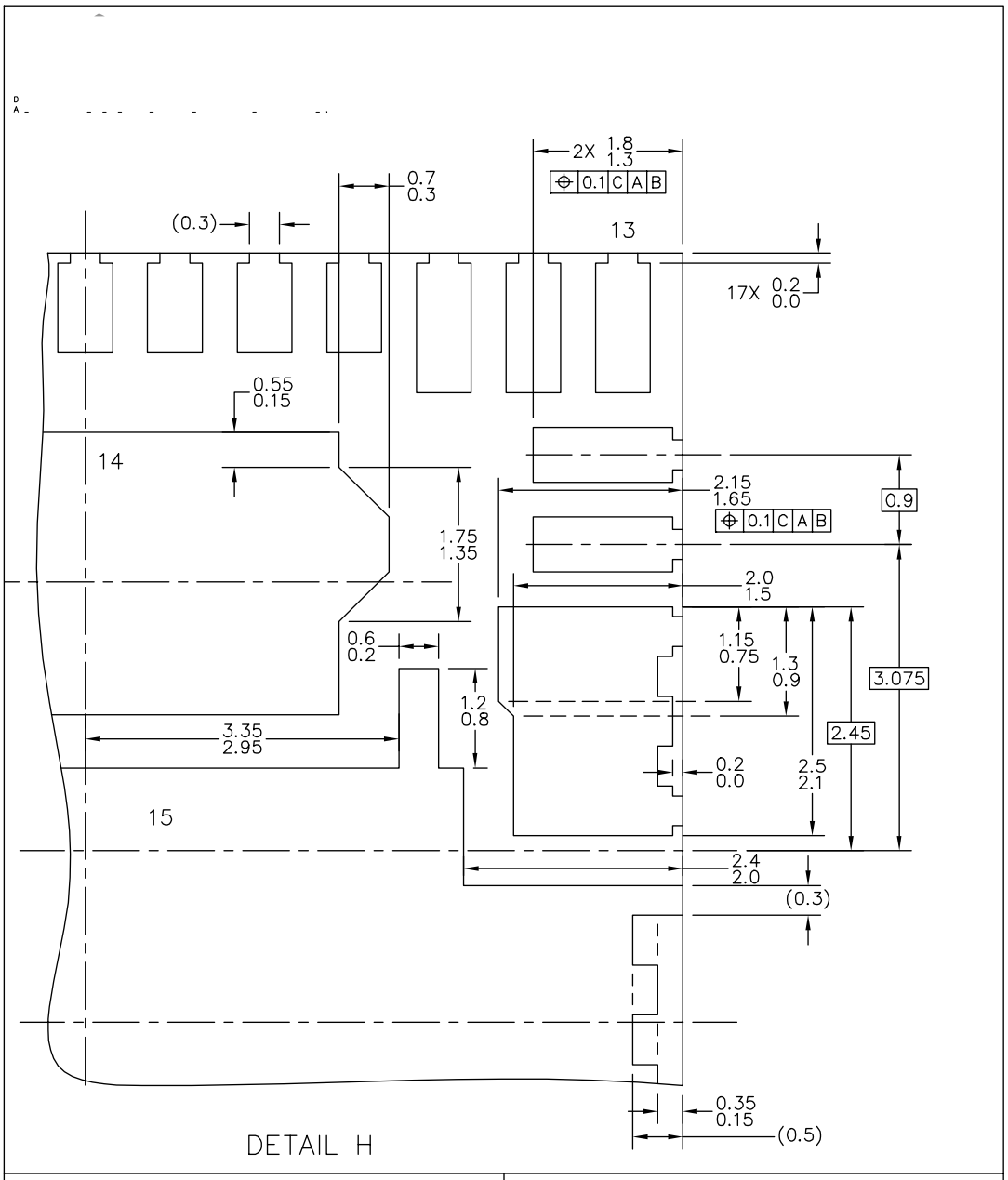


PNA SUFFIX
24-TERMINAL PQFN
PLASTIC PACKAGE
98ARL10596D
ISSUE B

33480



TITLE: POWER QUAD FLAT NON–LEADED PACKAGE (PWR QFN) 24 TERMINAL, 0.9 PITCH(12X12X2.1)	CASE NUMBER: 1593–03	
	STANDARD: FREESCALE	
	PACKAGE CODE: 6187	SHEET: 2 OF 5



TITLE: POWER QUAD FLAT NON–LEADED PACKAGE (PWR QFN) 24 TERMINAL, 0.9 PITCH(12X12X2.1)	CASE NUMBER: 1593–03
	STANDARD: FREESCALE
	PACKAGE CODE: 6187 SHEET: 3 OF 5

REVISION HISTORY

Revision	Date	Description of Changes
2.0	12/2005	• Implemented Revision History page • Converted to Freescale format

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