REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31		
REV STATUS OF SHEETS	REV																		
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14				

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
93-03-11

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 2K x 8 DUAL PORT STATIC RANDOM ACCESS MEMORY (SRAM), MONOLITHIC SILICON

SIZE	CAGE CODE	5962-90620
A	67268	

SHEET 1 OF 31

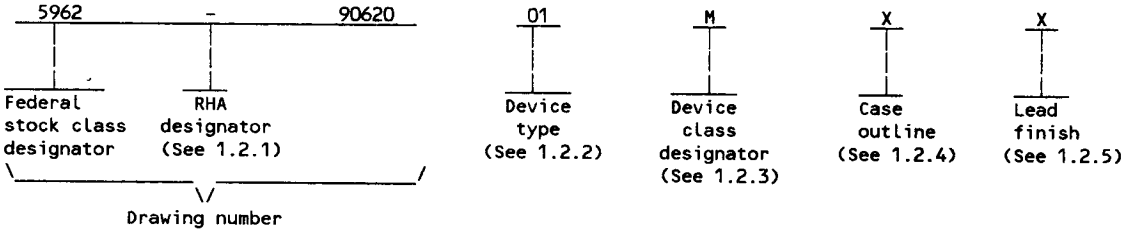
DESC FORM 193
JUL 91

5962-E495

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked device shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	7C132	2K X 8 Dual port SRAM, MASTER	55 ns
02	7C132	2K X 8 Dual port SRAM, MASTER	45 ns
03	7C132	2K X 8 Dual port SRAM, MASTER	35 ns
04	7C142	2K X 8 Dual port SRAM, SLAVE	55 ns
05	7C142	2K X 8 Dual port SRAM, SLAVE	45 ns
06	7C142	2K X 8 Dual port SRAM, SLAVE	35 ns
07	7C136	2K X 8 Dual port SRAM, MASTER	55 ns
08	7C136	2K X 8 Dual port SRAM, MASTER	45 ns
09	7C136	2K X 8 Dual port SRAM, MASTER	35 ns
10	7C146	2K X 8 Dual port SRAM, SLAVE	55 ns
11	7C146	2K X 8 Dual port SRAM, SLAVE	45 ns
12	7C146	2K X 8 Dual port SRAM, SLAVE	35 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level (see 6.7 herein) as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outlines shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CQCC1-N52	52	Square leadless chip carrier
Y	GDIP1-T48 or CDIP2-T48	48	Dual-in-line
Z	See figure 1	48	Square leadless chip carrier
U	See figure 1	48	Flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC voltage range applied to outputs in high Z state	-0.5 V dc to +7.0 V dc
DC Input voltage range	-3.0 V dc to +7.0 V dc
DC output current	20 mA
Maximum power dissipation 1/	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases X and Y	See MIL-STD-1835
Cases Z and U	10°C/W 2/
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Temperature under bias range	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0 V dc
Input high voltage range (V_{IH})	2.2 V dc to V_{CC} + 0.5 V dc
Input low voltage range (V_{IL}) 3/	-0.5 V dc to 0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	4/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ When a thermal resistance for this case is specified in MIL-STD-1835 that value shall supersede the value indicated herein.
3/ Negative undershoots to a minimum of -3.0 V are allowed with a maximum of 20 ns pulse width.
4/ When a QML source exists, a value shall be provided.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Military Drawings

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. This is a fully characterized military detail specification and is suitable for qualification of device classes B and S to the requirements of MIL-M-38510. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-M-38510) shall be subjected to and pass the internal moisture content test at 5000 ppm (method 1018 of MIL-STD-883), the frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity for class M or the qualifying activity for classes B and S. The TRB will ascertain the requirements as provided by MIL-I-38535 for classes Q and V. Samples may be pulled any time after seal.

3.2.5 Functional tests. Various functional tests used to test this device are contained in appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes B and S procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the qualifying activity. For classes Q and V procedures and circuits shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 41 (see MIL-M-38510, appendix E).

3.11 Serialization for device classes S and V. All device class S devices shall be serialized in accordance with MIL-M-38510. Class V shall be serialized in accordance with MIL-I-38535.

4.2.1 Additional criteria for device classes M, B, and S.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Static burn-in for device class S (method 1015 of MIL-STD-883, test condition A).

(a) All inputs shall be connected to GND. Outputs may be open or connected to 4.5 V minimum. Resistors R1 are optional on both inputs and outputs, and required on outputs connected to V_{CC} ±0.5 V. R1 = 220 Ω to 47 kΩ. For static II burn-in, reverse all input connections (i.e., V_{SS} to V_{CC}).

(b) V_{CC} = 4.5 V minimum.

(c) Ambient temperature (T_A) shall be +125°C minimum.

(d) Test duration for the static test shall be 48 hours minimum. The 48 hour burn-in shall be broken into two sequences of 24 hours each (static I and static II) followed by interim electrical measurements.

(2) Dynamic burn-in for device classes M, B, and S (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

d. For classes S and B devices, post dynamic burn-in electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.2.3 Percent defective allowable (PDA).

a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

b. The PDA for class B devices shall be in accordance with MIL-M-38510 for dynamic burn-in.

c. Static burn-in I and II failures shall be cumulative for determining PDA.

d. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits or electrical parameter limits specified in table I, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

e. The PDA for device classes Q and V shall be in accordance with MIL-I-38535 for dynamic burn-in.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Output high voltage	V_{OH}	V_{CC} = 4.5 V, $V_{IN} = V_{IH}, V_{IL}$, I_{OH} = -4.0 mA	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, $V_{IN} = V_{IH}, V_{IL}$					V
		I_{OL} = 4.0 mA	1, 2, 3	All		0.4	
		I_{OL} = 16.0 mA 1/	1, 2, 3	All		0.5	
Input high voltage 2/	V_{IH}		1, 2, 3	All	2.2		V
Input low voltage 2/	V_{IL}		1, 2, 3	All		0.8	V
Input leakage current	I_{IX}	V_{IN} = 5.5 V to GND	1, 2, 3	All	-5	5	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, V_{OUT} = 5.5 V and GND	1, 2, 3	All	-5	5	µA
Operating supply current	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, $\overline{CE}_L$ and $\overline{CE}_R = V_{IL}$, f = f_{MAX} 3/	1, 2, 3	01,02,04, 05,07,08, 10,11		120	mA
				03,06, 09,12		170	
Standby supply current, both ports, TTL inputs	I_{CC2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, $\overline{CE}_L$ and $\overline{CE}_R = V_{IH}$, f = f_{MAX} 3/	1, 2, 3	01,02,04, 05,07,08, 10,11		45	mA
				03,06, 09,12		65	
Standby supply current, one port, TTL inputs	I_{CC3}	V_{CC} = 5.5V, I_{OUT} = 0 mA, $\overline{CE}_R$ or $\overline{CE}_L = V_{IH}$, f = f_{MAX} 3/	1, 2, 3	01,02,04, 05,07,08, 10,11		90	mA
				03,06, 09,12		115	
Standby supply current, both ports, CMOS inputs	I_{CC4}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, $\overline{CE}_L$ and $\overline{CE}_R \ge (V_{CC} - 0.2\ V)$, all other inputs $\ge (V_{CC} - 0.2\ V)$, or ≤ 0.2 V, f = 0 3/	1, 2, 3	All		15	mA
Standby supply current, one port, CMOS inputs	I_{CC5}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, $\overline{CE}_L$ or $\overline{CE}_R \ge (V_{CC} - 0.2\ V)$, all other inputs $\ge (V_{CC} - 0.2\ V)$, or ≤ 0.2 V, f = f_{MAX} 3/	1, 2, 3	01,02,04, 05,07,08, 10,11		85	mA
				03,06, 09,12		105	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Input capacitance 4/	C_{IN}	V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz (See 4.4.1e)	4	All		15	pF
Output capacitance 4/	C_{OUT}	V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz (See 4.4.1e)	4	All		10	pF
Functional tests		See 4.4.1c	7,8A,8B	All			
Read cycle time	t_{AVAV}	See figures 4 and 5, read cycle timing 5/	9, 10, 11	01,04,07,10	55		ns
				02,05,08,11	45		
				03,06,09,12	35		
Address access time	t_{AVQV}		9, 10, 11	01,04,07,10		55	ns
				02,05,08,11		45	
				03,06,09,12		35	
Output hold from address change 4/	t_{AVQX}		9, 10, 11	All	0		ns
Chip enable access time	t_{ELQV}		9, 10, 11	01,04,07,10		55	ns
				02,05,08,11		45	
				03,06,09,12		35	
Output enable access time	t_{OLQV}		9, 10, 11	01,02,04,05,07,08,10,11		25	ns
				03,06,09,12		20	
Output enable to output active	t_{OLQX}	See figures 4 and 5, read cycle timing 4/ 6/	9, 10, 11	All	3		ns
Output enable to output inactive	t_{OHQZ}		9, 10, 11	01,04,07,10		25	ns
				02,03,05,06,08,09,11,12		20	
Chip enable to output active	t_{ELQX}		9, 10, 11	All	5		ns
Chip select to output inactive	t_{EHQZ}		9, 10, 11	01,04,07,10		25	ns
				02,03,05,06,08,09,11,12		20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Chip enable to power up 4/	t_{ELPU}	See figures 4 and 5, read cycle timing 5/	9, 10, 11	All	0		ns
Chip enable to power down 4/	t_{EHPD}		9, 10, 11	All		35	ns
Write cycle time	t_{AVAV}	See figures 4 and 5, write cycle timing 5/	9, 10, 11	01,04, 07,10	55		ns
				02,05, 08,11	45		
				03,06, 09,12	35		
Chip enable to write end	t_{ELWH}		9, 10, 11	01,04, 07,10	40		ns
				02,05, 08,11	35		
				03,06, 09,12	30		
Address setup to end of write	t_{AVWH}		9, 10, 11	01,04, 07,10	40		ns
				02,05, 08,11	35		
				03,06, 09,12	30		
Address hold from write end	t_{WHAX}		9, 10, 11	All	2		ns
Address setup to write start	t_{AVWL}		9, 10, 11	All	0		ns
Write enable pulse width	t_{WLWH}		9, 10, 11	01,02,04, 05,07,08, 10,11	30		ns
				03,06, 09,12	25		
Data setup to write end	t_{DVWH}		9, 10, 11	01,02,04, 05,07,08, 10,11	20		ns
				03,06, 09,12	15		
Data hold from write end	t_{WHDX}		9, 10, 11	All	0		ns
Write enable low to output inactive	t_{WLQZ}	See figures 4 and 5, write cycle timing 4/ 6/	9, 10, 11	01,04, 07,10		25	ns
				02,03,05, 06,08,09, 11,12		20	
Write enable high to output active	t_{WHQX}		9, 10, 11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Busy low from address match	t_{BLA}	See figures 4 and 5, busy cycle timing 5/	9, 10, 11	01,07		30	ns
				02,08		25	
				03,09		20	
Busy high from address mismatch 7/	t_{BHA}		9, 10, 11	01,07		30	ns
				02,08		25	
				03,09		20	
Busy low from chip enable low	t_{BLC}		9, 10, 11	01,07		30	ns
				02,08		25	
				03,09		20	
Busy high from chip enable high 7/	t_{BHC}		9, 10, 11	01,07		30	ns
				02,08		25	
				03,09		20	
Port setup for priority	t_{PS}		9, 10, 11	01-03, 07-09	5		ns
Write enable low after busy low	t_{WB}		9, 10, 11	04-06 10-12	0		ns
Write enable high after busy high	t_{WH}		9, 10, 11	04,05 10,11	35		ns
				06,12	30		
Busy high to valid data	t_{BDD}		9, 10, 11	01,02, 07,08		45	ns
				03,09		35	
Write data valid to read data valid 4/	t_{DDD}		9, 10, 11	01-03, 07-09		8/	ns
Write pulse to data delay 4/	t_{WDD}		9, 10, 11	01-03, 07-09		8/	ns
Write enable to interrupt set time	t_{WINS}	See figures 4 and 5, interrupt cycle timing 5/	9, 10, 11	07,10		45	ns
				08,11		35	
				09,12		25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Chip enable to interrupt set time	t_{EINS}	See figures 4 and 5, interrupt cycle timing 5/	9, 10, 11	07,10		45	ns
				08,11		35	
				09,12		25	
Address to interrupt set time	t_{INS}		9, 10, 11	07,10		45	ns
				08,11		35	
				09,12		25	
Output enable to interrupt reset time 7/	t_{OINR}		9, 10, 11	07,10		45	ns
				08,11		35	
				09,12		25	
Chip enable to interrupt reset time 7/	t_{EINR}		9, 10, 11	07,10		45	ns
				08,11		35	
				09,12		25	
Address to interrupt reset time 7/	t_{INR}		9, 10, 11	07,10		45	ns
				08,11		35	
				09,12		25	

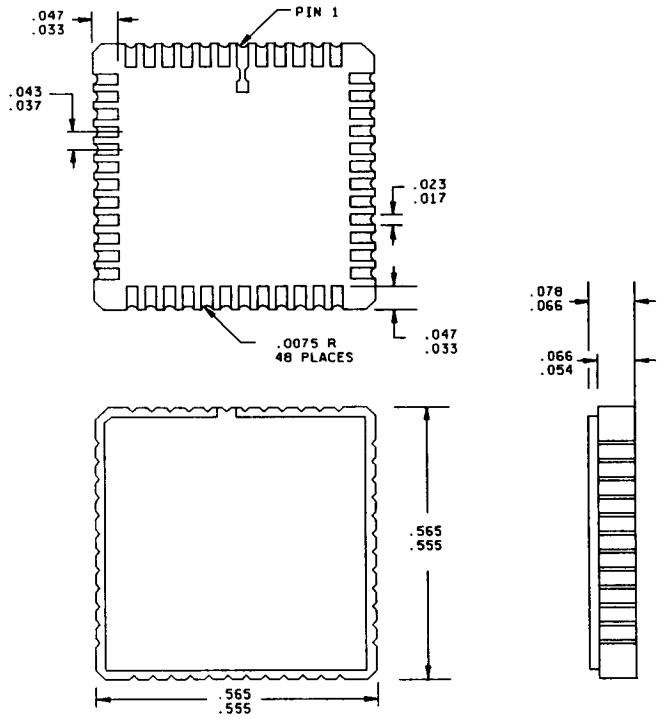
1/ $\overline{BUSY}$ and $\overline{INT}$ outputs only.
2/ These are absolute values with respect to device ground and all overshoots and undershoots due to system or tester noise are included.
3/ At $f = f_{MAX}$, address and data inputs are cycling at the maximum frequency of $1/t_{AVAV}$.
4/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
5/ AC tests are performed with transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load in figure 4 (circuit A). For BUSY and INT loads for devices 01-03 and 07-09 , see figure 4 (circuit C).
6/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input, C_L = 5 pF (including scope and jig). See figure 4 (circuit B). For BUSY and INT loads for devices 01-03 and 07-09, see figure 4 (circuit C).
7/ These parameters are measured from the input signal changing, until the output pin goes to the high-impedance state.
8/ A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
   A. BUSY on Port B goes HIGH.
   B. Port B's address toggled.
   C. CE for Port B is toggled.
   D. R/W for Port B is toggled, during valid read.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (per method 5005 table I)			Subgroups (per MIL-I-38535, table III)	
		Device class M	Device class B	Device class S	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9	1,7,9	1,7,9
2	Static burn-in I and II method 1015	Not required	Not required	Required	Not required	Required
3	Same as line 1			1*,7* Δ		1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required	Required	Required
5	Same as line 1			1*,7* Δ		1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**, 7,8A, 8B,9,10,11	1,2,3,4**, 7,8A, 8B,9,10,11	1,2,3,4**, 7,8A, 8B,9,10,11	1,2,3,4**, 7,8A, 8B,9,10,11	1,2,3,4**, 7,8A, 8B,9,10,11
8	Group B end-point electrical parameters			1,2,3,7, 8A,8B,9, 10,11 Δ		
9	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B Δ		1,2,3,7, 8A,8B Δ	1,2,3,7, 8A,8B,9, 10,11 Δ
10	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
11	Group E end-point electrical parameters	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δindicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters.
7/ See 4.4.1d.

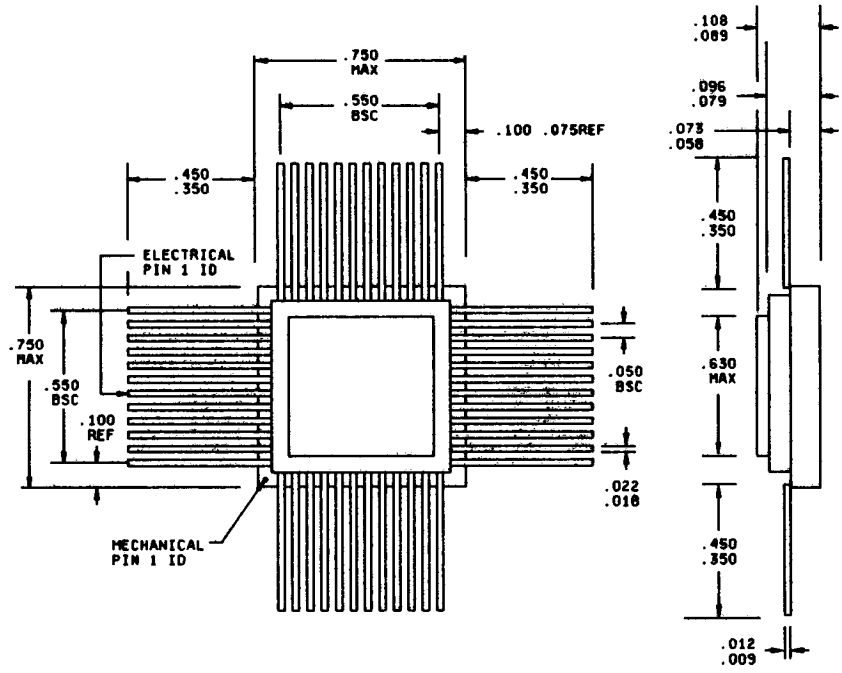
Case Z



Inches	mm	Inches	mm
.0075	0.191	.047	1.19
.017	0.43	.054	1.37
.023	0.58	.066	1.68
.033	0.84	.078	1.98
.037	0.94	.555	14.10
.043	1.09	.565	14.35

FIGURE 1. Case outlines.

Case U



Inches	mm	Inches	mm
.009	0.23	.096	2.44
.012	0.30	.100	2.54
.018	0.46	.108	2.74
.022	0.56	.350	8.89
.050	1.27	.450	11.43
.058	1.47	.550	13.97
.073	1.85	.630	16.00
.079	2.01	.750	19.05
.089	2.26		

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

FIGURE 1. Case outlines - Continued.

Device types	01-06	07-12	Device types	01-06	07-12
Case outlines	Y, Z, and U	X	Case outlines	Y, Z, and U	X
Terminal number	Terminal symbol		Terminal number	Terminal symbol	
1	$\overline{CE}_L$	$\overline{CE}_L$	27	I/O_{2R}	I/O_{0R}
2	$R/\overline{W}_L$	$R/\overline{W}_L$	28	I/O_{3R}	I/O_{1R}
3	$\overline{BUSY}_L$	$\overline{BUSY}_L$	29	I/O_{4R}	I/O_{2R}
4	A_{10L}	$\overline{INT}_L$	30	I/O_{5R}	I/O_{3R}
5	$\overline{OE}_L$	A_{10L}	31	I/O_{6R}	I/O_{4R}
6	A_{0L}	$\overline{OE}_L$	32	I/O_{7R}	I/O_{5R}
7	A_{1L}	A_{0L}	33	A_{9R}	I/O_{6R}
8	A_{2L}	A_{1L}	34	A_{8R}	I/O_{7R}
9	A_{3L}	A_{2L}	35	A_{7R}	NC
10	A_{4L}	A_{3L}	36	A_{6R}	A_{9R}
11	A_{5L}	A_{4L}	37	A_{5R}	A_{8R}
12	A_{6L}	A_{5L}	38	A_{4R}	A_{7R}
13	A_{7L}	A_{6L}	39	A_{3R}	A_{6R}
14	A_{8L}	A_{7L}	40	A_{2R}	A_{5R}
15	A_{9L}	A_{8L}	41	A_{1R}	A_{4R}
16	I/O_{0L}	A_{9L}	42	A_{0R}	A_{3R}
17	I/O_{1L}	I/O_{0L}	43	$\overline{OE}_R$	A_{2R}
18	I/O_{2L}	I/O_{1L}	44	A_{10R}	A_{1R}
19	I/O_{3L}	I/O_{2L}	45	$\overline{BUSY}_R$	A_{0R}
20	I/O_{4L}	I/O_{3L}	46	$R/\overline{W}_R$	$\overline{OE}_R$
21	I/O_{5L}	I/O_{4L}	47	$\overline{CE}_R$	A_{10R}
22	I/O_{6L}	I/O_{5L}	48	V_{CC}	$\overline{INT}_R$
23	I/O_{7L}	I/O_{6L}	49	---	$\overline{BUSY}_R$
24	GND	I/O_{7L}	50	---	$R/\overline{W}_R$
25	I/O_{0R}	NC	51	---	$\overline{CE}_R$
26	I/O_{1R}	GND	52	---	V_{CC}

FIGURE 2. Terminal connections.

Noncontention read/write control

Left or right port (see note 1)				
$R/\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	Function
X	H	X	Z	Port disabled and in power-down mode I_{CC3} or I_{CC5}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, power-down mode I_{CC2} or I_{CC4}
L	L	X	Data in	Data on port written into memory (see note 2)
H	L	L	Data out	Data in memory output on port (see note 3)
H	L	H	Z	High impedance outputs

NOTES:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
2. If $\overline{BUSY}$ = L, data is not written.
3. If BUSY = L, data may not be valid. See t_{WDD} and t_{DDD} timing.

H = High, L = Low, X = Don't care, Z = High impedance

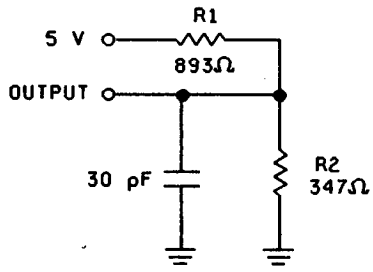
FIGURE 3. Truth tables.

Bus arbitration

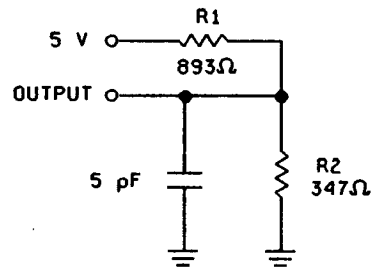
Left port		Right port		Flags (see notes)		Function
$\overline{CE}_L$	$A_{0L} - A_{10L}$	$\overline{CE}_R$	$A_{0R} - A_{10R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No contention
L	Any	H	X	H	H	No contention
H	X	L	Any	H	H	No contention
L	$\neq A_{0R} - A_{10R}$	L	$\neq A_{0L} - A_{10L}$	H	H	No contention
Address arbitration with $\overline{CE}$ low before address match						
L	LV5R	L	LV5R	H	L	Left-port wins
L	RV5L	L	RV5L	L	H	Right-port wins
L	Same	L	Same	H	L	Arbitration resolved
L	Same	L	Same	L	H	Arbitration resolved
$\overline{CE}$ arbitration with address match before $\overline{CE}$						
LL5R	$= A_{0R} - A_{10R}$	LL5R	$= A_{0L} - A_{10L}$	H	L	Left-port wins
RL5L	$= A_{0R} - A_{10R}$	RL5L	$= A_{0L} - A_{10L}$	L	H	Right-port wins
LW5R	$= A_{0R} - A_{10R}$	LW5R	$= A_{0L} - A_{10L}$	H	L	Arbitration resolved
LW5R	$= A_{0R} - A_{10R}$	LW5R	$= A_{0L} - A_{10L}$	L	H	Arbitration resolved

NOTES:
1. X = Don't care, L = Low, H = High.
2. LV5R = Left address valid $\geq$ 5 ns before right address.
3. RV5L = Right address valid $\geq$ 5 ns before left address.
4. Same = Left and right addresses match within 5 ns of each other.
5. LL5R = Left $\overline{CE}$ = Low $\geq$ 5 ns before left $\overline{CE}$.
6. RL5L = Right $\overline{CE}$ = Low $\geq$ 5 ns before left $\overline{CE}$.
7. LW5R = Left and right $\overline{CE}$ = Low within 5 ns of each other.

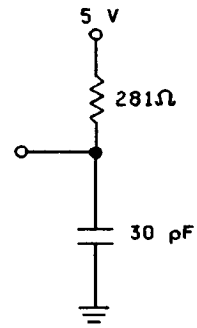
FIGURE 3. Truth tables - Continued.



CIRCUIT A
OUTPUT LOAD



CIRCUIT B
OUTPUT LOAD



CIRCUIT C
OUTPUT LOAD

(FOR t_{OLQX}, t_{OHQZ}, t_{ELQX}, t_{EHQZ}, t_{HLQZ}, t_{WHQX})

NOTES:
1. Capacitance includes scope and jig. (minimum values)
2. Circuit C is used only for BUSY and INT loads for devices 01-03 and 07-09.

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times (t_r, t_f)	≤ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

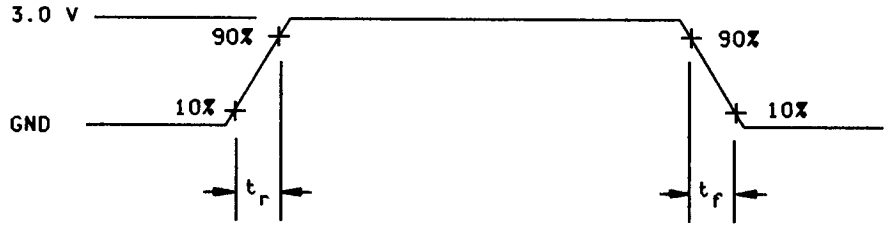
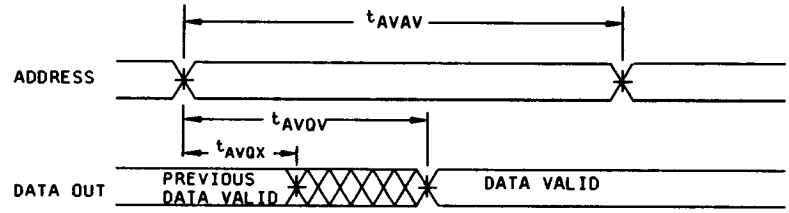
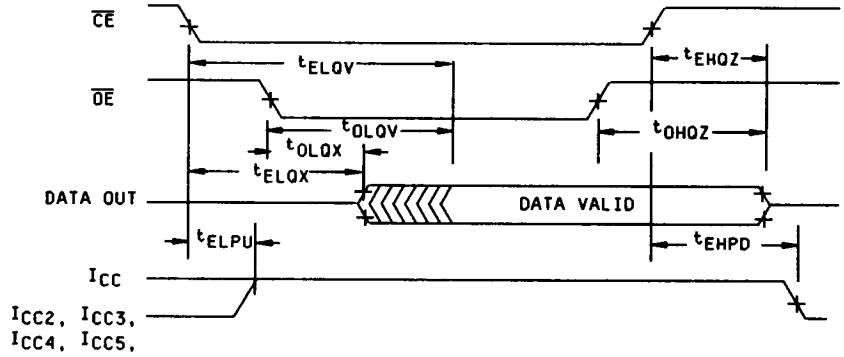


FIGURE 4. Output load circuit and test conditions.

Read cycle number 1 either port (see notes 1 and 2)



Read cycle number 2 either port (see notes 1 and 3)



Read cycle number 3 read with $\overline{BUSY}$ (see note 2) - master devices only

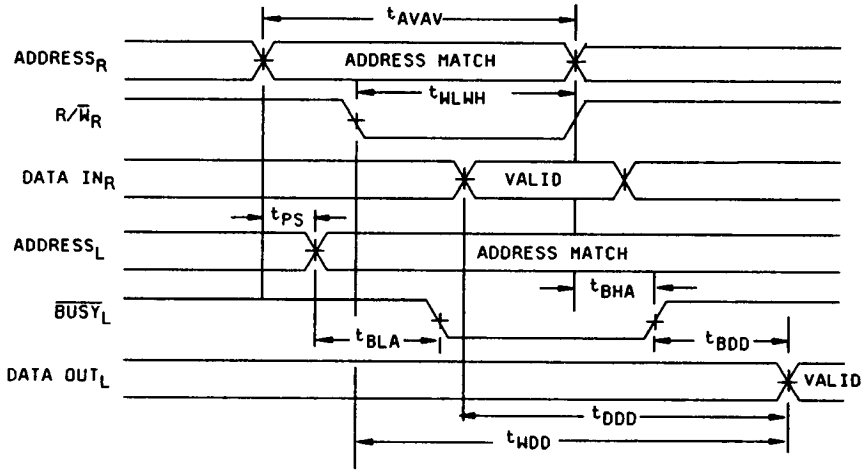
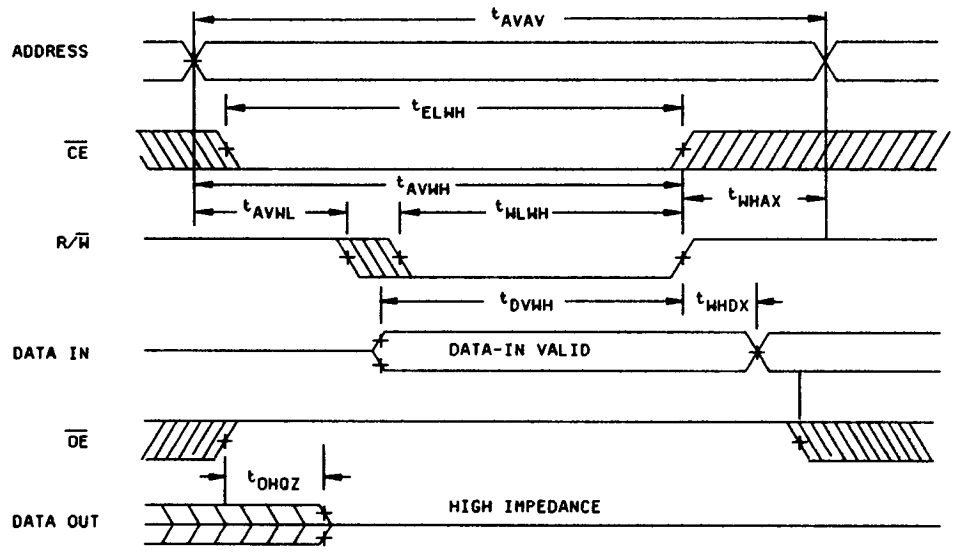


FIGURE 5. Timing waveforms.

Write cycle number 1 either port (see notes 4, 5, 6, and 7)



Write cycle number 2 either port (see notes 4, 5, 6, and 7)

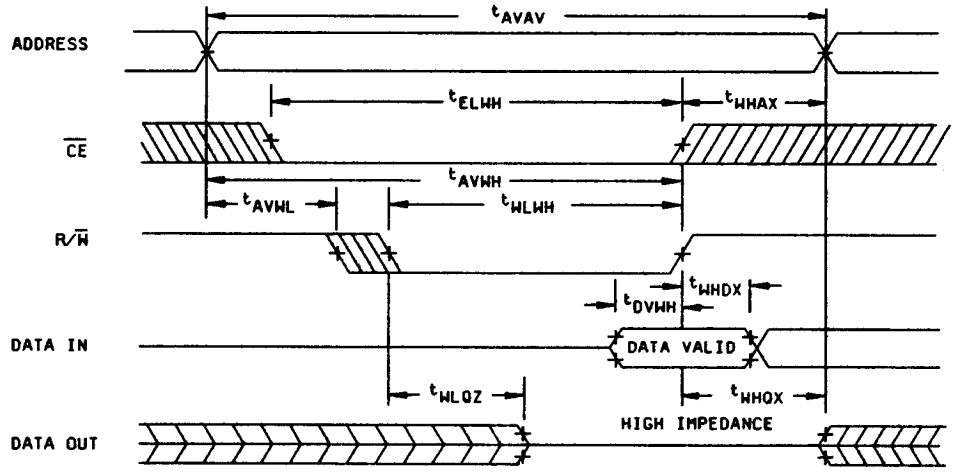
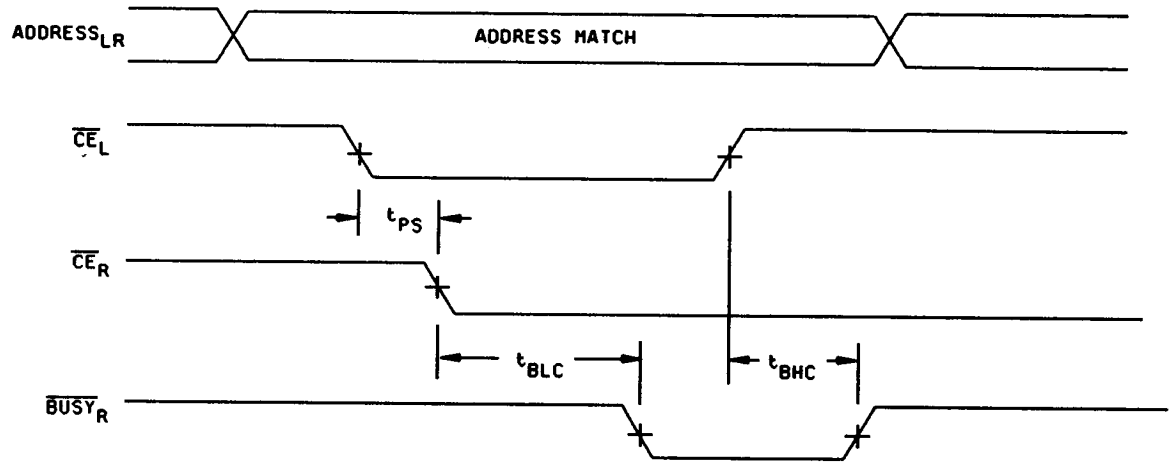


FIGURE 5. Timing waveforms - Continued.

Busy timing number 1 ($\overline{CE}$ arbitration) - master devices only

$\overline{CE}_L$ valid first:



$\overline{CE}_R$ valid first:

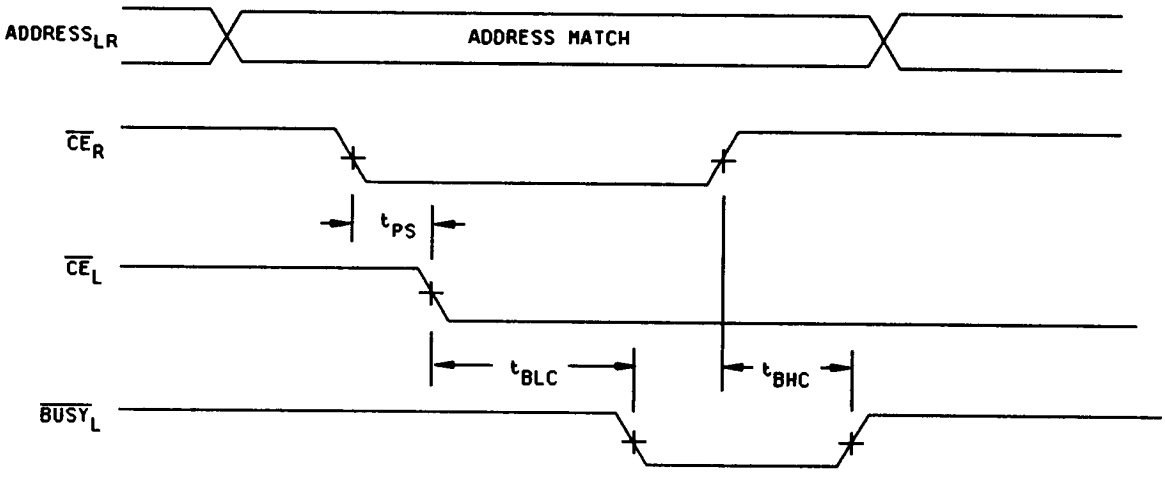
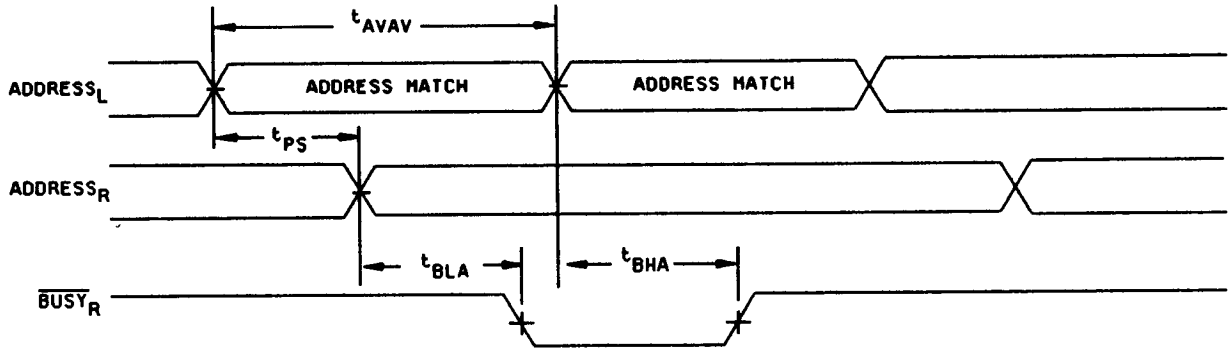


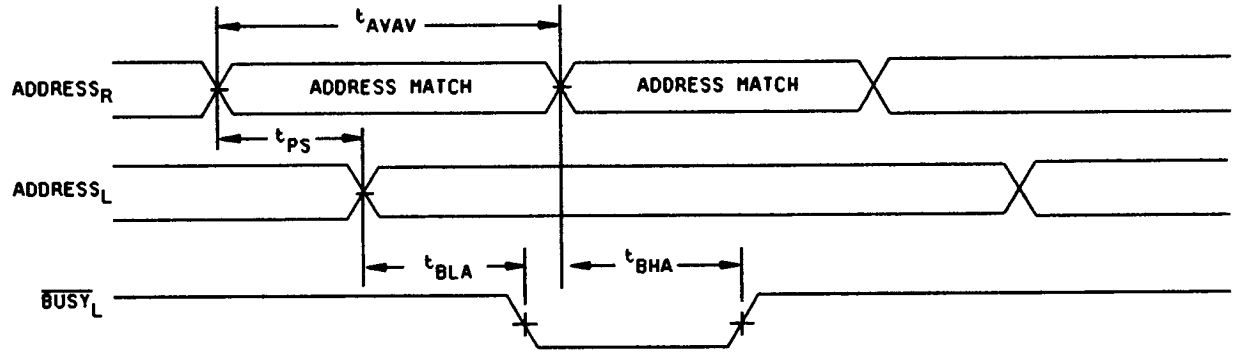
FIGURE 5. Timing waveforms - Continued.

Busy timing number 2 (address arbitration) - master devices only

Left address valid first



Right address valid first



Busy timing number 3 (Write with $\overline{BUSY}$) - slave devices only

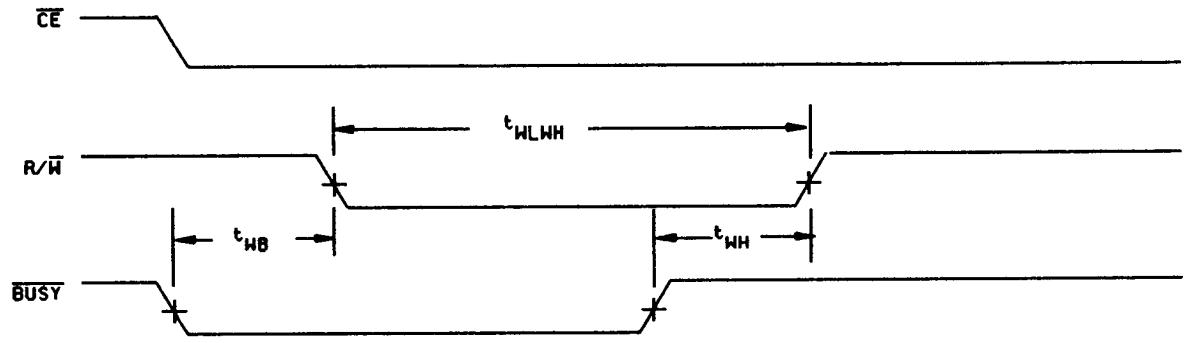
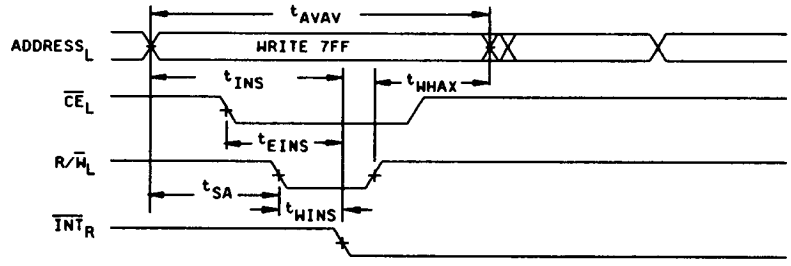


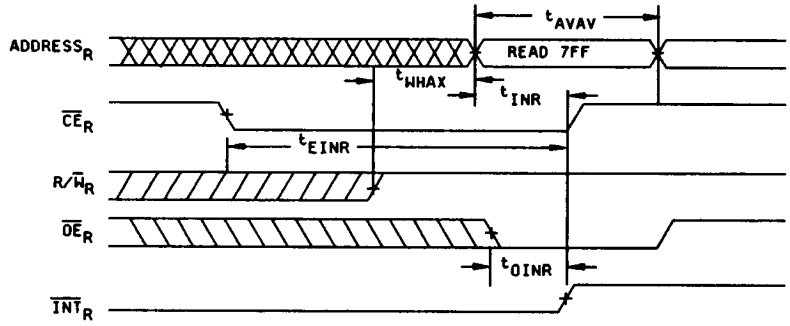
FIGURE 5. Timing waveforms - Continued.

Interrupt timing (device types 07 - 12)

Left side sets $\overline{INT}_R$:



Right side clears $\overline{INT}_R$:



Right side sets $\overline{INT}_L$:

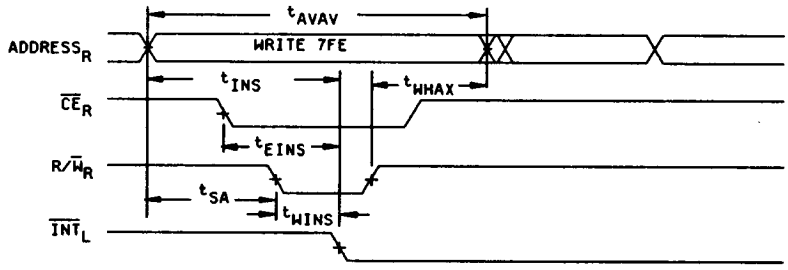
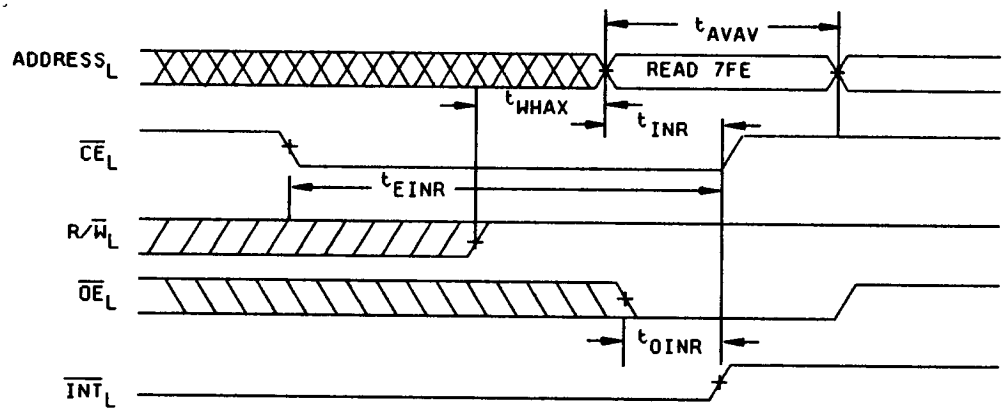


FIGURE 5. Timing waveforms - Continued.

Left side clears $\overline{INT}_L$:



NOTES:
1. R/$\overline{W}$ is high for read cycle.
2. For read cycles no. 1 and no. 3, device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
3. For read cycle no. 2, addresses are valid prior to or coincident with $\overline{CE}$ transition low.
4. A write occurs during the overlap of $\overline{CE}$ low and R/$\overline{W}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WLWH} or $t_{WLQZ} + t_{DVWH}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{DVWH}.
6. If $\overline{CE}$ switches low coincident with or after R/$\overline{W}$ switches low, the outputs will stay in a high impedance state.

FIGURE 5. Timing waveforms - Continued.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{CC4} standby	± 10 %
I_{IX}, I_{OZ}	± 10 %

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

4.2.3 Percent defective allowable (PDA).

a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

b. The PDA for class B devices shall be in accordance with MIL-M-38510 for dynamic burn-in.

c. Static burn-in I and II failures shall be cumulative for determining PDA.

d. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits or electrical parameter limits specified in table I, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

e. The PDA for device classes Q and V shall be in accordance with MIL-I-38535 for dynamic burn-in.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Qualification data for subgroups 7, 8A, and 8B shall be attributes only.

4.3.1.1 Qualification extension for device classes B and S. When authorized by the qualifying activity, if a manufacturer qualifies one device type which is identical (i.e., same die) to other device types on this specification, the slower device types may be part I qualified, upon the request of the manufacturer, without any further testing. The faster device types may be part I qualified by performing only group A qualification testing.

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q or V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes B and S subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes B and S, the procedures and circuits shall be maintained under document revision control by the manufacturer and shall be made available to the qualifying activity upon request. For device classes Q and V, the procedures and circuits shall be shall be under the control of the device manufacturer's (TRB) in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

a. For device class S, steady-state life test circuits shall be conducted using test condition D and the circuit described in 4.2.1b herein, or equivalent as approved by the qualifying activity.

b. For device class S only, end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 5 of group B inspections and shall consist of tests specified in table IIB herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M, shall be M and D.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device classes B,S,Q, and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513)296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513)296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

C_{IN} C_{OUT}	Input and bidirectional output, terminal-to-GND capacitance.
GND	Ground zero voltage potential.
I_{CC}	Supply current.
T_C	Case temperature.
T_A	Ambient temperature
V_{CC}	Positive supply voltage.
O/V	Latch-up over-voltage
O/I	Latch-up over-current

6.5.1 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case character subscripts. The initial character is always "t" and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal specify the signal name and the signal transitions. Thus the format is:

t X X X X

Signal name from which interval is derived

Transition direction for first signal

Signal name to which interval is defined

Transition direction for second signal

a. Signal definitions:

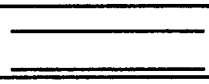
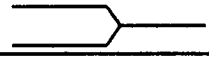
A = Address
D = Data in
Q = Data out
W = Write enable
E = Chip enable
O = Output enable

b. Transition definitions:

H = Transition to high
L = Transition to low
V = Transition to valid
X = Transition to invalid or don't care
Z = Transition to off (high impedance)

6.5.2 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.3 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN'S. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

30.2 Algorithm B (pattern 2).

30.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (All "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially, for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for, each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

30.3 Algorithm C (pattern 3).

30.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (All "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially, for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

30.4 Algorithm D (pattern 4).

30.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.