MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Document order number: MC33892
Rev 1.0, 03/2004

Preliminary Information

33892

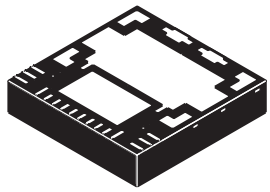
Quad Intelligent High-Side Switch (Dual 10 mΩ and Dual 35 mΩ)

QUAD INTELLIGENT HIGH-SIDE SWITCH

The 33892 is one in a family of devices designed for low-voltage automotive and industrial lighting and motor control applications. Its four low $R_{DS(ON)}$ MOSFETs (two 10 mΩ, two 35 mΩ) can control the high sides of four separate resistive or inductive loads or serve as high-side switches for a pair of DC motors.

Programming, control, and diagnostics are accomplished using a 16-bit SPI interface. Additionally, each output has its own parallel input for PWM control if desired. The 33892 allows the user to program via the SPI the fault current trip levels and duration of acceptable lamp inrush or motor stall intervals. Such programmability allows tight control of fault currents and can protect wiring harnesses and circuit boards as well as loads.

The 33892 is packaged in a power-enhanced 10 x 10 nonleaded Power QFN package with exposed tabs.



PNC SUFFIX
CASE 1558-02
24-TERMINAL PQFN

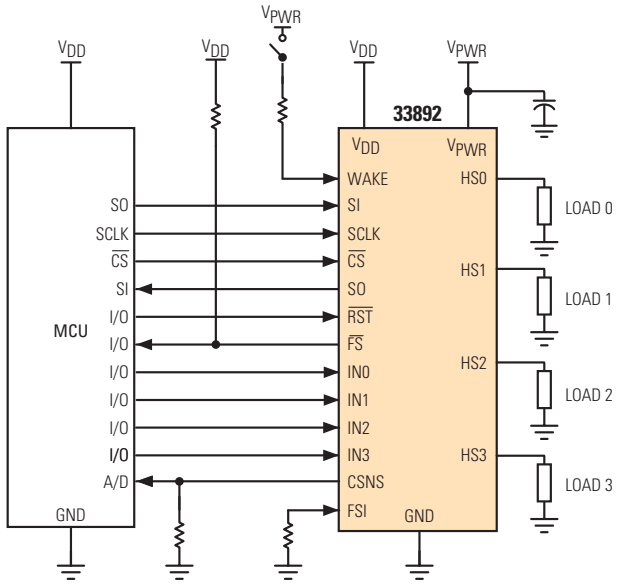
Features

- Dual 10 mΩ and Dual 35 mΩ High-Side Switches
- Operating Voltage Range of 6.0 V to 27 V with Standby Current < 5.0 μA
- SPI Control of Overcurrent Limit, Overcurrent Fault Blanking Time, Output-OFF Open Load Detection, Output ON/OFF Control, Watchdog Timeout, Slew Rates, and Fault Status Reporting
- SPI Status Reporting of Overcurrent, Open and Shorted Loads, Overtemperature, Undervoltage and Overvoltage Shutdown, Fail-Safe Terminal Status, and Program Status
- Analog Current Feedback with Selectable Ratio
- Enhanced 16 V Reverse Polarity V_{PWR} Protection

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
PC33892PNC/R2	-40°C to 125°C	24 PQFN

33892 Simplified Application Diagram



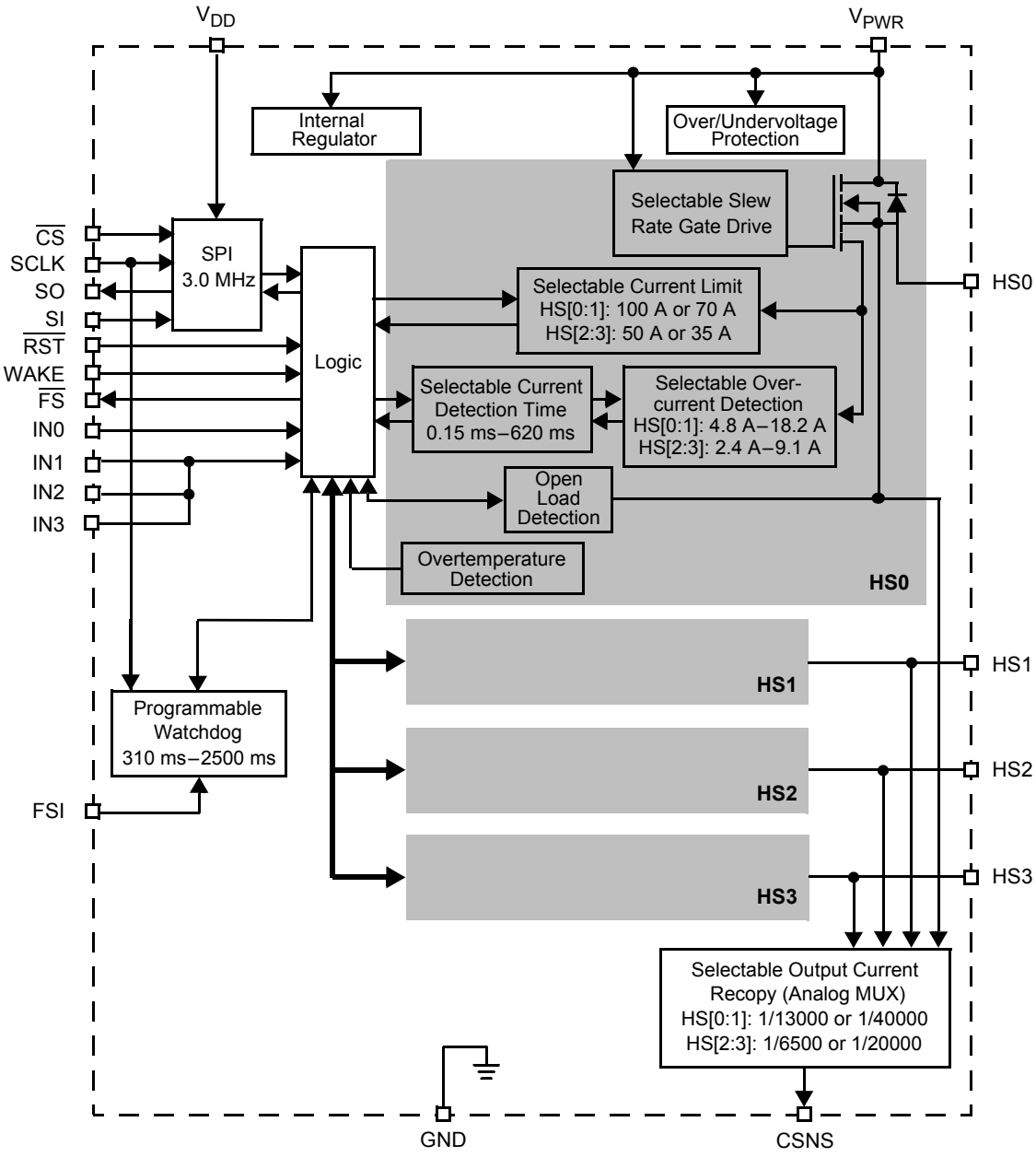
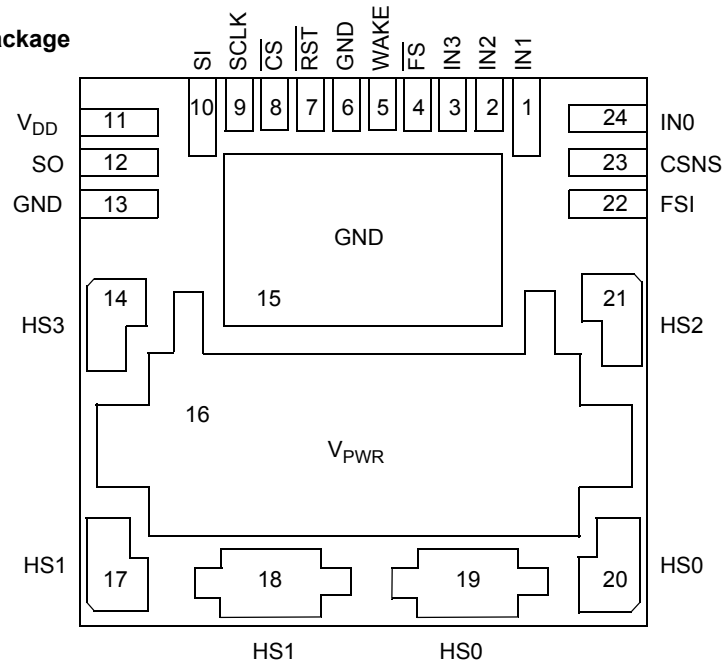


Figure 1. 33892 Simplified Internal Block Diagram

Transparent Top View of Package



TERMINAL FUNCTION DESCRIPTION

Terminal	Terminal Name	Formal Name	Definition
1 2 3 24	IN1 IN2 IN3 IN0	Serial Inputs	The IN0−IN3 high-side input terminals are used to directly control HS0−HS3 high-side output terminals, respectively. An SPI register determines if each input is activated or if the input logic state is ORed or ANDed with the SPI instruction. These terminals are to be driven with 5.0 V CMOS levels, and they have an internal active pull-down current source.
4	$\overline{FS}$	Fault Status (Active Low)	This terminal is an open drain configured output requiring an external pull-up resistor to V_{DD} for fault reporting. If a device fault condition is detected, this terminal is active LOW. Specific device diagnostic faults are reported via the SPI SO terminal.
5	WAKE	Wake	This terminal is an input that controls the device mode and watchdog timeout feature if enabled. An internal clamp protects this terminal from high damaging voltages when the output is current limited with an external resistor. This input has an internal passive pull-down.
6, 13, 15	GND	Ground	These terminals are the ground for the logic and analog circuitry of the device.
7	$\overline{RST}$	Reset	This terminal is an input used to initialize the device configuration and fault registers, as well as place the device in a low-current sleep mode. The terminal also starts the watchdog timer when transitioning from logic [0] to logic [1]. This terminal should not be allowed to be logic [1] until V_{DD} is in regulation. This terminal has an internal passive pull-down.
8	$\overline{CS}$	Chip Select (Active Low)	This terminal is an input terminal connected to a chip select output of a master microcontroller (MCU). The MCU determines which device is addressed (selected) to receive data by pulling the $\overline{CS}$ terminal of the selected device logic LOW, thereby enabling SPI communication with the device. Other *unselected* devices on the serial link having their $\overline{CS}$ terminals pulled up logic HIGH disregard the SPI communication data sent. This terminal has an internal active pull-up current source and requires CMOS logic levels.
9	SCLK	Serial Clock	This terminal is an input terminal connected to the MCU providing the required bit shift clock for SPI communication. It transitions one time per bit transferred at an operating frequency, f_{SPI}, defined by the communication interface. The 50 percent duty cycle CMOS level serial clock signal is idle between command transfers. The signal is used to shift data into and out-of the device. This terminal has an internal active pull-down.

TERMINAL FUNCTION DESCRIPTION (continued)

Terminal	Terminal Name	Formal Name	Definition
10	SI	Serial Input	This terminal is a command data input terminal connected to the SPI Serial Data Output of the MCU or to the SO terminal of the previous device of a daisy chain of devices. The input requires CMOS logic level signals and incorporates an internal active pull-down. Device control is facilitated by the input's receiving the MSB first of a serial 8-bit control command. The MCU ensures data is available upon the falling edge of SCLK. The logic state of SI present upon the rising edge of SCLK loads that bit command into the internal command shift register. This terminal has an internal active pull-down.
11	V_{DD}	Digital Drain Voltage (Power)	This terminal is an external voltage input terminal used to supply power to the SPI circuit. In the event V_{DD} is lost, an internal supply provides power to a portion of the logic, ensuring limited functionality of the device.
12	SO	Serial Output	This terminal is an output terminal connected to the SPI Serial Data Input terminal of the MCU or to the SI terminal of the next device of a daisy chain of devices. This output will remain tri-stated (high-impedance OFF condition) so long as the $\overline{CS}$ terminal of the device is logic HIGH. SO is only active when the $\overline{CS}$ terminal of the device is asserted logic LOW. The generated SO output signals are CMOS logic levels. SO output data is available on the falling edge of SCLK and transitions immediately on the rising edge of SCLK.
16	V_{PWR}	Positive Power Supply	This terminal connects to the positive power supply and is the source of operational power for the device. The V_{PWR} contact is the backside surface mount tab of the package.
14 21	HS3 HS2	High-Side Outputs	Protected 35 mΩ high-side power output terminals to the load.
17, 18 19, 20	HS1 (Note 1) HS0 (Note 2)	High-Side Outputs	Protected 10 mΩ high-side power output terminals to the load.
22	FSI	Fail-Safe Input	The value of the resistance connected between this terminal and ground determines the state of the outputs after a Watchdog timeout occurs. Depending on the resistance value, either all outputs are OFF or the output HSO only is ON. If the FSI terminal is left to float up to a logic [1] level, then the outputs HS0 and HS2 will turn ON when in the Fail-Safe state. When the FSI terminal is connected to GND, the Watchdog circuit and Fail-Safe operation are disabled. This terminal incorporates an active internal pull-up.
23	CSNS	Output Current Monitoring	The Current Sense terminal sources a current proportional to the designated HS0–HS3 output. That current is fed into a ground referenced resistor and its voltage is monitored by an MCU's A/D. The channel to be monitored is selected via the SPI. This terminal can be tri-stated through SPI.

Notes
1. HS1 output (17 and 18) must be connected externally on the PCB as close as possible to the terminals.
2. HS0 output (19 and 20) must be connected externally on the PCB as close as possible to the terminals.

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
Operating Voltage Range Steady-State	$V_{PWR(SS)}$	 -16 to 41	V
V_{DD} Supply Voltage	V_{DD}	0 to 5.5	V
Input/Output Voltage (Note 3)	$V_{IN[0:3]}$, $\overline{RST}$, FSI, CSNS, SI, SCLK, $\overline{CS}$, $\overline{FS}$	-0.3 to 7.0	V
SO Output Voltage (Note 3)	V_{SO}	-0.3 to V_{DD}+0.3	V
WAKE Input Clamp Current	$I_{CL(WAKE)}$	2.5	mA
CSNS Input Clamp Current	$I_{CL(CSNS)}$	10	mA
Output Current (Note 4)	I_{HS0}, I_{HS1}	25	A
Output Current (Note 4)	I_{HS2}, I_{HS3}	12	A
Output Clamp Energy (Note 5)	E_{CL0}, E_{CL1}	TBD	J
Output Clamp Energy (Note 5)	E_{CL2}, E_{CL3}	TBD	J
Storage Temperature	T_{STG}	-55 to 150	°C
Operating Ambient Temperature	T_A	-40 to 125	°C
Operating Junction Temperature	T_J	-40 to 150	°C
Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 <1.0 TBD	°C/W
ESD Voltage Human Body Model (Note 6) Machine Model (Note 7)	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V
Terminal Soldering Temperature (Note 8)	T_{SOLDER}	240	°C

Notes

3. Exceeding voltage limits on IN[0:3], $\overline{RST}$, FSI, CSNS, SI, SO, SCLK, $\overline{CS}$, or $\overline{FS}$ terminals may cause a malfunction or permanent damage to the device.
4. Continuous high-side output current rating so long as maximum junction temperature is not exceeded. Calculation of maximum output current using package thermal resistance is required.
5. Active clamp energy using single-pulse method (L = 16 mH, R_L = 0 Ω, V_{PWR} = 12 V, T_J = 150°C).
6. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
7. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω) and in accordance with the system module specification with a capacitor > 0.01 μF connected from high-side outputs to GND.
8. Terminal soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Battery Supply Voltage Range Fully Operational	V_{PWR}	 6.0	 –	 27	V
V_{PWR} Operating Supply Current Outputs ON, $I_{HS[0:3]}$ = 0 A	$I_{PWR(on)}$	 –	 –	 20	mA
V_{PWR} Supply Current Outputs OFF, Open Load Detection Disabled, WAKE > 0.7 V_{DD}, $\overline{RST}$ = $V_{LOGIC\ HIGH}$	$I_{PWR(sby)}$	 –	 –	 5.0	mA
Sleep State Supply Current (V_{PWR} < 14 V, $\overline{RST}$ < 0.5 V, WAKE < 0.5 V) T_J = 25°C T_J = 85°C	$I_{PWR(sleep)}$	 – –	 – –	 10 50	μA
V_{DD} Supply Voltage	$V_{DD(on)}$	4.5	5.0	5.5	V
V_{DD} Supply Current No SPI Communication 3.0 MHz SPI Communication	$I_{DD(on)}$	 – –	 – –	 1.0 5.0	mA
V_{DD} Sleep State Current	$I_{DD(sleep)}$	–	–	5.0	μA
Overvoltage Shutdown Threshold	$V_{PWR(OV)}$	28	32	36	V
Overvoltage Shutdown Hysteresis	$V_{PWR(OVHYS)}$	0.2	0.8	1.5	V
Undervoltage Shutdown Threshold (Note 9)	$V_{PWR(UV)}$	4.75	5.24	5.75	V
Undervoltage Hysteresis (Note 10)	$V_{PWR(UVHYS)}$	–	0.25	–	V
Undervoltage Power-ON Reset	$V_{PWR(UVPOR)}$	–	–	5.0	V

Notes

9. Output will automatically recover to instructed state when V_{PWR} voltage is restored to normal so long as the V_{PWR} degradation level did not go below the undervoltage power-ON reset threshold. This applies to all internal device logic that is supplied by V_{PWR} and assumes that the external V_{DD} supply is within specification.
10. This applies when the undervoltage fault is not latched (IN = 0).

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUTS HS0 AND HS1					
Output Drain-to-Source ON Resistance ($I_{HS[0:1]}$ = 10 A, T_J = 25°C)	$R_{DS(ON)25}$				mΩ
V_{PWR} = 6.0 V		–	–	15	
V_{PWR} = 10 V		–	–	10	
V_{PWR} = 13 V		–	–	10	
Output Drain-to-Source ON Resistance ($I_{HS[0:1]}$ = 10 A, T_J = 150°C)	$R_{DS(ON)150}$				mΩ
V_{PWR} = 6.0 V		–	–	26	
V_{PWR} = 10 V		–	–	17	
V_{PWR} = 13 V		–	–	17	
Output Source-to-Drain ON Resistance (Note 11)	$R_{SD(ON)}$				mΩ
I_{HS} = 15 A, T_J = 25°C, V_{PWR} = -12 V		–	10	20	
Output Overcurrent High Detection Levels (9.0 V ≤ V_{PWR} ≤ 16 V)					A
SOCH = 0	I_{OCH0}	80	100	120	
SOCH = 1	I_{OCH1}	56	70	84	
Overcurrent Low Detection Levels (SOCL[2:0], 9.0 V ≤ V_{PWR} ≤ 16 V)					A
000	I_{OCL0}	14.6	18.2	22.8	
001	I_{OCL1}	13.0	16.3	20.4	
010	I_{OCL2}	11.5	14.4	18	
011	I_{OCL3}	10.0	12.5	15.7	
100	I_{OCL4}	8.4	10.5	13.2	
101	I_{OCL5}	6.9	8.6	10.8	
110	I_{OCL6}	5.4	6.7	8.4	
111	I_{OCL7}	3.8	4.8	6.0	
Current Sense Ratio (9.0 V ≤ V_{PWR} ≤ 16 V, CSNS ≤ 4.5 V)					–
DICR D2 = 0	C_{SR0}	–	1/13000	–	
DICR D2 = 1	C_{SR1}	–	1/40000	–	
Current Sense Ratio (C_{SR0}) Accuracy	C_{SR0_ACC}				%
Output Current					
5.0 A		-20	–	20	
10 A		-14	–	14	
12.5 A		-13	–	13	
15 A		-12	–	12	
20 A		-13	–	13	
25 A		-13	–	13	

Notes

11. Source-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{PWR}.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUTS HS0 AND HS1 (continued)					
Current Sense Ratio (C_{SR1}) Accuracy	C_{SR1_ACC}				%
Output Current					
5.0 A		-25	–	25	
10 A		-19	–	19	
12.5 A		-18	–	18	
15 A		-17	–	17	
20 A		-18	–	18	
25 A		-18	–	18	
Maximum Current Sense Clamp Voltage	$V_{CL(MAXCSNS)}$				V
I_{CSNS} = 15 mA		4.5	6.0	7.0	
Open Load Detection Current (Note 12)	I_{OLDC}	30	–	100	μA
Output Fault Detection Threshold	$V_{OFD(THRES)}$				V
Output Programmed OFF		2.0	3.0	4.0	
Output Negative Clamp Voltage	V_{CL}				V
0.5 A ≤ = I_{HS} ≤ = 2.0 A, Output OFF		-20	–	–	
Overtemperature Shutdown (Note 13)	T_{SD}				°C
T_A = 125°C, Output OFF		150	175	190	
Overtemperature Shutdown Hysteresis (Note 13)	$T_{SD(HYS)}$	5.0	–	20	°C
OUTPUTS HS2 AND HS3					
Output Drain-to-Source ON Resistance ($I_{HS[2:3]}$ = 5.0 A, T_J = 25°C)	$R_{DS(ON)25}$				mΩ
V_{PWR} = 6.0 V		–	–	55	
V_{PWR} = 10 V		–	–	35	
V_{PWR} = 13 V		–	–	35	
Output Drain-to-Source ON Resistance ($I_{HS[2:3]}$ = 5.0 A, T_J = 150°C)	$R_{DS(ON)150}$				mΩ
V_{PWR} = 6.0 V		–	–	94	
V_{PWR} = 10 V		–	–	60	
V_{PWR} = 13 V		–	–	60	
Output Source-to-Drain ON Resistance (Note 14)	$R_{DS(ON)}$				mΩ
I_{HS} = 15 A, T_J = 25°C, V_{PWR} = -12 V		–	35	70	
Output Overcurrent High Detection Levels (9.0 V ≤ V_{PWR} ≤ 16 V)					A
SOCH = 0	I_{OCH0}	40	50	62	
SOCH = 1	I_{OCH1}	28	35	43	

Notes

12. Output OFF Open Load Detection Current is the current required to flow through the load for the purpose of detecting the existence of an open load condition when the specific output is commanded OFF.
13. Guaranteed by process monitoring. Not production tested.
14. Source-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{PWR}.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUTS HS2 AND HS3 (continued)					
Overcurrent Low Detection Levels (SOCL[2:0], 9.0 V ≤ V_{PWR} ≤ 16 V)					A
000	I_{OCL0}	7.2	9.1	11	
001	I_{OCL1}	6.5	8.15	9.8	
010	I_{OCL2}	5.7	7.2	8.7	
011	I_{OCL3}	5.0	6.25	7.5	
100	I_{OCL4}	4.2	5.25	6.3	
101	I_{OCL5}	3.4	4.3	5.2	
110	I_{OCL6}	2.6	3.35	4.1	
111	I_{OCL7}	1.9	2.4	2.9	
Current Sense Ratio (9.0 V ≤ V_{PWR} ≤ 16 V, CSNS ≤ 4.5 V)					–
DICR D2 = 0	C_{SR2}	–	1/6500	–	
DICR D2 = 1	C_{SR3}	–	1/20000	–	
Current Sense Ratio (C_{SR2}) Accuracy	C_{SR2_ACC}				%
Output Current					
2.0 A		-20	–	20	
5.0 A		-14	–	14	
10 A		-13	–	13	
12.5 A		-12	–	12	
15 A		-13	–	13	
20 A		-13	–	13	
Current Sense Ratio (C_{SR3}) Accuracy	C_{SR3_ACC}				%
Output Current					
5.0 A		-25	–	25	
10 A		-19	–	19	
12.5 A		-18	–	18	
15 A		-17	–	17	
20 A		-18	–	18	
25 A		-18	–	18	
Maximum Current Sense Clamp Voltage	$V_{CL(MAXCSNS)}$				V
I_{CSNS} = 15 mA		4.5	6.0	7.0	
Open Load Detection Current (Note 15)	I_{OLDC}	30	–	100	μA
Output Fault Detection Threshold	$V_{OFD(THRES)}$				V
Output Programmed OFF		2.0	3.0	4.0	
Output Negative Clamp Voltage	V_{CL}				V
0.5 A ≤ = I_{HS} ≤ = 2.0 A, Output OFF		-20	–	–	
Overtemperature Shutdown (Note 16)	T_{SD}				°C
T_A = 125°C, Output OFF		150	175	190	
Overtemperature Shutdown Hysteresis (Note 16)	$T_{SD(HYS)}$	5.0	–	20	°C

Notes

15. Output OFF Open Load Detection Current is the current required to flow through the load for the purpose of detecting the existence of an open load condition when the specific output is commanded OFF.
16. Guaranteed by process monitoring. Not production tested.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CONTROL INTERFACE					
Input Logic High Voltage (Note 17)	V_{IH}	$0.7V_{DD}$	–	–	V
Input Logic Low Voltage (Note 17)	V_{IL}	–	–	$0.2V_{DD}$	V
Input Logic Voltage Hysteresis (Note 17)	$V_{IN(HYS)}$	100	350	750	mV
Input Logic Pull-Down Current (SCLK, IN, SI, IN[0:3])	I_{DWN}	5.0	–	20	μA
$\overline{RST}$ Input Voltage Range	$V_{\overline{RST}}$	4.5	5.0	5.5	V
SO, $\overline{FS}$ Tri-State Capacitance (Note 18)	C_{SO}	–	–	20	pF
Input Logic Pull-Down Resistor ($\overline{RST}$) and WAKE	I_{DWN}	100	200	400	kΩ
Input Capacitance (Note 19)	C_{IN}	–	4.0	12	pF
Wake Input Clamp Voltage (Note 20) $I_{CL(WAKE)}$ < 2.5 mA	$V_{CL(WAKE)}$	7.0	–	14	V
Wake Input Forward Voltage $I_{CL(WAKE)}$ = -2.5 mA	$V_{F(WAKE)}$	-2.0	–	-0.3	V
SO High-State Output Voltage I_{OH} = 1.0 mA	V_{SOH}	$0.8V_{DD}$	–	–	V
$\overline{FS}$, SO Low-State Output Voltage I_{OL} = -1.6 mA	V_{SOL}	–	0.2	0.4	V
SO Tri-State Leakage Current $\overline{CS} \geq 0.7\,V_{DD}$	$I_{SO(LEAK)}$	-5.0	0	5.0	μA
Input Logic Pull-Up Current (Note 21) $\overline{CS}$, V_{IN} > 0.7 V_{DD}	I_{UP}	5.0	–	20	μA
FSI Input terminal External Pull-Down Resistance (Note 22)	RFS				kΩ
FSI Disabled, HS[0:3] Indeterminate	RFSdis	–	0	1.0	
FSI Enabled, all HS OFF	RFSoffoff	6.0	6.5	7.0	
FSI Enabled, HS0 ON, HS[1:3] OFF	RFSonoff	15	17	19	
FSI Enabled, HS0 and HS2 ON, HS1 and HS3 OFF	RFSonon	30	Infinite	–	

Notes

17. Upper and lower logic threshold voltage range applies to SI, $\overline{CS}$, SCLK, $\overline{RST}$, IN[0:3], and WAKE input signals. The WAKE and $\overline{RST}$ signals may be supplied by a derived voltage referenced to V_{PWR}.
18. Parameter is guaranteed by process monitoring but is not production tested.
19. Input capacitance of SI, $\overline{CS}$, SCLK, $\overline{RST}$, and WAKE. This parameter is guaranteed by process monitoring but is not production tested.
20. The current must be limited by a series resistance when using voltages > 7.0 V.
21. Pull-up current is with $\overline{CS}$ OPEN. $\overline{CS}$ has an active internal pull-up to V_{DD}.
22. The selection of the RFS must take into consideration the tolerance, temperature coefficient and lifetime duration to assure that the resistance value will always be within the desired (specified) range.

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING HS0, HS1, HS2, AND HS3					
Output Rising Slow Slew Rate A (DICR D3 = 0) (Note 23) 9.0 V < V_{PWR} < 16 V	SR_{RA_SLOW}	0.1	0.3	0.5	V/µs
Output Rising Slow Slew Rate B (DICR D3 = 0) (Note 24) 9.0 V < V_{PWR} < 16 V	SR_{RB_SLOW}	0.015	0.05	0.15	V/µs
Output Rising Fast Slew Rate A (DICR D3 = 1) (Note 23) 9.0 V < V_{PWR} < 16 V	SR_{RA_FAST}	0.2	0.5	1.5	V/µs
Output Rising Fast Slew Rate B (DICR D3 = 1) (Note 24) 9.0 V < V_{PWR} < 16 V	SR_{RB_FAST}	0.015	0.05	0.5	V/µs
Output Falling Slow Slew Rate A (DICR D3 = 0) (Note 23) 9.0 V < V_{PWR} < 16 V	SR_{FA_SLOW}	0.1	0.3	0.5	V/µs
Output Falling Slow Slew Rate B (DICR D3 = 0) (Note 24) 9.0 V < V_{PWR} < 16 V	SR_{FB_SLOW}	0.015	0.05	0.15	V/µs
Output Falling Fast Slew Rate A (DICR D3 = 1) (Note 23) 9.0 V < V_{PWR} < 16 V	SR_{FA_FAST}	0.4	1.0	2.0	V/µs
Output Falling Fast Slew Rate B (DICR D3 = 1) (Note 24) 9.0 V < V_{PWR} < 16 V	SR_{FB_FAST}	0.05	0.175	0.6	V/µs
Output Turn-ON Delay Time in Fast/Slow Slew Rate (Note 25) DICR = 0, DICR = 1	$t_{DLY(ON)}$	2.0	30	200	µs
Output Turn-OFF Delay Time in Slow Slew Rate Mode (Note 26) DICR = 0	$t_{DLY\_SLOW(OFF)}$	40	460	1000	µs
Output Turn-OFF Delay Time in Fast Slew Rate Mode (Note 26) DICR = 1	$t_{DLY\_FAST(OFF)}$	20	120	400	µs
Direct Input Switching Frequency (DICR D3 = 0)	f_{PWM}	–	–	300	Hz
Overcurrent Low Detection Blanking Time (OCLT[1:0]) 00 01 10 11	 t_{OCL0} t_{OCL1} t_{OCL2} t_{OCL3}	 108 434 55 0.08	 155 620 75 0.15	 202 806 95 0.25	ms

Notes

23. Rise and Fall Slew Rates A measured across a 5.0 Ω resistive load at high-side output = 0.5 V to V_{PWR}-3.5 V (see Figure 2, page 14). These parameters are guaranteed by process monitoring.
24. Rise and Fall Slew Rates B measured across a 5.0 Ω resistive load at high-side output = 0.5 V to V_{PWR}-3.5 V (see Figure 2). These parameters are guaranteed by process monitoring.
25. Turn-ON delay time measured from rising edge of any signal (IN[0:3], SCLK, $\overline{CS}$) that would turn the output ON to V_{HS} = 0.5 V with R_L = 5.0 Ω resistive load.
26. Turn-OFF delay time measured from falling edge of any signal (IN[0:3], SCLK, $\overline{CS}$) that would turn the output OFF to V_{HS} = V_{PWR}-0.5 V with R_L = 5.0 Ω resistive load.

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING HS0, HS1, HS2, AND HS3 (continued)					
Overcurrent High Detection Blanking Time	t_{OCH}	1.0	10	20	µs
$\overline{CS}$ to CSNS Valid Time (Note 27)	CNS_{VAL}	–	–	10	µs
Watchdog Timeout (WD[1:0]) (Note 28)					ms
00	t_{WDTO0}	496	620	806	
01	t_{WDTO1}	248	310	403	
10	t_{WDTO2}	2000	2500	3250	
11	t_{WDTO3}	1000	1250	1625	

Notes

27. Time necessary for the CSNS to be with ±5% of the targeted value.
28. Watchdog timeout delay measured from the rising edge of WAKE or $\overline{RST}$ from a sleep state condition, to output turn-ON with the output driven OFF and FSI floating. The values shown are for WDR setting of [00]. The accuracy of t_{WDTO} is consistent for all configured watchdog timeouts.

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 6.0 V ≤ V_{PWR} ≤ 27 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI INTERFACE CHARACTERISTICS					
Maximum Frequency of SPI Operation	f_{SPI}	–	–	3.0	MHz
Required Low State Duration for $\overline{RST}$ (Note 29)	$t_{W\overline{RST}}$	–	50	350	ns
Rising Edge of $\overline{CS}$ to Falling Edge of $\overline{CS}$ (Required Setup Time) (Note 30)	$t_{\overline{CS}}$	–	–	300	ns
Rising Edge of $\overline{RST}$ to Falling Edge of $\overline{CS}$ (Required Setup Time) (Note 30)	t_{ENBL}	–	–	5.0	µs
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (Required Setup Time) (Note 30)	t_{LEAD}	–	50	167	ns
Required High State Duration of SCLK (Required Setup Time) (Note 30)	t_{WSCLKh}	–	–	167	ns
Required Low State Duration of SCLK (Required Setup Time) (Note 30)	t_{WSCLKl}	–	–	167	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ (Required Setup Time) (Note 30)	t_{LAG}	–	50	167	ns
SI to Falling Edge of SCLK (Required Setup Time) (Note 31)	$t_{SI(SU)}$	–	25	83	ns
Falling Edge of SCLK to SI (Required Setup Time) (Note 31)	$t_{SI(HOLD)}$	–	25	83	ns
SO Rise Time C_L = 200 pF	t_{RSO}	–	25	50	ns
SO Fall Time C_L = 200 pF	t_{FSO}	–	25	50	ns
SI, $\overline{CS}$, SCLK, Incoming Signal Rise Time (Note 31)	t_{RSI}	–	–	50	ns
SI, $\overline{CS}$, SCLK, Incoming Signal Fall Time (Note 31)	t_{FSI}	–	–	50	ns
Time from Falling Edge of $\overline{CS}$ to SO Low Impedance (Note 32)	$t_{SO(EN)}$	–	–	145	ns
Time from Rising Edge of $\overline{CS}$ to SO High Impedance (Note 33)	$t_{SO(DIS)}$	–	65	145	ns
Time from Rising Edge of SCLK to SO Data Valid (Note 34) 0.2 V_{DD} ≤ SO ≥ 0.8 V_{DD}, C_L = 200 pF	t_{VALID}	–	65	105	ns

Notes

29. $\overline{RST}$ low duration measured with outputs enabled and going to OFF or disabled condition.
30. Maximum setup time required for the 33892 is the minimum guaranteed time needed from the microcontroller.
31. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
32. Time required for output status data to be available for use at SO. 1.0 kΩ on pull-up on $\overline{CS}$.
33. Time required for output status data to be terminated at SO. 1.0 kΩ on pull-up on $\overline{CS}$.
34. Time required to obtain valid data out from SO following the rise of SCLK.

Timing Diagrams

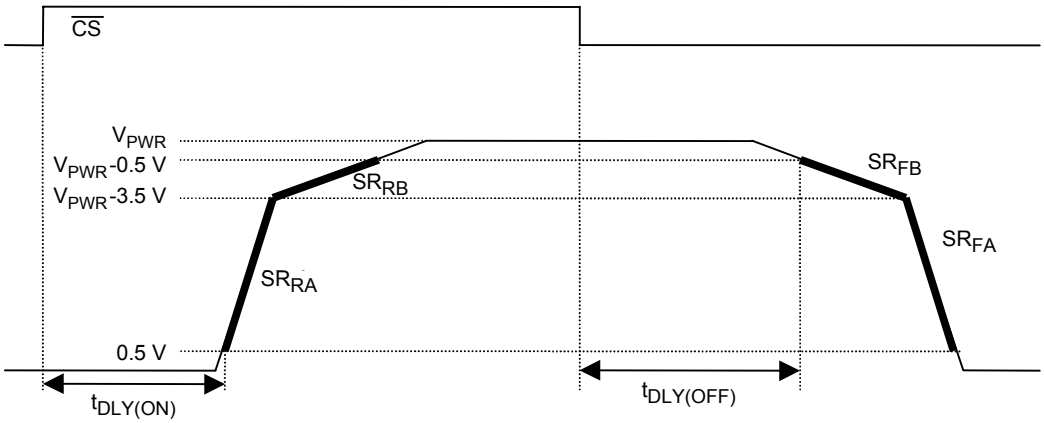


Figure 2. Output Slew Rate and Time Delays

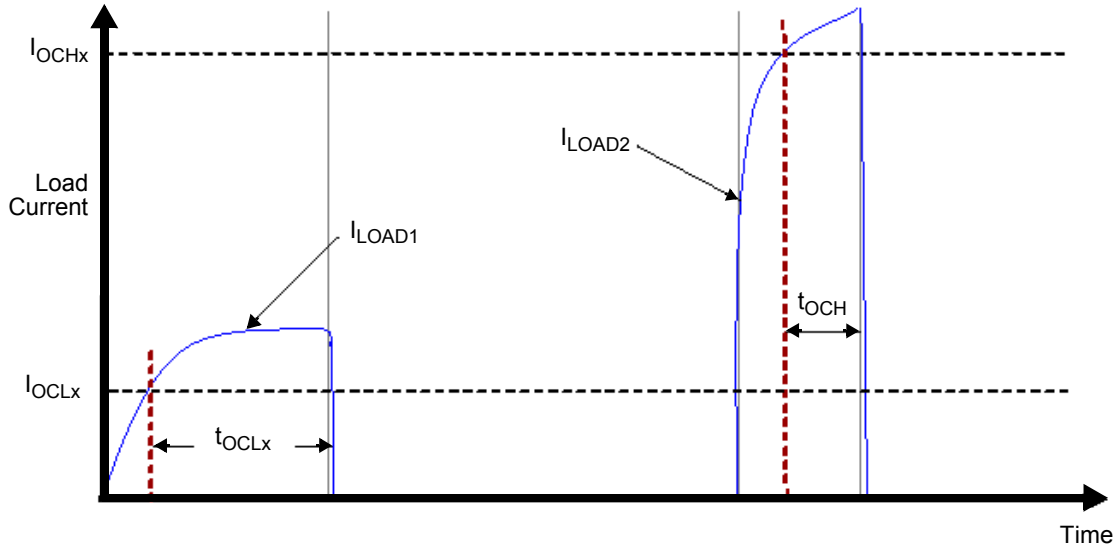


Figure 3. Overcurrent Shutdown

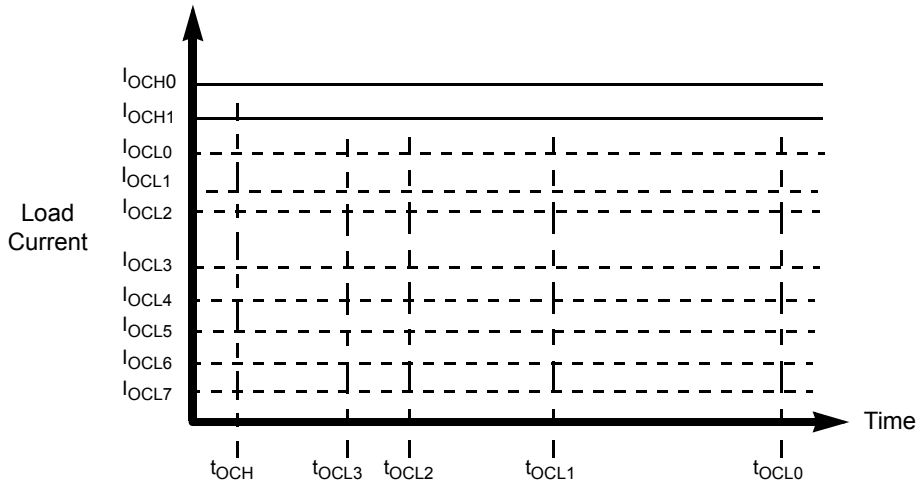


Figure 4. Overcurrent Low and High Detection

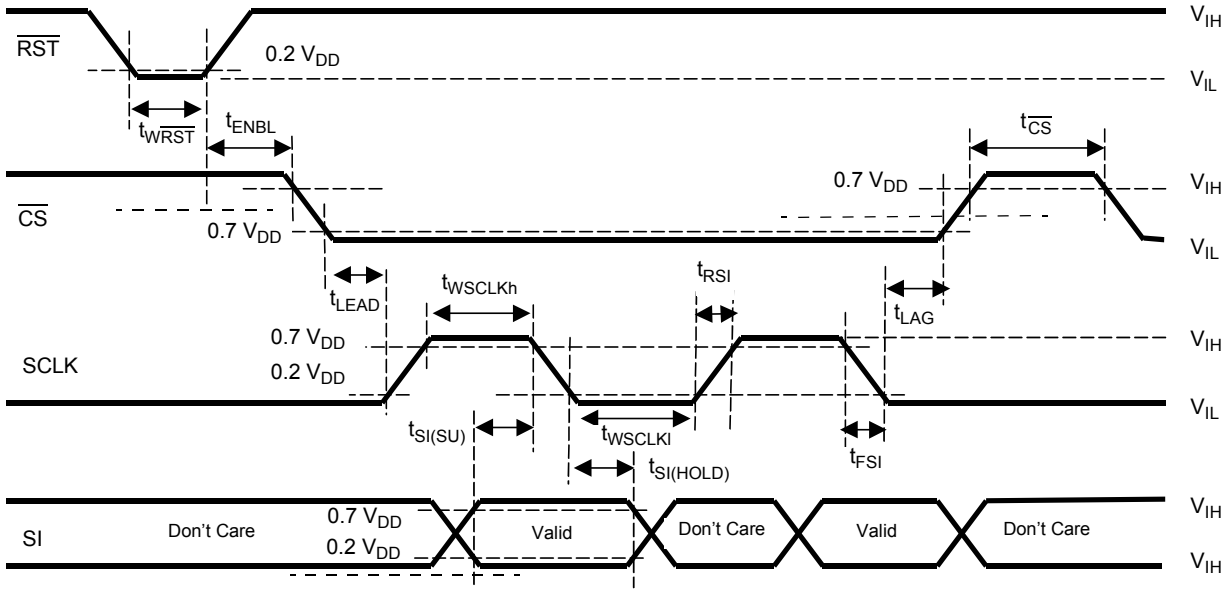


Figure 5. Input Timing Switching Characteristics

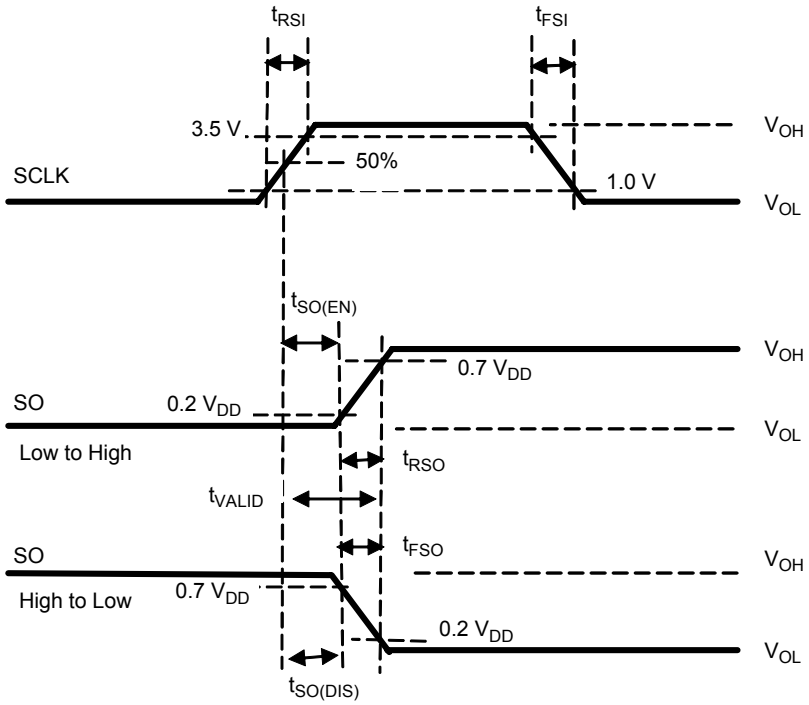


Figure 6. SCLK Waveform and Valid SO Data Delay Time

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 33892 is one in a family of devices designed for low-voltage automotive and industrial lighting and motor control applications. Its four low $R_{DS(ON)}$ MOSFETs (two 10 mΩ, two 35 mΩ) can control the high sides of four separate resistive or inductive loads or serve as high-side switches for a pair of DC motors.

Programming, control, and diagnostics are accomplished using a 16-bit SPI interface. Additionally, each output has its own parallel input for PWM control if desired. The 33892 allows the user to program via the SPI the fault current trip levels and duration of acceptable lamp inrush or motor stall intervals. Such programmability allows tight control of fault currents and can protect wiring harnesses and circuit boards as well as loads.

The 33892 is packaged in a power-enhanced 10 x 10 PQFN package with exposed tabs.

FUNCTIONAL DESCRIPTION

SPI Protocol Description

The SPI interface has a full duplex, three-wire synchronous data transfer with four I/O lines associated with it: Serial Input (SI), Serial Output (SO), Serial Clock (SCLK), and Chip Select ($\overline{CS}$).

The SI/SO terminals of the 33892 follow a first-in first-out (D15 to D0) protocol, with both input and output words transferring the most significant bit (MSB) first. All inputs are compatible with 5.0 V CMOS logic levels.

The SPI lines perform the following functions:

Serial Input (SI)

This is a serial interface (SI) command data input terminal. Each SI bit is read on the falling edge of SCLK. A 16-bit stream of serial data is required on the SI terminal, starting with D15 to D0. The internal registers of the 33892 are configured and controlled using a 5-bit addressing scheme described in Table 1, page 18. Register addressing and configuration are described in Table 2, page 19. The SI input has an internal pull-down, I_{DWN}.

Serial Output (SO)

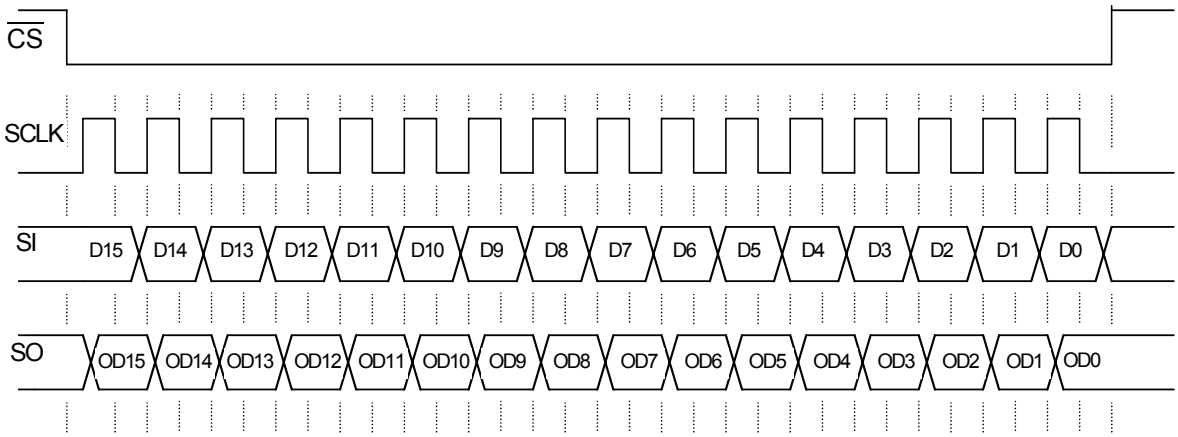
The SO data terminal is a tri-stateable output from the shift register. The SO terminal remains in a high-impedance state until the $\overline{CS}$ terminal is put into a logic [0] state. The SO data is capable of reporting the status of the output, the device configuration, and the state of the key inputs. The SO terminal changes state on the rising edge of SCLK and reads out on the falling edge of SCLK. Fault and input status descriptions are provided in Table 9, page 22.

Serial Clock (SCLK)

The SCLK terminal clocks the internal shift registers of the 33892 device. The serial input (SI) terminal accepts data into the input shift register on the falling edge of the SCLK signal while the serial output (SO) terminal shifts data information out of the SO line driver on the rising edge of the SCLK signal. It is important the SCLK terminal be in a logic low state whenever $\overline{CS}$ makes any transition. For this reason, it is recommended the SCLK terminal be in a logic [0] whenever the device is not accessed ($\overline{CS}$ logic [1] state). SCLK has an internal pull-down. When $\overline{CS}$ is logic [1], signals at the SCLK and SI terminals are ignored and SO is tri-stated (high impedance) (see Figure 7, page 18).

Chip Select ($\overline{CS}$)

The $\overline{CS}$ terminal enables communication with the master microcontroller (MCU). When this terminal is in a logic [0] state, the device is capable of transferring information to, and receiving information from, the MCU. The 33892 latches in data from the Input Shift registers to the addressed registers on the rising edge of $\overline{CS}$. The 33892 transfers status information from the power output to the Shift register on the falling edge of $\overline{CS}$. The SO output driver is enabled when $\overline{CS}$ is logic [0]. $\overline{CS}$ should transition from a logic [1] to a logic [0] state only when SCLK is a logic [0]. $\overline{CS}$ has an internal pull-up, I_{UP}.



Notes 1. $\overline{RST}$ is a logic [1] state during the above operation.
2. D15–D0 relate to the most recent ordered entry of data into the device.
3. OD15–OD0 relate to the first 16 bits of ordered fault and status data out of the device.

Figure 7. Single 16-Bit Word SPI Communication

Serial Input Communication

SPI communication is accomplished using 16-bit messages. A message is transmitted by the MCU starting with the MSB D15 and ending with the LSB, D0 (Table 1). Each incoming command message on the SI terminal can be interpreted using the following bit assignments: the MSB, D15, is the watchdog bit. In some cases, output channel selection is done with bits D12–D11. The next three bits, D10–D8, are used to select the command register. The remaining five bits, D4–D0, are used to configure and control the outputs and their protection features.

Multiple messages can be transmitted in succession to accommodate those applications where daisy chaining is desirable, or to confirm transmitted data, as long as the messages are all multiples of 16 bits. Any attempt made to latch in a message that is not 16 bits will be ignored.

The 33892 has defined registers, which are used to configure the device and to control the state of the outputs. Table 2, page 19, summarizes the SI registers.

Table 1. SI Message Bit Assignment

Bit Sig	SI Msg Bit	Message Bit Description
MSB	D15	Watchdog in: toggled to satisfy watchdog requirements.
	D14–D15	Not used.
	D12–D11	Register address bits used in some cases for output channel selection.
	D10–D8	Register address bits.
	D7–D5	Not used.
	D4–D1	Used to configure the inputs, outputs, and the device protection features and SO status content.
LSB	D0	Used to configure the inputs, outputs, and the device protection features and SO status content.

Table 2. Serial Input Address and Configuration Bit Map

SI Register	SI Data															
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
STATR	WDIN	x	x	x	x	0	0	0	x	x	x	SOA4	SOA3	SOA2	SOA1	SOA0
OCR0	WDIN	x	x	x	0	0	0	1	x	x	x	x	IN_SPI3	IN_SPI2	IN_SPI1	IN_SPI0
OCR1	WDIN	x	x	x	1	0	0	1	x	x	x	x	CSNS $\overline{EN}$3	CSNS $\overline{EN}$2	CSNS $\overline{EN}$1	CSNS $\overline{EN}$0
SOCHLR_s	WDIN	x	x	A_1	A_0	0	1	0	x	x	x	x	SOCH_s	SOCL2_s	SOCL1_s	SOCL0_s
CDTOLR_s	WDIN	x	x	A_1	A_0	0	1	1	x	x	x	x	OL_DIS_s	OCL_DIS_s	OCLT1_s	OCLT0_s
DICR_s	WDIN	x	x	A_1	A_0	1	0	0	x	x	x	x	FAST_SR_s	CSNS_high_s	DIR_DIS_s	A/O_s
UOVR	WDIN	x	x	x	0	1	0	1	x	x	x	x	x	x	UV_DIS	OV_DIS
WDR	WDIN	x	x	x	1	1	0	1	x	x	x	x	x	x	WD1	WD0
NAR	WDIN	x	x	x	x	1	1	0	x	x	x	x	No Action (Allow Toggling of D15–WDIN)			
TEST	WDIN	x	x	x	x	1	1	1	x	x	x	x	Motorola Internal Use (Test)			

x=Don't care.
s=Output selection with the bits A_1A_0 as defined in Table 3.

Device Register Addressing

The following section describes the possible register addresses and their impact on device operation.

Address xx000—Status Register (STATR)

The STATR register is used to read the device status and the various configuration register contents without disrupting the device operation or the register contents. The register bits D[4:0] determine the content of the first sixteen bits of SO data. In addition to the device status, this feature provides the ability to read the content of the OCR0, OCR1, SOCHLR, CDTOLR, DICR, UOVR, WDR, and NAR registers. (Refer to the section entitled Serial Output Communication (Device Status Return Data) beginning on page 21.)

Address x0001—Output Control Register (OCR0)

The OCR0 register allows the MCU to control the ON/OFF state of four outputs through the SPI. Incoming message bit D[3:0] reflects the desired states of the four high-side outputs (IN_SPI), respectively. A logic [1] enables the corresponding output switch and a logic [0] turns it OFF.

Address x1001—Output Control Register (OCR1)

Incoming message bit D[3:0] reflects the desired channel that will be mirrored on the Current Sense (CSNS) terminal. A logic [1] on message bit D[3:0] enables the CSNS terminal for the outputs HS3–HS0, respectively. In the event that the current sense is enabled for multiple outputs, the current will be summed. In the event that all bits D[3:0] are logic [0], the output CSNS will then tri-stated. This is useful when several CSNS terminals of several devices share the same A/D converter.

Address $A_1A_0$010—Select Overcurrent High and Low Register (SOCHLR_s)

The SOCHLR_s register allows the MCU to configure the output overcurrent low and high detection levels, respectively. Each output "s" is independently selected for configuration based on the state of the D12–D11 bits (Table 3).

Table 3. Channel Selection

A_1 (D12)	A_0 (D11)	HS_s
0	0	HS0
0	1	HS1
1	0	HS2
1	1	HS3

Each output can be configured to different levels. In addition to protecting the device, this slow blow fuse emulation feature can be used to optimize the load requirements matching system characteristics. Bits D2–D0 set the overcurrent low detection level to one of eight possible levels, as shown in Table 4, page 20. Bit D3 sets the overcurrent high detection level to one of two levels, as outlined in Table 5, page 20.

Table 4. Overcurrent Low Detection Levels

SOCL2_s* (D2)	SOCL1_s* (D1)	SOCL0_s* (D0)	Overcurrent Low Detection (Amperes)	
			HS0 or HS1	HS2 or HS3
0	0	0	18.2	9.1
0	0	1	16.3	8.15
0	1	0	14.4	7.2
0	1	1	12.5	6.25
1	0	0	10.5	5.25
1	0	1	8.6	4.3
1	1	0	6.7	3.35
1	1	1	4.8	2.4

* "_s" refers to the channel, which is selected through bits D12–D11; refer to Table 3, page 19.

Table 5. Overcurrent High Detection Levels

SOCH_s* (D3)	Overcurrent High Detection (Amperes)	
	HS0 or HS1	HS2 or HS3
0	100	50
1	70	35

* "_s" refers to the channel, which is selected through bits D12–D11; refer to Table 3, page 19.

Address $A_1A_0$011—Current Detection Time and Open Load Register (CDTOLR)

The CDTOLR register is used by the MCU to determine the amount of time the 33892 will allow an overcurrent low condition before an output latches OFF. Each output is independently selected for configuration based on A_1A_0, which are the state of the D12–D11 bits (refer to Table 3, page 19).

Bits D1–D0 (OCLT[1:0]_s) allow the MCU to select one of four overcurrent fault blanking times defined in Table 6. Note that these timeouts apply only to the overcurrent low detection levels. If the selected overcurrent high level is reached, the device will latch off within 20 μs.

Table 6. Overcurrent Low Detection Blanking Time

OCLT[1:0]_s*	Timing
00	155 ms
01	620 ms
10	75 ms
11	150 μs

* "_s" refers to the channel, which is selected through bits D12–D11; refer to Table 3, page 19.

A logic [1] on bit D2 (OCL_DIS_s) disables the overcurrent low detection feature. When disabled, there is no timeout for the selected output and the overcurrent low detection feature is disabled.

A logic [1] on bit D3 (OL_DIS_s) disables the open load (OL) detection feature for the channel corresponding to the state of bits D12–D11.

Address $A_1A_0$100—Direct Input Control Register (DICR)

The DICR register is used by the MCU to enable, disable, or configure the direct IN terminal control of each output. Each output is independently selected for configuration based on the state bits D12–D11 (refer to Table 3, page 19).

For the selected output, a logic [0] on bit D1 (DIR_DIS_s) will enable the output for direct control. A logic [1] on bit D1 will disable the output from direct control.

While addressing this register, if the Input was enabled for direct control, a logic [1] for the D0 (A/O_s) bit will result in a Boolean AND of the IN terminal with its corresponding IN_SPI D[4:0] message bit when addressing OCR0. Similarly, a logic [0] on the D0 terminal results in a Boolean OR of the IN terminal to the corresponding message bits when addressing the OCR0. This register is especially useful if several loads are required to be independently PWM controlled. For example, the IN terminals of several devices can be configured to operate all of the outputs with one PWM output from the MCU. If each output is then configured to be Boolean ANDed to its respective IN terminal, each output can be individually turned OFF by SPI while controlling all of the outputs, commanded on with the single PWM output.

A logic [1] on bit D2 (CSNS_high_s) is used to select the high ratio on the CSNS terminal for the selected output. The default value [0] is used to select the low ratio (Table 7).

Table 7. Current Sense Ratio

CSNS_high_s* (D2)	Current Sense Ratio	
	HS0 or HS1	HS2 or HS3
0	1/13000	1/6500
1	1/40000	1/20000

* "_s" refers to the channel, which is selected through bits D12–D11; refer to Table 3, page 19.

A logic [1] on bit D3 (FAST_SR_s) is used to select the high speed slew rate for the selected output, the default value [0] corresponds to the low speed slew rate

Address x0101—Undervoltage/Overvoltage Register (UOVR)

The UOVR register disables the undervoltage (D1) and/or overvoltage (D0) protection. When these two bits are [0], the under- and overvoltage are active (default value).

Address x1101— Watchdog Register (WDR)

The WDR register is used by the MCU to configure the Watchdog timeout. The Watchdog timeout is configured using bits D1 and D0. When D1 and D0 bits are programmed for the desired watchdog timeout period (Table 8), the WDSPI bit should be toggled as well, ensuring the new timeout period is programmed at the beginning of a new count sequence.

Table 8. Watchdog Timeout

WD[1:0] (D1, D0)	Timing (ms)
00	620
01	310
10	2500
11	1250

Address xx110—No Action Register (NAR)

The NAR register can be used to no-operation fill SPI data packets in a daisy-chain SPI configuration. This would allow devices to be unaffected by commands being clocked over a daisy-chained SPI configuration. By toggling the WD bit (D15) the watchdog circuitry would continue to be reset while no programming or data read back functions are being requested from the device.

Address xx111—TEST

The TEST register is reserved for test and is not accessible with SPI during normal operation.

Serial Output Communication (Device Status Return Data)

When the $\overline{CS}$ terminal is pulled low, the output register is loaded. Meanwhile, the data is clocked out MSB- (OD15-) first as the new message data is clocked into the SI terminal. The first sixteen bits of data clocking out of the SO, and following a $\overline{CS}$ transition, is dependent upon the previously written SPI word.

Any bits clocked out of the Serial Output (SO) terminal after the first 16 bits will be representative of the initial message bits clocked into the SI terminal since the $\overline{CS}$ terminal first transitioned to a logic [0]. This feature is useful for daisy chaining devices as well as message verification.

A valid message length is determined following a $\overline{CS}$ transition of [0] to [1]. If there is a valid message length, the data is latched into the appropriate registers. A valid message length is a multiple of 16 bits. At this time, the SO terminal is tri-stated and the fault status register is now able to accept new fault status information.

SO data will represent information ranging from fault status to register contents, user selected by writing to the STATR bits OD4, OD3, OD2, OD1, and OD0. The value of the previous bits SOA4 and SOA3 will determine which output the SO information applies to for the registers which are output specific; viz., Fault, SOCHLR, CDTOLR, and DICR registers.

Note that the SO data will continue to reflect the information for each output (depending on the previous OD4, OD3 state) that was selected during the most recent STATR write until changed with an updated STATR write.

The output status register correctly reflects the status of the STATR-selected register data at the time that the $\overline{CS}$ is pulled to a logic [0] during SPI communication, and/or for the period of time since the last valid SPI communication, with the following exceptions:

- The previous SPI communication was determined to be invalid. In this case, the status will be reported as though the invalid SPI communication never occurred.
- Battery transients below 6.0 V resulting in an under-voltage shutdown of the outputs may result in incorrect data loaded into the status register. The SO data transmitted to the MCU during the first SPI communication following an undervoltage V_{PWR} condition should be ignored.
- The $\overline{RST}$ terminal transition from a logic [0] to [1] while the WAKE terminal is at logic [0] may result in incorrect data loaded into the Status register. The SO data transmitted to the MCU during the first SPI communication following this condition should be ignored.

Serial Output Bit Assignment

The 16 bits of serial output data depend on the previous serial input message, as explained in the following paragraphs. Table 9, page 22, summarizes SO returned data for bits OD15 through OD0.

- Bit OD15 is the MSB; it reflects the state of the Watchdog bit from the previously clocked-in message.
- Bit OD14 remains logic [0] except when an undervoltage condition occurred.
- Bit OD13 remains logic [0] except when an overvoltage condition occurred.
- Bits OD[12:8] reflect the state of the bits SOA[4:0] from the previously clocked in message.
- Bits OD[7:4] give the fault status flag of the outputs HS3, HS2, HS1, and HS0, respectively.
- The contents of bits OD[3:0] depend on bits D[4:0] from the most recent STATR command SOA[4:0] as explained in the paragraphs following the table.

Table 9. Serial Output Bit Map Description

Previous STATR					SO Returned Data														
SOA4	SOA3	SOA2	SOA1	SOA0	OD15	OD14	OD13	OD12	OD11	OD10	OD9	OD8	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
A_1	A_0	0	0	0	WDIN	UVF	OVF	SOA4	SOA3	SOA2	SOA1	SOA0	ST3	ST2	ST1	ST0	OTF_s	OCHF_s	OCLF_s	OLF_s
x	0	0	0	1	WDIN	UVF	OVF	SOA4	SOA3	SOA2	SOA1	SOA0	ST3	ST2	ST1	ST0	IN_SPI3	IN_SPI2	IN_SPI1	IN_SPI0
x	1	0	0	1	WDIN	UVF	OVF	SOA4	SOA3	SOA2	SOA1	SOA0	ST3	ST2	ST1	ST0	CSNS $\overline{EN}$3	CSNS $\overline{EN}$2	CSNS $\overline{EN}$1	CSNS $\overline{EN}$0
A_1	A_0	0	1	0	WDIN	UVF	OVF	SOA4	SOA3	SOA2	SOA1	SOA0	ST3	ST2	ST1	ST0	SOCH_s	SOCL2_s	SOCL1_s	SOCL0_s
A_1	A_0	0	1	1	WDIN	UVF	OVF	SOA4	SOA3	SOA2	SOA1	SOA0	ST3	ST2	ST1	ST0	OL_DIS_s	OCL_DIS_s	OCLT1_s	OCLT0_s
A_1	A_0	1	0	0	WDIN	UVF	OVF	SOA4	SOA3	SOA2	SOA1	SOA0	ST3	ST2	ST1	ST0	Fast_SR_s	CSNS_high_s	DIR_DIS_s	A/O_s
x	0	1	0	1	WDIN	UVF	OVF	SOA4	SOA3	SOA2	SOA1	SOA0	ST3	ST2	ST1	ST0	–	–	UV_DIS	OV_DIS
x	1	1	0	1	WDIN	UVF	OVF	SOA4	SOA3	SOA2	SOA1	SOA0	ST3	ST2	ST1	ST0	–	WDTO	WD1	WD0
x	0	1	1	0	WDIN	UVF	OVF	SOA4	SOA3	SOA2	SOA1	SOA0	ST3	ST2	ST1	ST0	HS2_failsaf	HS0_failsaf	WD_en	WAKE
x	1	1	1	0	WDIN	UVF	OVF	SOA4	SOA3	SOA2	SOA1	SOA0	ST3	ST2	ST1	ST0	IN3	IN2	IN1	IN0

x=Don't care.
s=Output selection with the bits A_1A_0 as defined in Table 3, page 19.

Previous Address SOA[4:0]=$A_1A_0$000

The bits OD[3:0] will reflect the current state of the Fault Register (FLTR) corresponding to the output previously selected with the bits A_1A_0 (Table 10).

Table 10. Channel-Specific Fault Register

OD3	OD2	OD1	OD0
OTF_s	OCHF_s	OCLF_s	OLF_s

s=Selection of the output.

Note The $\overline{FS}$ terminal reports all faults. For latched faults, this terminal is reset by a new Switch ON command (via SPI or direct input IN).

Previous Address SOA[4:0]=x0001

Data in bits OD[3:0] contains IN_SPI[3:0]-programmed bits for channel from HS3 to HS0, respectively.

Previous Address SOA[4:0]=x1001

Data in bits OD[3:0] contains the programmed CSNS $\overline{EN}$[3:0] bits for channels HS3 to HS0, respectively.

Previous Address SOA[4:0]=$A_1A_0$010

Data returned in bits OD[3:0] are programmed current values for the overcurrent high detection level (refer to Table 5, page 20) and the overcurrent low detection level (refer to Table 4, page 20), corresponding to the output previously selected with A_1A_0.

Previous Address SOA[4:0]=$A_1A_0$011

The returned data contains the programmed values in the CDTOLR register for the output selected with A_1A_0.

Previous Address SOA[4:0]=$A_1A_0$100

The returned data contains the programmed values in the DICR register for the output selected with A_1A_0.

Previous Address SOA[4:0]=$A_1A_0$101

The returned data contains the programmed values in the UOVR register.

Previous Address SOA[4:0]=x1101

The returned data contains the programmed values in the WDR register. Bit OD2 (WDTO) reflects the status of the watchdog circuitry. If WDTO bit is [1], the watchdog has timed out and the 33892 is in Fail-Safe mode. IF WDTO is [0], the device is in Normal mode (assuming the device is powered and not in the Sleep mode), with the watchdog either enabled or disabled.

Previous Address SOA[4:0]=x0110

The returned data OD3 and OD2 contain the state of the outputs HS2 and HS0, respectively, in case of Fail-Safe state. This information is stated with the external resistance placed at the FSI terminal. OD1 indicates if the watchdog is enabled or not. OD0 returns the state of the WAKE terminal.

Previous Address SOA[4:0]=x1110

The returned data OD[3:0] reflects the state of the direct terminals IN3 to IN0, respectively.

MODES OF OPERATION

The 33892 has four operating modes. They are Sleep, Normal, Fault, and Fail-Safe. Table 11 summarizes details contained in succeeding paragraphs.

Table 11. Fail-Safe Operation and Transitions to Other 33892 Modes

Mode	$\overline{FS}$	Wake	$\overline{RST}$	WDTO	Comments
Sleep	x	0	0	x	Device is in Sleep mode. All outputs are OFF
Normal	1	x	1	No	Normal mode. Watchdog is active if enabled.
Fault	0	1	1	No	Device is currently in fault mode. The faulted output(s) is (are) OFF.
	0	1	0		
	0	x	1		
Fail-Safe	1	0	1	Yes	Watchdog has timed out and the device is in Fail-Safe Mode. The outputs are as configured with the RFS resistor connected to FSI. $\overline{RST}$ and WAKE must be transitioned to logic [0] simultaneously to bring the device out of the Fail-safe mode or momentarily tied the FSI pin to ground.
	1	1	1		
	1	1	0		

x = Don't care.

Sleep Mode

The Default mode of the 33892 is the Sleep mode. This is the state of the device after first applying battery voltage (V_{PWR}) prior to any I/O transitions. This is also the state of the device when the WAKE and $\overline{RST}$ are both logic [0]. In the Sleep mode, the output and all unused internal circuitry, such as the internal 5.0 V regulator, are off to minimize current draw. In addition, all SPI-configurable features of the device are as if set to logic [0]. The device will transition to the Normal or Fail-Safe operating modes based on the WAKE and $\overline{RST}$ inputs as defined in Table 11.

Normal Mode

The 33892 is in Normal mode when:

- V_{PWR} is within the normal voltage range.
- $\overline{RST}$ terminal is logic [1].
- No fault has occurred.

Fail-Safe Mode

Fail-Safe Mode and Watchdog

If the FSI input is not grounded, the watchdog timeout detection is active when either the WAKE or $\overline{RST}$ input terminal transitions from logic [0] to [1]. The WAKE input is capable of being pulled up to V_{PWR} with a series of limiting resistance limiting the internal clamp current according to the specification.

The Watchdog timeout is a multiple of an internal oscillator and is specified in the Table 8, page 21. As long as the WD bit (D15) of an incoming SPI message is toggled within the minimum watchdog timeout period (WDTO), based on the programmed value of the WDR, the device will operate normally. If an internal watchdog timeout occurs before the WD bit, the device will revert to a Fail-Safe mode until the device is reinitialized.

During the Fail-Safe mode, the outputs will be ON or OFF depending upon the resistor RFS connected to the FSI pin, regardless of the state of the various direct inputs and modes (Table 12).

Table 12. Output State During Fail-Safe Mode

RFS (kΩ)	High-Side State
0	Fail-Safe Mode Disabled
6.0	All HS OFF
15	HS0 ON HS[1:3] OFF
30	HS0 and HS2 ON HS1 and HS3 OFF

In the Fail-Safe mode, the SPI register content is retained except for overcurrent high and low detection levels and timing, which are reset to their default value (SOCL, SOCH, and OCTL). Then the watchdog, overvoltage, overtemperature, and overcurrent circuitry (with default value) are fully operational.

The Fail-Safe mode can be detected by monitoring the WDTO bit D2 of the WD register. This bit is logic [1] when the device is in Fail-Safe mode. The device can be brought out of the Fail-Safe mode by transitioning the WAKE and $\overline{RST}$ pins from logic [1] to logic [0] or forcing the FSI pin to logic [0]. Table 11 summarizes the various methods for resetting the device from the latched Fail-Safe mode.

If the FSI pin is tied to GND, the Watchdog Fail-Safe operation is disabled.

Loss of V_{DD}

If the external 5.0 V supply is not within specification, or even disconnected, all register content is reset. The outputs can still be driven by the direct inputs IN[0:3]. The 33892 uses the battery input to power the output MOSFET-related current sense circuitry and any other internal logic providing fail-safe device operation with no V_{DD} supplied. In this state, the watchdog, overvoltage, overtemperature, and overcurrent circuitry are fully operational with default values.

Fault Mode

The 33892 indicates the faults below as they occur by driving the $\overline{FS}$ terminal to [0]:

- Overtemperature fault
- Overvoltage and Undervoltage fault
- Open load fault
- Overcurrent fault (high and low)

The $\overline{FS}$ terminal will automatically return to [1] when the fault condition is removed, except for overcurrent and in some cases undervoltage.

Fault information is retained in the fault register and is available (and reset) via the SO terminal during the first valid SPI communication (refer to Table 10, page 22).

Overtemperature Fault (Non-Latching)

The 33892 incorporates overtemperature detection and shutdown circuitry in the output structure. Overtemperature detection is enabled when the output is in the ON state.

For the output, an overtemperature fault (OTF) condition results in the faulted output turning OFF until the temperature falls below the $T_{SD(HYS)}$. This cycle will continue indefinitely until action is taken by the MCU to shut OFF the output, or until the offending load is removed.

When experiencing this fault, the OTF fault bit will be set in the status register and cleared after either a valid SPI read or a power reset of the device.

Overvoltage Fault (Non-Latching)

The 33892 shuts down the output during an overvoltage fault (OVF) condition on the V_{PWR} terminal. The output remains in the OFF state until the overvoltage condition is removed. When experiencing this fault, the OVF fault bit is set in the bit D1 and cleared after either a valid SPI read or a power reset of the device.

The overvoltage protection can be disabled through SPI (bit OV_DIS). When disabled, the returned SO bit OD13 still reflects any overvoltage condition (overvoltage warning).

Undervoltage Shutdown (Latching or Non-Latching)

The output latches OFF at some battery voltage between 4.75 V and 5.75 V. As long as the V_{DD} level stays within the normal specified range, the internal logic states within the device will be sustained. This ensures that when the battery level then returns above 5.75 V, the 33892 can be returned to the state that it was in prior to the low V_{PWR} excursion. Once the output latches OFF, the outputs must be turned OFF and ON again to re-enable them. In the case IN[1:0]=0, this fault is non-latched.

The undervoltage protection can be disabled through SPI (bit UV_DIS). When disabled, the returned SO bit OD14 still reflects any undervoltage condition (undervoltage warning).

Open Load Fault (Non-Latching)

The 33892 incorporates open load detection circuitry on the output. Output open load fault (OLF) is detected and reported as a fault condition when the output is disabled (OFF). The open load fault is detected and latched into the status register after the internal gate voltage is pulled low enough to turn OFF the output. The OLF fault bit is set in the status register. If the open load fault is removed, the status register will be cleared after reading the register.

The open load protection can be disabled trough SPI (bit OL_DIS).

Overcurrent Fault (Latching)

The 33892 has eight programmable overcurrent low detection levels (I_{OCL}) and two programmable overcurrent high detection levels (I_{OCH}) for maximum device protection. The two selectable, simultaneously active overcurrent detection levels, defined by I_{OCH} and I_{OCL}, are illustrated in Figure 4, page 15. The eight different overcurrent low detection levels (I_{OCL0}, I_{OCL1}, I_{OCL2}, I_{OCL3}, I_{OCL4}, I_{OCL5}, I_{OCL6}, and I_{OCL7}) are illustrated in Figure 4.

If the load current level ever reaches the selected overcurrent low detection level and the overcurrent condition exceeds the programmed overcurrent time period (t_{OCx}), the device will latch the output OFF.

If, at any time, the current reaches the selected I_{OCH} level, then the device will immediately latch the fault and turn OFF the output, regardless of the selected t_{OCLx} driver.

For both cases, the device output will stay off indefinitely until the device is commanded OFF and then ON again.

Reverse Battery

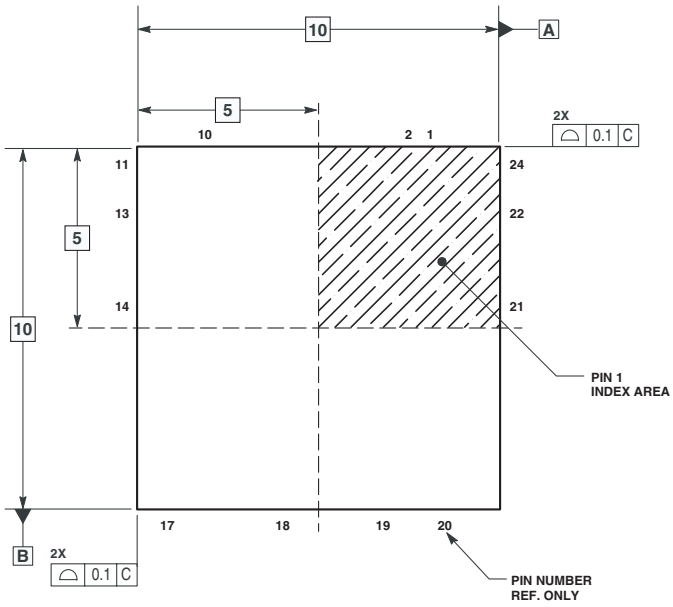
The output survives the application of reverse voltage as low as -16 V. Under these conditions, the output's gate is enhanced to keep the junction temperature less than 150°C. The ON resistance of the output is fairly similar to that in the Normal mode. No additional passive components are required.

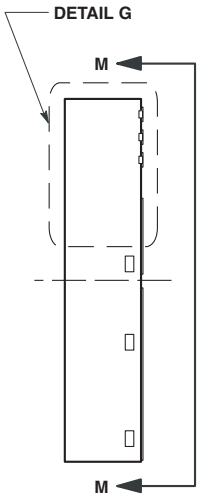
Ground Disconnect Protection

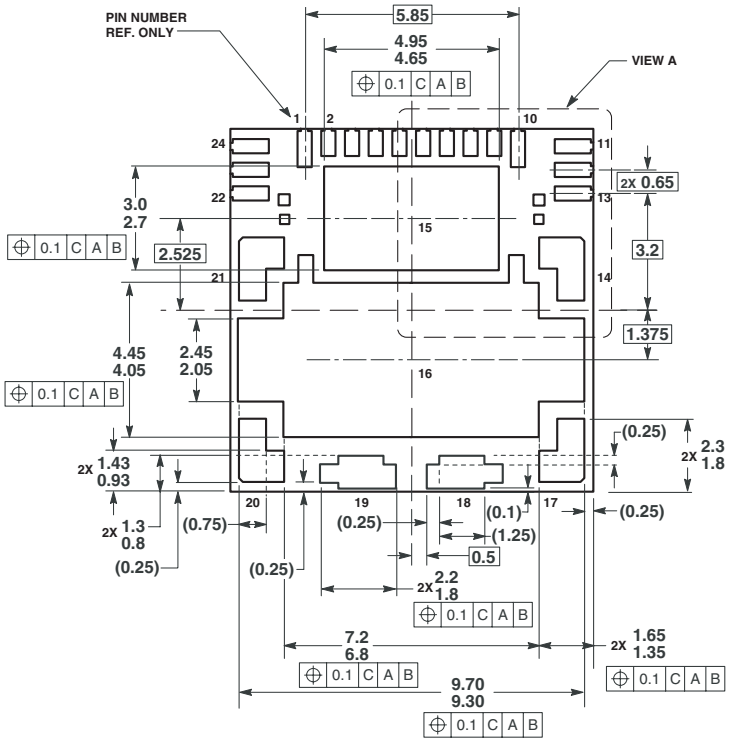
In the event the 33892 ground is disconnected from load ground, the device protects itself and safely turns OFF the output regardless of the state of the output at the time of disconnection.

PACKAGE DIMENSIONS

PNC SUFFIX
24-TERMINAL POWER QFN
NON-LEADED PACKAGE
CASE 1558-02
ISSUE A
SHEET 1 OF 2



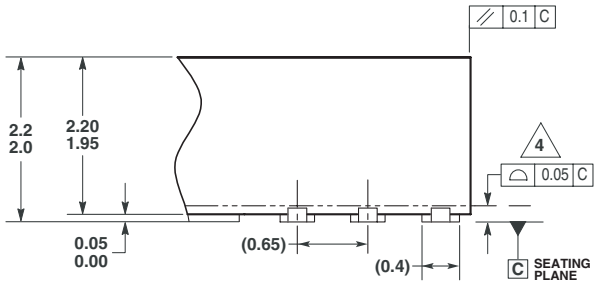




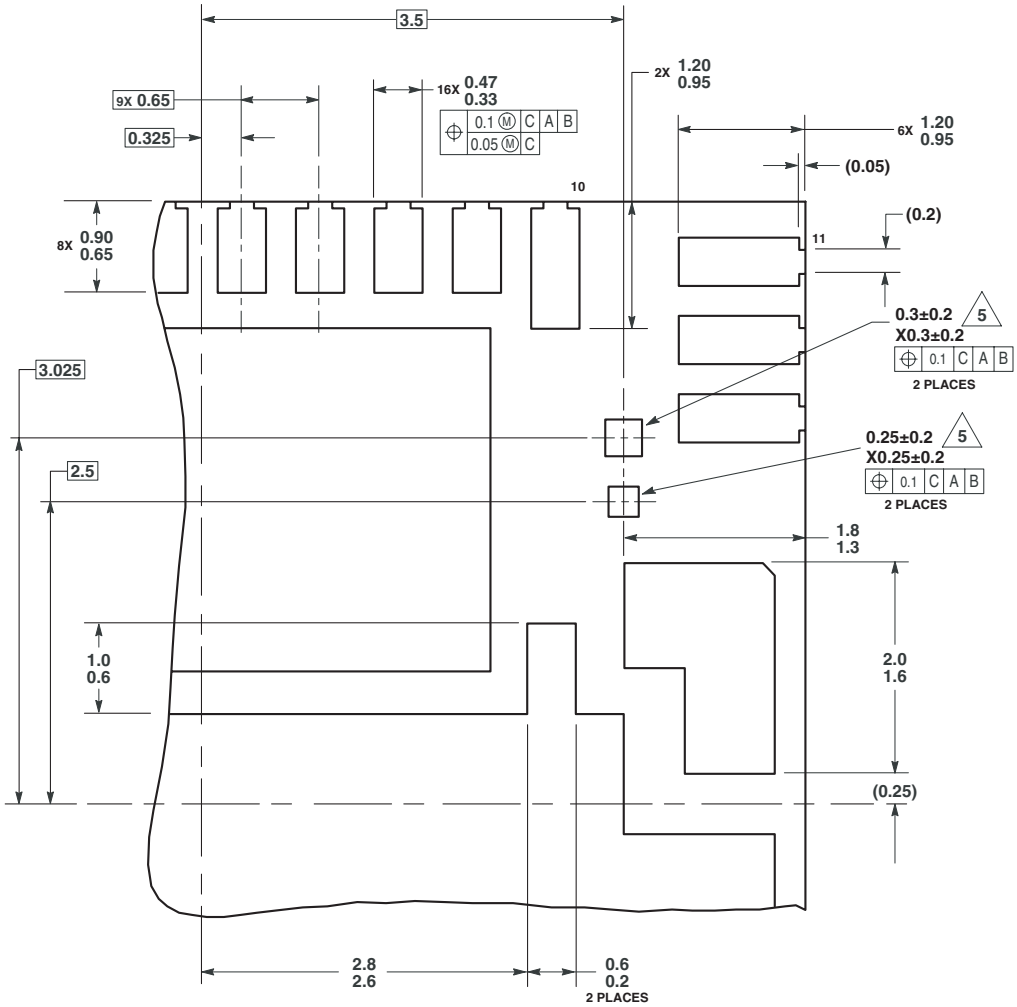
VIEW M–M

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFP-N.
4. COPLANARITY APPLIES TO LEADS AND CORNER LEADS.
5. METAL PADS CONNECTED TO THE GND.
6. MINIMUM METAL GAP SHOULD BE 0.25MM.

PNC SUFFIX
24-TERMINAL POWER QFN
NON-LEADED PACKAGE
CASE 1558-02
ISSUE A
SHEET 2 OF 2



DETAIL G
VIEW ROTATED 90° CW



VIEW A

NOTES

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