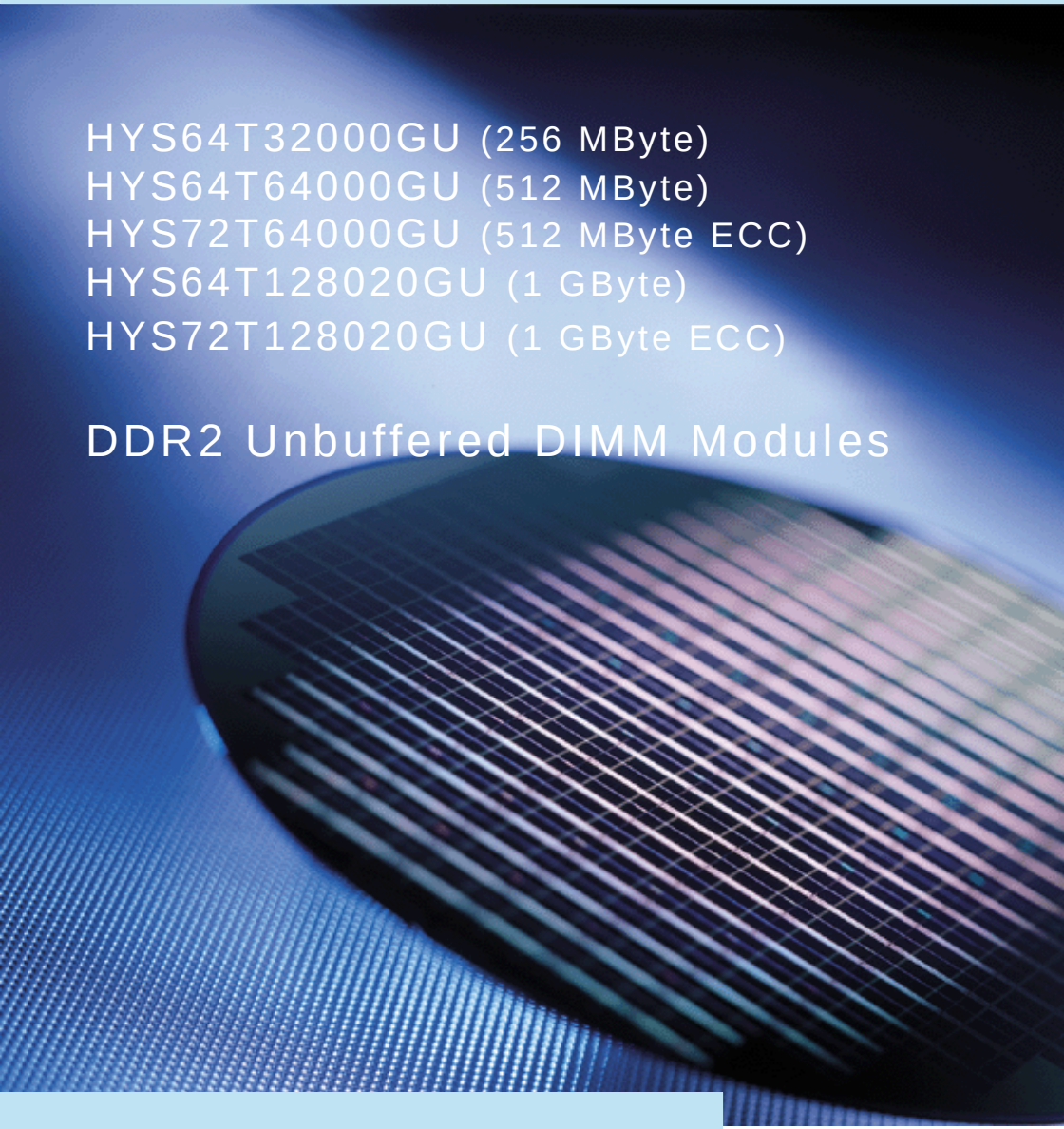
Data Sheet, V0.84, Jan. 2004

HYS64T32000GU (256 MByte)
HYS64T64000GU (512 MByte)
HYS72T64000GU (512 MByte ECC)
HYS64T128020GU (1 GByte)
HYS72T128020GU (1 GByte ECC)

DDR2 Unbuffered DIMM Modules



Memory Products

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1.8 V 240-pin Unbuffered DDR2 SDRAM Modules

256 MByte, 512 MByte & 1 GByte ECC and non-ECC Modules
PC2-3200U /-4300U /-5400U

- 240-pin ECC and Non-ECC Unbuffered 8-Byte Dual-In-Line DDR2 SDRAM Module for PC, Workstation and Server main memory applications
- One rank 32M x 64, 32M x 72, 64M x 64, 64M x 72 and two ranks 128M × 64 and 128M x 72 organization
- JEDEC standard Double Data Rate 2 Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- Built with 512Mb DDR2 SDRAMs in 60-ball / 84-ball FBGA chipsize packages
- Programmable $\overline{\text{CAS}}$ Latencies (3, 4 & 5), Burst Length (8 & 4) and Burst Type
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_1.8 compatible
- OCD (Off-Chip Driver Impedance Adjustment) and ODT (On-Die Termination)
- Serial Presence Detect with E^2PROM
- Low Profile Modules form factor: 133.35 mm x 30,00 mm (MO-237)
- Based on JEDEC standard reference card layouts Raw Card “A”, “B” & “C”

- Performance:

Speed Grade Indicator	-5	-3.7	-3	Unit
Component Speed Grade	DDR2-400	DDR2-533	DDR2-667	
Module Speed Grade	PC2-3200	PC2-4300	PC2-5400	
Max. Clock Frequency @ CL = 3	200	200	200	MHz
Max. Clock Frequency @ CL = 4 & 5	200	266	333	MHz

1.0 Introduction

The INFINEON HYS64/72Txxxx0GU module family are low profile Unbuffered DIMM modules with 30,0 mm height based on DDR2 technology. DIMMs are available as non-ECC modules in 32M x 64 (256MB), 64M x 64 (512MB) and 128M x 64 (1024MB) and as ECC-modules in 32M x 72 (256MB), 64M x 72 (512MB) and 128M x 72 (1024MB) organisation and density, intended for mounting into 240 pin connector sockets.

The memory array is designed with 512Mb Double Data Rate (DDR2) Synchronous DRAMs for ECC and Non-ECC applications. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

1.1 Ordering Information

Type & Partnumber	Compliance Code	Description	ECC/ Non-ECC	SDRAM Technology
PC2-3200:				
HYS64T32000GU-5-A	PC2-3200U-33310-C	one rank 256 MB Unb. DIMM	Non-ECC	512 Mbit (x16)
HYS64T64000GU-5-A	PC2-3200U-33310-A	one rank 512 MB Unb.DIMM	Non-ECC	512 Mbit (x8)
HYS72T64000GU-5-A	PC2-3200U-33310-A	one rank 512 MB Unb.DIMM	ECC	512 Mbit (x8)
HYS64T128020GU-5-A	PC2-3200U-33310-B	two ranks 1 GB Unb. DIMM	Non-ECC	512 Mbit (x8)
HYS72T128020GU-5-A	PC2-3200U-33310-B	two ranks 1 GB Unb. DIMM	ECC	512 Mbit (x8)
PC2-4300:				
HYS64T32000GU-3.7-A	PC2-4300U-44410-C	one rank 256 MB Unb. DIMM	Non-ECC	512 Mbit (x16)
HYS64T64000GU-3.7-A	PC2-4300U-44410-A	one rank 512 MB Unb.DIMM	Non-ECC	512 Mbit (x8)
HYS72T64000GU-3.7-A	PC2-4300U-44410-A	one rank 512 MB Unb.DIMM	ECC	512 Mbit (x8)
HYS64T128020GU-3.7-A	PC2-4300U-44410-B	two ranks 1 GB Unb. DIMM	Non-ECC	512 Mbit (x8)
HYS72T128020GU-3.7-A	PC2-4300U-44410-B	two ranks 1 GB Unb. DIMM	ECC	512 Mbit (x8)
PC2-5400:				
HYS64T32000GU-3-A	PC2-5400U-44410-C	one rank 256 MB Unb. DIMM	Non-ECC	512 Mbit (x16)
HYS64T64000GU-3-A	PC2-5400U-44410-A	one rank 512 MB Unb.DIMM	Non-ECC	512 Mbit (x8)
HYS72T64000GU-3-A	PC2-5400U-44410-A	one rank 512 MB Unb.DIMM	ECC	512 Mbit (x8)
HYS64T128020GU-3-A	PC2-5400U-44410-B	two ranks 1 GB Unb. DIMM	Non-ECC	512 Mbit (x8)
HYS72T128020GU-3-A	PC2-5400U-44410-B	two ranks 1 GB Unb. DIMM	ECC	512 Mbit (x8)

Notes:

1. All part numbers end with a place code, designating the silicon die revision. Example: HYS 72T64000GU-5-A, indicating Rev. A dies are used for DDR2 SDRAM components. For all INFINEON DDR2 module and component nomenclature see section 8 of this datasheet.
2. The Compliance Code is printed on the module label and describes the speed grade, f.e. “PC2-4300U-44410-C”, where 4300U means Unbuffered DIMM modules with 4.26 GB/sec Module Bandwidth and “44410” means $\overline{\text{CAS}}$ latency = 4, trcd latency = 4 and trp latency = 4 using the latest JEDEC SPD Revision 1.0 and produced on the Raw Card “C”.

1.2 Address Format

Part Number	DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/ columns bits	Raw Card
HYS64T32000GU	256 MB	32M x 64	1	Non-ECC	4	13/2/10	C
HYS64T64000GU	512 MB	64M × 64	1	Non-ECC	8	14/2/10	A
HYS72T64000GU	512 MB	64M × 72	1	ECC	9	14/2/10	A
HYS64T128020GU	1024 MB	2 x 64M × 64	2	Non-ECC	16	14/2/10	B
HYS72T128020GU	1024 MB	2 x 64M × 72	2	ECC	18	14/2/10	B

1.3 Components on Modules and RawCard

DIMM Density	DRAM components reference datasheet	DRAM Density	DRAM Organisation	Raw Card
256 MB	HYB18T512160AC	512 Mbit	32Mb x 16	C
512 MB	HYB18T512800AC	512 Mbit	64Mb x 8	A
1024 MB	HYB18T512800AC	512 Mbit	64Mb x 8	B
For a detailed description of all functionalities of the DRAM components on these modules see the referenced component datasheet				

1.4 Pin Definition and Function

Pin Name	Description	Pin Name	Description
A[13:0]	Row Address Inputs [4]	CB[7:0]	DIMM ECC Check Bits [2]
A[9:0]	Column Address Inputs	DQS[8:0]	SDRAM data strobes [2] (positive line of differential pair)
A10/AP	Column Address Input for Auto-Precharge	$\overline{\text{DQS}}$[8:0]	SDRAM data strobes [2] (negative line of differential pair)
BA[1:0]	SDRAM Bank Selects	DM[8:0]	SDRAM data mask [2]
CK[2:0]	Clock input (positive line of differential pair)	SCL	Serial bus clock
$\overline{\text{CK}}$[2:0]	Clock input (negative line of differential pair)	SDA	Serial bus data line
$\overline{\text{RAS}}$	Row Address Strobe	SA[2:0]	slave address select
$\overline{\text{CAS}}$	Column Address Strobe	V_{DD}	Power (+ 1.8 V)
$\overline{\text{WE}}$	Read/Write Input	V_{REF}	I/O reference supply
$\overline{\text{CS}}$[1:0]	Chip Select [3]	V_{SS}	Ground
CKE[1:0]	Clock Enable [3]	V_{DDSPD}	EEPROM power supply
ODT[1:0]	Active termination control lines [1] [3]	NC	no connect
DQ[63:0]	Data Input/Output		

1) Active termination only applies to DQ, DQS, $\overline{\text{DQS}}$ and DM signals
2) CB[7:0], DQS8, $\overline{\text{DQS8}}$ and DM8 are used on ECC modules only and are not connected to components on Non-ECC modules
3) $\overline{\text{CS1}}$, ODT1 and CKE1 are used on dual rank modules only
4) A13 is not used on memory modules based on x16 organised memory components

1.5 Pin Configuration

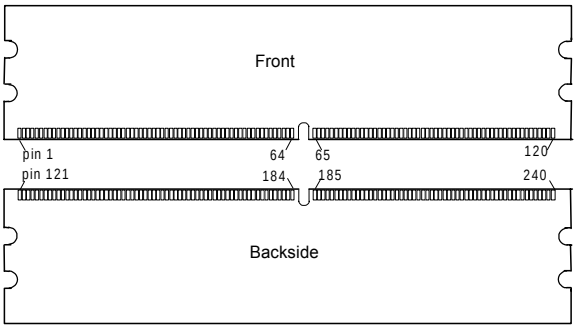
PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
1	VREF	121	VSS	61	A4	181	VDDQ
2	VSS	122	DQ4	62	VDDQ	182	A3
3	DQ0	123	DQ5	63	A2	183	A1
4	DQ1	124	VSS	64	VDD	184	VDD
5	VSS	125	DM0	KEY		KEY	
6	$\overline{\text{DQS0}}$	126	$\overline{\text{DQS9}}$	65	VSS	185	$\overline{\text{CK0}}$
7	DQS0	127	VSS	66	VSS	186	CK0
8	VSS	128	DQ6	67	VDD	187	VDD
9	DQ2	129	DQ7	68	NC	188	A0
10	DQ3	130	VSS	69	VDD	189	VDD
11	VSS	131	DQ12	70	A10/AP	190	BA1
12	DQ8	132	DQ13	71	BA0	191	VDDQ
13	DQ9	133	VSS	72	VDDQ	192	$\overline{\text{RAS}}$
14	VSS	134	DM1	73	$\overline{\text{WE}}$	193	$\overline{\text{CS0}}$
15	$\overline{\text{DQS1}}$	135	NC	74	$\overline{\text{CAS}}$	194	VDDQ
16	DQS1	136	VSS	75	VDDQ	195	ODT0
17	VSS	137	CK1	76	$\overline{\text{CS1}}$	196	A13 / NC [3]
18	NC	138	$\overline{\text{CK1}}$	77	ODT1	197	VDD
19	NC	139	$\overline{\text{VSS}}$	78	VDDQ	198	VSS
20	VSS	140	DQ14	79	VSS	199	DQ36
21	DQ10	141	DQ15	80	DQ32	200	DQ37
22	DQ11	142	VSS	81	DQ33	201	VSS
23	VSS	143	DQ20	82	VSS	202	DM4
24	DQ16	144	DQ21	83	$\overline{\text{DQS4}}$	203	NC
25	DQ17	145	VSS	84	DQS4	204	VSS
26	VSS	146	DM2	85	VSS	205	DQ38
27	$\overline{\text{DQS2}}$	147	NC	86	DQ34	206	DQ39
28	DQS2	148	VSS	87	DQ35	207	VSS
29	VSS	149	DQ22	88	VSS	208	DQ44
30	DQ18	150	DQ23	89	DQ40	209	DQ45
31	DQ19	151	VSS	90	DQ41	210	VSS
32	VSS	152	DQ28	91	VSS	211	DM5
33	DQ24	153	DQ29	92	$\overline{\text{DQS5}}$	212	NC
34	DQ25	154	VSS	93	DQS5	213	VSS
35	VSS	155	DM3	94	VSS	214	DQ46
36	$\overline{\text{DQS3}}$	156	NC	95	DQ42	215	DQ47
37	DQS3	157	VSS	96	DQ43	216	VSS
38	VSS	158	DQ30	97	VSS	217	DQ52
39	DQ26	159	DQ31	98	DQ48	218	DQ53
40	DQ27	160	VSS	99	DQ49	219	VSS
41	VSS	161	CB4 / NC [2]	100	VSS	220	CK2
42	CB0 / NC [2]	162	CB5 / NC [2]	101	SA2	221	$\overline{\text{CK2}}$

Pin Configuration (cont'd)

PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
43	CB1 / NC [2]	163	VSS	102	NC	222	VSS
44	VSS	164	DM8	103	VSS	223	DM6
45	$\overline{\text{DQS8}}$	165	NC	104	$\overline{\text{DQS6}}$	224	NC
46	DQS8	166	VSS	105	DQS6	225	VSS
47	VSS	167	CB6 / NC [2]	106	VSS	226	DQ54
48	CB2 / NC [2]	168	CB7 / NC [2]	107	DQ50	227	DQ55
49	CB3 / NC [2]	169	VSS	108	DQ51	228	VSS
50	VSS	170	VDDQ	109	VSS	229	DQ60
51	VDDQ	171	CKE1	110	DQ56	230	DQ61
52	CKE0	172	VDD	111	DQ57	231	VSS
53	VDD	173	NC, (A15)[1]	112	VSS	232	DM7
54	NC, (BA2)[1]	174	NC, (A14)[1]	113	$\overline{\text{DQS7}}$	233	NC
55	$\overline{\text{NC}}$	175	VDDQ	114	NC	234	VSS
56	VDDQ	176	A12	115	VSS	235	DQ62
57	A11	177	A9	116	DQ58	236	DQ63
58	A7	178	VDD	117	DQ59	237	VSS
59	VDD	179	A8	118	VSS	238	VDDSPD
60	A5	180	A6	119	SDA	239	SA0
				120	SCL	240	SA1

1) Pins 54, 173 and 174 are not connected on this modules and are reserved for future DIMM module products based on higher density memory components.
2) These pins are the check bit DQ's for ECC unbuffered DIMMs and no-connects for Non-ECC DIMMs
3) Address A13 is not used on memory modules based on x 16 components

1.6 Pin Locations



240 pin Modules (MO-237)

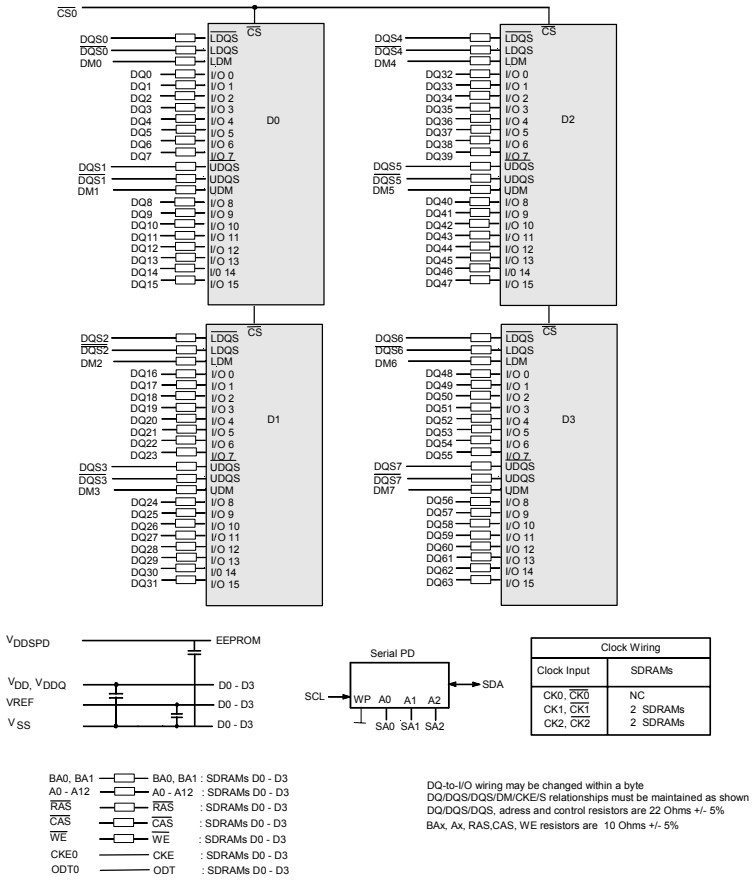
1.7 Unbuffered DIMM Input/Output Functional Description

Symbol	Type	Polarity	Function
CK[2:0], $\overline{CK}$[2:0]	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of $\overline{CK}$.
CKE[1:0]	Input	Active High	Activates the SDRAM clock signals when high and deactivates when low. By deactivating the clocks, CKE low initiates the Power Down Mode or the Self Refresh Mode
$\overline{CS}$[1:0]	Input	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue. This signal provides for external rank selection on systems with multiple ranks.
ODT[1:0]	Input	Active High	When high, termination resistance is enabled for all DQ, DQS and DM pins, assuming this function is enabled in the Extended mode Register Set (EMRS).
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Active Low	When sampled at the positive edge of the clock, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation to be executed by the SDRAM.
DM[8:0]	Input	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a write access. DM is samples on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
BA[1:0]	Input	-	Selects which internal SDRAM memory bank is activated
A[13:0]	Input	-	During Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, A10(=AP) is used to invoke Auto-Precharge operation at the end of the burst read or write cycle. If AP is high, Auto Precharge is selected and BA[1:0] defines the bank to be precharged. If AP is low, Auto-Precharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[1:0] to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA[1:0]. If AP is low, BA[1:0] are used to define which bank to precharge.
DQ[63:0], CB[7:0]	I/O	-	Data and Check Bit Input /Output pins.
DQS[8:0], $\overline{DQS}$[8:0]	I/O	Cross point	The data strobes, associated with one data byte, source with data transfer. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sources by the DDR2 SDRAM and is sent at the leading edge of the data window. $\overline{DQS}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$. If the module is to be operated in single ended strobe mode, all $\overline{DQS}$ signals must be tied on the system board to VSS and DDR2 SDRAM mode registers programmed appropriately.
SA[2:0]	Input	-	These signals are tied at the system planar to either VSS or VDDSPD to configure the serial SPD EEPROM address range
SDA	I/O	-	This bidirectional pin is used to transfer data into and out of the SPD EEPROM. A resistor maybe connected from the SDA bus line to VDDSPD on the system level to act as a pull-up.
SCL	Input	-	This signal is used to clock data into the SPD EEPROM. A resistor maybe connected from the SCL bus line to VDDSPD on the system planar to act as a pull-up.
V_{DDQ}	Supply	-	Isolated power supply for the SDRAM output buffers to provide improved noise immunity.
V_{DD}, V_{SS}	Supply	-	Power and ground for the DDR SDRAM input buffers and core logic.
VREF	Supply	-	Reference voltage for the SSTL-18 inputs.
VDDSPD	Supply	-	Serial EEPROM positive power supply, wired to a separated power pin at the connector which supports from 1.7 Volt to 3.6 Volt.
Note: $\overline{CS1}$, ODT1 and CKE1 are used on dual rank modules only.			

2.0 Block Diagrams

2.2 One Rank 32M x 64 (256 MByte) DDR2 SDRAM DIMM Modules (x16 components.)

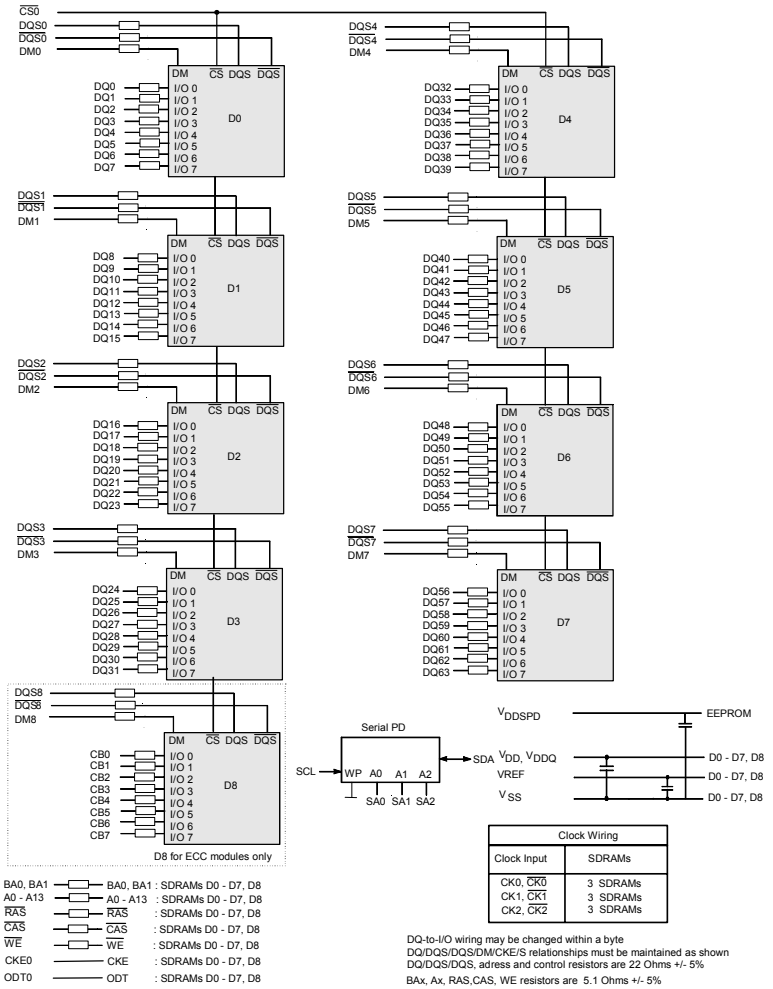
HYS64T32000GU on Raw Card C



Block Diagrams

2.2 One Rank 64M x 64 / 72 (512 MByte) DDR2 SDRAM DIMM Modules (x8 comp.)

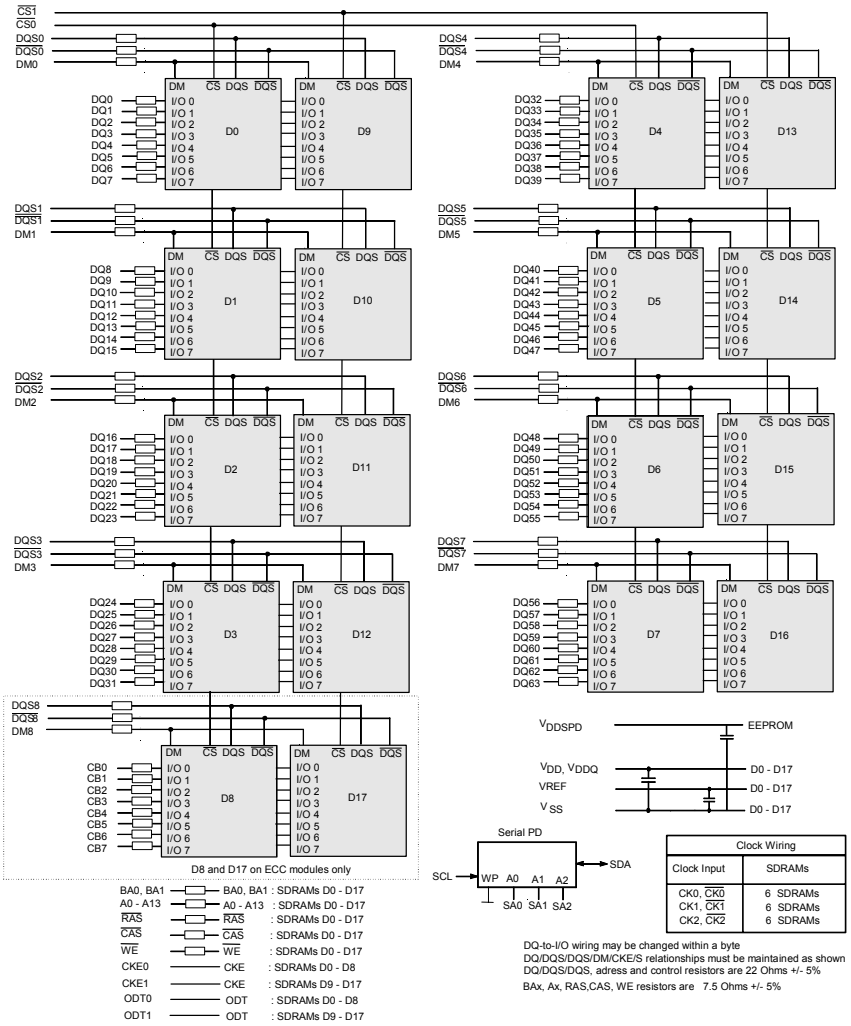
HYS64T64000GU / HYS72T64000GU on Raw Card A



Block Diagrams

2.3 128M x 64/72 (1GByte) two rank DDR2 SDRAM DIMM Modules (x8 comp.)

HYS64T128020GU / HYS72T128020GU on Raw Card B



3.0 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	– 0.5	2.3	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}	– 1.0	2.3	V
Voltage on $V_{DD\,Q}$ relative to V_{SS}	V_{DDQ}	– 0.5	2.3	
Storage temperature range	T_{STG}	-55	+100	°C

Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3.1 Operating Temperature Range

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
DIMM Module Operating Temperature Range (ambient)	TOPR	0	+55	°C	
DRAM Component Case Temperature Range	TCASE	0	+95	°C	1 - 4

1. DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. Within the DRAM Component Case Temperature range all DRAM specification will be supported.
3. Above 85°C DRAM case temperature the Auto-Refresh command interval has to be reduced to tREFI = 3.9 µs.
4. Self-Refresh period is hard-coded in the DRAMs and therefore it is imperative that the system ensures the DRAM is below 85°C case temperature before initiating self-refresh operation.

3.2 Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Limit Values			Unit	Notes
		min.	nom.	max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	-
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V	2)
EEPROM Supply Voltage	V_{DDSPD}	1.7	–	3.6	V	
DC Input Logic High	$V_{IH\,(DC)}$	V_{REF} + 0.125	–	V_{DDQ} + 0.3	V	
DC Input Logic Low	$V_{IL\,(DC)}$	– 0.30	–	V_{REF} – 0.125	V	
In / Output Leakage Current	I_L	– 5		5	µA	3)

1 Under all conditions, V_{DDQ} must be less than or equal to V_{DD}
2 Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\,(DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.
3 For any pin on the DIMM connector under test input of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V.

4.0 I_{DD} Specifications and Conditions

4.1 256 MByte Non- ECC Module HYS64T32000GU (one rank, four components x16)

256 MByte HYS64T32000GU		PC2-3200 -5”	PC2-4300 “-3.7”	PC2-5400 “-3”		
Symbol	Parameter / Condition	max.	max.	max.	Unit	Note
I_{DD0}	Operating Current	280	320	360	mA	1
I_{DD1}	Operating Current	300	360	420	mA	1
I_{DD2P}	Precharge PD Standby Current	16	16	16	mA	1
I_{DD2N}	Precharge Standby Current	128	160	200	mA	1
I_{DD2Q}	Precharge Quiet Standby Current	100	120	140	mA	1
$I_{DD3P(0)}$	Active PD Standby Current	52	64	80	mA	1
$I_{DD3P(1)}$	LP Active PD Standby Current	20	20	20	mA	1
I_{DD3N}	Active Standby Current	140	160	200	mA	1
I_{DD4R}	Operating Current Burst Read	340	400	500	mA	1
I_{DD4W}	Operating Current Burst Write	360	440	520	mA	1
I_{DD5B}	Auto-Refresh Current (tRFCmin.)	480	520	520	mA	1
I_{DD5D}	Auto-Refresh Current (tREFI)	24	24	24	mA	1
I_{DD6}	Self-Refresh Current	16	16	16	mA	1
I_{DD7}	Operating Current	840	880	960	mA	1

Notes: 1) Calculated values from component data. ODT disabled. IDD1, IDD4R, and IDD7 are defined with the outputs disabled.

4.2 512 MByte Non-ECC Module HYS64T64000GU (one rank, eight components x8)

512 MByte HYS64T64000GU		PC2-3200 “-5”	PC2-4300 “-3.7”	PC2-5400 “-3”		
Symbol	Parameter / Condition	max.	max.	max.	Unit	Note
I_{DD0}	Operating Current	440	520	600	mA	1
I_{DD1}	Operating Current	480	600	720	mA	1
I_{DD2P}	Precharge PD Standby Current	32	32	32	mA	1
I_{DD2N}	Precharge Standby Current	256	320	400	mA	1
I_{DD2Q}	Precharge Quiet Standby Current	200	240	280	mA	1
$I_{DD3P(0)}$	Active PD Standby Current	104	128	160	mA	1
$I_{DD3P(1)}$	LP Active PD Standby Current	40	40	40	mA	1
I_{DD3N}	Active Standby Current	280	320	400	mA	1
I_{DD4R}	Operating Current Burst Read	560	720	840	mA	1
I_{DD4W}	Operating Current Burst Write	600	760	880	mA	1
I_{DD5B}	Auto-Refresh Current (tRFCmin.)	960	1040	1120	mA	1
I_{DD5D}	Auto-Refresh Current (tREFI)	48	48	48	mA	1
I_{DD6}	Self-Refresh Current	32	32	32	mA	1
I_{DD7}	Operating Current	1040	1120	1280	mA	1

Notes: 1) Calculated values from component data. ODT disabled. IDD1, IDD4R, and IDD7 are defined with the outputs disabled.

4.3 512 MByte ECC Module HYS72T64000GU (one rank, nine components x8)

512 MByte HYS72T64000GU		PC2-3200 “-5”	PC2-4300 “-3.7”	PC2-5400 “-3”		
Symbol	Parameter / Condition	max.	max.	max.	Unit	Note
I_{DD0}	Operating Current	495	585	675	mA	1
I_{DD1}	Operating Current	540	675	810	mA	1
I_{DD2P}	Precharge PD Standby Current	36	36	36	mA	1
I_{DD2N}	Precharge Standby Current	288	360	450	mA	1
I_{DD2Q}	Precharge Quiet Standby Current	225	270	315	mA	1
$I_{DD3P(0)}$	Active PD Standby Current	117	144	180	mA	1
$I_{DD3P(1)}$	LP Active PD Standby Current	45	45	45	mA	1
I_{DD3N}	Active Standby Current	315	360	450	mA	1
I_{DD4R}	Operating Current Burst Read	630	810	945	mA	1
I_{DD4W}	Operating Current Burst Write	675	855	990	mA	1
I_{DD5B}	Auto-Refresh Current (tRFCmin.)	1080	1170	1260	mA	1
I_{DD5D}	Auto-Refresh Current (tREFI)	54	54	54	mA	1
I_{DD6}	Self-Refresh Current	36	36	36	mA	1
I_{DD7}	Operating Current	1170	1260	1440	mA	1

Notes: 1) Calculated values from component data. ODT disabled. IDD1, IDD4R, and IDD7 are defined with the outputs disabled.

4.4 1024 MByte Non-ECC Module HYS64128020GU (two ranks, sixteen components x8)

1024 MByte HYS64T128020GU		PC2-3200 “-5”	PC2-4300 “-3.7”	PC2-5400 “-3”		
Symbol	Parameter / Condition	max.	max.	max.	Unit	Note
I_{DD0}	Operating Current	472	552	632	mA	1, 2
I_{DD1}	Operating Current	512	632	752	mA	1, 2
I_{DD2P}	Precharge PD Standby Current	64	64	64	mA	1, 3
I_{DD2N}	Precharge Standby Current	512	640	800	mA	1, 3
I_{DD2Q}	Precharge Quiet Standby Current	400	480	560	mA	1, 3
$I_{DD3P(0)}$	Active PD Standby Current	208	256	320	mA	1, 3
$I_{DD3P(1)}$	LP Active PD Standby Current	80	80	80	mA	1, 3
I_{DD3N}	Active Standby Current	560	640	800	mA	1, 3
I_{DD4R}	Operating Current Burst Read	592	752	872	mA	1, 2
I_{DD4W}	Operating Current Burst Write	632	792	912	mA	1, 2
I_{DD5B}	Auto-Refresh Current (tRFCmin.)	976	1060	1120	mA	1, 2
I_{DD5D}	Auto-Refresh Current (tREFI)	96	96	96	mA	1, 3
I_{DD6}	Self-Refresh Current	64	64	64	mA	1, 3
I_{DD7}	Operating Current	1072	1152	1312	mA	1, 2

Notes: 1) Calculated values from component data. ODT disabled. IDD1, IDD4R, and IDD7 are defined with the outputs disabled.
2) The other rank is in IDD2P Precharge Power-Down Standby Current mode
3) Both ranks are in the same IDD current mode

4.5 1024 MByte ECC Module HYS72T128020GU (two ranks, eighteen components x8)

1024 MByte HYS72T128020GU		PC2-3200 “-5”	PC2-4300 “-3.7”	PC2-5400 “-3”		
Symbol	Parameter / Condition	max.	max.	max.	Unit	Note
I_{DD0}	Operating Current	531	621	711	mA	1, 2
I_{DD1}	Operating Current	576	711	846	mA	1, 2
I_{DD2P}	Precharge PD Standby Current	72	72	72	mA	1, 3
I_{DD2N}	Precharge Standby Current	576	720	900	mA	1, 3
I_{DD2Q}	Precharge Quiet Standby Current	450	540	630	mA	1, 3
$I_{DD3P(0)}$	Active PD Standby Current	234	288	360	mA	1, 3
$I_{DD3P(1)}$	LP Active PD Standby Current	90	90	90	mA	1, 3
I_{DD3N}	Active Standby Current	630	720	900	mA	1, 3
I_{DD4R}	Operating Current Burst Read	666	846	981	mA	1, 2
I_{DD4W}	Operating Current Burst Write	711	891	1026	mA	1, 2
I_{DD5B}	Auto-Refresh Current (tRFCmin.)	1116	1206	1296	mA	1, 2
I_{DD5D}	Auto-Refresh Current (tREFI)	108	108	108	mA	1, 3
I_{DD6}	Self-Refresh Current	72	72	72	mA	1,3
I_{DD7}	Operating Current	1206	1296	1476	mA	1, 2

Notes: 1) Calculated values from component data. ODT disabled. IDD1, IDD4R, and IDD7 are defined with the outputs disabled.
2) The other rank is in IDD2P Precharge Power-Down Standby Current mode
3) Both ranks are in the same IDD current mode

4.6 I_{DD} Measurement Conditions

(VDDQ = 1.8V ± 0.1V; VDD = 1.8V ± 0.1V)

Symbol	Parameter/Condition
I_{DD0}	**Operating Current - One bank Active - Precharge** tCK = tCKmin., tRC = tRCmin., tRAS = tRASmin., CKE is HIGH, $\overline{CS}$ is high between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.
I_{DD1}	**Operating Current - One bank Active - Read - Precharge** IOUT = 0 mA, BL = 4, tCK = tCKmin., tRC = tRCmin., tRAS = tRASmin.,tRCD = tRCDmin.,AL = 0, CL = CLmin.; CKE is HIGH, CS is high between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.
I_{DD2P}	**Precharge Power-Down Current:** All banks idle; CKE is LOW; tCK = tCKmin.; Other control and address inputs are STABLE, Data bus inputs are FLOATING.
I_{DD2N}	**Precharge Standby Current**: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; tCK = tCKmin.; Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.
I_{DD2Q}	**Precharge Quiet Standby Current**: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; tCK = tCKmin.; Other control and address inputs are STABLE, Data bus inputs are FLOATING.
$I_{DD3P(0)}$	**Active Power-Down Current**: All banks open; tCK = tCKmin., CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to "0" (Fast Power-down Exit);
$I_{DD3P(1)}$	**Active Power-Down Current**: All banks open; tCK = tCKmin., CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to "1" (Slow Power-down Exit);
I_{DD3N}	**Active Standby Current**: All banks open; tCK = tCKmin.; tRAS = tRASmax; tRP = tRPmin.,CKE is HIGH; $\overline{CS}$ is high between valid commands. Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.
I_{DD4R}	**Operating Current - Burst Read:** All banks open; Continuous burst reads; BL = 4;AL = 0, CL = CLmin.; tCK = tCKmin.; tRAS = tRASmax., tRP = tRPmin.; CKE is HIGH, CS is high between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; IOUT = 0mA.
I_{DD4W}	**Operating Current - Burst Write:** All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CLmin.; tCK = tCKmin.; tRAS = tRASmax., tRP = tRPmin.; CKE is HIGH, CS is high between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;
I_{DD5B}	**Burst Auto-Refresh Current**: tCK = tCKmin., Refresh command every tRFC = tRFCmin. interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.
I_{DD5D}	**Distributed Auto-Refresh Current**: tCK = tCKmin., Refresh command every tRFC = tREFI interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.
I_{DD6}	**Self-Refresh Current**: CKE ≤ 0.2V; external clock off, CK and $\overline{CK}$ at 0V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. RESET = Low. IDD6 current values are guaranteed up to TCASE of 85ºC max.
I_{DD7}	**All Bank Interleave Read Current:** 1. All banks are being interleaved at minimum tRC without violating tRRD using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. Iout = 0mA. 2. Timing pattern: - ***DDR2 -400-333***: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D D (12 clocks) - ***DDR2 -533-444***: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D (16 clocks) - ***DDR2 -667-444***: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D (19 clocks) 3. Legend: A = Activate, RA = Read with Auto-Precharge, D=DESELECT

Notes:

1. IDD specifications are tested after the device is properly initialized and IDD parameter are specified with ODT disabled.
2. Definitions for IDD:
   LOW is defined as VIN <= VIL(ac)max; HIGH is defined as VIN >= VIH(ac)min.
   STABLE is defined as inputs are stable at a HIGH or LOW level.
   FLOATING is defined as inputs are VREF = VDDQ / 2.
   SWITCHING is defined as:
   inputs are changing between HIGH and LOW every other clock (once per two cycles) for address and control signals, and inputs changing between HIGH and LOW every other clock (once per cycle) for DQ signals not including mask or strobes.
3. IDD1, IDD4R, and IDD7A current measurements are defined with the outputs disabled (Iout = 0 mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.
3. For two rank modules: For all active current measurements the other rank is in Precharge Power-Down Mode IDD2P

4.6 I_{DD} Measurement Conditions (cont'd)

For testing the IDD parameters, the following timing parameters are used:

Parameter		Symbol	-5 PC2-3200	-3.7 PC2-4300	-3 PC2-5400	Unit
			3-3-3	4-4-4	4-4-4	
CAS Latency		CLmin	3	4	4	tCK
Clock Cycle Time		tCKmin	5	3.75	3	ns
Active to Read or Write delay		tRCDmin	15	15	12	ns
Active to Active / Auto-Refresh command period		tRCmin	60	60	57	ns
Active bank A to Active bank B command delay	x8 [1]	tRRDmin	7.5	7.5	7.5	ns
	x16 [2]	tRRDmin	10	10	10	ns
Active to Precharge Command		tRASmin	45	45	45	ns
Precharge Command Period		tRPmin	15	15	12	ns
Auto-Refresh to Active / Auto-Refresh command period		tRFCmin	105	105	105	ns
Average periodic Refresh interval		tREFI	7.8	7.8	7.8	µs
Notes: 1) For modules based on x8 components 2) For modules based on x16 components						

4.7 ODT (On Die Termination) Current

The ODT function adds additional current consumption to the DDR2 SDRAM when enabled by the EMRS(1). Depending on address bits A6 & A2 in the EMRS(1) a "week" or "strong" termination can be selected. The current consumption for any terminated input pin, depends on the input pin is in tri-state or driving "0" or "1", as long a ODT is enabled during a given period of time.

ODT current per terminated pin:

		EMRS(1) State	min.	typ.	max.	Unit
Enabled ODT current per DQ added IDDQ current for ODT enabled; ODT is HIGH; Data Bus inputs are FLOATING	IODTO	A6 = 0, A2 = 1	5	6	7.5	mA/DQ
		A6 = 1, A2 = 0	2.5	3	3.75	mA/DQ
Active ODT current per DQ added IDDQ current for ODT enabled; ODT is HIGH; worst case of Data Bus inputs are STABLE or SWITCHING.	IODTT	A6 = 0, A2 = 1	10	12	15	mA/DQ
		A6 = 1, A2 = 0	5	6	7.5	mA/DQ
note: For power consumption calculations the ODT duty cycle has to be taken into account						

5.0 Electrical Characteristics & AC Timings

5.1 AC Timing Parameter by Speed Grade (Component level data, for reference only)

Symbol	Parameter		-5 DDR2 -400		-3.7 DDR2 -533		-3 DDR2 -667		Unit
			Min	Max	Min	Max	Min	Max	
t_{AC}	DQ output access time from CK/$\overline{CK}$		– 600	+ 600	-500	+500	-450	+450	ps
t_{DQSCK}	DQS output access time from CK/$\overline{CK}$		– 500	+ 500	–450	+450	-400	+400	ps
t_{CH}	CK, $\overline{CK}$ high-level width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
t_{CL}	CK, $\overline{CK}$ low-level width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
t_{HP}	Clock Half Period		min. (t_{CL}, t_{CH})		min. (t_{CL}, t_{CH})		min. (t_{CL}, t_{CH})		
t_{CK}	Clock cycle time	CL = 3	5000	8000	5000	8000	5000	8000	ps
		CL = 4 & 5	5000	8000	3750	8000	3000	8000	ps
t_{IS}	Address and control input setup time		600	-	600	-	tbd.	-	ps
t_{IH}	Address and control input hold time		600	-	600	-	tbd.	-	ps
t_{DH}	DQ and DM input hold time		400	-	350	-	300	-	ps
t_{DS}	DQ and DM input setup time		400	-	350	-	300	-	ps
t_{IPW}	Control and Addr. input pulse width (each input)		0.6	-	0.6	-	0.6	-	t_{CK}
t_{DIPW}	DQ and DM input pulse width (each input)		0.35	-	0.35	-	0.35	-	t_{CK}
t_{HZ}	Data-out high-impedance time from CK/$\overline{CK}$		-	tACmax	-	tACmax	-	tACmax	ps
$t_{LZ(DQ)}$	DQ low-impedance from CK / $\overline{CK}$		2*tACmin	tACmax	2*tACmin	tACmax	2*tACmin	tACmax	ps
$t_{LZ(DQS)}$	DQS low-impedance from CK / $\overline{CK}$		tACmin	tACmax	tACmin	tACmax	tACmin	tACmax	ps
t_{DQSQ}	DQS-DQ skew (for DQS & associated DQ signals)		-	350	-	300	-	250	ps
t_{QHS}	Data hold skew factor		-	450	-	400	-	350	ps
t_{QH}	Data Output hold time from DQS		t_{HP}-t_{QHS}	-	t_{HP}-t_{QHS}	-	t_{HP}-t_{QHS}	-	
t_{DQSS}	Write command to 1st DQS latching transition		WL -0.25	WL +0.25	WL -0.25	WL +0.25	WL -0.25	WL +0.25	t_{CK}
$t_{DQSL,H}$	DQS input low (high) pulse width (write cycle)		0.35	-	0.35	-	0.35	-	t_{CK}
t_{DSS}	DQS falling edge to CLK setup time (write cycle)		0.2	-	0.2	-	0.2	-	t_{CK}
t_{DSH}	DQS falling edge hold time from CLK (write cycle)		0.2	-	0.2	-	0.2	-	t_{CK}
t_{MRD}	Mode register set command cycle time		2	-	2	-	2	-	t_{CK}
t_{WPRE}	Write preamble		0.25	-	0.25	-	0.35	-	t_{CK}
t_{WPST}	Write postamble		0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}
t_{RPRE}	Read preamble		0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
t_{RPST}	Read postamble		0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}
t_{RAS}	Active to Precharge command		45	70000	45	70000	45	70000	ns
t_{RC}	Active to Active/Auto-refresh command period		60	-	60	-	57	-	ns
t_{RFC}	Auto-refresh to Active/Auto-refresh command period		105	-	105	-	105	-	ns

Symbol	Parameter		-5 DDR2 -400		-3.7 DDR2 -533		-3 DDR2 -667		Unit
			Min	Max	Min	Max	Min	Max	
t_{RCD}	Active to Read or Write delay (with and without Auto-Precharge) delay		15	-	15	-	12	-	ns
t_{RP}	Precharge command period		15	-	15	-	12	-	ns
t_{RRD}	Active bank A to Active bank B command	x8 (1k page size)	7.5	-	7.5	-	7.5	-	ns
		x16 (2k page size)	10	-	10	-	10	-	ns
t_{CCD}	$\overline{CAS}$ A to $\overline{CAS}$ B Command Period		2	-	2	-	2	-	t_{CK}
t_{WR}	Write recovery time		15	-	15	-	15	-	ns
t_{DAL}	Auto precharge write recovery + precharge time		WR+tRP	-	WR+tRP	-	WR+tRP	-	t_{CK}
t_{WTR}	Internal write to read command delay		10	-	7.5	-	7.5	-	ns
t_{RTP}	Internal read to precharge command delay		7.5	-	7.5	-	7.5	-	ns
t_{XARD}	Exit power down to any valid command (other than NOP or Deselect)		2	-	2	-	2	-	t_{CK}
t_{XARDS}	Exit active power-down mode to read command (slew exit, lower power)		6 - AL	-	6 - AL	-	6 - AL	-	t_{CK}
t_{XP}	Exit precharge power-down to any valid command (other than NOP or Deselect)		2	-	2	-	2	-	t_{CK}
t_{XSRD}	Exit Self-Refresh to read command		200	-	200	-	200	-	t_{CK}
t_{XSNR}	Exit Self-Refresh to non-read command		tRFC + 10	-	tRFC + 10	-	tRFC + 10	-	ns
t_{CKE}	CKE minimum high and low pulse width		3	-	3	-	3	-	t_{CK}
t_{OIT}	OCD drive mode output delay		0	12	0	12	0	12	ns
t_{DELAY}	Minimum time clocks remain ON after CKE asynchronously drops low		tIS+tCK +tIH	-	tIS+tCK +tIH	-	tIS+tCK +tIH	-	ns
t_{REFI}	Average Periodic Refresh Interval	0°C - 85°C	-	7.8	-	7.8	-	7.8	µs
		85°C - 95°C	-	3.9	-	3.9	-	3.9	

1. For details and notes see the relevant INFINEON component datasheet
2. Timing definition and values for tis, tih, tds and tdh may change due to actual JEDEC work. This may also effect the SPD code for these parameters

5.2 ODT AC Electrical Characteristics and Operating Conditions (all speed bins)

Symbol	Parameter / Condition		min.	max.	Units
t_{AOND}	ODT turn-on delay		2	2	t_{CK}
t_{AON}	ODT turn-on	DDR2-400/533	tAC(min)	tAC(max) + 1 ns	ns
		DDR2-667	tAC(min)	tAC(max) + 0.7 ns	
t_{AONPD}	ODT turn-on (Power-Down Modes)		tAC(min) + 2 ns	2 tCK + tAC(max) + 1 ns	ns
t_{AOFD}	ODT turn-off delay		2.5	2.5	t_{CK}
t_{AOF}	ODT turn-off		tAC(min)	tAC(max) + 0.6 ns	ns
t_{AOFPD}	ODT turn-off delay (Power-Down Modes)		tAC(min) + 2 ns	2.5 tCK + tAC(max) + 1 ns	ns
t_{ANPD}	ODT to Power Down Mode Entry Latency		3	-	t_{CK}
t_{AXPD}	ODT Power Down Exit Latency		8	-	t_{CK}

6.0 Serial Presence Detect Codes for Unbuffered DIMM Modules

Byte#	Description	Speed Grade	SPD Entry Value	Hex Value				
				HYS64T32000GU	HYS64T64000GU	HYS72T64000GU	HYS64T128020GU	HYS72T128020GU
0	Number of SPD Bytes	all	128	80				
1	Total Bytes in Serial PD	all	256	08				
2	Memory Type	all	DDR2-SDRAM	08				
3	Number of Row Addresses	all	13 / 14	0D	0E	0E	0E	0E
4	Number of Column Addresses	all	10	0A	0A	0A	0A	0A
5	Number of DIMM Ranks, Package and Height	all	1 / 2	60	60	60	61	61
6	Module Data Width	all	x64 / x72	40	40	48	40	48
7	Not used	all	not used	00				
8	Module Interface Levels	all	SSTL_1.8	05				
9	Min. Clock Cycle Time at CAS Latency = 5	-5	5 ns	50				
		-3.7	3.7 ns	3D				
		-3	3 ns	30				
10	SDRAM Access Time from Clock at CL = 5	-5	0.6 ns	60				
		-3.7	0.5 ns	50				
		-3	0.45 ns	45				
11	DIMM Configuration Type	all	non-ECC / ECC	00	00	02	00	02
12	Refresh Rate/Type	all	7.8 µs, SR	82				
13	SDRAM Width, Primary	all	x16, x8	10	08	08	08	08
14	Error Checking SDRAM Data Width	all	na / x8	00	00	08	00	08
15	Reserved	all	-	00				
16	Burst Length Supported	all	4 & 8	0C				
17	Number of SDRAM Banks	all	4	04				
18	Supported $\overline{CAS}$ Latencies	all	5, 4, 3	38				
19	Not used	all	not used	00				
20	DIMM Type Information	all	unbuffered DIMM	02				
21	SDRAM Module Attributes	all	normal DIMM	00				
22	SDRAM Device Attributes: General	all	incl. weak driver	01				
23	Min. Clock Cycle Time at $\overline{CAS}$ Latency = 4	-5	5 ns	50				
		-3.7	3.7 ns	3D				
		-3	3 ns	30				
24	SDRAM Access Time from Clock for CL = 4	-5	0.6 ns	60				
		-3.7	0.5 ns	50				
		-3	0.45 ns	45				
25	Minimum Clock Cycle Time at CL = 3	all	5 ns	50				
26	Access Time from Clock at CL = 3	all	0.6 ns	60				
27	Minimum Row Precharge Time (tRP)	-5 & -3.7	15 ns	3C				
		-3	12 ns	30				
28	Minimum Row Act. to Row Act. Delay (tRRD)	all	10 / 7.5 ns	28	1E	1E	1E	1E
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay (tRCD)	-5 & -3.7	15 ns	3C				
		-3	12 ns	30				
30	Minimum $\overline{RAS}$ Pulse Width (tRAS)	all	45 ns	2D				
31	Module Density (per rank)			40	80	80	80	80
32	Address and Command Setup Time (tIS)	-5	0.60 ns	60				
		-3.7	0.50 ns	50				
		-3	0.45 ns	45				

Byte#	Description	Speed Grade	SPD Entry Value	Hex Value				
				HYS64T32000GU	HYS64T64000GU	HYS72T64000GU	HYS64T128020GU	HYS72T128020GU
33	Address and Command Hold Time (tIH)	-5	0.60 ns	60				
		-3.7	0.50 ns	50				
		-3	0.45 ns	45				
34	Data Input Setup Time (tDS)	-5	0.40 ns	40				
		-3.7	0.35 ns	35				
		-3	0.30 ns	30				
35	Data Input Hold Time (tDH)	-5	0.40 ns	40				
		-3.7	0.35 ns	35				
		-3	0.30 ns	30				
36	Write Recovery Time (tWR)	all	15 ns	3C				
37	Internal Write to Read Command delay (tWTR)	-5	10 ns	28				
		-3.7 & -3	7.5 ns	1E				
38	Internal Read to Precharge delay (tRTP)	all	7.5 ns			1E		
39	Not used		not used	00				
40	Extension of Byte 41 tRC and Byte 42 tRFC	all		00				
41	Minimum Core Cycle Time (tRC)	-5 & -3.7	60 ns	3C				
		-3	57 ns	39				
42	Min. Auto Refresh Cycle Time (tRFC)	all	105 ns	69				
43	Maximum Clock Cycle Time tck	all	8 ns	80				
44	Max. DQS-DQ Skew (tDQSQmax.)	-5	0.35 ns	23				
		-3.7	0.30 ns	1E				
		-3	0.25 ns	19				
45	Read Data Hold Skew Factor (tQHS)	-5	0.45 ns	2D				
		-3.7	0.40 ns	28				
		-3	0.35 ns	23				
46	Not used		not used	00				
47-61	Reserved for “Delta Temperature in SPD”		see note 1	00	00	00	00	00
62	SPD Revision		Revision 1.0	10				
63	Checksum for Bytes 0 - 62	-5		tbd	tbd	tbd	tbd	tbd
		-3.7		tbd	tbd	tbd	tbd	tbd
		-3		tbd	tbd	tbd	tbd	tbd
64	Manufacturers JEDEC ID Code		INFINEON	C1				
65-71	Not used			00				
72	Module Assembly Location			XX				
73-90	Module Part Number			XX				
91-92	Module Revision Code			XX				
93-94	Module Manufacturing Date		Year/Week Code	XX				
95-98	Module Serial Number		Serial Number	XX				
99-127	Manufacturer’s Specific Data		blank	FF				
128-255	Open for Customer use		blank					

Note 1 : Will be used for future SPD Code Revisions. For details of “Delta Temperature in SPD” see JEDEC ballot JC-42.5 Item # 1468.

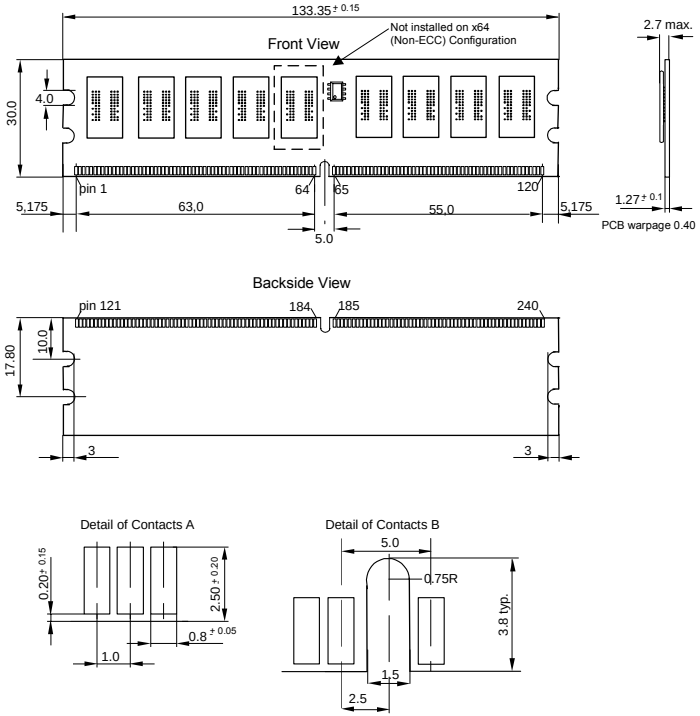
7.0 Package Outlines

7.1 Raw Card A

Module Package

DDR2 Unbuffered DIMM Modules Raw Card A

one physical rank, 8 (Non-ECC) or 9 (ECC) components x8



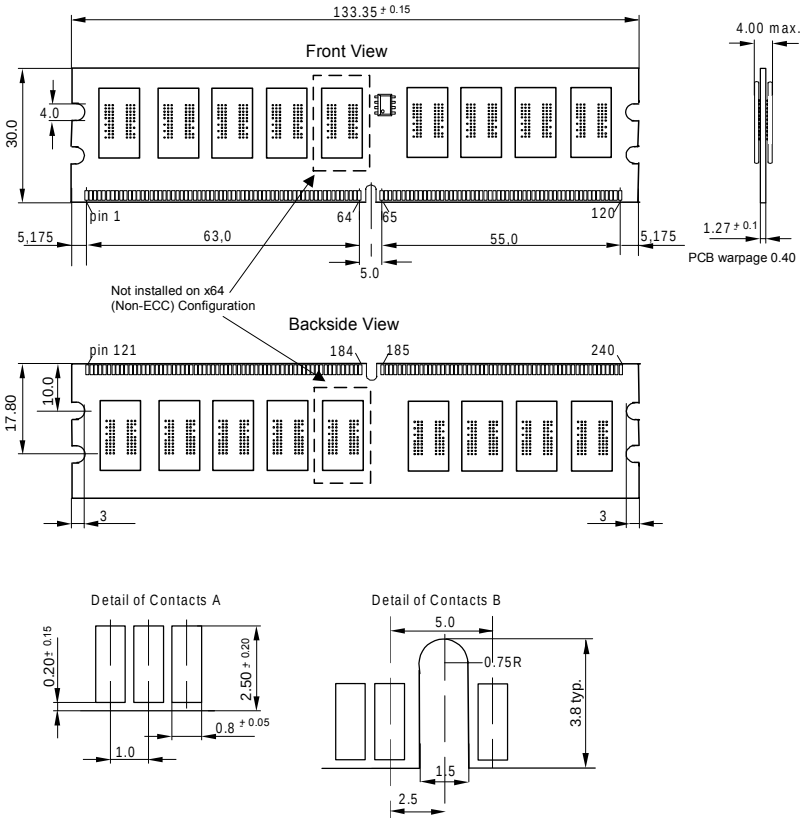
note: all outline dimensions and tolerances are in accordance with the JEDEC standard (MO-237)

7.2 Raw Card B

Module Package

DDR2 Unbuffered DIMM Modules Raw Card B

two physical ranks, 16 (Non-ECC) or 18 (ECC) components x8



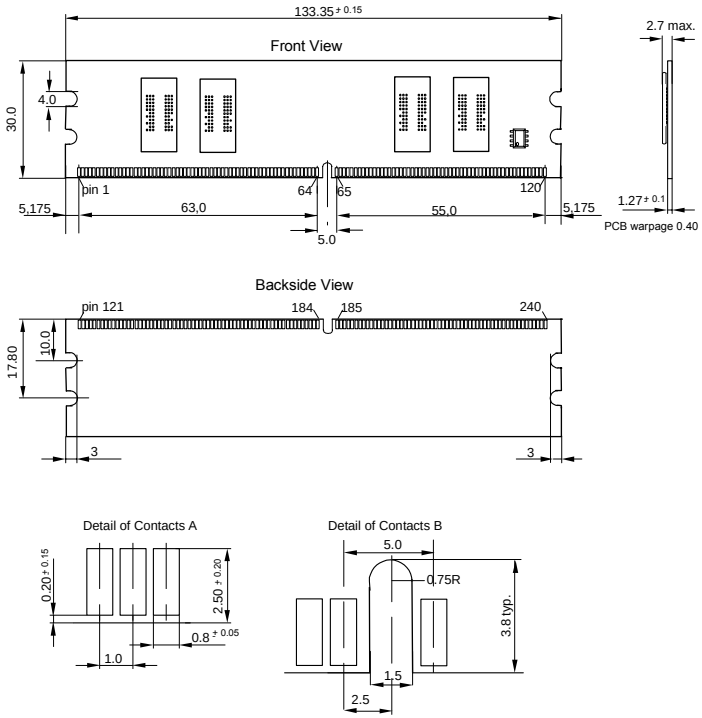
note: all outline dimensions and tolerances are in accordance with the JEDEC standard (MO-237)

7.3 Raw Card C

Module Package

DDR2 Registered DIMM Modules Raw Card C

one physical rank, 4 components x16 (tbd.)



note: all outline dimensions and tolerances are in accordance with the JEDEC standard (MO-237)

8.0 Nomenclature (Modules & Components)

8.1 DDR2 DIMM Modules

	1	2	3	4	5	6	7	8	9	10	11
Example:	HYS	72	T	128	0	2	0	G	U	-5	-A

1	INFINEON Prefix	HYS for DIMM Modules	7	Product Variations	0 = standard
2	Module Data Width	64 = Non-ECC Modules 72 = ECC Modules	8	Package	G = standard modules H = “green” modules
3	DRAM Technology	T = DDR2	9	Module Type	R = Registered DIMMs U = Unbuffered DIMMs DL = Small Outline DIMMs)
4	Memory Density per I/O	64 = 64 Mb 128 = 128 Mb 256 = 256 Mb	10	Speed Grade	-5 = PC2-3200 (DDR2-400) -3.7 = PC2-4300 (DDR2-533) -3 = PC2-5400 (DDR2-667)
5	Raw Card Generation	0 = first generation	11	Die Revision	A = 1st Generation B = 2nd Generation C = 3rd Generation
6	Number of Memory Ranks	0 = One Rank 2 = Two Ranks	Multiplying “Memory Density per I/O” with “Module Data Width” and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes.		

8.2 DDR2 Memory Components

	1	2	3	4	5	6	7	8	9
Example:	HYB	18	T	512	80	0	A	C	-5

1	INFINEON Component Prefix	HYB for DRAM Components	6	Product Variations	0 = standard
2	Power Supply Voltage	18 = 1.8 V Power Supply	7	Die Revision	A = 1st Generation B = 2nd Generation C = 3rd Generation
3	DRAM Technology	T = DDR2	8	Package Type	C = BGA package F = BGA package (lead and halogen free)
4	Memory Density	256 = 256 Mb 512 = 512 Mb 1G = 1024Mb	9	Speed Grade	-5 =...DDR2-400 -3.7 =.DDR2-533 -3 =...DDR2-667
5	Memory Organisation	40 = x4, 4 data in/outputs 80 = x8, 8 data in/outputs 16 = x16, 16 data in/outputs			