

# SANYO Semiconductors DATA SHEET

## LA6504H — Monolithic Linear IC DVD System motor Drives

## Overview

The LA6504H is a DVD system motor drives.

### Functions

• PWM H bridge driver (3CH) + power operation amplifier (2CH)

## **Specifications**

#### Absolute Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Output block supply voltage	V <sub>M</sub> 1, 2 max		16.0	V
Output current 1	I <sub>O</sub> max1	FOCUS, TRACKING, LOADING	1.0	А
Output current 2	I <sub>O</sub> max2	FOCUS, TRACKING : 1msec	1.8	А
Output current 3	IO max3	SLED	0.7	А
Allowable power dissipation 1	Pd max1	Independent IC	0.8	W
Allowable power dissipation 2	Pd max2	Mounted on a board.	1.8	W
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

\* Specified substrate : 114.3mm×76.1mm×1.6mm, glass epoxy board.

#### **Recommended Operating Conditions** at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Output block supply voltage	V <sub>M</sub> 1, 2		8 to 14	V

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## LA6504H

Parameter	Symbol	Conditions	Ratings			Unit
Falamelei		Conditions	min	typ	max	Unit
Supply current 1		MUTE pin H at no load		20	35	mA
Supply current 2 I <sub>CC</sub> 2		MUTE pin L *1 at no load		45	60	mA
Supply current 3	ICC3	MUTE pin L *2 at no load		70	110	mA
Standby current	ICC <sup>4</sup>	MUTE pin L *3 at no load		0.2	0.4	mA
Overheat protection circuit						
Heat protection circuit operation temperature	TSD	Design target value *5	150	180		°C
Temperature hysteresis width	ΔTSD	Design target value *5		40		°C
SLED, loading input pin						
H level input voltage range	VIH		2.5		5.0	V
L level input voltage range	VIL		0		0.6	V
Input current	IIN			0.1	0.15	mA
MUTE pin			•		·	
H level input voltage range	V <sub>MU</sub> H	MUTE OFF	2.5		5.0	V
L level input voltage range	VMUL	MUTE ON	0		0.6	V
Input current	IINM			0.1	0.15	m/
Output block	•		•		•	
Saturation voltage 1	VSAT1	FOCUS, TRACKING : I <sub>O</sub> = 0.5A		1.5	2.3	V
Saturation voltage 2	VSAT2	SLED : I <sub>O</sub> = 0.5A		2.2	3.0	V
Saturation voltage 3	VSAT3	LOADING : I <sub>O</sub> = 0.5A		1.5	2.3	V
BTL block		•	•		·	
Output offset voltage	VOFF	Voltage difference between outputs of each channel RL = $12\Omega$ *4	-50		50	m∖
Maximum output amplitude	V <sub>O</sub> A	$R_L = 12\Omega$	7.9	10		V
Voltage gain	VGAIN	Gain between input and output $R_L = 12\Omega *4$	16	18	20	dB
Input OPAMP block						
Common-phase input range	VINOP		0.5		4.0	V
Input offset voltage	V <sub>OFF</sub> OP	*4	-6.0		6.0	m∖
Input bias current	IBIASOP				300	nA
Output high level voltage	V <sub>O</sub> HOP		3.7	4.0		V
Output low level voltage	V <sub>O</sub> LOP		1	0.2	0.5	V
TD OFST output offset voltage	VOFFTD	*4	-40		40	m∖
TD OFST pin maximum voltage	V <sub>TD</sub> MAX		2.7	3.0	3.3	V

\*1 : During LD motor rotation. IN4F = Hi, IN4R = Low.

\*2 : At braking of LD motor. IN4F = Hi, IN4R = Hi.

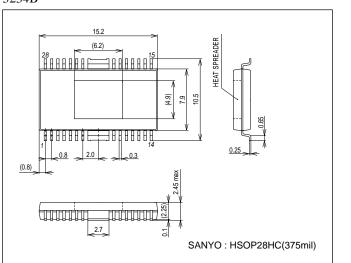
\*3 : At standby. IN4F = Low, IN4R = Low.

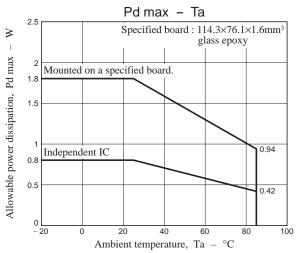
\*4 : Pre-OPAMP is used as buffer.

\*5 : Design target value. It doesn't measurement.

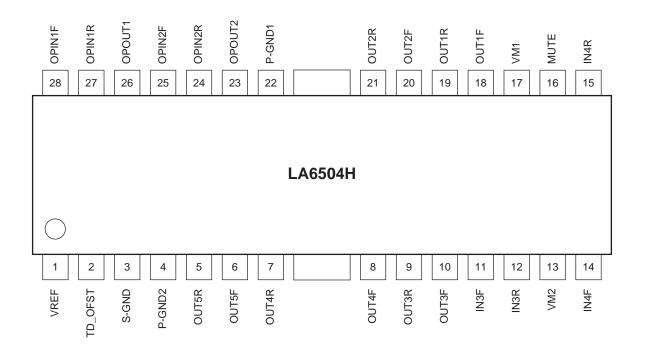
## Package Dimensions

unit : mm (typ) 3234B

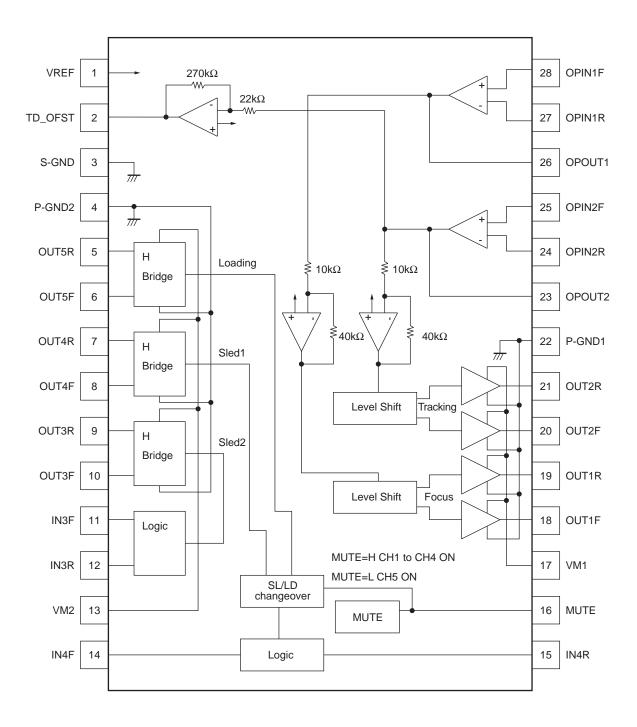




## **Pin Assignment**



## **Block Diagram**



## **Pin Functions**

Pin No.	Pin Name	Description (Function)
1	VREF	Reference voltage pin
2	TD_OFST	TD_OFST pin
3	S-GND	Signal system GND
4	P-GND2	Power system GND for CH3, 4, and 5
5	OUT5R	Loading output (-)
6	OUT5F	Loading output (+)
7	OUT4R	CH4 output pin (-)
8	OUT4F	CH4 output pin (+)
9	OUT3R	CH3 output pin (-)
10	OUT3F	CH3 output pin (+)
11	IN3F	CH3 input pin (+)
12	IN3R	CH3 input pin (-)
13	VM2	Power system power supply for CH3, 4, and 5
14	IN4F	CH4 input pin (+)
15	IN4R	CH4 input pin (-)
16	MUTE	MUTE pin
17	VM1	Power supply for the power and other systems for CH1 and 2
18	OUT1F	CH1 BTL AMP output pin (+)
19	OUT1R	CH1 BTL AMP output pin (-)
20	OUT2F	CH2 BTL AMP output pin (+)
21	OUT2R	CH2 BTL AMP output pin (-)
22	P-GND1	Power system GND for CH1 and 2
23	OPOUT2	OP-AMP output pin for CH2
24	OPIN2R	OP-AMP input pin (-) for CH2
25	OPIN2F	O-AMP input pin (+) for CH2
26	OPOUT1	OP-AMP output pin for CH1
27	OPIN1R	OP-AMP input pin (-) for CH1
28	OPIN1F	OP-AMP input pin (+) for CH1

\* The center frame (FR) functions as the power system GND. Set it to the minimum potential together with S-GND.

Pin dese	cription		
Pin No.	Pin name	Function	Equivalent circuit
27 28 24 25	OPIN1R OPIN1F OPIN2R OPIN2F	Input pin (CH1 to 2)	OPIN*R OPIN*F OPIN*F
11 12 14 15	IN3F IM3R IN4F IN4R	CH3(PWM) input CH4, 5(PWM) input	IN*R/F 300Ω 50kΩ 100kΩ 50kΩ
26 23 18 19 20 21	OPOUT1 OPOUT2 OUT1F OUT1R OUT2F OUT2R	CH1 and 2 outputs	$\begin{array}{c} OPOUT^{*} \\ 5k\Omega \lessapprox \\ 5k\Omega \swarrow \\ 6 \\ 40k\Omega \Biggr \\ 5k\Omega \\ 5k\Omega \\ 40k\Omega \\ 5 \\ 5k\Omega \\ 40k\Omega \\ 5 \\ 5 \\ 6 \\ 5 \\ 6 \\ 5 \\ 6 \\ 6 \\ 5 \\ 6 \\ 6$
10 9 8 7	OUT3F OUT3R OUT4F OUT4R	CH3(PWM) output CH4(PWM) output	2kΩ 2kΩ

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	m preceding pag		
Pin No.	Pin name	Function	Equivalent circuit
6 5	OUT5F OUT5R	CH5(PWM) output	2kΩ 2kΩ
16	MUTE	MUTE pin	MUTE $40k\Omega \ge$ $20k\Omega \ge$ $10k\Omega \ge$
1	VREF	VREF pin	
2	TD_OFST	TD_OFST pin	

## Actuator truth table

Loading block

0				
MUTE	IN4F	IN4R	OUT5F	OUT5R
L	L	L	Z	Z
L	Н	L	Н	L
L	L	Н	L	Н
L	н	н	L	L
Н	×	×	Z	Z

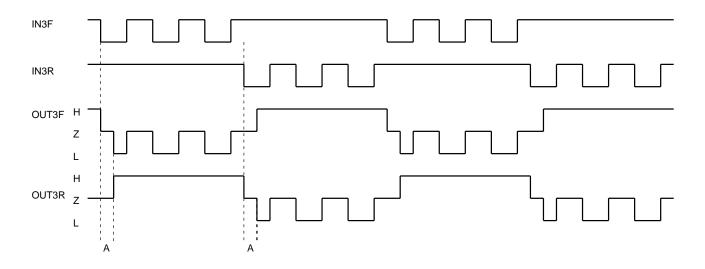
#### SLED block

MUTE	IN3, 4F	IN3, 4R	OUT3, 4F	OUT3, 4R
н	L	L	н	н
н	Н	L	Н	L
н	L	н	L	н
н	н	н	н	н
L	×	×	Z	Z

Z : open

Loading input is shared also by the SLED input pin (IN4F/IN4R pin).

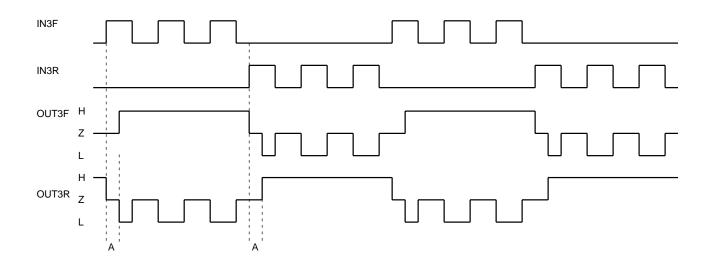
### SLED timing chart



SLED performs PWM on the lower side. In this case, the upper side of another phase is always ON. Only initial changeover contains the OFF section A (about  $1\mu s$ ) as a measure for through operation. OUT4F and R do the same operation.

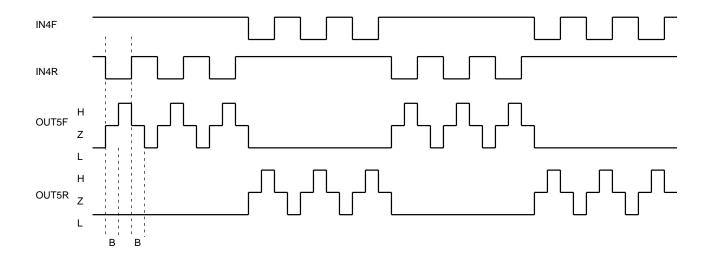
## LA6504H

SLED timing chart



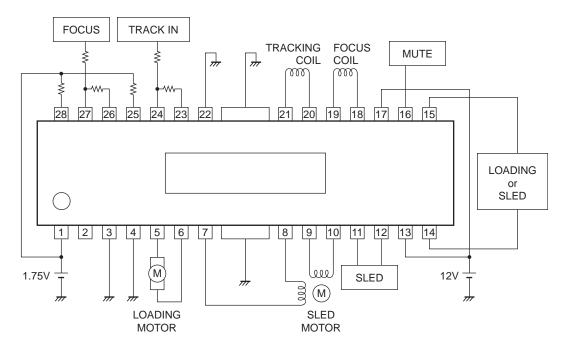
SLED performs PWM on the lower side. In this case, the upper side of another phase is always ON. Only initial changeover contains the OFF section A (about  $1\mu s$ ) as a measure for through operation. OUT4F and R do the same operation.

## SLED timing chart



LOADING contains the OFF section B (about  $1\mu s$ ) on both edges for changeover of the input. With the input at HH, the short braking occurs on the lower side.

## **Sample Application Circuit**



#### Cautions for use

1. GND

The center frame (FR) functions as a power system GND. Set it to the minimum potential together with S-GND. 2. Bypass capacitor

For power supply, connect the bypass capacitor immediately near the pin of this IC.

3. Lightening, ground fault, and short-circuit between outputs

Avoid short-circuit between the output pin and power supply (lightening), short-circuit between the output pin and GND (ground fault), and short-circuit between output pins (load short-circuit). When mounting IC to the substrate, pay attention to the direction of IC. Mounting in the wrong direction may cause damage to IC, and fuming in certain cases.

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