Microchip

27HC64

64K (8K x 8) High Speed CMOS UV Erasable PROM

FEATURES

- Bipolar Performance
  - — 40ns Maximum Access Time
- CMOS Technology For Low Power Consumption
  - — 80mA Active Current
  - — 100µA Standby Current (Low Power Option)
- OTP (One Time Programming) Available
- Auto-Insertion-Compatible Plastic Packages
- Auto ID™ Aids Automated Programming
- Separate Chip Enable and Output Enable Controls
- Two Programming Algorithms Allow Improved Programming Times
  - — Fast Programming
  - — Express
- Organized 8K x 8: JEDEC Standard Pinouts
  - — 28 Pin Dual in Line Package
  - — 32 Pin Chip Carrier (Leadless or Plastic)
- Available for Extended Temperature Ranges:
  - — Commercial: 0° C to 70° C
  - — Industrial: -40° C to 85° C
  - — Military**: -55° C to 125° C

DESCRIPTION

The Microchip Technology Inc 27HC64 is a CMOS 64K bit ultraviolet light Erasable (electrically) Programmable Read Only Memory. The device is organized as 8K words by 8 bits (8K bytes). An advanced CMOS design allows bipolar speed with a significant reduction in power over bipolar PROMs. A low power option (L) allows further standby power reduction to 100µA. The 27HC64 is configured in a standard 64K EPROM pinout, which allows an easy upgrade for 27C64 sockets. This very high speed device allows digital signal processors (DSP) or other sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

A complete family of packages is offered to provide the most flexibility in applications. One Time Programming (OTP) is available for low cost (plastic) applications.

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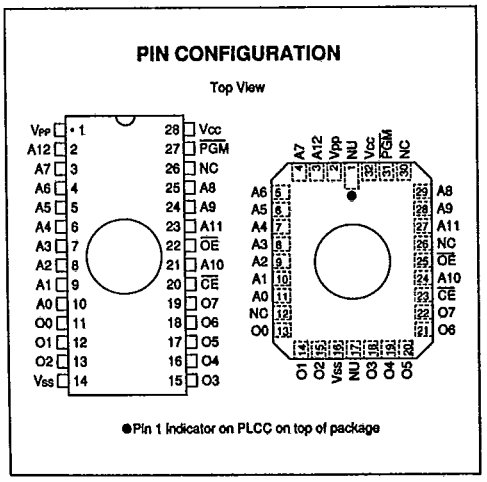

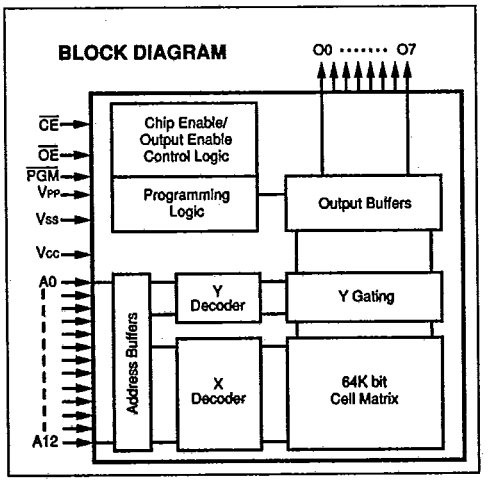

** See 27HC64 Military Data sheet DS60006

PIN FUNCTION TABLE	
Name	**Function**
A0 - A12	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

ELECTRICAL CHARACTERISTICS
Maximum Ratings*

VCC and input voltages w.r.t. VSS ... -0.6V to + 7.25V
VPP voltage w.r.t. VSS during programming ..... -0.6V to + 14V
Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V
Output voltage w.r.t. VSS ..... -0.6V to VCC +1.0V
Storage temperature ..... -65° C to 150° C
Ambient temp. with power applied -65° C to 125° C
ESD protection on all pins 2KV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = - 4mA IOL = 16mA
Leakage	all		ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all		CIN		6	pF	VIN = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT = 0V; Tamb = 25° C; f = 1MHz
Power Suppy Current, Active	S,L SX,LX	TTL input TTL input	ICC1 ICC2		80 90	mA mA	VCC = 5.5V; VPP = VCC f = 2MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0mA; VIL = -0.1 to 0.8 V; VIH = 2.0 to VCC; Note 1
Power Supply Current, Standby	S SX		ICC(S)1		40 50	mA mA	
Power Supply Current, Standby	L LX L, LX	TTL input TTL input CMOS input	ICC(S)2		2 3 100	mA mA µA	$\overline{CE}$ = VCC ±0.2V
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	 VCC-0.7	100 VCC	µA V	VPP = 5.5V Note 2

* Parts: S = Standard Power; L = Low Power; X = Industrial Temp Range;
Notes: (1) AC Power component above 2 MHz: 3mA/MHz for standard part; 5 mA/MHz for industrial temperature range part.
(2) VCC must be applied before (or simultaneously with VPP), and be removed after (or simultaneously with) VPP.

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 3.0V and V_{IL} = 0.0V; V_{OH} = V_{OL} = 1.5V
Output Load: 1 TTL Load + 30 pF
Input Rise and Fall Times: 5 nsec
Ambient Temperature: Commercial: Tamb = 0° C to 70° C
Industrial: Tamb = -40° C to 85° C

Parameter	Part*	Sym	27HC64-40		27HC64-45		27HC64-55		27HC64-70		Units	Conditions
			Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	all	t_{ACC}		40		45		55		70	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	L S	t_{CE1} t_{CE2}		40 30		45 30		55 35		70 45	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	all	t_{OE}		25		25		25		25	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	all	t_{OFF}	0	20	0	20	0	20	0	25	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	all	t_{OH}	0		0		0		0		ns	

* Parts: S = Standard Power; L = Low Power
** 27HC64-40 is only available in commercial temperature range

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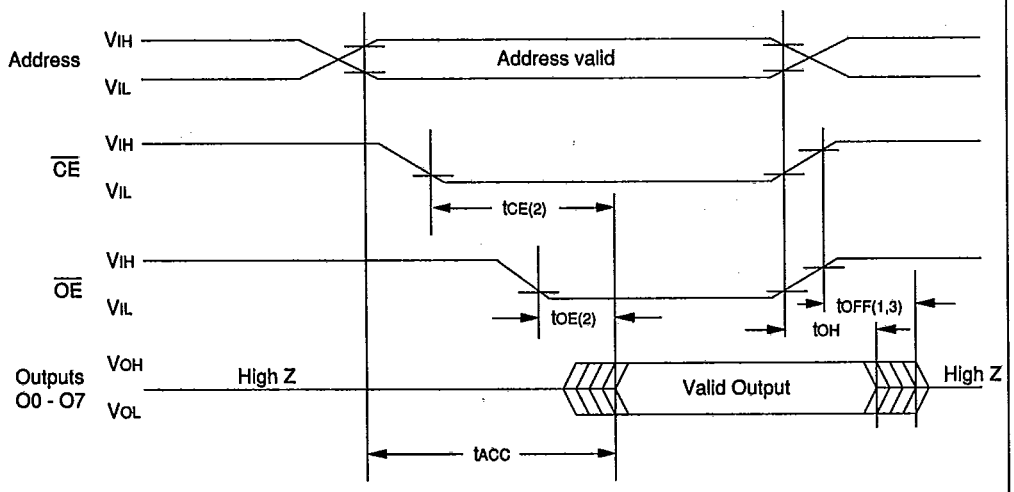
READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

PROGRAMMING DC Characteristics

Ambient Temperature: Tamb = 25° C ±5° C
For V_{PP} and V_{CC} Voltages refer to Programming Algorithms

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage		I_{LI}	-10	10	µA	V_{IN} = OV to V_{CC}
Output Voltages	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = - 4mA I_{OL} = 16mA
V_{CC} Current, program & verify		I_{CC}		80	mA	Note 1
V_{PP} Current,program		I_{PP}		40	mA	Note 1
A9 Product Identification		V_H	11.5	12.5	V	

Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

PROGRAMMING AC Characteristics

for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: V_{IH} = 2.4 V and V_{IL} = 0.45 V; V_{OH} = 2.0 V; V_{OL} = 0.8 V
Output Load: 1 TTL Load + 100 pF
Ambient Temperature: Tamb = 25° C ±5° C
For V_{PP} and V_{CC} Voltages, refer to Programming Algorithms

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	2		µs	
Data Set-Up Time	t_{DS}	2		µs	
Data Hold Time	t_{DH}	2		µs	
Address Hold Time	t_{AH}	0		µs	
Float Delay (3)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2		µs	
Program Pulse Width (1)	t_{PW}	0.95	1.05	ms	1 ms typical
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2		µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2		µs	
V_{PP} Set-Up Time	t_{VPS}	2		µs	
Overprogram Pulse Width (2)	t_{OPW}	2.85	78.75	ms	
Data Valid from $\overline{OE}$	t_{OE}		100	ns	

Notes: (1) For Express algorithm, initial programming width tolerance is 100 µsec ±5%. For fast programming algorithm, initial program pulse width tolerance is 1 msec ± 5%.
(2) For fast programming algorithm, the length of the overprogram pulse may vary from 2.85 to 78.75 msec as a function of the iteration counter value.
(3) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

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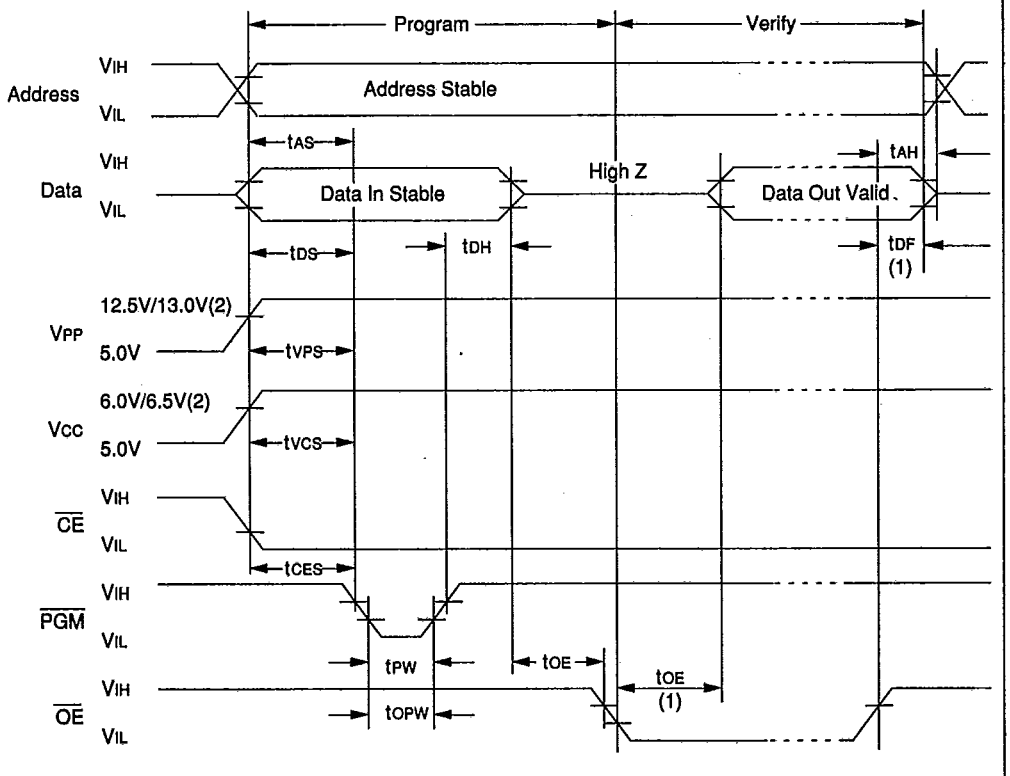
PROGRAMMING Waveforms



Notes: (1) tDF and tOE are characteristics of the device but must be accommodated by the programmer
(2) VCC = 6.0 V ±0.25 V, VPP = VH = 12.5 V ±0.25 V for fast programming algorithm
VCC = 6.5 V ±0.25 V, VPP = VH = 13.0V ±0.25 V for Express algorithm

MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VPP	A9	O0 - O7
Read	VIL	VIL	VIH	VCC	X	DOUT
Program	VIL	VIH	VIL	VH	X	DIN
Program Verify	VIL	VIL	VIH	VH	X	DOUT
Program Inhibit	VIH	X	X	VH	X	High Z
Standby	VIH	X	X	VCC	X	High Z
Output Disable	VIL	VIH	VIH	VCC	X	High Z
Identity	VIL	VIL	VIH	VCC	VH	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}$ pin is low to gate the data to the output pins.

For Read operations on the low powered version, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). A faster $\overline{CE}$ access time (tCE) is available on the standard part to provide the additional time for decoding of the $\overline{CE}$ signal. Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (V_{IH}).

When this condition is met, the supply current will drop from 80mA to 100µA on the low power part and to 40mA on the standard part.

Output Enable

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when

- The $\overline{OE}$ pin is high and a program is not defined.

Erase Mode

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all 1's state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm² is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm² for 20 minutes.

Programming Mode

Two programming algorithms are available. The fast programming algorithm is the industry-standard programming mode that requires both initial programming pulses and overprogramming pulses. A flowchart of the fast programming algorithm is shown in Figure 1.

The Express algorithm has been developed to improve on the programming throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the Express algorithm is shown in Figure 2.

Programming takes place when:

a) Vcc is brought to proper voltage,
b) V_{PP} is brought to proper V_H level,
c) the $\overline{CE}$ pin is low,
d) the $\overline{OE}$ pin is high, and
e) the $\overline{PGM}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A12 and the data to be programmed is presented to pins O0-O7. When data and address are stable, $\overline{OE}$ is high, $\overline{CE}$ is low and a low-going pulse on the $\overline{PGM}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) Vcc is at the proper level,
b) V_{PP} is at the proper V_H level,
c) the $\overline{CE}$ line is low,
d) the $\overline{PGM}$ line is high, and
e) the $\overline{OE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ need be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device in conjunction with the $\overline{PGM}$ line low, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on $\overline{CE}$ or $\overline{PGM}$); and the device is inhibited from programming.

Identity Mode

In this mode specific data is outputted which identifies the manufacturer as Microchip Technology Inc., and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	1	0	0	0	1	91

* Code subject to change.

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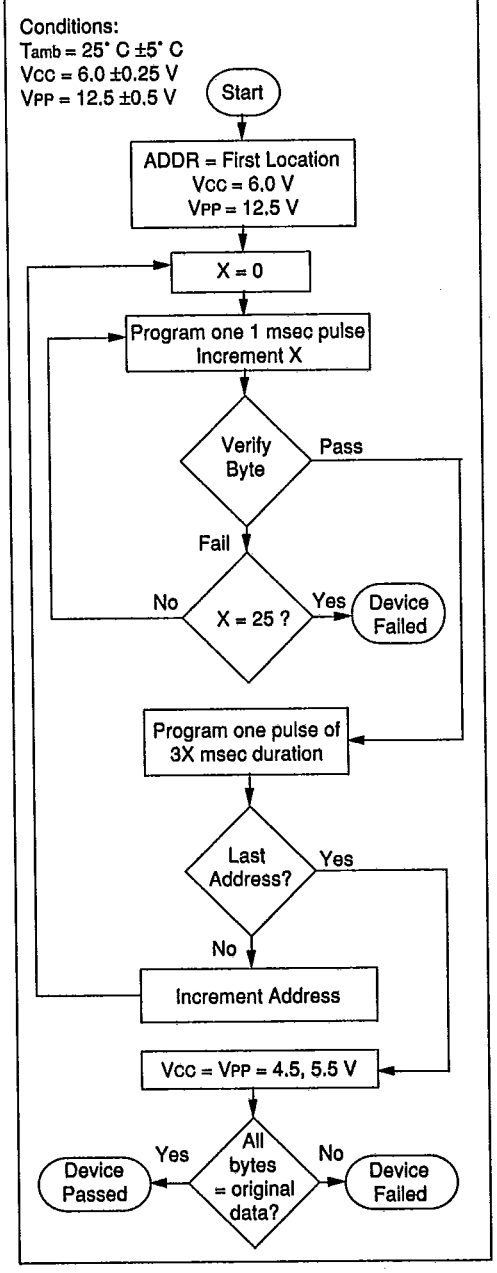
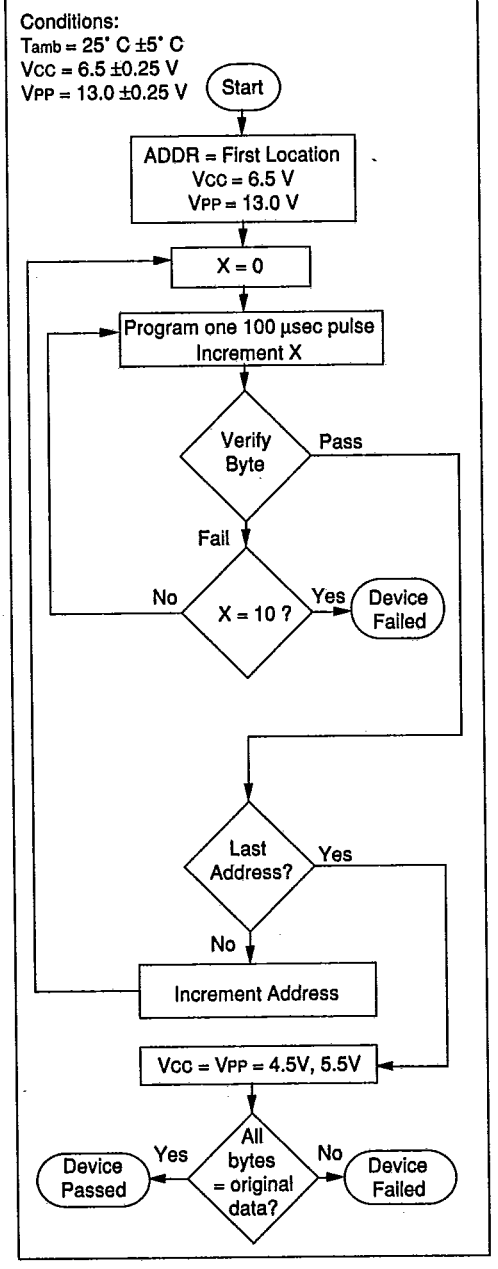
PROGRAMMING - Figure 1
Fast Algorithm



PROGRAMMING - Figure 2
Express Algorithm



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27HC64 - 45 I / K

Package:	J	Cerdip DIP
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier (OTP Available)
	P	Plastic DIP (OTP Available)
Temperature Range:	Blank	0° C to 70° C
	I	-40° C to 85° C
Access Time:	40	40 nsec
	45	45 nsec
	55	55 nsec
	70	70 nsec
Device:	27HC64	64K (8K x 8) High Speed CMOS EPROM
	27HC64L	64K (8K x 8) High Speed Low Power CMOS EPROM