FEATURES

- **Direct interface to CL-PS7111 low-power microcontroller**
  - — Custom multiplexed address/data bus for low pin count
  - — Supports 13- and 18-MHz operating frequencies
- **Fully compatible with PC Card (PCMCIA) Release 2.01 specification**
- **One or two CL-PS6700s per system**
- **Low power states**
  - — Operating (25 mW, typical)
  - — Idle
  - — Standby (virtually zero power drain)
- **Support for PC Card hot insertion and removal**
- **Read and write buffers**
- **Support for 3.3- and 5-V PC Cards**
- **Endian conversion**
- **Supports the following PC Cards:**
  - — Memory-only card; flash, EPROM, or SRAM
  - — I/O card; modem and communications
  - — Cards configured as both I/O and memory
  - — DMA-capable cards (through software emulation)
- **100-pin VQFP package**

Low-Power PC Card Controller for the CL-PS7111

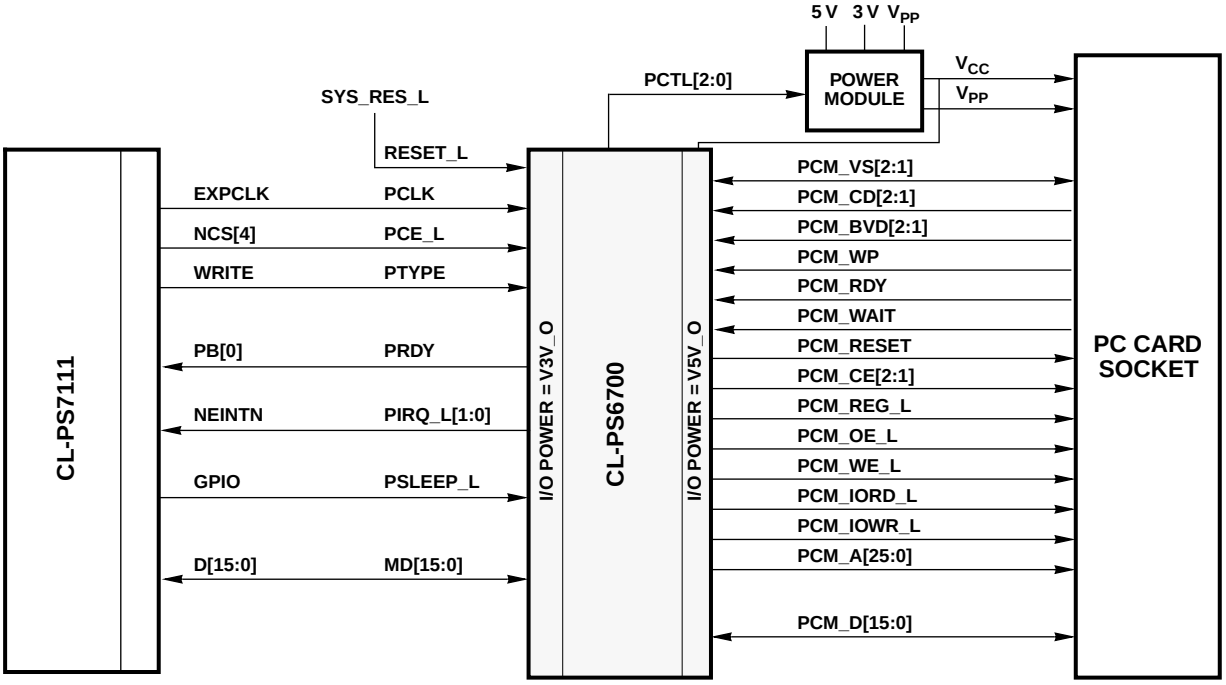
OVERVIEW

The CL-PS6700 connects directly to a PC Card (PCMCIA) Release 2.01 socket and has a custom interface to the CL-PS7111 microcontroller. The CL-PS7111 can support up to two CL-PS6700 devices, which allows up to two PC Card sockets per system. Addresses and data are passed to the CL-PS6700 through 16 bits of the 32-bit Data bus (D[15:0]).

The PC Card socket is effectively isolated by the CL-PS6700. Except for power and ground pins, the pins on the socket only connect to the rest of the system through the CL-PS6700.

(cont.)

CL-PS7111-to-CL-PS6700 Interface



OVERVIEW (cont.)

CL-PS7111-to-CL-PS6700 Interface

The PC Card interface requires a 26-bit address bus and a 16-bit data bus. The interface between the CL-PS6700 and CL-PS7111 consists of a 16-bit bus that carries the address and data information, and several control signals. This bus defines a two-clock address phase during which the 26-bit PC Card address and 6 control bits are transferred, and a one- or two-clock data phase during which one or four bytes of data are transferred. The data phase for reads can be deferred (for example, for a DMA access to the frame buffer of the CL-PS7111).

If a write transfer is indicated, write data appears in the third clock phase. If a word write is indicated, write data also appears in the fourth clock phase. For read transfers, the CL-PS6700 drives the bus with read data during the first one or two clocks of the data phase. This interface bus is also shared by other memory devices and up to one additional CL-PS6700 device.

The CL-PS7111 accesses the CL-PS6700 as a memory-mapped peripheral on the 16-bit memory bus. A Chip Enable signal (NCS[4]) from the CL-PS7111 selects one CL-PS6700 device for access to a particular PC Card socket. Another Chip Enable signal (NCS[5]) connects a second PC Card socket.

The CL-PS6700 implements the low-level interface to the PC Card socket and provides voltage translation for mixed-voltage systems. The CL-PS6700 also provides the data buffer and interrupt controls for the PC Card. Transfers between the two devices can be either one or four bytes.

The CL-PS6700 can be programmed to assemble/disassemble CL-PS7111 transfers to the width of the PC Card. The CL-PS6700 has read and write buffers that allow posting of both reads and writes. The read queue is single entry; the write FIFO can queue up to four CL-PS7111 transactions (up to 16 bytes).

Hot Insertion Support

The CL-PS6700 PC Card controller allows PC Cards to be inserted or removed while system power is on. The CL-PS7111 controller typically applies power to a PC Card socket after it has detected a properly inserted card. The device removes the power before the card is removed (that is, when the CPU detects that the card lock is deasserted). Since each card is isolated from the system by the associated CL-PS6700, insertion and removal of cards do not cause interference on the system buses.

Card Configuration and Access

After power-on or reset, a PC Card defaults to a memory-only card. The CL-PS7111 then reads the CIS of the card to determine the card type, access time, and so on, and configures the CL-PS6700 to access the card.

Each PC Card's V_{CC} and V_{PP} pins are individually controlled by its associated CL-PS6700. The CL-PS7111 controls the power to a card by writing to the CL-PS6700 registers. The CL-PS6700 ensures that its signals to the sockets are in the proper state before applying or removing power.

The CL-PS6700 device is available in an 100-pin VQFP package. The device can be used with both operating frequencies of the CL-PS7111 (13 and 18 MHz at 2.7 and 3.3 V).

TABLE OF CONTENTS

CONVENTIONS

This section presents conventions, abbreviations and acronyms, pin type abbreviations, and units of measure used in this data book.

Abbreviations and Acronyms

Acronym or Abbreviation	Definition
CIS	card information structure
CMOS	complementary metal-oxide semiconductor
CPU	central processing unit
DC	direct current
DMA	direct-memory access
EPROM	erasable/programmable read-only memory
FIFO	first in/first out
GPIO	general-purpose I/O
LSB	least-significant bit
MSB	most-significant bit
RAM	random-access memory
ROM	read-only memory
SRAM	static random-access memory
VQFP	very-tight-pitch quad flat pack

Pin Type Abbreviations

Abbreviation	Type
I	Input
O	Output
I/O	Input/output
OD-O	Open-drain output

Units of Measure

Symbol	Units of Measure
°C	degree Celsius
Hz	hertz (cycle per second)
Kbyte	kilobyte (1,024 bytes)
kΩ	kilohm
µA	microampere
µs	microsecond (1,000 nanoseconds)
Mbyte	megabyte (1,048,576 bytes)
MHz	megahertz (1,000 kilohertz)
mA	milliampere
ms	millisecond (1,000 microseconds)
mW	milliwatt
ns	nanosecond
V	volt
µW	microwatt

OTHER CONVENTIONS

Hexadecimal numbers are presented with all letters in uppercase and a lowercase *h* appended. For example, *14h* and *03CAh* are hexadecimal numbers.

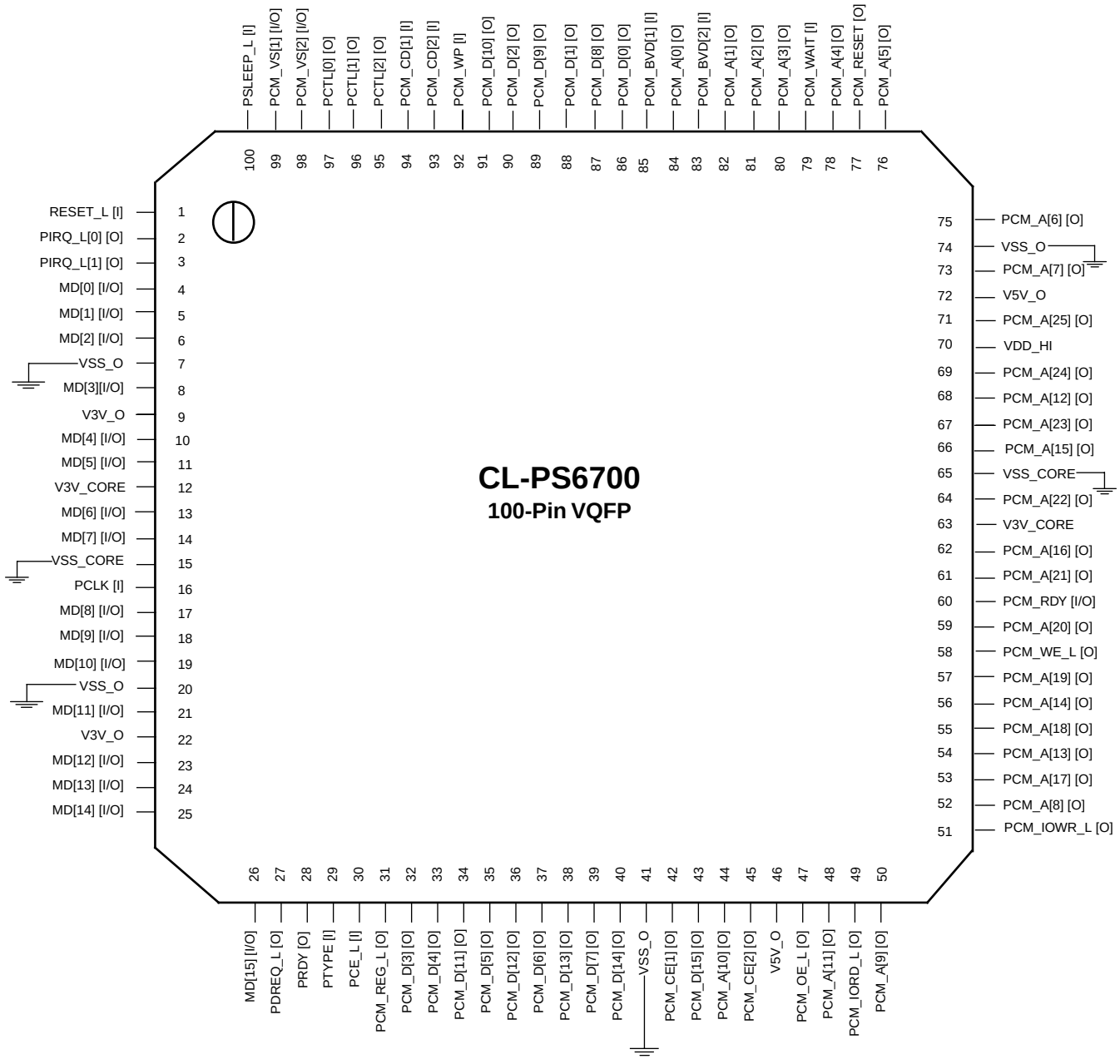
Binary numbers are enclosed in single quotation marks when in text. For example, *'11'* is a binary number.

Numbers not indicated by an *h* or single quotation marks are decimal.

The use of 'tbd' indicates values that are 'to be determined', 'n/a' designates 'not available', and 'n/c' indicates a pin that is a 'no connect'.

1. PIN INFORMATION

1.1 100-Pin VQFP Pin Diagram



1.2 Pin Listings

Table 1-1 lists the pins of the CL-PS6700 in alphabetical order. Table 1-2 lists the pins in numerical order.

Table 1-1. Alphabetical Listing

Signal Name	Pin No.	Type	Signal Name	Pin No.	Type	Signal Name	Pin No.	Type	Signal Name	Pin No.	Type
MD[0]	4	I/O	PCM_A[7]	73	O	PCM_D[0]	86	O	PCM_WE_L	58	O
MD[1]	5	I/O	PCM_A[8]	52	O	PCM_D[1]	88	O	PCM_WP	92	I
MD[2]	6	I/O	PCM_A[9]	50	O	PCM_D[2]	90	O	PCTL[0]	97	O
MD[3]	8	I/O	PCM_A[10]	44	O	PCM_D[3]	32	O	PCTL[1]	96	O
MD[4]	10	I/O	PCM_A[11]	48	O	PCM_D[4]	33	O	PCTL[2]	95	O
MD[5]	11	I/O	PCM_A[12]	68	O	PCM_D[5]	35	O	PDREQ_L	27	O
MD[6]	13	I/O	PCM_A[13]	54	O	PCM_D[6]	37	O	PIRQ_L[0]	2	O
MD[7]	14	I/O	PCM_A[14]	56	O	PCM_D[7]	39	O	PIRQ_L[1]	3	O
MD[8]	17	I/O	PCM_A[15]	66	O	PCM_D[8]	87	O	PRDY	28	O
MD[9]	18	I/O	PCM_A[16]	62	O	PCM_D[9]	89	O	PSLEEP_L	100	I
MD[10]	19	I/O	PCM_A[17]	53	O	PCM_D[10]	91	O	PTYPE	29	I
MD[11]	21	I/O	PCM_A[18]	55	O	PCM_D[11]	34	O	RESET_L	1	I
MD[12]	23	I/O	PCM_A[19]	57	O	PCM_D[12]	36	O	V3V_CORE	12	–
MD[13]	24	I/O	PCM_A[20]	59	O	PCM_D[13]	38	O	V3V_CORE	63	–
MD[14]	25	I/O	PCM_A[21]	61	O	PCM_D[14]	40	O	V3V_O	22	–
MD[15]	26	I/O	PCM_A[22]	64	O	PCM_D[15]	43	O	V3V_O	9	–
PCE_L	30	I	PCM_A[23]	67	O	PCM_IORD_L	49	O	V5V_O	46	–
PCLK	16	I	PCM_A[24]	69	O	PCM_IOWR_L	51	O	V5V_O	72	–
PCM_A[0]	84	O	PCM_A[25]	71	O	PCM_OE_L	47	O	VDD_HI	70	–
PCM_A[1]	82	O	PCM_BVD[1]	85	I	PCM_RDY	60	I/O	VSS_CORE	15	–
PCM_A[2]	81	O	PCM_BVD[2]	83	I	PCM_REG_L	31	O	VSS_CORE	65	–
PCM_A[3]	80	O	PCM_CD[1]	94	I	PCM_RESET	77	O	VSS_O	20	–
PCM_A[4]	78	O	PCM_CD[2]	93	I	PCM_VS[1]	99	I/O	VSS_O	41	–
PCM_A[5]	76	O	PCM_CE[1]	42	O	PCM_VS[2]	98	I/O	VSS_O	7	–
PCM_A[6]	75	O	PCM_CE[2]	45	O	PCM_WAIT	79	I	VSS_O	74	–

Table 1-2. Numerical Listing

Pin No.	Signal Name	Type	Pin No.	Signal Name	Type	Pin No.	Signal Name	Type	Pin No.	Signal Name	Type
1	RESET_L	I	26	MD[15]	I/O	51	PCM_IOWR_L	O	76	PCM_A[5]	O
2	PIRQ_L[0]	O	27	PDREQ_L	O	52	PCM_A[8]	O	77	PCM_RESET	O
3	PIRQ_L[1]	O	28	PRDY	O	53	PCM_A[17]	O	78	PCM_A[4]	O
4	MD[0]	I/O	29	PTYPE	I	54	PCM_A[13]	O	79	PCM_WAIT	I
5	MD[1]	I/O	30	PCE_L	I	55	PCM_A[18]	O	80	PCM_A[3]	O
6	MD[2]	I/O	31	PCM_REG_L	O	56	PCM_A[14]	O	81	PCM_A[2]	O
7	VSS_O	–	32	PCM_D[3]	O	57	PCM_A[19]	O	82	PCM_A[1]	O
8	MD[3]	I/O	33	PCM_D[4]	O	58	PCM_WE_L	O	83	PCM_BVD[2]	I
9	V3V_O	–	34	PCM_D[11]	O	59	PCM_A[20]	O	84	PCM_A[0]	O
10	MD[4]	I/O	35	PCM_D[5]	O	60	PCM_RDY	I/O	85	PCM_BVD[1]	I
11	MD[5]	I/O	36	PCM_D[12]	O	61	PCM_A[21]	O	86	PCM_D[0]	O
12	V3V_CORE	–	37	PCM_D[6]	O	62	PCM_A[16]	O	87	PCM_D[8]	O
13	MD[6]	I/O	38	PCM_D[13]	O	63	V3V_CORE	–	88	PCM_D[1]	O
14	MD[7]	I/O	39	PCM_D[7]	O	64	PCM_A[22]	O	89	PCM_D[9]	O
15	VSS_CORE	–	40	PCM_D[14]	O	65	VSS_CORE	–	90	PCM_D[2]	O
16	PCLK	I	41	VSS_O	–	66	PCM_A[15]	O	91	PCM_D[10]	O
17	MD[8]	I/O	42	PCM_CE[1]	O	67	PCM_A[23]	O	92	PCM_WP	I
18	MD[9]	I/O	43	PCM_D[15]	O	68	PCM_A[12]	O	93	PCM_CD[2]	I
19	MD[10]	I/O	44	PCM_A[10]	O	69	PCM_A[24]	O	94	PCM_CD[1]	I
20	VSS_O	–	45	PCM_CE[2]	O	70	VDD_HI	–	95	PCTL[2]	O
21	MD[11]	I/O	46	V5V_O	–	71	PCM_A[25]	O	96	PCTL[1]	O
22	V3V_O	–	47	PCM_OE_L	O	72	V5V_O	–	97	PCTL[0]	O
23	MD[12]	I/O	48	PCM_A[11]	O	73	PCM_A[7]	O	98	PCM_VS[2]	I/O
24	MD[13]	I/O	49	PCM_IORD_L	O	74	VSS_O	–	99	PCM_VS[1]	I/O
25	MD[14]	I/O	50	PCM_A[9]	O	75	PCM_A[6]	O	100	PSLEEP_L	I

2. PIN DESCRIPTIONS

2.1 CL-PS7111-to-CL-PS6700 Interface Signals

The conventions used for the power sources on the CL-PS7111-to-CL-PS6700 interface are listed in Table 2-1.

Table 2-1. Power Source Conventions[a]

Symbol	Power Source
sys	system
pcm	PCMCIA
VDDhi	VDDhi pin

[a] See Section 2.3 on page 17 for details on power and ground pins.

2.1.1 Address/Data Bus Signals

Signal	Type	Power Source	Description
MD[15:0]	I/O	sys	**Multiplexed address and data bus:** The MD bus carries address information during a two-clock address phase and data during a one- or two-clock data phase. **Address Phase:** A PC Card address is a 26-bit byte address. The MD bus carries the upper 10 address bits, plus control bits during the first clock of Chip Enable (PCE_L low), and the remaining (lower) 16 address bits during the second clock.

2.1.1 Address/Data Bus Signals *(cont.)*

Signal	Type	Power Source	Description
MD[15:0] *(cont.)*	I/O	sys	**Data Phase:** If a write transfer is indicated (during the address phase), write data appears in the third clock (also a word write, during the fourth clock) of Chip Enable. For register read transfers, a two-clock data phase follows the two clocks of address phase after a one clock bus turnaround cycle. For card reads, the data phase is deferred until card data has been collected as signaled by PRDY; the data phase is initiated by a second assertion of PCE_L, and the CL-PS6700 drives this bus with read data in the clock following the assertion of PCE_L (if a word read, during the second clock following PCE_L). The data phase of MD[15:0] carries the transfer size and space required for the data (see Table 2-2 and Table 2-3). SLOT[1:0] is a space reserved for future expansion.

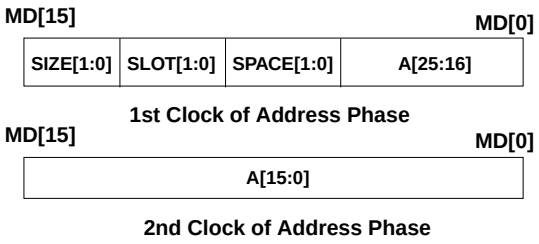


Table 2-2. Transfer Size

SIZE[1:0]	Number of bytes
00	1
11	4

Table 2-3. Area Accessed

SPACE[1:0]	Area Accessed
00	Attribute space
01	I/O space
10	Common memory
11	CL-PS6700 register space

2.1.2 Access Control Signals

Signal	Type	Power Source	Description
PCE_L	I	sys	**PC Card Chip Enable:** This signal, if asserted, enables the strobing of address and data information between the CL-PS7111 and the CL-PS6700 through the MD bus. For a read from PC Card memory or I/O space, the CL-PS7111 asserts PCE_L during the address phase and (possibly much later) during the data phase of a read transaction. Depending on the transaction, PCE_L is low for between two and five PCLK periods. When a read is pending, the CL-PS7111 waits for PRDY from the CL-PS6700 to complete the data phase. If the CL-PS6700 does not respond within a given time period, the CL-PS7111 times out and performs a dummy data phase by asserting PCE_L without receiving PRDY, causing the CL-PS6700 to abort the card read. If the CL-PS6700 times out card writes, it issues a WR_FAIL interrupt.
PTYPE	I	sys	**PC Card Transaction Type:** During the first clock of PCE_L, this signal indicates whether the operation is a write or a read. A low level indicates a write and a high level indicates a read. During the second clock of the address phase, this signal indicates if the transaction was initiated by the CPU or an optional DMA controller. A low level indicates the DMA controller, and a high level indicates the CPU. If initiated by the DMA controller and the address targets the card's I/O space, a properly configured CL-PS6700 performs a DMA transfer at the card. This feature is not supported by the CL-PS7111 and is for future use only.
PRDY	I/O	sys	**NOTE:** PRDY should be pulled up with a 100-kΩ resistor. **PC Card ready:** This signal goes to the CL-PS7111 and serves as both an address ready and data ready signal. It can also indicate a busy (card RDY/BUSY pin) status of the corresponding PC Card socket (see configuration bit "Include Card Ready in PRDY"). Normally, the CL-PS6700 leaves this signal asserted (high). When the CL-PS7111 targets a read or write transaction to the CL-PS6700, the CL-PS6700 deasserts PRDY in the second clock of the address phase until it has processed the transaction. For a **card write**, PRDY remains deasserted only if the write queue becomes full due to the current transaction. Otherwise, PRDY is reasserted during the next clock. When the CL-PS6700 write queue is full, PRDY is reasserted only after a queued write is disassembled (if necessary) and propagated to the PC Card socket, freeing an entry in the write queue. Therefore, the CL-PS7111 is assured that it does not get data wait states for card write operations. For a **card read**, the CL-PS6700 asserts PRDY when it has collected the required bytes from the PC Card. The CL-PS7111 then initiates the data phase by issuing a second PCE_L without driving the MD bus to the CL-PS6700(s). Then, the CL-PS6700 with a posted read responds with the read data. The CL-PS6700 registers can be read regardless of the state of PRDY. Therefore, PRDY cannot toggle during the address phase of register access if it is already deasserted. PRDY is a don't care input to the CL-PS7111 during the four (for write) or five (for read) clocks of register accesses.

Table 2-4. PTYPE Signal Encoding During PCE_L

PTYPE during Address Phase		MD Bus Transfer Type
Cycle 1 (RD/WR)	Cycle 2 (CPU/DMA)	
0	0	Write operation initiated by DMA controller.
0	1	Write operation initiated by CPU.
1	0	Read operation initiated by DMA controller.
1	1	Read operation initiated by CPU.

2.1.2 Access Control Signals *(cont.)*

Signal	Type	Power Source	Description
PDREQ_L/ GPIO	I/O	sys	**PC Card DMA Request:** When configured as PDREQ_L, this wire-OR'ed signal indicates to the CL-PS7111 that one of the PC Card sockets has issued a DMA request. Since this is shared by all PC Card sockets, the system should enable DMA to only one socket at a time and program the CL-PS7111 DMA routine. **General-Purpose I/O:** When configured as GPIO, this signal can be used as an input capable of generating an interrupt. As a general-purpose output, it is actively driven in both output states, high and low.

2.1.3 Interrupt and Abort Signals

Signal	Type	Power Source	Description
PIRQ_L[1:0]	OD-O	sys	**PC Card Interrupt Request:** The interrupt request lines can be wire-OR'ed if there are two CL-PS6700 controllers. It signals that one or two CL-PS6700s have an interrupt pending. The exact source of pending interrupts can be read in a CL-PS6700 Interrupt Source register. External pull-up resistors for these signals are required. Alternatively, every interrupt request line can be connected to one of the CL-PS7111 active-low interrupt inputs.

2.1.4 Clock, Reset, and Sleep Signals

Signal	Type	Power Source	Description
PCLK	I	sys	All transfers between the CL-PS7111 and the CL-PS6700 are synchronous to this clock signal. To conserve power, PCLK can be disabled when the PC Card subsystem is not in use.
RESET_L	I	sys	This reset signal can be driven by one of the GPIO outputs of the CL-PS7111 or by a system reset. It is an active-low input and places all CL-PS6700 registers and outputs in their default power-up/reset condition.
PSLEEP_L	I	sys	The CL-PS7111 drives this signal either by the RUN output or by any GPIO. This active-low signal is synchronous to the rising edge of PCLK. PSLEEP_L causes the CL-PS6700 to complete or abort (as configured) any card operation in progress, enter the lowest power mode, and disable its I/O according to the Table 4-2 on page 32. The CL-PS7111 can discontinue transactions to CL-PS6700 before asserting PSLEEP_L; if a card transaction in progress or in the queue is lost due to PSLEEP_L being asserted, an interrupt (RD_FAIL or WR_FAIL) is generated. There must be two PCLKs after PSLEEP_L is asserted to go into Standby mode.

2.2 PC Card Interface Signals

A PC Card socket can be configured as either *memory only* or *combined I/O-memory*. Some pins on the PC Card interface have different meanings in memory and I/O modes. These pins are listed as dual-mode. The mode is selected by a configuration register bit. When I/O mode is programmed, the CPU accesses either I/O space or memory space on the card according to the upper address bits. The CPU Attribute memory is accessible in either memory or I/O modes, again, selected by the upper address bits. A card DMA device is accessible only in I/O mode.

2.2.1 Address and Data Signals

Signal	Type	Power Source	Description
PCM_D[15:0]	I/O	pcm	**PC Card data bus:** Single-mode. Data transfer can be either byte or half-word (16-bit) as configured by the CPU. All byte accesses are transferred through their natural byte lane only (odd bytes on PCM_D[15:8] and even bytes on PCM_D[7:0]).
PCM_A[25:0]	O	pcm	**PC Card address bus:** Single-mode. This is a byte address during byte operations and a half-word address during half-word (16-bit) accesses (that is, A[0] is kept low).

2.2.2 Access Control Signals

Signal	Type	Power Source	Description
PCM_CE_L[2:1]	O	pcm	**Card enables:** Single-mode. These are the byte enable lines for the data bus. PCM_CE_L[1] enables even bytes, D[7:0], and PCM_CE_L[2] enables odd bytes, D[15:8].
PCM_OE_L	O	pcm	**Output enable for memory read data.** Single-mode. PCM_OE_L enables the card's data outputs. During a write operation, this signal is deasserted (high). During a card read DMA transfer, this signal is used as a terminal count and is asserted along with PCM_IORD_L during the last DMA card read.
PCM_WE_L	O	pcm	**Write enable signal for common memory and DMA:** Single-mode. During a card write DMA transfer, this signal is used as a terminal count and is asserted along with PCM_IOWR_L during the last DMA card write.

2.2.2 Access Control Signals *(cont.)*

Signal	Type	Power Source	Description
PCM_REG_L	O	pcm	Single-mode. This signal, in conjunction with the card data strobes, PCM_OE_L, PCM_WE_L, PCM_IORD_L, and PCM_IOWR_L, determine which of the three address spaces (I/O, common memory, or attribute memory) is chosen and if the transfer is a DMA or non-DMA type. 1 – common memory or DMA access 0 – I/O space or attribute memory space access
PCM_WP	I	pcm	Dual-mode. **Memory Mode:** This signal indicates that the card has been set to be write-protected. **I/O Mode:** This signal becomes IOIS16_L. An asserted level (low) indicates that the I/O card is a 16-bit device. If IOIS16_L is not asserted (high), the device is assumed to be 8-bit, and data transfer occurs over byte lane D[7:0]. In this mode, the WP status of the card is available as an on-card register bit. **DMA Mode:** This signal can be selected as DREQ from the PC Card.
PCM_WAIT_L	I	pcm	Single-mode. This data wait signal is used by the card to delay completion of an in-progress memory or I/O access cycle. It is sampled by the CL-PS6700 with a flip-flop clocked on the rising edge of PCLK, then fed to the card interface logic. In order to be recognized, this signal must be asserted at least two clocks before the end of the command strobe.
PCM_RDY	I	pcm	Dual-mode. **Memory Mode:** This signal is deasserted while the card is busy processing a previous transfer. It is intended to signal the completion of potentially lengthy operations within the card. This signal is available as a status bit for polling by the CPU, and can generate an interrupt to the CPU. It can also form the PRDY signal to the CL-PS7111 for handshake, preventing masters from targeting a busy card. **I/O Mode:** This signal is IREQ_L, an interrupt request generated by the I/O card. The RDY function of memory mode is available as an on-card register bit. **DMA Mode:** This input can be selected as DREQ from the PC Card.

Table 2-5. PC Card Access Types

Card Access Type	PCM_OE_L PCM_WE_L	PCM_IORD_L PCM_IOWR_L	PCM_REG_L
Common Memory Read/Write	Data strobe	Deasserted	Deasserted
Attribute Memory Read/Write	Data strobe	Deasserted	Asserted
Card I/O Read/Write	Deasserted	Data strobe	Asserted
Card DMA Read/Write	Terminal count	Data strobe	Deasserted

2.2.3 Additional Control for I/O Signals

Signal	Type	Power Source	Description
PCM_IORD_L PCM_IOWR_L	O	pcm	Single-mode. Dual-mode. **Memory Mode:** These signals remain deasserted. **I/O Mode:** These signals are asserted during read (PCM_IORD_L) and write transfer (PCM_IOWR_L) to the card I/O space or DMA devices. A PC Card does not respond to these signals unless it is configured for I/O by the system.

2.2.4 Card Detect and Battery Status Signals

Signal	Type	Power Source	Description
PCM_CD_L[2:1]	I	VDDhi	00 – Card inserted 01 – Card partially inserted 10 – Card partially inserted 11 – Card not inserted Single-mode. These pins indicate whether a card has been inserted into a socket. They are positioned at opposite ends of the connector to ensure valid detection of card insertion; a properly inserted card pulls both lines *low*. They are pulled up to VDDhi within the CL-PS6700 until a card is inserted (which pulls them low). These signals are available as status bits in a register, and any state change can also cause an interrupt informing the system that a card has been inserted or removed.
PCM_BVD[2:1]	I	pcm	Dual-mode. **Memory Mode:** These bits indicate the card battery condition as outlined in Table 2-6. **I/O Mode:** PCM_BVD[2] becomes SPKR_L, the Audio Digital Waveform signal, while PCM_BVD[1] becomes the STSCHG_L signal, a status line that indicates state changes of BVD, CD, and WP. The state of the BVD inputs can be read by the CPU in the CL-PS6700 Status registers and are also available on the PC Card registers.

Table 2-6. PC Card Battery Voltage Detect Encoding

PCM_BVD[2:1]	Battery Condition
X0	Battery dead
01	Battery low
11	Battery OK

2.2.5 Card Voltages and Reset Signals

Signal	Type	Power Source	Description
PCM_VS[2:1]	I/O	VDDhi	Single-mode. These signals inform the host system of the voltage requirements and capabilities of the card for reading its CIS before applying power to the card. This allows 3.3-V only cards (which need not support 5-V operation during configuration). VS[2] primarily differentiates between 3.3- and 5-V cards, while VS[1] primarily differentiates between 3.3-V and X.X-V cards. These signals, and the three power control signals, are bidirectional signals under software control (register bits) for flexibility. All five signals are capable of generating interrupts. VS[2] can also be configured to act as the card DREQ input.
PCTL[2:0]	I/O	VDDhi	Single-mode. These GPIO signals typically control the corresponding card's power module or switch. They determine the proper voltage for the V_{CC} and/or the V_{PP} pins of the socket. These signals are directly controlled by register bits and thus, can control serially-controlled power modules. They can also be programmed to transition to a new value automatically when the PSLEEP_L input is asserted to automatically shut down card power in case of power fault conditions. PCTL[2:0] are inputs during reset and therefore require an external pull-down or pull-up resistor to avoid power being applied to the card socket.
PCM_RESET	O	pcm	Single-mode. This signal resets the PC Card, placing it into its default memory-only mode. The signal remains in a high-impedance state after power-on or system reset. Cards that implement the reset function pull up this signal with >100 kΩ. The CPU (after >1 ms) should pull this signal low by writing a '0' to bit 12 of the Card Interface Configuration register.

2.3 Power and Ground Pins

Signal	Group	Description
V3V_Core	core	Power to core logic; either 5 V or 3.3 V.
V3V_O	sys	Power to system interface I/O buffers; either 5 V or 3.3 V, but must be the same as the CL-PS7111 power plane (V3V_Core).
V5V_O	pcm	Power to PC Card interface I/O buffers; either 5 V, 3.3 V, or 0 V.
VDD_HI	VDDhi	This pin should be tied to the highest voltage in the system (as seen by CL-PS6700; either 5 V or 3.3 V).
VSS_Core		Ground pins for the core and input buffers.
VSS_O		Ground pins for output buffers.

3. FUNCTIONAL DESCRIPTION

The CL-PS7111 communicates with the CL-PS6700 through the memory bus. This bus has a special multiplexed mode that uses 16 bits of the data bus to transfer address and data messages to the CL-PS6700. This split transaction bus supports posting a (single) read transaction so that the potentially long access time of a PC Card does not disrupt the memory bus. The protocol defines two clocks to transmit address messages, and one or two clocks for data messages. This allows efficient transfer of 32-bit words, as well as bytes and half words.

3.1 PC Card (PCMCIA) Interface

3.1.1 PC Card Types

The supported PC Card v2.01 card types are:

- Memory-only card, such as flash or SRAM
- I/O card, such as a modem card
- Multifunction cards with both I/O and memory
- DMA-capable cards

Each card can be 3.3 V or 5 V, and power to each card is managed independently by the CL-PS7111 and the corresponding CL-PS6700. General-purpose digital I/O (PCM_VS pins on the CL-PS6700) can be used by the CPU to detect the voltage requirements of a card before applying power.

3.1.2 PC Card Address/Data Bus

The PC Card supports a 26-bit address bus and a 16-bit data bus. The CL-PS7111 multiplexes these buses into a single 16-bit bus MD[15:0]. This bus is demultiplexed by the CL-PS6700, which also implements the low-level interface to the PC Card and provides voltage translation for mixed-voltage systems. The CL-PS6700 also provides data buffering, endian conversion, and interrupt control for the PC Card. Transfers between the CL-PS7111 and the CL-PS6700 are one or four bytes.

The CL-PS7111 accesses the CL-PS6700 as a memory-mapped peripheral on the memory bus. A chip enable signal, PCE_L of CL-PS6700, is connected to CS[4] (and CS[5] for a second PC Card socket) from the CL-PS7111.

3.1.3 PC Card Address Spaces and DMA

The PC Card standard defines three address spaces for PC Cards: memory space, I/O space, and attribute space. Each of these is 64 Mbytes, requiring 26 address bits, while other command bits select the space to be accessed.

Attribute memory space contains setup information such as the CIS. Attribute memory is accessed as an 8-bit device, but only at half-word boundaries (even bytes only).

Memory and I/O space for a card can each be 8 or 16 bits in width. The width of the access made to each of these spaces by the CL-PS6700 is software configurable. In addition, I/O space accesses can be sized dynamically by the PCM_WP (IOIS16_L) input.

All three address spaces for each card are mapped into the CL-PS7111 memory map and are directly accessible by the CPU. In addition to these three address spaces, a card can contain a DMA target. The

CL-PS7111 does not implement a DMA controller for the PC Card, but the CPU can emulate DMA cycles by appropriately configuring the CL-PS6700, then accessing card I/O space (see Table 4.4.2 on page 27). In this case, the CL-PS6700 accesses the card using a newly defined DMA cycle (IORD/WR strobes used with -REG high).

The PC Card standard requires all cards to follow the little-endian memory model. The CL-PS7111 can support both the little-endian and big-endian modes of operation. Thus, the CL-PS6700 provides for endian conversion, which is software configurable.

3.1.4 Byte Assembly/Disassembly and Queueing

Since all spaces on the cards (even I/O cards) are memory mapped, the CL-PS7111 can access the cards directly. The CL-PS6700 can be programmed to assemble/disassemble the CL-PS7111 transfers to the width of the PC Card. The CL-PS6700 has read and write buffers, allowing posting of both reads and writes. The read queue is single entry, and the write FIFO can queue up to four CL-PS7111 transactions (up to 16 bytes). Reads do not bypass queued writes (card transactions are processed in order).

Certain card access timing parameters are programmable and can be set to operate faster than the PC Card specification allows. The CL-PS6700 contains a watchdog timer that ensures that a card access is aborted if it exceeds a preprogrammed time limit, generating an interrupt to the CL-PS7111.

3.1.5 Card Configuration

After power-on or reset, a PC Card defaults to a memory-only card. The CPU then reads the card's CIS to determine the card type, access time, and so on, configuring the CL-PS6700 to properly access the card.

Each PC Card's V_{CC} and V_{PP} pins are individually controlled by its corresponding CL-PS6700 pins. The CL-PS7111 controls the power to a card by writing to the CL-PS6700 registers. The CL-PS6700 ensures that its signals to the sockets are in the proper state before applying and removing power to the sockets.

3.1.6 Hot Insertion Support

PC Cards are often used like floppies: The user can insert or remove cards while system power is on. Typically, the CPU only applies power to a PC Card socket after it has detected a properly inserted card and removes the power before the card is removed (that is, when the CPU detects that card lock is deasserted). Since each card is isolated from the system by its CL-PS6700, insertion and removal of cards should not cause glitches on the system buses.

3.2 Power States

3.2.1 Active State

The Active State is the normal operating state entered whenever PC Card accesses are required. In this state the PCLK input is active, the PSLEEP_L input is deasserted, and the Idle bit in the Power Management register is cleared.

3.2.2 Idle State

Normally, Idle State is entered/exited dynamically in hardware (by CL-PS6700 control logic) transparent to software. This method is invoked by setting the Enable Auto Idle Mode bit in the Power Management register, and appears identical to the Active State, except that some internal clocks are gated off between transactions to conserve power. The software can enter Idle State explicitly by setting the Idle mode. In this case, access to the CL-PS6700 registers is supported, but PC Card accesses do not propagate to the card and a read fail or write fail event can occur, which can generate an interrupt to the host.

3.2.3 Standby State

Standby State is the lowest power state in the system and is entered by asserting the PSLEEP_L input. At least two (rising) clock edges are required after PSLEEP_L is asserted before the PCLK is shut off. In the Standby State the CL-PS6700 core and system interface power can remain on, but consumes near zero power (microwatts). If card transactions are queued in the CL-PS6700 when PSLEEP_L is asserted, they are either aborted or continue until finished (requiring more than two clocks), depending on the setting of bit 9 (Standby Request During Card Access) in the Power Management register.

4. REGISTERS

The CL-PS6700 registers are spaced at 1-Kbyte boundaries and must be accessed by the CPU in word mode (not byte mode), even though they are all 16 bits or less in actual width. The upper 16 bits of register reads should be treated as undefined. The CL-PS6700 registers are accessible in all power states where the CL-PS6700 is powered and has a running PCLK (regardless of the state of PRDY). PC Card access should be done only when the CL-PS6700 is in Active mode.

Since register access circumvents the CL-PS6700 write queue, control of register bits, which can affect posted writes or prefetch reads such as applying and removing card power, should be done only after checking that the CL-PS6700 is idle using the Idle bit in the Interrupt Input Level register.

4.1 Register Addresses

The following address conventions are used in the register tables.

The tables show the offset from the base addresses. In a CL-PS7111 based system, the CL-PS6700 address spaces start with base addresses 0x4000_0000 for the first PC Card socket (that is, the one connected to NCS[4]), and 0x5000_0000 for the second CL-PS6700 (connected to NCS[5]). To calculate the address for any register, add the offset (for example, 0X0C00_2800 for the Power Management register) to the base (for example, 0x4000_0000 for the CL-PS6700 connected to NCS[4]) to get the address (0X4C00_2800).

Offset from Base Address	Description	Default	R/W
0X0C002800	Power Management register	0	R/W
0X0C002C00	Card Power Control register	0	R/W
0X0C002000	System Interface Configuration register	0x1F8	R/W
0X0C004000	DMA Control register	0	R/W
0X0C004400	Device Information register	0x0040	R/W
0X0C002400	Card Interface Configuration register	0	R/W
0X0C003000	Card Interface Timing register 0A	0x1F00	R/W
0X0C003400	Card Interface Timing register 0B	0	R/W
0X0C003800	Card Interface Timing register 1A	0x1F00	R/W
0X0C003C00	Card Interface Timing register 1B	0	R/W
0X0C000000	PC Card Interrupt Status register	0	R
0X0C000400	PC Card Interrupt Mask register	0	R/W
0X0C000800	PC Card Interrupt Clear register	XX	W
0X0C000C00	PC Card Interrupt Output Select register	0	W

Offset from Base Address	Description	Default	R/W
0X0C001000	PC Card Interrupt Reserved register 1	0	W
0X0C001400	PC Card Interrupt Reserved register 2	0	W
0X0C001800	PC Card Interrupt Reserved register 3	0	W
0X0C001C00	PC Card Interrupt Input Level register	Input Level	R

NOTE: The three Reserved Interrupt registers must be written with all ones (32'hFFFFFFFF) before interrupts can be captured and output to the PIRQ[1:0] pins.

4.2 Interrupt Structure

Interrupt sources in the CL-PS6700 include card inputs, GPIO pins (PCTL/PDREQ_L), and internal status signals. All interrupts in the CL-PS6700 are edge triggered. There are five register bits that control each interrupt, as shwon in Table 4-1.

The Interrupt Status register indicates which interrupt inputs have transitioned (rising edge or falling edge) since they were last cleared (using the Interrupt Clear register). The OR'ing of bits in the Interrupt Status register (bits not masked by the Mask register) generates an interrupt on either the PIRQ[0]_L or PIRQ[1]_L output as selected in the Interrupt Output Select register. A bit set to '1' in the Interrupt Output Select register routes the corresponding interrupt to PIRQ[1]. The Interrupt Input Level register reflects the current state of the raw interrupt sources (signals directly from the PC Card socket, GPIO pins, and internal status signals).

Table 4-1. Interrupt Register Set[a]

		Interrupt Sources														
Bit Position		**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Register Name	**R/W**	**RESERVED**	**RD_FAIL**	**WR_FAIL**	**IDLE**	**FIFO THLD**	**PCM_RDY_L**	**PCM_WP**	**PCTL [2:0]**	**PDREQ_L**	**PCM_VS2**	**PCM_VS1**	**PCM_CD2**	**PCM_CD1**	**PCM_BVD2**	**PCM_BVD1**
Interrupt Status	R	–	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Interrupt Mask	R/W	–	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Interrupt Clear	W	–	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Interrupt Output Select	R/W	–	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Interrupt Input Level	R	–	x	x	x	x	x	x	x	x	x	x	x	x	x	x

[a] x means available.
– means unavailable.

4.3 Power Management Registers

4.3.1 Power Management Register (0X0C002800)

Bit(s)	Description	Default	R/W
15:14	Reserved	00	R/W
13	**Disable Protection for PCM_BVD[1] Input During Card Power Off.** The input pull-up is controlled in the same way as other card inputs.	0	R/W
12	**Input Pull-Up Enable.** This bit applies to card inputs BVD[2], BVD[1], RDY, WAIT, WP. During CardOut or Standby, the pull-up resistors are disconnected and inputs are protected regardless of the state of this bit. 'Protected input' (PI) means the input can float without causing excessive current. CardOut means that the Card Detect inputs are high (no card inserted) or that the card power is off (Card Power Enable bit 5 is low and Monitor Card Power Enable bit 6 is high).	0	R/W
11:10	**Card Detect.** Weak internal pull-up resistor. 00 – Pull-up is off and Card Detect inputs are not protected. This assumes that there are external pull-up resistors. 01 – Pull-up is off and Card Detect inputs are protected. 10 – Weak pull-up, except when in Standby mode. 11 – Weak pull-up always on. This allows Card Detect during Standby.	00	R/W
9	**Standby Request During Card Access.** This bit controls pending card accesses when entering Standby mode. 0 – Abort any card access when entering Standby mode. 1 – Complete pending card access, then halt.	0	R/W
8	**Standby Disable.** When this bit is set, the PSLEEP_L input is effectively disabled.	0	R/W
7	**PDREQ_L Select.** If this bit is set, the PDREQ_L pin is a GPIO pin.	0	R/W
6	**Monitor Card Power Enable** (Bit 5). 0 – Card power is assumed to be always on. 1 – Enable monitoring of power. This bit has no effect on card power or the CL-PS6700 power modes such as Standby and Idle.	0	R/W
5	**Card Power Enable.** 0 – Outputs state of bits [5:3] of Card Power Control register to the PCTL[2:0] pins. 1 – Outputs state of bits [2:0] of Card Power Control register to the PCTL[2:0] pins. If card access is attempted with this bit clear, a RD_FAIL or WR_FAIL interrupt can be generated.	0	R/W
4	**Auto Disable Card Access on Card Removal.** If this bit is set, the Card Enable bit (bit 10 in the Card Interface Configuration register) is cleared when the card is removed.	0	R/W
3	**Auto Power Down Card on Card Removal.** If this bit is set, the Card Power Enable bit (bit 5) is cleared when the card is removed.	0	R/W
2	**Auto Power Down Card on Standby.** If this bit is set, the Card Power Enable bit (bit 5) is cleared when Standby mode is entered.	0	R/W
1	**Idle.** When this bit is set, it forces the CL-PS6700 into Low Power mode. Most internal clocks are stopped with the exception of register access. Idle mode has no affect on I/O pads or card power control.	0	R/W
0	**Enable Auto Idle Mode.** When this bit is set, some internal clocks are stopped whenever the CL-PS6700 is idle.	0	R/W

4.3.2 Card Power Control Register (0X0C002C00)

Bit(s)	Description	Default	R/W
15:14	**VS[2:1] Direction.** 0 – Input 1 – Output Input pull–up resistors are weak. During Standby mode the pull–up resistors are disabled.	00	R/W
13:12	**VS[2:1] Output Value.**	00	R/W
11	**GPIO Direction.** See Note. 0 – Input 1 – Output	0	R/W
10	**GPIO Output Value When Card Power Enable Bit is Low.** See Note.	0	R/W
9	**GPIO Output Value When Card Power Enable Bit is High.** See Note.	0	R/W
8:6	**PCTL[2:0] Direction.** 0 – Input 1 – Output	00	R/W
5:3	**PCTL[2:0] Output Value When Card Power Enable Bit is Low.** PCTL[0] is a tristate output only. PCTL[2:1] are bidirectional. The PCTL[2:1] input value is at the Interrupt Pins register and can generate an interrupt while PCTL[0] cannot generate an interrupt.	000	R/W
2:0	**PCTL[2:0] Output Value When Card Power Enable Bit is High.**	000	R/W

NOTE: If Power Management register bit 7 is cleared, then this bit is a don't care.

4.4 System Interface Registers

4.4.1 System Interface Configuration Register (0X0C002000)

Bit(s)	Description	Default	R/W
15:10	Reserved	–	–
9	**Enable Active Pull-up on Open-Drain Interrupt Outputs PIRQ_L[1:0].** During Standby, active pull-up is disabled.	0	R/W
8	**Enable Assembly and Disassembly.** If this bit is set, assembly and disassembly of card accesses by CPU or DMA is allowed. When this bit is cleared, the card transaction size is limited to the width of the card defined by the Card Interface Configuration register bit 7.	1	R/W
7	**Enable Handshake Using Card Ready Signal.** When this bit is set, a low-level on PCM_RDY prevents access to the card. When this bit is cleared, RDY is ignored, but can still generate interrupts.	1	R/W
6	**Report Read Failure.** When this bit is set, a read failure generates an RD_FAIL interrupt. Read failure can occur due to a time-out condition. Normally, this bit should be cleared so the CL-PS7111 reports read failures.	1	R/W
5	**Endian Conversion Enable.** 0 – Disable byte swapping 1 – Enable byte swapping PC Cards are defined as little–endian, while the ARM CPU inside the CL-PS7111 can be big–endian or little–endian.	1	R/W
4	**Transaction Queue Enable.** When this bit is set, it enables queuing one or more CL-PS7111 write operations. If this bit is cleared, then PRDY goes low after a write until the write is complete.	1	R/W
3	**Transaction Queue Threshold Control.** 0 – FIFO THLD interrupt when two entries are free in queue. 1 – FIFO THLD interrupt when four entries are free in queue.	1	R/W
2	**Transaction Queue Flush.** Discard data in queue.	0	R/W
1:0	Reserved	00	R/W

4.4.2 DMA Control Register (0X0C004000)

Bit(s)	Description	Default	R/W
15:9	Reserved	–	–
8	**Enable Handshake with CL-PS7111 Using PDREQ_L.** If this bit is cleared, then PDREQ_L is always deasserted. If Power Management register bit 7 is set, then this bit is a *don't care*.	0	R/W
7	**Card DMA Enable.** Enables card DMA transfer. A DMA transfer is defined by REG_L deasserted and IORD_L or IOWR_L asserted. OE_L and WE_L indicate the terminal count for read and write, respectively.	0	R/W
6:4	**DMA Request Input Select.** Selects input to be used for DMA handshake between the CL-PS6700 and the card. Currently, there is no dedicated card pin assigned for DMA request. 000 – Disable DMA access 001 – PCTL[2] 010 – PCM_VS[2] 011 – Reserved 101 – PCM_WP input 110 – PCM_BVD2 111 – Card always requesting DMA transfer (no handshake between CL-PS6700 and card). After each DMA transfer from CL-PS7111 to CL-PS6700, PDREQ_L is immediately reasserted.	000	R/W
3	**DMA Request Polarity Select.** If this bit is set, the selected DMA request input (as described above) is inverted to be active-low.	0	R/W
2	**Transparent DMA Request.** If this bit is set, then external DMA request input is passed through to the PDREQ_L output after being synchronized to PCLK.	0	R/W
1	**CPU Initiated DMA.** This allows the CPU to generate a card DMA transfer. If this bit is set, a CPU access to I/O space is converted to a DMA transfer. REG_L is kept high (deasserted), and IORD_L or IOWR_L is used to transfer data.	0	R/W
0	**CPU Initiated DMA with Terminal Count.** If this bit is set, a CPU access to I/O space is converted to a DMA transfer. REG_L is kept high (deasserted). The end of DMA is indicated to the card by OE_L low (read) or WE_L low (write). IORD_L or IOWR_L are used to transfer data.	0	R/W

4.4.3 Device Information Register (0X0C004400)

Bit(s)	Description	Default	R/W
7:6	**Chip ID**	01	R
5	**Dual/Single Socket.** Single-socket device if low.	0	R
4:2	**Revision Level.** This changes as new revisions become available.	00	R
1:0	Reserved	00	R

4.5 Card Interface Registers

4.5.1 Card Interface Configuration Register (0X0C002400)

Bit(s)	Description	Default	R/W
15:13	Reserved	0	–
12	**Card Reset.** 0 – The PCM_RESET output is deasserted (low). 1 – The PCM_RESET output is asserted (high).	0	R/W
11	**Card Reset Output Enable.** If this bit is set, PCM_RESET is driven with the value of bit 12. If this bit is cleared, the output is tristated.	0	R/W
10	**Card Enable.** This bit must be set for the CL-PS6700 to make a card access. If a card access is attempted by the CL-PS7111 while this bit is cleared, a read time–out or WR_FAIL interrupt occurs.	0	R/W
9	**Card Write Protect.** If this bit is set, a card is write–protected in memory and I/O mode. The card Write Protect signal protects the card only in Memory mode.	0	R/W
8	**Memory or I/O Mode Select.** 0 – Card in memory mode. 1 – Card in I/O mode. Write Protect becomes IOIS16. Other Dual mode inputs are not interpreted by the CL-PS6700, and remain register bits that can generate interrupts. **CAUTION:** This bit must be set when interfacing to the CL–PS7111 when addressing I/O space; otherwise the system may hang.	0	R/W
7	**Card Access Width.** If this bit is set, the card width for memory and I/O access is 16 bits. If the Auto Size bit is set, then I/O access width is determined by IOIS16_L rather than this bit.	0	R/W
6	**Auto Size I/O Accesses.** 0 – I/O access width on the PC Card bus is determined by the Card Access Width bit. 1 – Dynamic bus sizing is enabled. If IOIS16_L is asserted, the data width is 16 bits; otherwise, it is 8 bits.	0	R/W
5	**Timer Select for Memory Space Write.** 0 – Select timer 0 (0A and 0B) 1 – Select timer 1 (1A and 1B)	0	R/W
4	**Timer Select for Memory Space Read.** 0 – Select timer 0 1 – Select timer 1	0	R/W
3	**Timer Select for I/O Space Write.** 0 – Select timer 0 1 – Select timer 1	0	R/W
2	**Timer Select for I/O Space Read.** 0 – Select timer 0 1 – Select timer 1	0	R/W
1	**Timer Select for Attribute Space Write.** 0 – Select timer 0 1 – Select timer 1	0	R/W
0	**Timer Select for Attribute Space Read.** 0 – Select timer 0 1 – Select timer 1	0	R/W

4.5.2 Card Interface Timing Register 0A (0X0C003000)

Bit(s)	Description	Default	R/W
15:14	**Prescaler Field for Watchdog Timer.** 00 – Divide by 1 01 – Divide by 16 10 – Divide by 256 11 – Divide by 8192	00	R/W
13:8	**Count Field for Watchdog Timer.** Settings of 00 to 3Fh correspond to values between 1 and 64 times the prescale value. The period starts at the end of the command width period and continues as long as PCM_WAIT_L is low. If terminal count is reached, an interrupt can be generated.	1Fh	R/W
7:6	**Prescaler Field for Command Strobe Width.** 00 – Divide by 1 01 – Divide by 16 10 – Divide by 256 11 – Divide by 8192	00	R/W
5:0	**Count Field for Command Strobe Width.** This field has values between 1 and 64. The command width equals: $t_{CMD} = t_{PCLK} \times ([Prescale \times Count] + 2)$	00h	R/W

4.5.3 Card Interface Timing Register 0B (0X0C003400)

Bit(s)	Description	Default	R/W
15:14	**Prescaler Field for Address and Data Hold Time.** 00 – Divide by 1 01 – Divide by 16 10 – Divide by 256 11 – Divide by 8192	00	R/W
13:8	**Count Field for Hold Period.** Settings of 00 to 3Fh correspond to 1 to 64 times the prescale value. The period starts at the end of the command strobe. The hold time equals: $t_{Hold} = t_{PCLK} \times ([Prescale \times Count] + 1) + constant$	00h	R/W
7:6	**Prescaler Field for Address and Data Setup Time.** 00 – Divide by 1 01 – Divide by 16 10 – Divide by 256 11 – Divide by 8192	0	R/W
5:0	**Count Field for Address and Data Setup Time.** Settings of 00 to 3Fh correspond to 1 to 64 times the prescale value. The period starts at valid address and ends when the command strobe is active. The setup time equals: $t_{setup} = t_{PCLK} \times ([Prescale \times Count] + 1) - constant$	0	R/W

4.5.4 Card Interface Timing Register 1A (0X0C003800)

Bit(s)	Description	Default	R/W
15:14	**Prescaler Field for Watchdog Timer.** 00 – Divide by 1 01 – Divide by 16 10 – Divide by 256 11 – Divide by 8192	00	R/W
13:8	**Count Field for Watchdog Timer.** Settings of 00 to 3Fh correspond to values between 1 and 64 times the prescale value. The period starts at the end of the command width period and continues as long as PCM_WAIT_L is low. If terminal count is reached, an interrupt can be generated.	1Fh	R/W
7:6	**Prescaler Field for Command Strobe Width.** 00 – Divide by 1 01 – Divide by 16 10 – Divide by 256 11 – Divide by 8192	00	R/W
5:0	**Count Field for Command Strobe Width.** This field has values between 1 and 64. The command width equals: $t_{CMD} = t_{PCLK} \times ([Prescale \times Count] + 2)$	00h	R/W

4.5.5 Card Interface Timing Register 1B (0X0C003C00)

Bit(s)	Description	Default	R/W
15:14	**Prescaler Field for Address and Data Hold Time.** 00 – Divide by 1 01 – Divide by 16 10 – Divide by 256 11 – Divide by 8192	00	R/W
13:8	**Count Field for Hold Period.** Settings of 00 to 3Fh correspond to 1 to 64 times the prescale value. The period starts at the end of the command strobe. The hold time equals: $t_{Hold} = t_{PCLK} \times ([Prescale \times Count] + 1) + constant$	00h	R/W
7:6	**Prescaler Field for Address and Data Setup Time.** 00 – Divide by 1 01 – Divide by 16 10 – Divide by 256 11 – Divide by 8192	00	R/W
5:0	**Count Field for Address and Data Setup Time.** Settings of 00 to 3Fh correspond to 1 to 64 times the prescale value. The period starts at valid address and ends when command strobe is active. The setup time equals: $t_{Setup} = t_{PCLK} \times ([Prescale \times Count] + 1) - constant$	00h	R/W

4.6 I/O Properties

Table 4-2 on page 32 summarizes the CL-PS6700 signals.

Conventions for Table 4-2

Acronym	Definition
Assert	
H	Voltage high
L	Voltage low
Type	
O	Output
I	Input
I/O	Bidirectional signal
Power Group	
sys	System
pcm	PCMCIA
VDDhi	VDD_HI pin
Synchronous Signal [a]	
S	Synchronous signal
A	Asynchronous signal
Resistor	
PU	Pull-up resistor
PD	Pull-down resistor
Reset, Standby, Card Power Off, Idle [b]	
T	Output in high-impedance
A	Normally operating output; can be high, low, or high-impedance.
PO	The state of an output during the deep Standby state is programmable, either low or high.
PI	Protected input; that is, the internal input buffer is de-coupled from the pin.
N	Normally operating input

[a] Synchronous signal indicates whether a signal is synchronous to PCLK.

[b] These indicate the state of each output signal or the input pin during various states of the device.

For Reset, Table 4-2 on page 32 indicates the state of each signal when RESET_L is asserted and power stabilizes.

Table 4-2. CL-PS6700 I/O Properties

Signal	Alternate Name	Assert	Type	Power Group	SYN	Resistor	Reset	Standby	Card Power Off	Idle[a]	Load pF
CL-PS7111 Interface: Multiplexed Address/Data Bus and Control											
PCLK		H	I	sys	S	none	N	N	N	N	10
RESET_L		L	I	sys	A	none	N	N	N	N	10
PSLEEP_L		L	I	sys	A	none	N	N	N	N	10
PCE_L		L	I	sys	S	none	N	N	N	N	10
PTYPE		H	I	sys	S	none	N	N	N	N	10
PRDY	INIT	H	O	sys	S	none	T	A	A	A	25
			I	sys	S	none	N	N	N	N	10
PDREQ_L		L	O	sys	S	none	T	PO	A	A	50
			I	sys	S	prog. PU	N	N	N	N	10
PIRQ_L[0]		L	O	sys	A	none	T	A	A	A	50
PIRQ_L[1]		L	O	sys	A	none	T	A	A	A	50
MD[15:0]		H	O	sys	S	none	T	A	A	A	70
			I	sys	S	none	N	N	N	N	10
PC Card Interface											
PCM_WP		H	I	pcm	A	prog. PU	PI	N	PI	N	10
PCM_BVD[2:1]		H	I	pcm	A	prog. PU	PI	N	PI[b]	N	10
PCM_RDY		H	I	pcm	A	prog. PU	PI	N	PI	N	10
PCM_WAIT_L		L	I	pcm	A	prog. PU	PI	N	PI	N	10
PCM_CE_L[2:1]		L	O	pcm	A	none	T	A	T	A	50
PCM_REG_L		L	O	pcm	S	none	T	A	T	A	50
PCM_OE_L		L	O	pcm	S	none	T	A	T	A	50
PCM_WE_L		L	O	pcm	S	none	T	A	T	A	50
PCM_IORD_L		L	O	pcm	S	none	T	A	T	A	50
PCM_IOWR_L		L	O	pcm	S	none	T	A	T	A	50
PCM_RESET		L	O	pcm	S	none	T	A	T	A	50
PCM_A[25:0]		H	O	pcm	S	none	T	A	T	A	100
PCM_D[15:0]		H	O	pcm	S	none	T	A	T	A	50
			I	pcm	A	none	PI	PI	PI	PI	10
PCM_CD_L[2:1]		Prog.	I	VDDhi	S	prog. PU	PI	prog. PI	N	N	50
PCM_VS[2:1]		Prog.	O	VDDhi	S	none	T	A	T	A	50
			I	VDDhi	A	prog. PU	PI	N	PI	N	10
PCTL[2:0]		Prog.	O	VDDhi	S	none	T	PO	A	A	50
			I	VDDhi	A	prog. PU	N	N	N	N	10

[a] The Idle mode is entered and exited by writing the register bit *Idle*. In Idle mode most internal clocks are gated off, and only the CL-PS6700 register access is supported. All CL-PS6700 inputs and outputs function normally.

[b] The PCM_BVD[1] input protection can be disabled during Card power-off.

5. ELECTRICAL SPECIFICATIONS

Table 5-1. Absolute Maximum Ratings

Description	Absolute Maximum Rating
Ambient temperature under bias	0^oC to 70^oC
Storage temperature	-65^oC to 150^oC
Voltage on any pin with respect to ground	–0.3 to V_{CC} + 0.5 V
Operating power dissipation	100 mW
Standby state power dissipation	10 µW
Power supply voltage	7 V
Injection current (latch up)	25 mA

NOTE: Stressing the device above those listed in Absolute Maximum Ratings may cause permanent damage to the component. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 5-2. DC Specifications

Symbol	Parameter	MIN	Typical	MAX	Unit	Conditions
$V_{CC}5V$	Power supply voltage			5.5	V	Normal operation
$V_{CC}3V$	Power supply voltage	3.0		3.6	V	Normal operation[a]
V_{ILC}	Input low voltage CMOS			0.2 V_{CC}	V	Normal operation
V_{IHC}	Input high voltage CMOS	0.7 V_{CC}			V	Normal operation
I_{OL6}	Output low current – 2mA type			2	mA	Normal operation: $V_{CC}3V$ = MIN
I_{OL12}	Output low current – 8mA type			8	mA	Normal operation: $V_{CC}3V$ = MIN
IOH6	Output high current – 2mA type			–1	mA	Normal operation: $V_{CC}3V$ = MIN
IOH12	Output high current – 8mA type			–4	mA	Normal operation: $V_{CC}3V$ = MIN
VOL	Output low voltage			0.5	V	Normal operation: at rated I_{OL}
V_{OH}	Output high voltage	V_{CC} – 0.5			V	Normal operation: at rated I_{OH}
I_L	Input leakage	–10		10	µA	Normal operation: $0 < V_{IN} < V_{CC}$
I_{LPD}	Input leakage – power down type	–1		1	µA	Pad power-down active
I_{PU}	Internal pull-up current	–30		–300	µA	Normal operation
C_{IN}	Input capacitance			10	pF	Normal operation
C_{OUT}	Output capacitance			10	pF	Normal operation
I_{CCtot1}	Power supply current, Active mode – V3V_CORE		15	<25	mA	$V_{CC}3V$ = 3.3 V, PCLK = 18 MHz
I_{CCtot2}	Power supply current, Idle mode – V3V_CORE		3	<6	mA	$V_{CC}3V$ = 3.3 V, PCLK = DC[b]
I_{CCtot4}	Power supply current, Active mode – V3V_O		YMMV[c]		mA	$V_{CC}3V$ = 3.3 V, PCLK = 18 MHz
I_{CCtot5}	Power supply current, Idle mode – V3V_O			<20	µA	$V_{CC}3V$ = 3.3 V, PCLK = DC
I_{CCtot6}	Power supply current, Standby mode – V3V_O			<20	µA	$V_{CC}3V$ = Lithium backup V PCLK = DC (stopped)
I_{CCtot7}	Power supply current, operating (Run) – V5V_O		YMMV[c]		mA	$V_{CC}5V$ = 5.0 V, PCLK = 18 MHz
I_{CCtot8}	Power supply current, Idle mode – V5V_O			<20	µA	$V_{CC}5V$ = 5.0 V, PCLK = DC
I_{CCtot9}	Power supply current, Standby mode – V5V_O			0	µA	$V_{CC}5V$ = 0 V PCLK = DC
$I_{CCtot10}$	Power supply current, Active mode – V3V_CORE		20	<35	mA	$V_{CC}3V$ = 5.0 V, PCL = 18 MHz
$I_{CCtot11}$	Power supply current, Suspend (Idle) – V3V_CORE		6	<12	mA	$V_{CC}3V$ = 5.0 V, PCLK = DC
$I_{CCtot13}$	Power supply current, suspend (Idle) – V3V_O			<20	µA	$V_{CC}3V$ = 5.0 V, PCLK = DC

[a] Can be run at 4.5 to 5.5 V for higher performance, but at a cost of increased power consumption (tbd).

[b] As low as 2.7 V.

[c] This is system-design dependent, since it supplies power to the pads only.

5.1 Bus Timing — System Bus

Table 5-3. System Bus Timing Parameters

Symbol	Parameter	MIN	MAX	Unit
t_{1a}	PCE_L input setup	12		ns
t_{1b}	PCE_L input hold	6		ns
t_{2a}	PTYPE input setup	8		ns
t_{2b}	PTYPE input hold	8		ns
t_{3a}	MD bus address phase input setup	7		ns
t_{3b}	MD bus address phase input hold	12		ns
t_{3c}	MD bus data phase input setup	7		ns
t_{3d}	MD bus data phase input hold	12		
t_{3e}	PCLK high to MD bus output new data		36	ns
t_{3f}	PCE_L to MD bus output driven	8		ns
t_{3g}	PCLK high to MD bus output High-Z		30	ns
t_{4a}	PRDY input setup	6		ns
t_{4b}	PRDY input hold	8		ns
t_{4c}	RESET_L input high to PRDY input high	$1 \times T_{PCLK}$		ns
t_{4d}	PCLK high to PRDY low		25	ns
t_{4e}	PCLK high to PRDY high		25	ns
t_{4f}	PCLK high to PRDY output driven		25	ns
t_{4g}	RESET_L low to PRDY output High-Z		35	ns
t_{5a}	External interrupt to PIRQ_L[1:0] low		40	ns
t_{5b}	PCLK high to PIRQ_L[1:0] low (internal interrupt sources)		45	ns
t_{5c}	PIRQ_L[1:0] low-to-high during Wake mode		$8 \times T_{PCLK}$	ns
t_{6a}	PDREQ_L input setup	6		ns
t_{6b}	PDREQ_L input hold	8		ns
t_{6c}	PCLK to PDREQ_L high/low		31	ns
t_{6d}	PCLK high to PDREQ_L driven		30	ns
t_{6e}	PCLK high to PDREQ_L High-Z (when GPIO)		30	ns
t_{6f}	PCLK low to PDREQ_L High-Z (when PDREQ_L)		30	ns
t_{18a}	PCTL inputs setup	6		ns
t_{18b}	PCTL inputs hold	8		ns

Table 5-3. System Bus Timing Parameters *(cont.)*

Symbol	Parameter	MIN	MAX	Unit
t_{18c}	PCLK high to PCTL outputs		45	ns
t_{18d}	PCM_CD_L high to PCTL[2:0] outputs		35	ns
t_{18e}	PCLK high to PCTL driven	8	35	ns
t_{18f}	PCLK high to PCTL High-Z		35	ns
t_{16c}	RESET_L input pulse width	$2 \times T_{PCLK}$		ns
t_{17a}	PSLEEP_L input setup	6		ns
t_{17b}	PSLEEP_L input hold	8		ns

Table 5-4. PC Card Bus Timing Parameters

Symbol	Parameter	MIN	MAX	Unit
t_{7a}	MD to PCM_A, PCM_REG_L, PCM_CE_L outputs		n/a	ns
t_{7b}	PCLK low to PCM_A, PCM_REG_L, PCM_CE_L outputs		n/a	ns
t_{7c}	PCLK high to PCM_A, PCM_REG_L, PCM_CE_L outputs		40	ns
t_{7d}	PCLK high to card outputs[a] Driven		40	ns
t_{7e}	PCLK high to card outputs[a] High-Z		50	ns
t_{7f}	PCM_CD_L high to card outputs[a] High-Z		45	ns
t_{8a}	PCM_D input setup	6		ns
t_{8b}	PCM_D input hold	10		
t_{8c}	PCLK low to PCM_D outputs		40	ns
t_{8d}	PCLK low to PCM_D driven (following card read)	8	40	ns
t_{8e}	PCLK high to PCM_D High-Z (card read)		45	ns
t_{9a}	PCLK high to command strobes[b] low		32	ns
t_{9b}	PCLK high to command strobes[b] high		32	ns
t_{9c}	PCLK low to command strobes[b] low (DMA terminal count)		32	ns
t_{9d}	PCLK low to command strobes[b] high (DMA terminal count)		32	ns
t_{10a}	card inputs[c] setup	12		ns
t_{10b}	card inputs[c] hold	8		ns
t_{11}	PCM_A, PCM_REG_L, PCM_CE_L to command strobe[b] low setup	eqn 1		ns
t_{12}	Command strobe[b] width	eqn 2		ns
t_{13}	Command strobe[b] high to PCM_A, PCM_REG_L, PCM_CE_L hold	eqn 3		ns

Table 5-4. PC Card Bus Timing Parameters *(cont.)*

Symbol	Parameter	MIN	MAX	Unit
t_{14}	PCM_D to command strobe[b] high setup	eqn 4		ns
t_{15c}	PCLK high to PCM_VS output		35	ns
t_{15d}	PCLK high to PCM_VS output driven	6	35	ns
t_{15e}	PCLK high to PCM_VS output High-Z		35	ns
t_{19a}	PCLK high to PCM_RESET output		35	ns
t_{19b}	PCLK high to PCM_RESET output driven	6	35	ns
t_{19c}	PCLK high to PCM_RESET output High-Z		35	ns

[a] Card outputs refer to PCM_A, PCM_REG_L, PCM_CE_L, PCM_OE_L, PCM_WE_L, PCM_IORD_L, and PCM_IOWR_L.
[b] Command strobe refers to PCM_OE_L, PCM_WE_L, PCM_IORD_L, and PCM_IOWR_L.
[c] Card inputs refer to PCM_CD_L, PCM_VS_L, PCM_BVD, PCM_WP, PCM_WAIT_L, and PCM_RDY.

5.2 Bus Operations

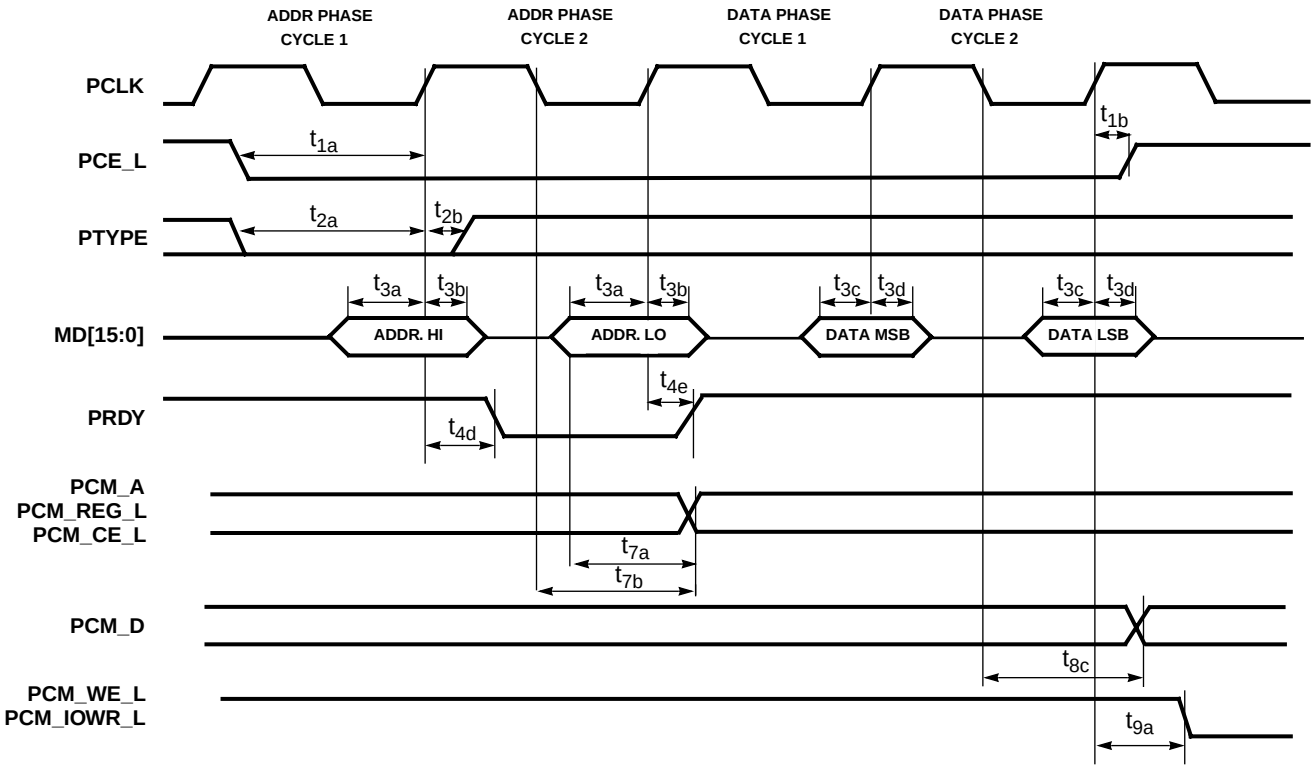


Figure 5-1. Memory or Register Write

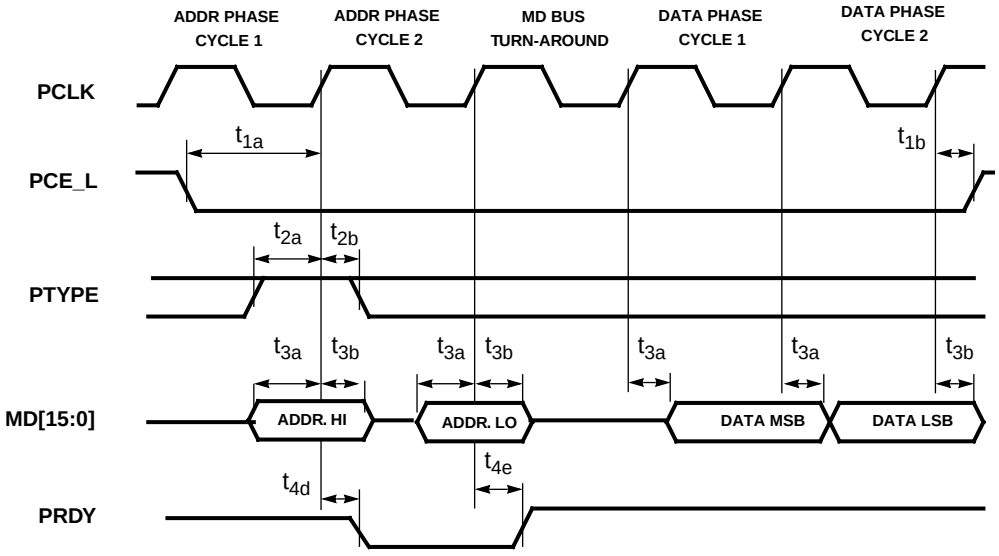


Figure 5-2. Register Read

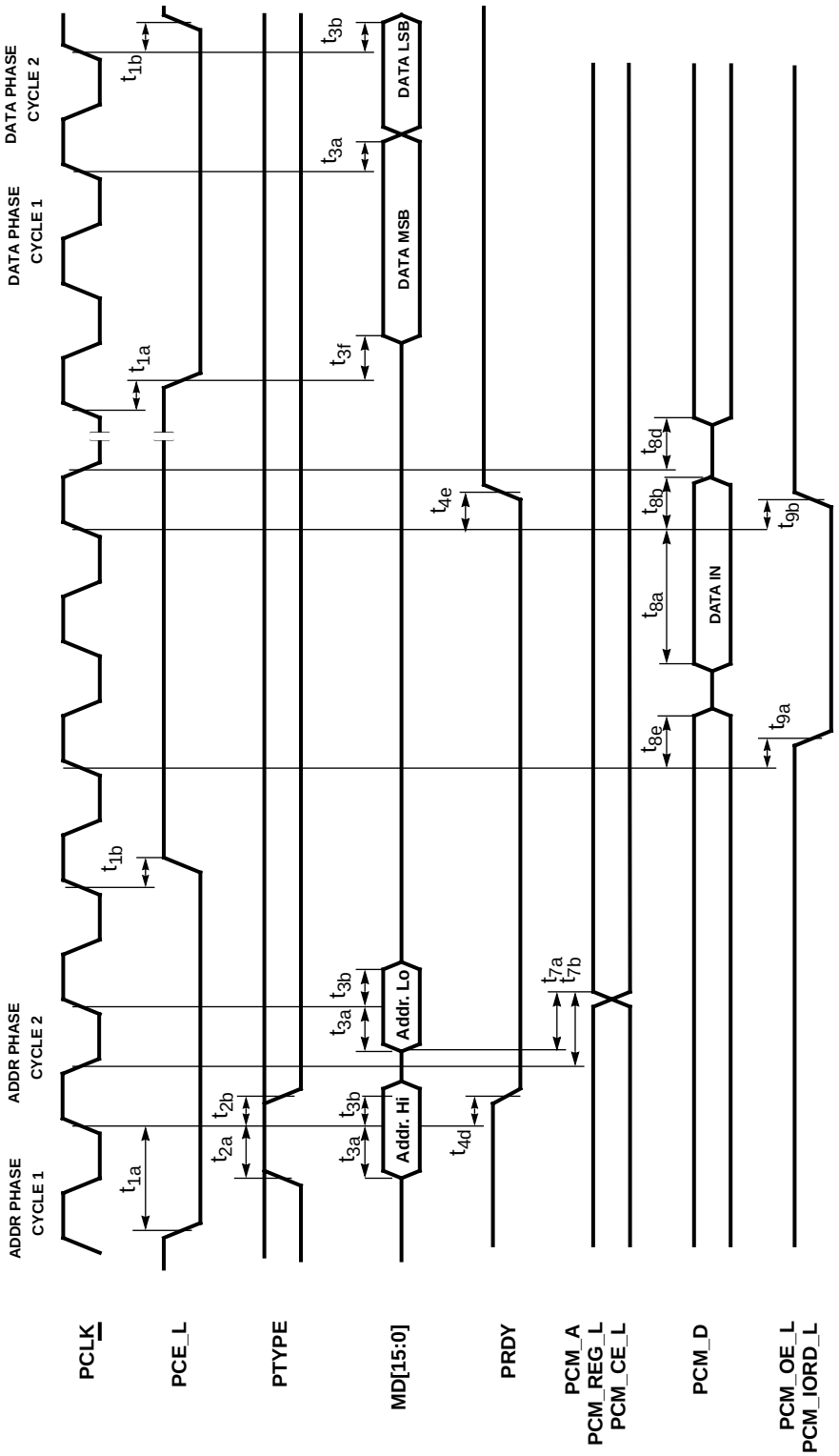


Figure 5-3. System Bus: Card Data Read

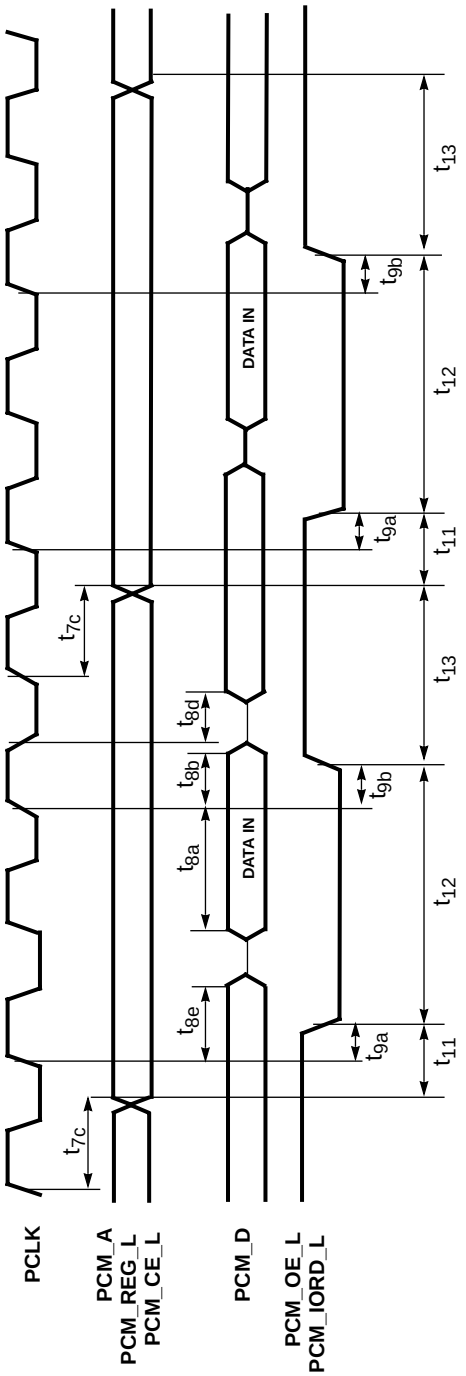


Figure 5-4. PC Card Bus Read Operation

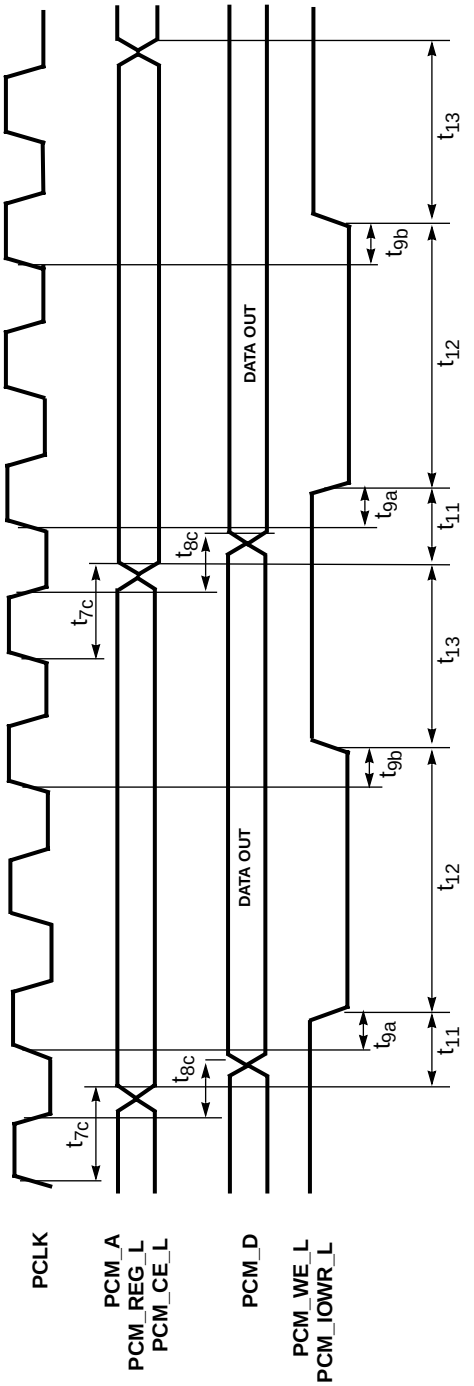


Figure 5-5. PC Card Bus Write Operation

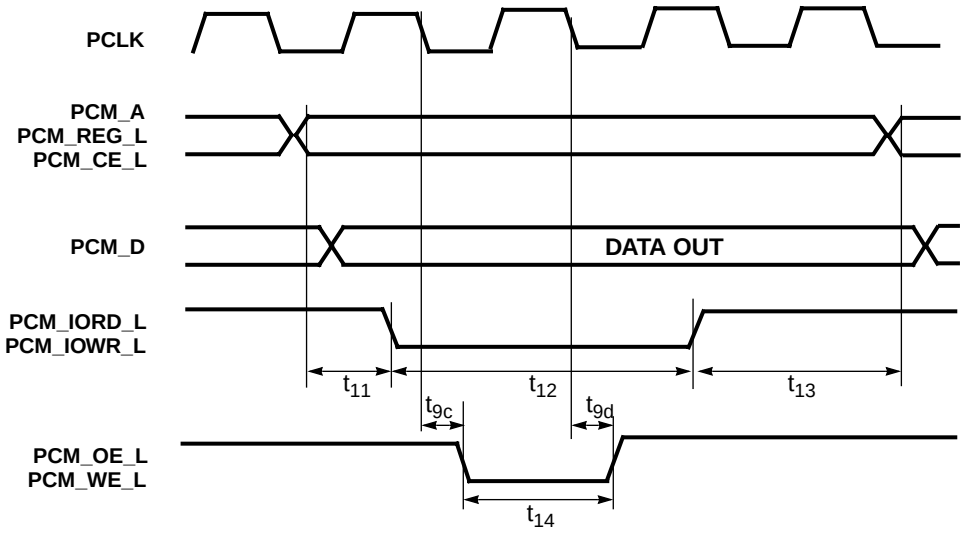


Figure 5-6. PC Card Bus DMA Transaction with Terminal Count

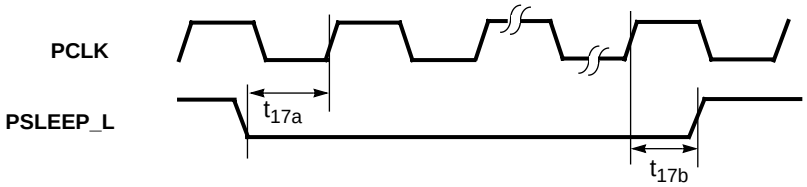
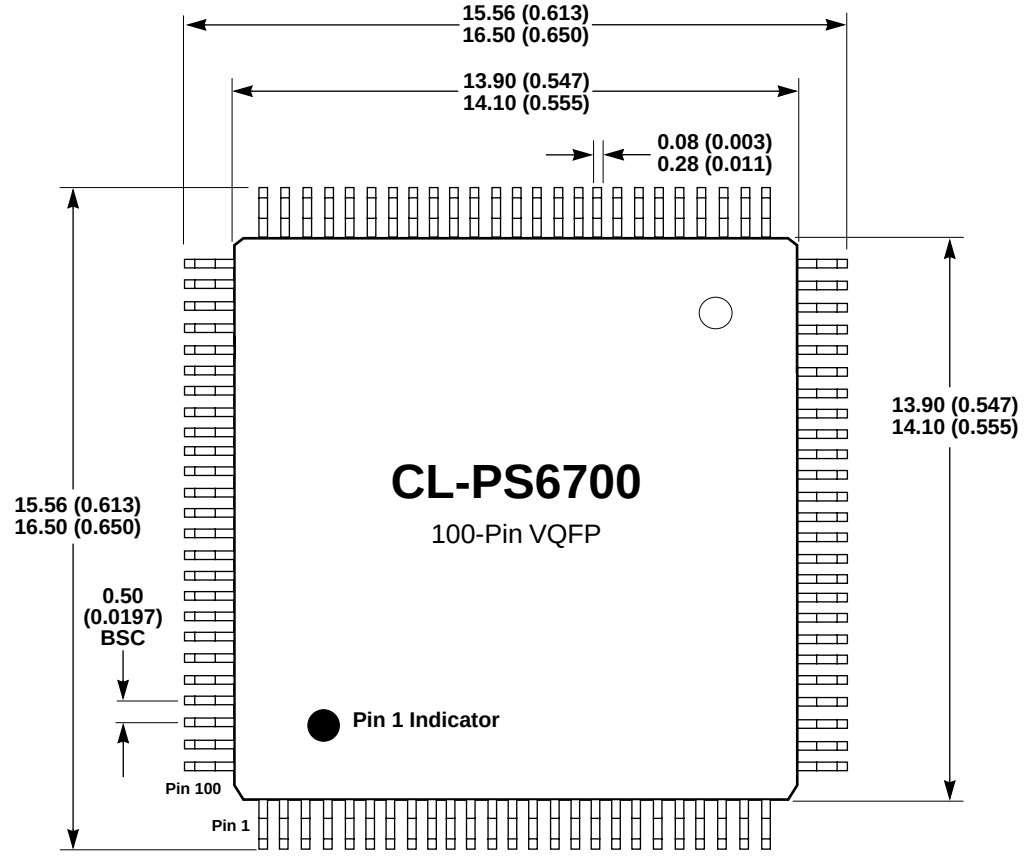
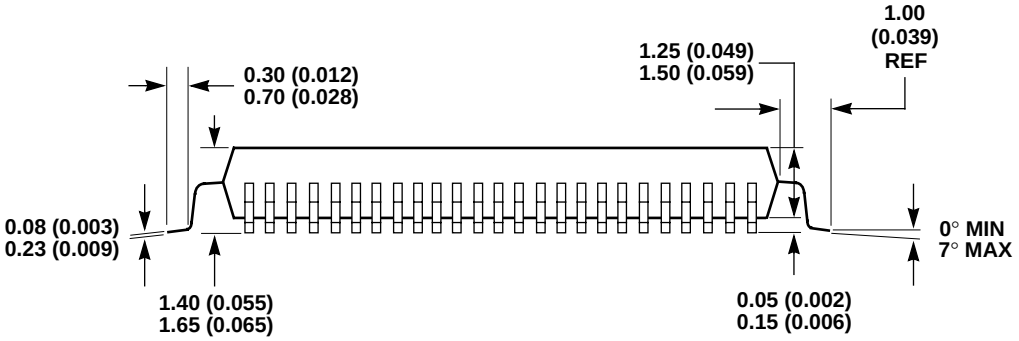


Figure 5-7. Standby Mode Timing

6. PACKAGE SPECIFICATIONS

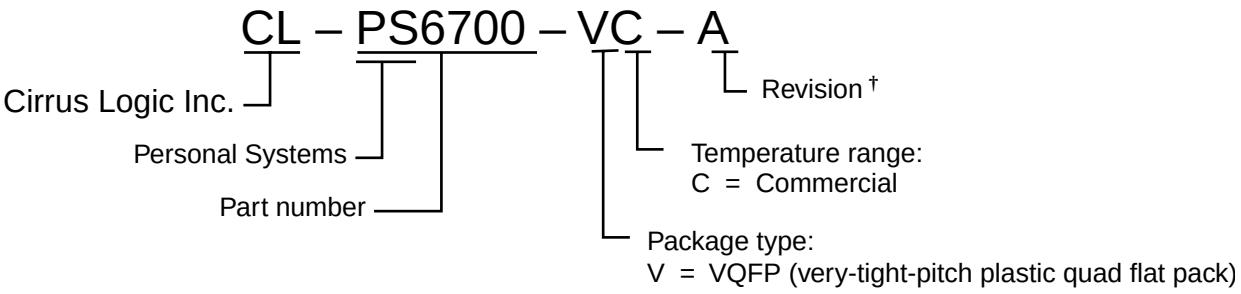




NOTES:

1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

7. ORDERING INFORMATION



† Contact Cirrus Logic for up-to-date information on revisions.

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