DS222
Dual RS–232 Transmitter/Receiver with Shutdown

DALLAS
SEMICONDUCTOR

FEATURES

- Compatible with MAX222

- High data rate – 250 kbits/sec under load

- 18–pin DIP or SOIC package

- 20–pin TSSOP package for height restricted applications

- Operate from single +5V power

- Meets all EIA–232E and V.28 specifications

- Uses small capacitors: 0.1 μF

- 3–state driver and receiver outputs

- Shutdown pin

- Optional industrial temperature range available (–40°C to +85°C)

ORDERING INFORMATION

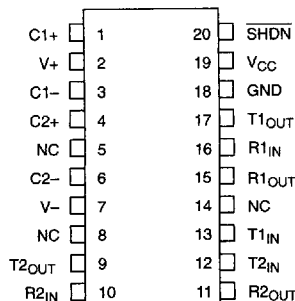|	
DS222	18–pin DIP
DS222–N	18–pin DIP (Industrial)
DS222S	18–pin SOIC
DS222S–N	18–pin SOIC (Industrial)
DS222E	20–pin TSSOP
DS222E–N	20–pin TSSOP (Industrial)

DESCRIPTION

The DS222 is a dual RS–232 driver/receiver pair that generates RS–232 voltage levels from a single +5 volt power supply. Additional ±12 volt supplies are not needed since the DS222 uses on–board charge pumps to convert the +5 volt supply to ±10 volts. The DS222 is fully compliant with EIA RS–232E and V.28/V.24 standards. The DS222 contains two drivers and two receivers. A shutdown pin ($\overline{\text{SHDN}}$) is provided to disable the device and place all drivers and receivers into a high impedance state; when shut down, supply current is less that 10 μA. Driver slew rates and data rates are guaranteed up to 250 kbits/sec. The DS222 operates with only 0.1 μF charge pump capacitors.

PIN ASSIGNMENT

NC	1	18	$\overline{\text{SHDN}}$
C1+	2	17	V_{CC}
V+	3	16	GND
C1–	4	15	$T1_{OUT}$
C2+	5	14	$R1_{IN}$
C2–	6	13	$R1_{OUT}$
V–	7	12	$T1_{IN}$
$T2_{OUT}$	8	11	$T2_{IN}$
$R2_{IN}$	9	10	$R2_{OUT}$

18–PIN DIP AND SOIC

C1+	1	20	$\overline{\text{SHDN}}$
V+	2	19	V_{CC}
C1–	3	18	GND
C2+	4	17	$T1_{OUT}$
NC	5	16	$R1_{IN}$
C2–	6	15	$R1_{OUT}$
V–	7	14	NC
NC	8	13	$T1_{IN}$
$T2_{OUT}$	9	12	$T2_{IN}$
$R2_{IN}$	10	11	$R2_{OUT}$
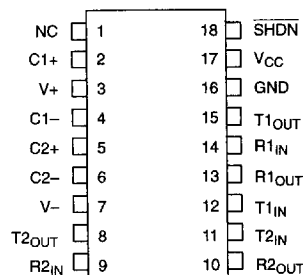
20–PIN TSSOP

PIN DESCRIPTION

V_{CC}	–	+5 Volt Supply
GND	–	Ground
V+	–	Positive Supply Output
V–	–	Negative Supply Output
$T1_{IN}$, $T2_{IN}$	–	RS–232 Driver Inputs
$T1_{OUT}$, $T2_{OUT}$	–	RS–232 Driver Outputs
$R1_{IN}$, $R2_{IN}$	–	Receiver Inputs
$R1_{OUT}$, $R2_{OUT}$	–	Receiver Outputs
C1+, C1–	–	Capacitor 1 Connections
C2+, C2–	–	Capacitor 2 Connections
$\overline{\text{SHDN}}$	–	Shutdown Input

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OPERATION

The diagram in Figure 1 shows the main elements of the DS222. The following paragraphs describe the function of each pin.

FUNCTIONAL DIAGRAM OF DS222 Figure 1
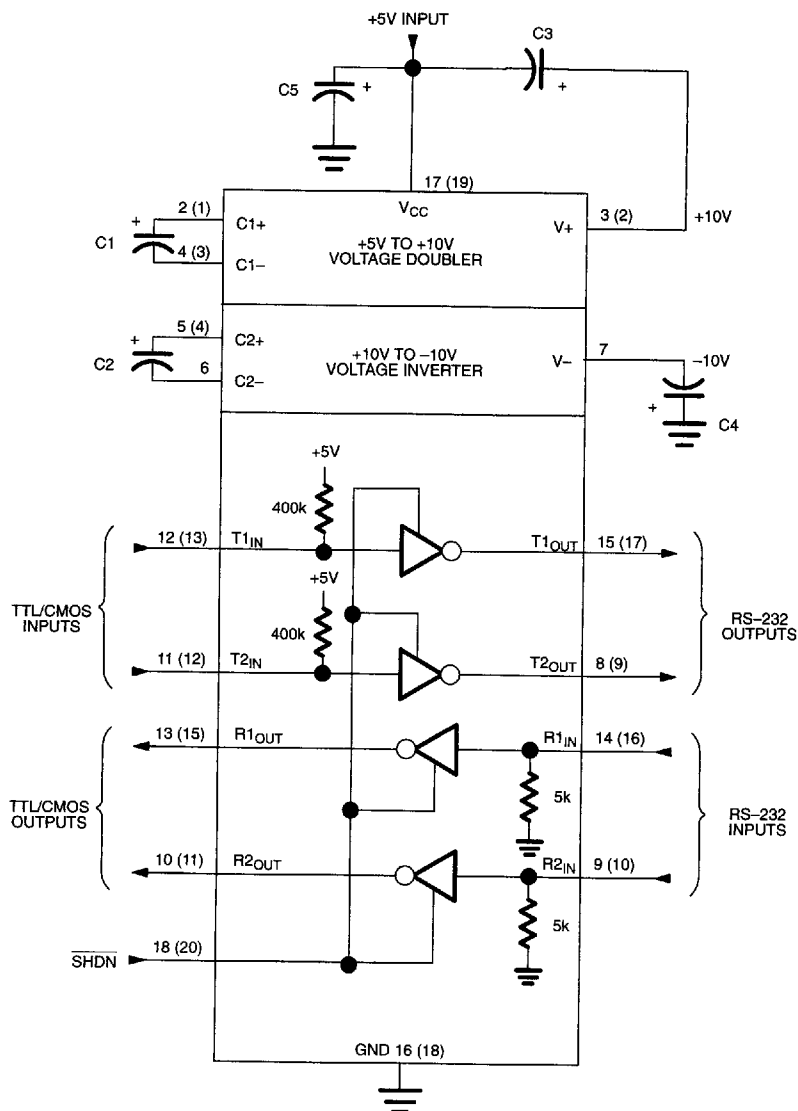
NOTE: C5 is a recommended decoupling capacitor which is the same value as C1, C2, C3, and C4.

( ) Are for TSSOP package only.

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PIN DESCRIPTIONS

V_{CC}, GND: DC power is provided to the device on these pins. V_{CC} is the +5 volt input.

V+: Positive supply output (RS–232). V+ requires an external storage charge capacitor of at least 0.1 μF. A larger capacitor (up to 10 μF) can be used to reduce supply ripple.

V–: Negative supply output (RS–232). V– requires an external storage capacitor of at least 0.1 μF. A larger capacitor (up to 10 μF) can be used to reduce supply ripple.

$T1_{IN}$, $T2_{IN}$: Standard TTL/CMOS inputs for the RS–232 drivers. The inputs of unused drivers can be left unconnected since each input has a 400 kΩ pull–up resistor. These inputs are placed into a high impedance state when the DS222 is in shut down mode.

$T1_{OUT}$, $T2_{OUT}$: Driver outputs at RS–232 levels. Driver output swing meets RS–232 levels for loads up to 3 kΩ. These driver outputs provide current necessary to meet RS–232 levels for loads up to 2500 pF.

$R1_{IN}$, $R2_{IN}$: Receiver inputs. These inputs accept RS–232 level signals (±25 volts) into a protected 5 kΩ terminating resistor. Each receiver provides 0.5V hysteresis (typical) for noise immunity.

$R1_{OUT}$, $R2_{OUT}$: Receiver outputs at TTL/CMOS levels.

C1+, C1–, C2+, C2–: Charge pump capacitor inputs. These pins require two external capacitors (0.1 μF minimum, 10 μF maximum and should be the same size as C3 and C4). Capacitor 1 is connected between C1+ and C1–. Capacitor 2 is connected between C2+ and C2–.

$\overline{SHDN}$: Shutdown input. When this pin is driven low, all drivers and receivers are placed into a high impedance state. When shut down, supply current is less than 10 μA.

DUAL CHARGE PUMP CONVERTERS

The DS222 has a two stage on–board charge pump circuit that is used to generate ±10 volts from a single +5 volt supply. In the first stage, capacitor C1 doubles the +5V supply to +10 volts which is then stored on capacitor C3. The second stage uses capacitor C2 to invert the +10V potential to –10V. This charge is then stored on capacitor C4. The ±10 volt supplies allow the DS222 to provide the necessary output levels for RS–232 communication. The DS222 will operate with charge pump capacitors as low as 0.1 μF. Larger capacitors (up to 10 μF) can be used to reduce supply ripple.

The DS222 should not be used in applications where an external +12 volt power supply is connected to V+ (instead of using the internal charge pump to generate the RS–232 level) because V+ is internally connected to V_{CC} when in shutdown mode. The DS232A is the preferred device for this type of application. However, the DS222 can be used if the $\overline{SHDN}$ pin is tied to V_{CC} and capacitor C1 is removed.

RS–232 DRIVERS

The two RS–232 drivers are powered by the internal ±10 volt supplies generated by the on–board charge pump. The driver inputs are both TTL and CMOS compatible. Each input has an internal 400 kΩ pull–up resistor so that unused transmitter inputs can be left unconnected. The open circuit output voltage swing is from (V+ – 0.6) to V– volts. Worst case conditions for EIA–232E/V.28 of ±5 volt driving a 3 kΩ load and 2500 pF are met at maximum operating temperature and V_{CC} equal to 4.5 volts. Typical voltage swings of ±8 volts occur when loaded with a nominal 5 kΩ RS–232 receiver. As required by EIA–232E and V.28 specifications, the slew rate at the output is limited to less than 30 volts/μs. Typical slew rates are 20 volts/μs unloaded and 12 volts/μs with 3 kΩ and 2500 pF load. These slew rates allow for bit rates of over 250 kbits/s. Driver outputs maintain high impedance when power is off. In shutdown mode ($\overline{SHDN}$=0), the internal 400 KΩ pullup resistors and driver outputs are disabled to minimize current drain.

RS–232 RECEIVERS

The two receivers conform fully to the RS–232E specifications. The input impedance is typically 5 kΩ and can withstand up to ±25 volts with or without V_{CC} applied. The input switching thresholds are within the ±3 volt limit of RS–232E specification with an input threshold low of 0.8 volts and an input threshold high of 2.4 volts. The receivers have 0.5 volts of hysteresis (typical) to improve noise rejection. The TTL/CMOS compatible outputs of the receivers will be low whenever the RS–232 input is greater than 2.4 volts. The receiver output will be high when the input is floating or driven between +0.8 volts and –25 volts.

SHUTDOWN MODE

The DS222 provides a shutdown mode for power sensitive applications. The $\overline{SHDN}$ pin disables the device when driven low and places all drivers and receivers into a high impedance state. When shut down, the DS222 supply current is less than 10 μA.

ABSOLUTE MAXIMUM RATINGS*

Absolute Maximum Ratings

V_{CC}	−0.3V to +7.0V
V+	(V_{CC}−0.3V) to +14V
V−	+0.3V to −14V

Input Voltages

T_{IN}	−0.3V to (V_{CC}+0.3V)
R_{IN}	±30V

Output Voltages

T_{OUT}	(V+ + 0.3V) to (V− − 0.3V)
R_{OUT}	−0.3V to (V_{CC} + 0.3V)
Short Circuit Duration, T_{OUT}	Continuous

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS   (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Votlage	V_{CC}	4.5		5.5	V	1

DC ELECTRICAL CHARACTERISTICS   (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current (No Load)	I_{CC1}		4	10	mA	8
Power Supply Current (3 kΩ Load Both Outputs)	I_{CC2}		15		mA	8
Shutdown Supply Current (t_A=25°C)	I_{CCS}		0.1	10	μA	
Shutdown Supply Current (t_A=0°C to +70°C)	I_{CCS}		2	50	μA	
Shutdown Supply Current (t_A=−40°C to +85°C)	I_{CCS}		2	50	μA	
$\overline{SHDN}$ Input Leakage Current	$I_{\overline{SHDN}}$			±1	μA	
$\overline{SHDN}$ Threshold Low	V_{STL}	0.8	1.4		V	
$\overline{SHDN}$ Threshold High	V_{STH}		1.4	2.0	V	

DC ELECTRICAL CHARACTERISTICS (cont'd) (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RS–232 Transmitters						
Output Voltage Swing	V_{ORS}	±5	±8		V	2
Input Logic Threshold Low	V_{TTL}	0.8	1.4		V	
Input Logic Threshold High	V_{TTH}		1.4	2.0	V	
Maximum Data Rate	f_D	250	350		kbits/s	
Logic Pull–up/Input Current ($\overline{SHDN}=V_{CC}$)	I_{PU}		5	40	μA	
Logic Pull–up/Input Current ($\overline{SHDN}=0V$)	I_{PU}		±0.01	±1	μA	
Output Leakage Current ($\overline{SHDN}=0$)	I_{OUT}		±0.01	±10	μA	9
Transmitter Output Resistance	R_{OUT}	300	10M		Ω	3
Output Short–Circuit Current	I_{TSC}	±15	±30	±100	mA	4
RS–232 Receivers						
RS–232 Input Voltage Operating Range	V_{IR}	±25	±30		V	
RS–232 Input Threshold Low	V_{RTL}	0.8	1.3		V	
RS–232 Input Threshold High	V_{RTH}		1.8	2.4	V	
RS–232 Input Hysteresis	V_{HY}	0.2	0.5	1	V	
RS–232 Input Resistance	R_{IN}	3	5	7	kΩ	
TTL/CMOS Output Voltage Low	V_{ROL}		0.2	0.4	V	5
TTL/CMOS Output Voltage High	V_{ROH}	3.5	$V_{CC}-0.2$		V	6
TTL/CMOS Output Short Circuit Current ($V_{OUT}=GND$)	I_{RSC}	–2	–10		mA	
TTL/CMOS Output Short Circuit Current ($V_{OUT}=V_{CC}$)	I_{RSC}	10	30		mA	
TTL/CMOS Output Leakage Current ($\overline{SHDN}=0$)	I_{ROUT}		±0.05	±10	μA	11

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AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C)

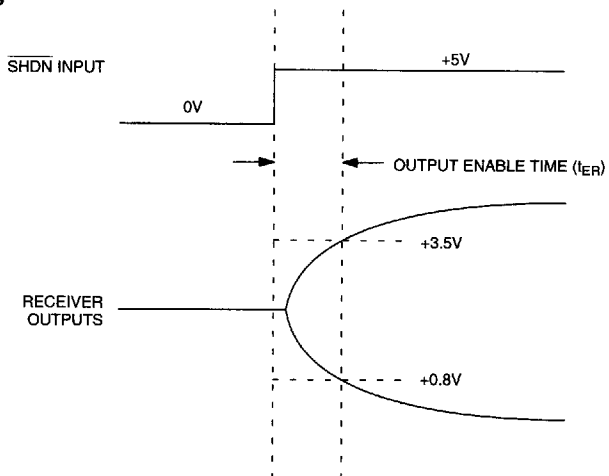| PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Transition Slew Rate	t_{SR}	6	12	30	V/μs	7
Transmitter Propagation Delay TTL to RS–232	t_{PHLT} t_{PLHT}		1.3 1.5	3.5 3.5	μs μs	
Receiver Propagation Delay RS–232 to TTL	t_{PHLR} t_{PLHR}		0.5 0.6	1 1	μs μs	
Transmitter + to – Propagation Delay Difference	t_{PHLT} $-t_{PLHT}$		300		ns	
Receiver + to – Propagation Delay Difference	t_{PHLR} $-t_{PLHR}$		100		ns	
Receiver Output Enable Time	t_{ER}		125	500	ns	
Receiver Output Disable Time	t_{DR}		160	500	ns	
Transmitter Output Enable Time ($\overline{SHDN}$ goes high)	t_{ET}		250		μs	10
Transmitter Output Disable Time ($\overline{SHDN}$ goes low)	t_{DT}		600		ns	10

NOTES:

1. All voltages are referenced to ground.

2. All transmitter outputs loaded with 3 kΩ to ground.

3. $V_{CC} = V+ = V- = 0V$; $V_{OUT} = \pm 2V$.

4. $V_{OUT} = 0V$.

5. $I_{OUT} = 3.2$ mA.

6. $I_{OUT} = -1.0$ mA.

7. $C_L = 50$ pF – 2500 pF; $RL = 3$ kΩ – 7 kΩ; $V_{CC} = 5V$; TA = 25°C.

8. $\overline{SHDN} = V_{CC}$

9. $V_{CC}=5.5V$ and $V_{OUT}=\pm 15V$ or $V_{CC}=0V$ and $V_{OUT}=\pm 15V$.

10. $C_1=C_2=C_3=C_4=0.1$ μF.

11. $0V \leq V_{OUT} \leq V_{CC}$

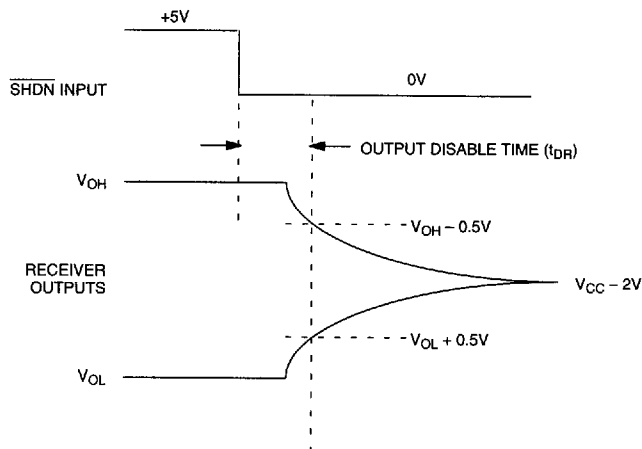## TRANSMITTER PROPAGATION DELAY TIMING Figure 2

INPUT

+3V

0V

OUTPUT

V+

0V

V−

t_{PLHT}

t_{PHLT}

RECEIVER PROPAGATION DELAY TIMING Figure 3

INPUT

+3V

0V-

−3V

OUTPUT

V_{CC}

−50%

−50%

GND

t_{PHLR}

t_{PLHR}
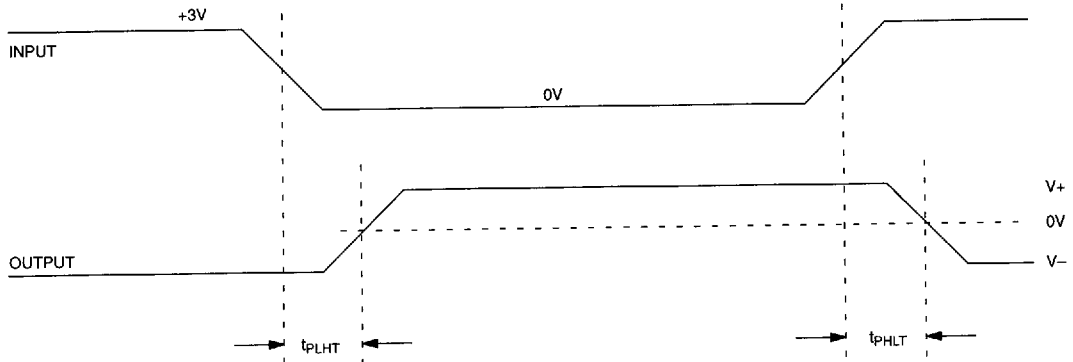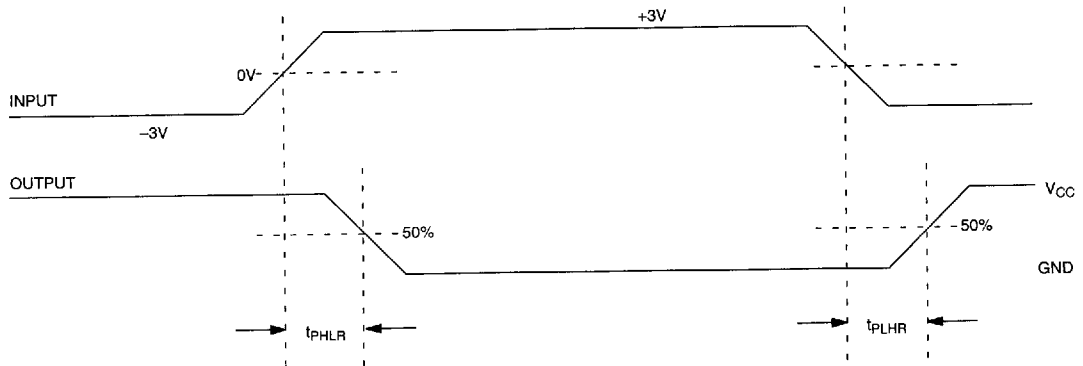
RECEIVER OUTPUT ENABLE AND DISABLE TIMING Figure 4

A. Enable Timing

$\overline{SHDN}$ INPUT

0V

+5V

OUTPUT ENABLE TIME (t_{ER})

+3.5V

RECEIVER
OUTPUTS

+0.8V

B. Disable Timing

+5V

$\overline{SHDN}$ INPUT

0V

OUTPUT DISABLE TIME (t_{DR})

V_{OH}

$V_{OH} - 0.5V$

RECEIVER
OUTPUTS

$V_{CC} - 2V$

$V_{OL} + 0.5V$

V_{OL}

C. Test Circuit

$\overline{SHDN}$

R_X IN

R_X

R_X OUT

1K

$V_{CC} - 2V$

150 pF

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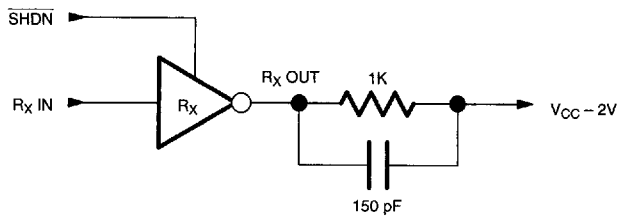
TRANSMITTER OUTPUT ENABLE AND DISABLE TIMING Figure 5

A. Enable Timing

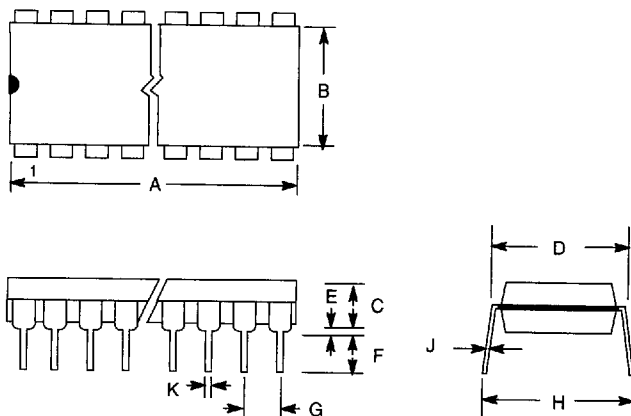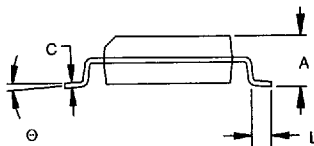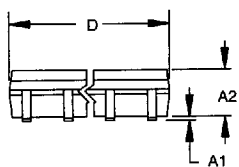$\overline{\text{SHDN}}$ INPUT

+5V

0V

OUTPUT ENABLE TIME (t_{ET})

5V

TRANSMITTER OUTPUTS

5V

B. Disable Timing

$\overline{\text{SHDN}}$

+5V

0V

OUTPUT DISABLE TIME (t_{DT})

V+

+5V

TRANSMITTER OUTPUTS

0V

−5V

V−

C. Test Circuit

TX$_{IN}$

T$_X$

TX$_{OUT}$

3K

50 pF
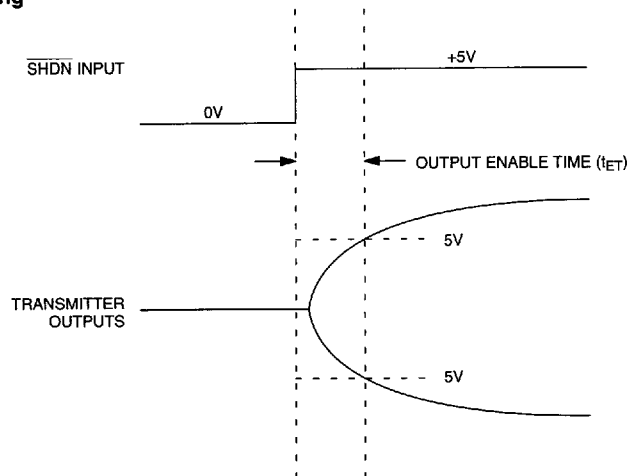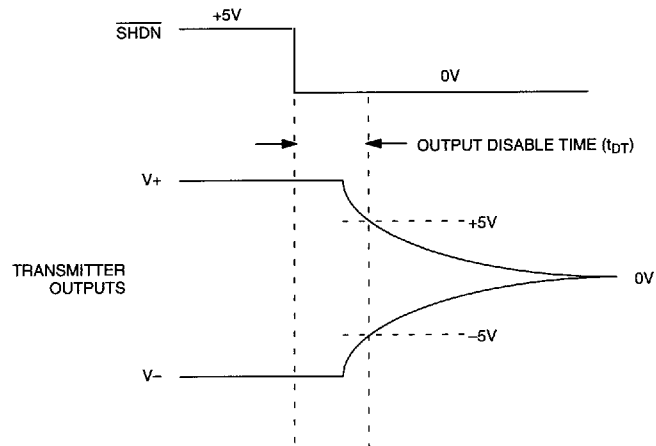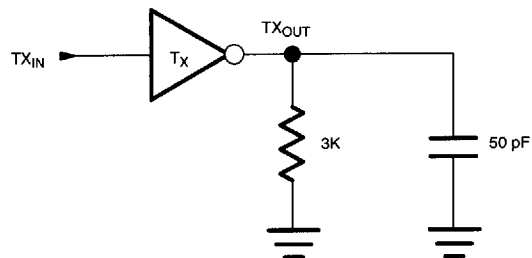
18–PIN DIP (300 MIL)

PKG	18-PIN	
DIM	**MIN**	**MAX**
A IN. MM	0.890 22.61	0.920 23.36
B IN. MM	0.240 6.10	0.260 6.60
C IN. MM	0.120 3.05	0.140 3.56
D IN. MM	0.300 7.62	0.325 8.26
E IN. MM	0.015 0.38	0.040 1.02
F IN. MM	0.120 3.04	0.140 3.56
G IN. MM	0.090 2.23	0.110 2.79
H IN MM	0.320 8.13	0.370 9.40
J IN MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.021 0.53

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18–PIN SOIC (300 MIL)
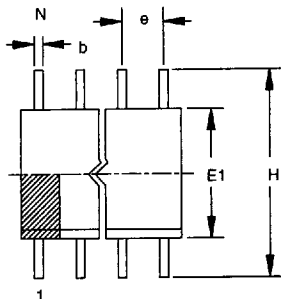
PKG	18-PIN	
DIM	MIN	MAX
A IN. MM	0.094 2.39	0.105 2.67
A1 IN. MM	0.004 0.102	0.012 0.30
A2 IN. MM	0.089 2.26	0.095 2.41
b IN. MM	0.013 0.33	0.020 0.51
C IN. MM	0.009 0.229	0.013 0.33
D IN. MM	0.448 11.38	0.462 11.73
e IN. MM	0.050 BSC 1.27 BSC	
E1 IN MM	0.290 7.37	0.300 7.62
H IN MM	0.398 10.11	0.416 10.57
L IN. MM	0.016 0.40	0.040 1.02
Θ	0°	8°

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20-PIN TSSOP (PRELIMINARY)
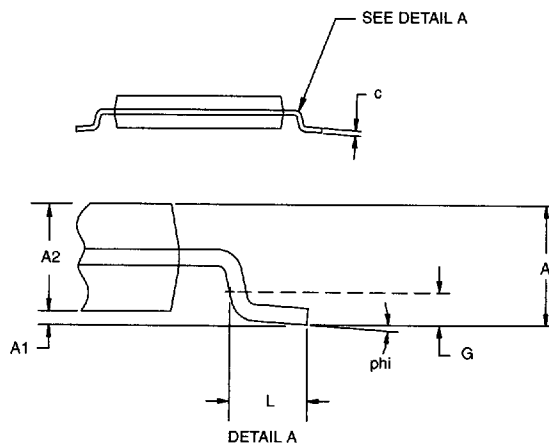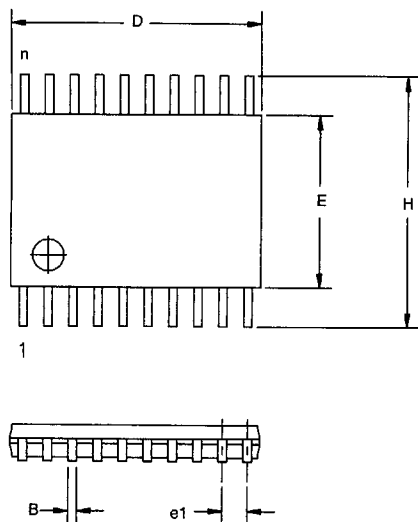
DIM	MIN	MAX
A MM	–	1.10
A1 MM	0.05	–
A2 MM	0.75	1.05
C MM	0.09	0.18
L MM	0.50	0.70
e1 MM	0.65 BSC	
B MM	0.18	0.30
D MM	6.40	6.90
E MM	4.40 NOM	
G MM	0.25 REF	
H MM	6.25	6.55
phi	0°	8°