3mW, 100kSPS, 14-Bit ADC in 6 Lead SOT-23

Preliminary Technical Data — AD7940

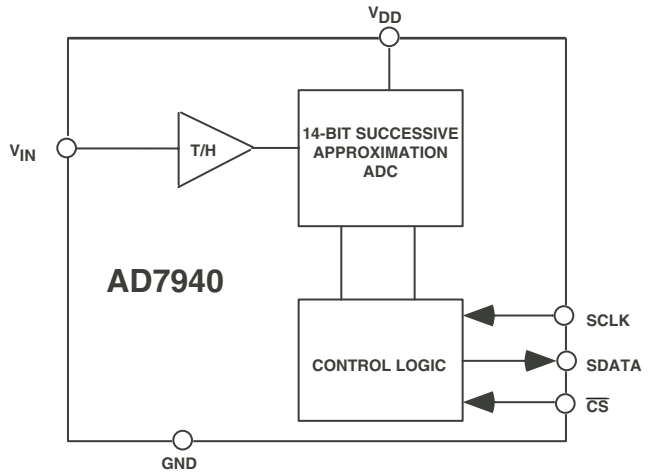
FEATURES

Fast Throughput Rate: 100kSPS
Specified for V_{DD} of 2.5 V to 5.25 V
Low Power:
2.5mW typ at 100kSPS with 3V Supplies
15mW typ at 100kSPS with 5V Supplies
Wide Input Bandwidth:
80dB SNR at 10kHz Input Frequency
Flexible Power/Serial Clock Speed Management
No Pipeline Delays
High Speed Serial Interface
SPI/QSPI/µWire/DSP Compatible
Standby Mode: 0.5 µA max
6-Lead SOT-23, and 8-Lead MSOP Packages

APPLICATIONS

Battery-Powered Systems
Personal Digital Assistants
Medical Instruments
Mobile Communications
Instrumentation and Control Systems
Remote Data Acquisition Systems

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. First 14-Bit ADC in a SOT-23 package.
2. High Throughput with Low Power Consumption
3. Flexible Power/Serial Clock Speed Management
   The conversion rate is determined by the serial clock allowing the conversion time to be reduced through the serial clock speed increase. This allows the average power cunsumption to be reduced when a powerdown mode is used while not converting. The part also features a shutdown mode to maximize power efficiency at lower throughput rates. Power consumption is 0.5µA max when in shutdown.
4. Reference derived from the power supply.
5. No Pipeline Delay
   The part features a standard successive-approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once off conversion control.

GENERAL DESCRIPTION

The AD7940 is a 14-bit, fast, low power, successive-approximation ADC. The part operates from a single 2.5 V to 5.25 V power supply and features throughput rates up to 100kSPS. The part contains a low-noise, wide bandwidth track/hold amplifier which can handle input frequencies in excess of 100kHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$ and the conversion is also initiated at this point. There are no pipelined delays associated with the part.

The AD7940 uses advanced design techniques to achieve very low-power dissipation at fast throughput rates.

The reference for the part is taken internally from V_{DD}. This allows the widest dynamic input range to the ADC. Thus the analog input range for the part is 0 to V_{DD}. The conversion rate is determined by the SCLK frequency.

REV. PrB 11/02

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AD7940–SPECIFICATIONS[1] (V_{DD} = +2.5 V to +5.25 V, f_{SCLK} = 2.5MHz, f_{SAMPLE} = 100Ksps unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	B Version[1,2]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			F_{IN} = 10kHz Sine Wave
Signal to Noise + Distortion (SINAD)[3]	78	dB min	V_{DD} = 3V
Signal to Noise Ratio (SNR)[3]	80	dB min	V_{DD} = 5V; 83 dB typ
	79	dB min	V_{DD} = 3V; 82 dB typ
Total Harmonic Distortion (THD)[3]	-85	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[3]	-89	dB typ	
Intermodulation Distortion (IMD)[3]			
Second Order Terms	-90	dB typ	
Third Order Terms	-90	dB typ	
Aperture Delay	10	ns max	
Aperture Jitter	30	ps typ	
Full Power Bandwidth	TBD	MHz typ	@ 3 dB
	TBD	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	14	Bits	
Integral Nonlinearity[3]	±1.5	LSB max	
Differential Nonlinearity[3]	±0.9	LSB max	Guaranteed No Missed Codes to 14 Bits
Offset Error[3]	±1.5	LSB max	
Gain Error[3]	±2.5	LSB max	V_{DD} = 5V
	±1.5	LSB max	V_{DD} = 3V
ANALOG INPUT			
Input Voltage Ranges	0 to V_{DD}	Volts	
DC Leakage Current	±1	µA max	
Input Capacitance	30	pF typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.4	V min	
Input Low Voltage, V_{INL}	0.4	V max	V_{DD} = 3V
	0.8	V max	V_{DD} = 5V
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[3,4]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} -0.2	V min	I_{SOURCE} = 200 µA; V_{DD} = 2.5 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} =200 µA
Floating-State Leakage Current	±1	µA max	
Floating-State Output Capacitance[3,4]	10	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	8	µs max	Sixteen SCLK cycles
Track/Hold Acquisition Time	500	ns max	Full-scale step input
	400	ns max	Sine wave input <= 10KHz
Throughput Rate	100	kSPS max	See Serial Interface Section

NOTES
[1]Temperature ranges as follows: B Version: –40°C to +85°C.
[2] Operational from V_{DD} = 2V
[3]See Terminology.
[4]Sample tested @ +25°C to ensure compliance.
[5]See POWER VERSUS THROUGHPUT RATE section.
Specifications subject to change without notice.

AD7940–SPECIFICATIONS[1] (V_{DD} = +2.5 V to +5.25 V, f_{SCLK} = 2.5MHz, f_{SAMPLE} = 100Ksps unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	B Version[1,2]	Units	Test Conditions/Comments
POWER REQUIREMENTS			
V_{DD}	+2.5/+5.25	V min/max	
I_{DD}			Digital I/Ps = 0V or V_{DD}.
Normal Mode(Static)	3.55	mA max	V_{DD} = 4.75V to 5.25V. SCLK on or off.
	0.95	mA max	V_{DD} = 2.5V to 3.5V. SCLK on or off.
Normal Mode (Operational)	3.25	mA max	V_{DD} = 4.75V to 5.25V. F_{SAMPLE} = 100 kSPS
	0.9	mA max	V_{DD} = 2.5V to 3.5V. F_{SAMPLE} = 100 kSPS
Full Power-Down Mode	0.5	µA max	SCLK on or off.
Power Dissipation[5]			
Normal Mode (Operational)	16.25	mW max	V_{DD} = 5V. F_{SAMPLE} = 100 kSPS
	2.85	mW max	V_{DD} = 3V. F_{SAMPLE} = 100 kSPS
Full Power-Down	2.5	µW max	V_{DD} = 5 V.
	1.5	µW max	V_{DD} = 3 V.

NOTES
[1]Temperature ranges as follows: B Version: –40°C to +85°C.
[2] Operational from 2 V
[3]See Terminology.
[4]Sample tested @ +25°C to ensure compliance.
[5]See POWER VERSUS THROUGHPUT RATE section.

Specifications subject to change without notice.

AD7940

TIMING SPECIFICATIONS[1] (V_{DD} = +2.5 V to +5.25 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} 3 V	5V	Units	Description
f_{SCLK} [2]	10	10	kHz min	
	2.5	2.5	MHz max	
$t_{CONVERT}$	16 x t_{SCLK}	16 x t_{SCLK}		
t_{quiet}	50	50	ns min	Minimum Quiet Time required between Bus Relinquish and start of next conversion
t_1	10	10	ns min	Minimum $\overline{CS}$ Pulse Width
t_2	10	10	ns min	$\overline{CS}$ to SCLK Setup Time
t_3 [3]	20	20	ns max	Delay from $\overline{CS}$ Until SDATA 3-State Disabled
t_4 [3]	40	40	ns max	Data Access Time After SCLK Falling Edge
t_5	$0.4t_{SCLK}$	$0.4t_{SCLK}$	ns min	SCLK Low Pulse Width
t_6	$0.4t_{SCLK}$	$0.4t_{SCLK}$	ns min	SCLK High Pulse Width
t_7	10	10	ns min	SCLK to Data Valid Hold Time
t_8 [4]	25	25	ns max	SCLK falling Edge to SDATA High Impedance
$t_{power-up}$ [5]	1	1	µs typ	Power up time from Full Power-down.

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 Volts.
[2]Mark/Space ratio for the SCLK input is 40/60 to 60/40.
[3]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.0 V.
[4]t_8 is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.
[5]See Power-up Time section.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND .....–0.3 V to +7 V
Analog Input Voltage to GND..... –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND.....–0.3 V to +7 V
Digital Output Voltage to GND.....–0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2] .....±10 mA
Operating Temperature Range
Commercial (B Version).....–40°C to +85°C
Storage Temperature Range.....–65°C to +150°C
Junction Temperature.....+150°C
SOT-23 Package, Power Dissipation.....450 mW
θ_{JA} Thermal Impedance.....229.6°C/W
θ_{JC} Thermal Impedance.....91.99°C/W
µSOIC Package, Power Dissipation.....450 mW
θ_{JA} Thermal Impedance.....205.9°C/W
θ_{JC} Thermal Impedance..... 43.74°C/W
Lead Temperature, Soldering
Vapor Phase (60 secs).....215°C
Infared (15 secs).....220°C
ESD.....3.5kV

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch up.

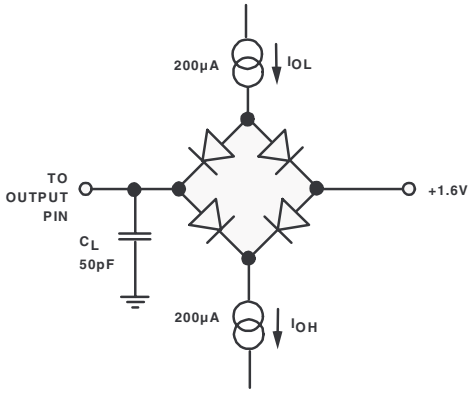


Figure 1. Load Circuit for Digital Output Timing Specifications

CAUTION

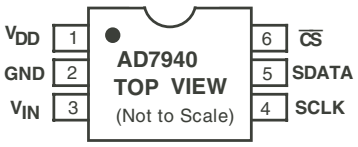
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7940 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

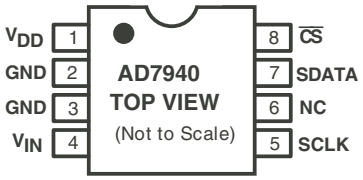
Pin Mnemonic	Function
V_{DD}	Power Supply Input. The V_{DD} range for the AD7940 is from +2.5V to +5.25V.
GND	Analog Ground. Ground reference point for all circuitry on the AD7940. All analog input signals should be referred to this GND voltage.
V_{IN}	Analog Input. Single-ended analog input channel. The input range is 0 to V_{DD}.
SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7940's conversion process.
SDATA	Data Out. Logic Output. The conversion result from the AD7940 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7940 consists of 2 leading zeros followed by 14 bits of conversion data which is provided MSB first. See serial Interface section.
$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7940 and framing the serial data transfer.
NC	No Connect. This pin should be left unconnected.

AD7940 PIN CONFIGURATIONS

SOT-23



MSOP



ORDERING GUIDE

Model	Range	Linearity Error (LSB)[1]	Package Option[2]	Branding
AD7940BRJ	-40°C to +85°C	±1.5 max	RJ-6	CRB
AD7940BRM	-40°C to +85°C	±1.5 max	RM-8	CRB

NOTES
[1]Linearity error here refers to integral nonlinearity
[2]RJ = SOT-23.
[2]RM = MSOP.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e AGND + 1LSB

Gain Error
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., V_{REF} – 1 LSB) after the offset error has been adjusted out.

Track/Hold Acquisition Time
The track/hold amplifier returns into track mode at the end of conversion. Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±0.5 LSB, after the end of conversion. See serial interface timing section for more details.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

Signal to (*Noise* + *Distortion*) = (6.02 *N* + 1.76) *dB*

Thus for a 14-bit converter, this is 86 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7940, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7940 is tested using the CCIF standard where two input frequencies nearthe top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

PERFORMANCE CURVES

TPC 1 shows a typical FFT plot for the AD7940 at 100kSPS sample rate and 10kHz input frequency. TPC 2 shows the signal-to-(noise+distortion) ratio performance versus input frequency for various supply voltages while sampling at 100kSPS with an SCLK of 2.5MHz.

TPC 3 shows a graph of total harmonic distortion versus analog input frequency for various supply voltages, while TPC 4 shows a graph of total harmonic distortion versus analog input frequency for various source impedances. See Analog Input section.

TPC 5 and TPC 6 show typical DNL and INL plots for the AD7940.

Typical Performance Characteristics

TBD

TPC 1. AD7940 Dynamic Performance at 100 kSPS

TBD

TPC 2. AD7940 SINAD vs. Analog Input Frequency for Various Supply Voltages at 100 kSPS

TBD

TPC 3. AD7940 THD vs. Analog Input Frequency for Various Supply Voltages at 100 kSPS

TBD

TPC 4. AD7940 THD vs. Analog Input Frequency for Various Source Impedances

TBD

TPC 6. AD7940 Typical INL

TBD

TPC 7. AD7940 Typical DNL

CIRCUIT INFORMATION

The AD7940 is a fast, low power, 14-bit, single supply, A/D converter. The part can be operated from a 2.5V to 5.25V supply. When operated from either a 5V or 3V supply, the AD7940 is capable of throughput rates of 100 kSPS when provided with a 2.5MHz clock.

The AD7940 provides the user with an on-chip track/hold, A/D converter, and a serial interface housed in a tiny 6-lead SOT-23 package or 8-ld MSOP package which offer the user considerable space saving advantages over alternative solutions. The serial clock input accesses data from the part and also provides the clock source for the successive-approximation A/D converter. The analog input range for the AD7940 is 0 to V_{DD}. An external reference is not required for the ADC, nor is there a reference on-chip. The reference for the AD7940 is derived from the power supply and thus gives the widest dynamic input range.

The AD7940 also features a power-down option to save power between conversions. The power-down feature is implemented across the standard serial interface as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7940 is a 14-bit, successive approximation analog-to -digital converter based around a capacitive DAC. The AD7940 can convert analog input signals in the range 0 V to V_{DD}. Figures 2 and 3 show simplified schematics of the ADC. The ADC comprises of Control Logic, SAR and a Capacitive DAC, which are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. Figure 2 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on the selected V_{IN} channel.

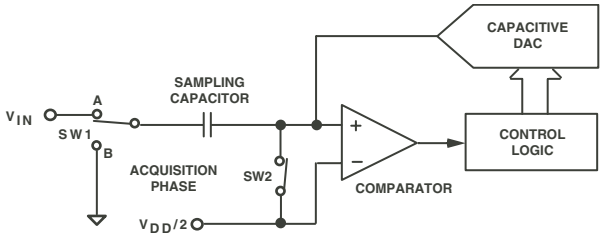


Figure 2. ADC Acquisition Phase

When the ADC starts a conversion, see figure 3, SW2 will open and SW1 will move to position B causing the comparator to become unbalanced. The Control Logic and the Capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced the conversion is complete. The Control Logic generates the ADC output code. Figure 4 shows the ADC transfer function.

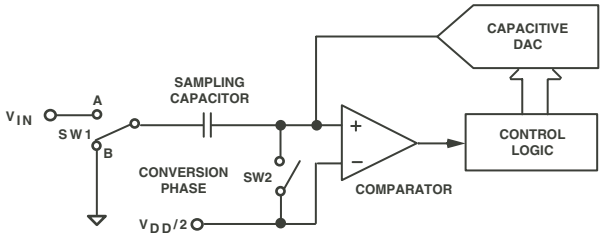


Figure 3. ADC Conversion Phase

Analog Input

Figure 4 shows an equivalent circuit of the analog input structure of the AD7940. The two diodes D1 and D2 provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 300mV. This will cause these diodes to become forward biased and start conducting current into the substrate. 10mA is the maximum current these diodes can conduct without causing irreversible damage to the part. The capacitor C1 in Figure 4 is typically about 4pF and can primarily be attributed to pin capacitance. The resistor R1 is a lumped component made up of the on resistance of a switch (track

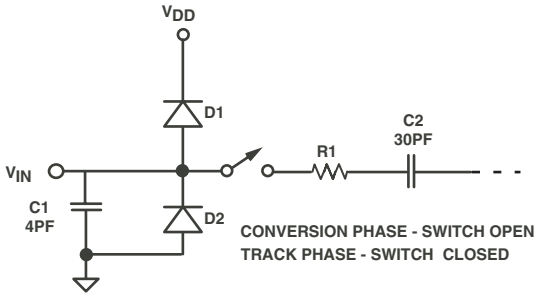


Figure 4. Equivalent Analog Input Circuit

and hold switch). This resistor is typically about 100 Ω. The capacitor C2 is the ADC sampling capacitor and has a capacitance of 30pF typically. For ac applications, removing high frequency components from the analog input signal is recommended by use of an RC low-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal to noise ratio are critical the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp will be a function of the particular application. When no amplifier is used to drive the analog input the source impedance should be limited to low values. The maximum source impedance will depend on the amount of total harmonic distortion (THD) that can be tolerated. The THD will increase as the source impedance increases and performance will degrade (see TPC4).

ADC TRANSFER FUNCTION

The output coding of the AD7940 is straight binary. The designed code transitions occur at successive integer LSB values (i.e., 1 LSB, 2 LSBs, etc.). The LSB size is = V_{DD}/16384. The ideal transfer characteristic for the AD7940 is shown in Figure 5.

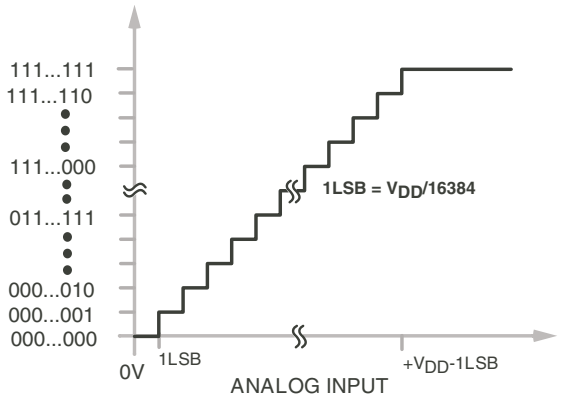


Figure 5. AD7940 Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 6 shows a typical connection diagram for the AD7940. V_{REF} is taken internally from V_{DD} and as such should be well decoupled. This provides an analog input range of 0 V to V_{DD}. The conversion result is output in a 16-bit word. This 16-bit data stream consists of two leading zeros, followed by the 14 bits of conversion data MSB first. For applications where power consumption is of concern, the power-down mode should be used between conversions or bursts of several conversions to improve power performance. See Modes of Operation section of the datasheet.

In fact, because the supply current required by the AD7940 is so low, a precision reference can be used as the supply source to the AD7940. For example, a REF19x voltage reference (REF195 for 5 V or REF193 for 3 V etc.) can be used to supply the required voltage to the ADC (see Figure 6). This configuration is especially useful if the power supply available is quite noisy or if the system supply voltages are at some value other than the required operating voltage of the AD7940 (e.g. 15V). The REF19x will output a steady voltage to the AD7940.

TBD

Figure 6. Typical Connection Diagram

Digital Inputs

The digital inputs applied to the AD7940 are not limited by the maximum ratings which limit the analog inputs. Instead, the digital inputs applied can go to 7V and are not restricted by the V_{DD} +0.3V limit as on the analog inputs. For example, if the AD7940 was operated with a V_{DD} of 3V, then 5V logic levels could be used on the digital inputs. However, it is important to note that the data output on SDATA will still have 3 V logic levels when V_{DD} = 3 V.

Another advantage of SCLK, and $\overline{CS}$ not being restricted by the V_{DD} + 0.3 V limit is the fact that power supply sequencing issues are avoided. If one of these digital inputs is applied before V_{DD} then there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3 V was applied prior to V_{DD}.

MODES OF OPERATION

The mode of operation of the AD7940 is selected by controlling the (logic) state of the $\overline{CS}$ signal during a conversion . There are two possible modes of operation, Normal Mode and Power-Down Mode. The point at which $\overline{CS}$ is pulled high after the conversion has been initiated will determine whether the AD7940 will enter Power-down Mode or not. Similarly, if already in Power-down then $\overline{CS}$ can control whether the device will return to Normal operation or remain in Power-down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements.

Normal Mode

This mode is intended for fastest throughput rate performance as the user does not have to worry about any power-up times with the AD7940 remaining fully-powered all the time. Figure 7 shows the general diagram of the operation of the AD7940 in this mode.

The conversion is iniated on the falling edge of $\overline{CS}$ as described in the Serial Interface section. To ensure the part remains fully powered up at all times $\overline{CS}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high any time after the 10th SCLK falling edge but before the 16th SCLK falling edge the part will remain powered up but the conversion will be terminated and SDATA will go back into tri-state. At least sixteen serial clock cycles are required to complete the conversion and access the complete conversion result. $\overline{CS}$ may idle high until the next conversion or may idle low until $\overline{CS}$ returns high sometime prior to the next conversion, (effectively idling $\overline{CS}$ low).

Once a data transfer is complete (SDATA has returned to tri-state), another conversion can be initiated after the quiet time, t_{quiet}, has elapsed by bringing $\overline{CS}$ low again.

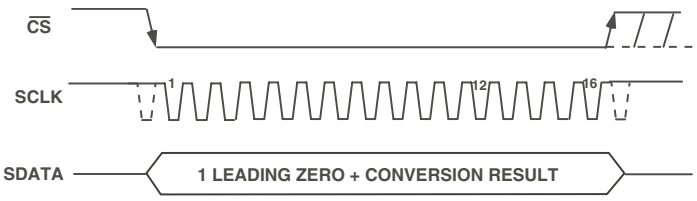


Figure 7. Normal Mode Operation

Power-Down Mode

This mode is intended for use in applications where slower throughput rates are required; either the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate and then the ADC is powered down for a relatively long duration between these bursts of several conversions. When the AD7940 is in power down, all analog circuitry is powered down.

To enter Power-Down, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the tenth falling edge of SCLK as shown in Figure 8. Once $\overline{CS}$ has been brought high in this window of SCLKs, then the part will enter power down and the conversion that was intiated by the falling edge of $\overline{CS}$ will be terminated and SDATA will go back into tri-state. If $\overline{CS}$ is brought high before the second SCLK falling edge, then the part will remain in Normal Mode and will not power-down. This will avoid accidental powerdown due to glitches on the $\overline{CS}$ line.

In order to exit this mode of operation and power the AD7940 up again, a dummy conversion is performed. On the falling edge of $\overline{CS}$ the device will begin to power up, and will continue to power up as long as $\overline{CS}$ is held low until after the falling edge of the tenth SCLK. The device will be fully powered up once at least 16 SCLKs (or approximately 6us) have elapsed and valid data will result from the next conversion as shown in figure 9. If $\overline{CS}$ is brought high before the tenth falling edge of SCLK, regardless of SCLK frequency, then the AD7940 will go back into power down again. This avoids accidental power up due to glitches on the $\overline{CS}$ line or an inadvertent burst of 8 SCLK cycles while $\overline{CS}$ is low. So although the device may begin to power up on the falling edge of $\overline{CS}$, it will power down again on the rising edge of $\overline{CS}$ as long as it occurs before the tenth SCLK falling edge.

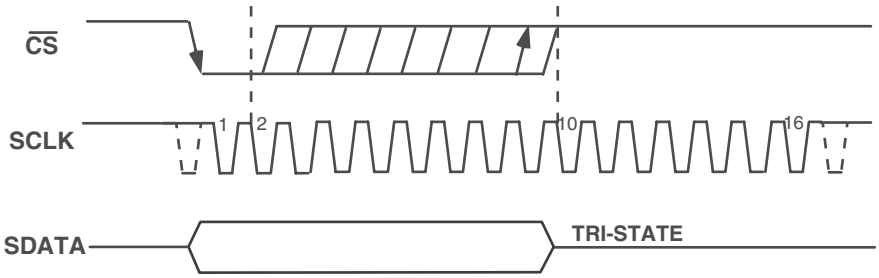


Figure 8. Entering Power Down Mode

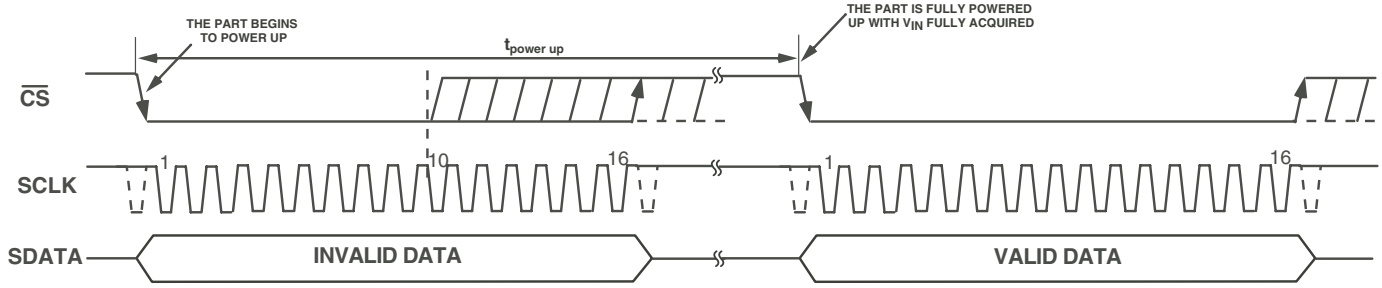


Figure 9. Exiting Power Down Mode

SERIAL INTERFACE

Figure 10 shows the detailed timing diagram for serial interfacing to the AD7940. The serial clock provides the conversion clock and also controls the transfer of information from the AD7940 during conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track and hold into hold mode, takes the bus out of tristate and the analog input is sampled at this point. The conversion is also initiated at this point and will require at least 16 SCLK cycles to complete. Once 15 SCLK falling edges have elapsed, then the track and hold will go back into track on the next SCLK rising edge as shown in Figure 10 at point B. On the 16th SCLK falling edge the SDATA line will go back into tristate. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed then the conversion will be terminated and the SDATA line will go back into tristate, otherwise SDATA returns to tri-state on the 16th SCLK falling edge as shown in Figure 10.

Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7940. $\overline{CS}$ going low provides the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges beginning with the 2nd leading zero, thus the first falling clock edge on the serial clock has the first leading zero provided and also clocks out the second leading zero. The data transfer will consist of two leading zeros followed by the fourteen bits of data. The final bit in the data transfer is valid on the sixteenth falling edge, having being clocked out on the previous (15th) falling edge.

It is also possible to read in data on each SCLK rising edge rather than falling edge as the SCLK cycle time is long enough to ensure the data is ready on the rising edge of SCLK. However, the first leading zero will still be driven by the $\overline{CS}$ falling edge and so can only be taken on the first SCLK falling edge. It may be ignored and the first rising edge of SCLK after the $\overline{CS}$ falling edge would have the second leading zero provided and the 15th rising SCLK edge would have DB0 provided. This method may not work with most Micros/DSPs, but could possibly be used with FPGAs and ASICs.

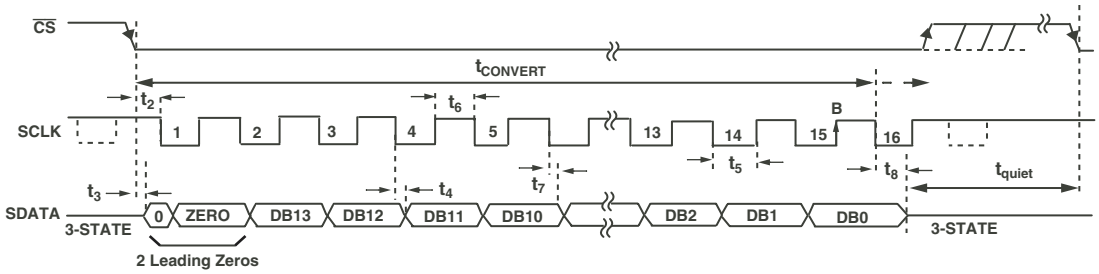


Figure 10. AD7940 Serial Interface Timing Diagram

MICROPROCESSOR INTERFACING

The serial interface on the AD7940 allows the part to be directly connected to a range of many different microprocessors. This section explains how to interface the AD7940 with some of the more common microcontroller and DSP serial interface protocols.

AD7940 to TMS320C541

The serial interface on the TMS320C541 uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices like the AD7940. The $\overline{CS}$ input allows easy interfacing between the TMS320C541 and the AD7940 without any glue logic required. The serial port of the TMS320C541 is set up to operate in burst mode with internal CLKX (TX serial clock) and FSX (TX frame sync). The serial port control register (SPC) must have the following setup:
FO = 0, FSM = 1, MCM = 1 and TXM = 1.
The format bit, FO, may be set to 1 to set the word length to 8-bits, in order to implement the power-down mode on the AD7940.

The connection diagram is shown in Figure 11. It should be noted that for signal processing applications, it is imperative that the frame synchronisation signal from the TMS320C541 will provide equidistant sampling.

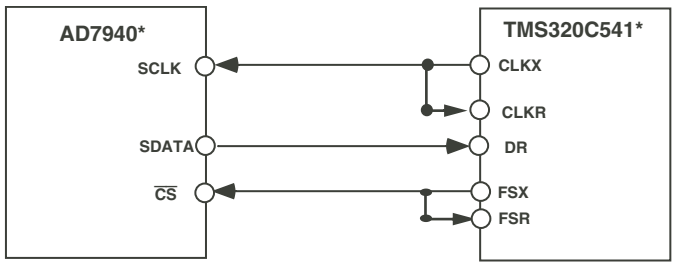


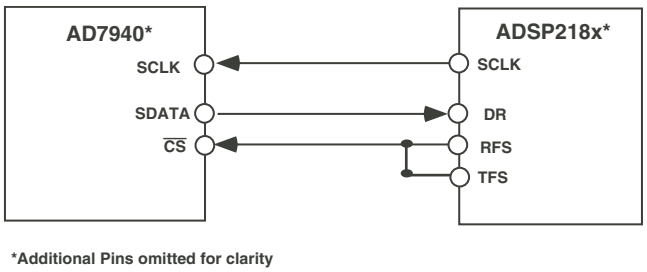
Figure 11. Interfacing to the TMS320C541

AD7476/AD7477 to ADSP218x

The ADSP218x family of DSPs are interfaced directly to the AD7940 without any glue logic required. The SPORT control register should be set up as follows:
TFSW = RFSW = 1, Alternate Framing
INVRFS = INVTFS = 1, Active Low Frame Signal
DTYPE = 00, Right Justify Data
SLEN = 1111, 16-Bit Data words
ISCLK = 1, Internal serial clock
TFSR = RFSR = 1, Frame every word
IRFS = 0,
ITFS = 1.
To implement the power-down mode SLEN should be set to 1001 to issue an 8-bit SCLK burst.
The connection diagram is shown in Figure 12. The ADSP218x has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in Alternate Framing Mode and the SPORT control register is set up as described. The frame synchronisation signal generated on the TFS is tied to $\overline{CS}$ and as with all signal processing applications equidistant sampling is necessary. However, in this example, the timer interrupt is used to control the sampling rate of the ADC and under certain conditions, equidistant sampling may not be acheived.

The Timer registers etc. are loaded with a value which will provide an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and hence the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instrustion to transmit with TFS is given, (i.e. AX0=TX0), the state of the SCLK is checked. The DSP will wait until the SCLK has gone High, Low and High before transmission will start. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, then the data may be transmitted or it may wait until the next clock edge.

For example, the ADSP2189 had a 20 MHz crystal, such that it had a master clock frequency of 40 MHz then the master cycle time would be 25 ns. If the SCLKDIV register is loaded with the value 3, a SCLK of 5 MHz is obtained, and 8 master clock periods will elapse for every 1 SCLK period. Depending on the throughput rate selected, if the timer register was loaded with the value, say 803, (803+1 = 804) then 100.5 SCLKs will occur between interrupts and subsequently between transmit instructions. This situation will result in non-equidistant sampling as the transmit instruction is occuring on a SCLK edge. If the number of SCLKs between interrupts is a whole integer figure of N, then equidistant sampling will be implemented by the DSP.

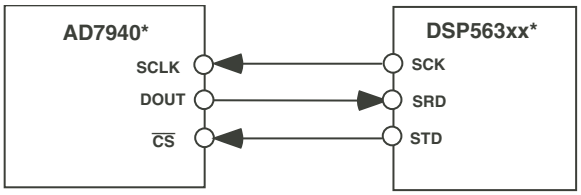


*Additional Pins omitted for clarity

Figure 12. Interfacing to the ADSP-218x

AD7940 to DSP563xx

The connection diagram in Figure 13 shows how the AD7940 can be connected to the ESSI (Synchronous Serial Interface) of the DSP563xx family of DSPs from Motorola. Each ESSI (2 on board) is operated in Synchronous Mode (SYN bit in CRB =1) with internally generated 1-bit clock period frame sync for both TX and RX (bits FSL1 =0 and FSL0 =0 in CRB). Normal operation of the ESSI is selected by making MOD = 0 in the CRB. Set the word length to 16 by setting bits WL1 =1 and WL0 = 0 in CRA. The FSP bit in the CRB should be set to 1 so the frame sync is negative. It should be noted that for signal processing applications, it is imperative that the frame synchronisation signal from the DSP563xx will provide equidistant sampling.
In the example shown in Figure 13 below, the serial clock is taken from the ESSI so the SCK0 pin must be set as an output, SCKD = 1.



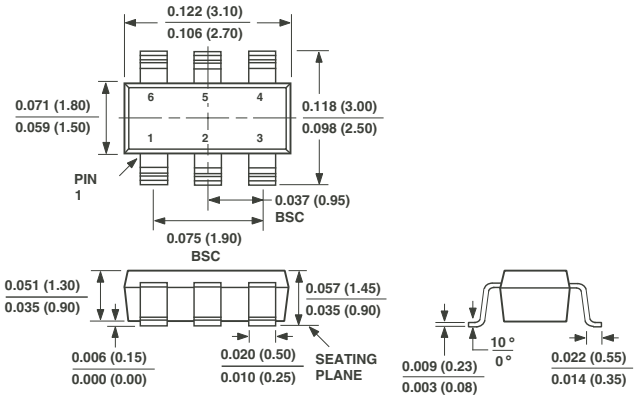
*Additional Pins omitted for clarity

Figure 13. Interfacing to the DSP563xx

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

6-lead SOT23 (RJ-6)



8-lead MSOP (RM-8)