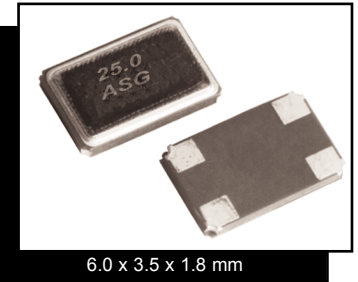


HC MOS/TTL COMPATIBLE • CERAMIC SURFACE MOUNT
CRYSTAL CLOCK OSCILLATORS
ASG and ASGL



FEATURES:

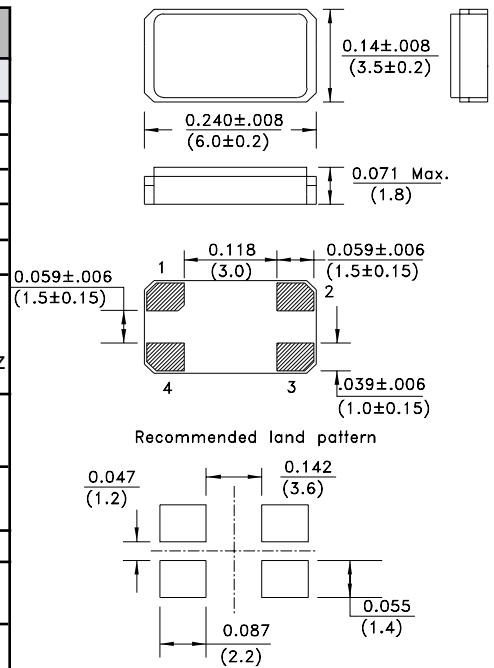
- Compact and low in height.
- Low current consumption
- Tristate Enable/Disable function.
- Suitable for high density SMT., Reflow capable.
- Tight stability option.
- Seam welding.

APPLICATIONS:

- CCD clock for VTR camera.
- Equipment.
- Thin equipment.

STANDARD SPECIFICATIONS

PARAMETERS	ASG	ASGL
Frequency Range (F ₀)	0.5MHz ~ 107MHz	0.5MHz ~ 125MHz
Operating Temperature (T _{OPR})	-10°C to +70°C (See Options)	
Storage Temperature (T _{STO})	-55°C to +125°C	
Frequency Stability (ΔF/F ₀)	±100ppm max. (See Options)	
Supply Voltage (V _{DD})	5.0Vdc ±10%	3.3Vdc ±10%
Input Current (I _{DD})	25mA max. for F < 40MHz 40mA max. for F < 70MHz 60mA max. for F ≤ 107MHz	20mA max. for F < 40MHz 35mA max. for F < 80MHz 50mA max. for F ≤ 125MHz
Duty Cycle or Symmetry	45/55% max. for F ≤ 50MHz 40/60% max. for F > 50MHz	40/60% max.
Rise and Fall Times (T _r / T _f)	10ns max. for F ≤ 40MHz 6ns max. for F > 40MHz	
Output Load	1.5pF (50pF max.)	5TTL or 15pF
Output Voltage (V _{OH}) (V _{OL})	0.9 * V _{DD} min. 0.1 * V _{DD} max.	
E/D Function (V _{IH}) (V _{IL})	"1" or Open: Oscillation ≥ 2.2V "0": Output disabled in high impedance (HiZ) < 0.8V	

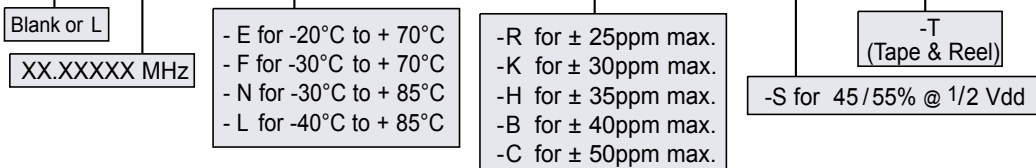


Connect a By-Pass capacitor 0.01 μF between V_{DD} and GND.
 Environmental, and mechanical specifications, see appendix C. Group 2.
 Marking, see appendix G. Test circuit, waveforms, see appendix B.
 Tape and Reel, see appendix H.(1,000 pcs/reel). Reflow profile, see appendix E.
 Application notes, see appendix A. Recommended handling, see appendix F.

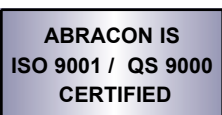
Dimensions: Inches (mm)

ORDERING OPTIONS

ASG X - Frequency - Temperature - Overall Frequency Stability - Duty Cycle - Packaging



PIN NO.	FUNCTION
1	Tristate E/D
2	GND / Case
3	Output
4	V _{DD}



NOTE: Left blank if standard • All specifications and markings subject to change without notice

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