C-5™ Network Processor Data Sheet

Supporting C-5 Network Processor Version D0

C-PORT™
A Motorola Company

Feature List

Complete programmability

- Programmability at all levels of the protocol stack: Layers 2-7
- Examples of C-5 enabled systems:
  - Multiservice Access Platforms (MSAPs)
  - Optical edge switch/routers
  - IP Gigabit/Terabit routers
  - WAN Customer Premises Equipment (CPE)
  - Load balancing web server switches

Simple programming model

- C/C++ programmable
- Standard instruction set
- Standard Applications Programming Interface (C-Ware API™)
- Comprehensive C-Ware™ Software Toolset (easy to program, debug, and tune applications)

Maximum system flexibility

- Software implementation of functions from physical interfaces through switching fabric support
- Reprogram to support new functionality and ratified standards, improving your time-in-market™ metric
- Deliver new services to market through simple software upgrades — no forklift

Massive processing power

- Operating frequencies: 166MHz, 200MHz, and 233MHz
- 5Gbps of bandwidth (for non-blocking throughput)
- More than 3,000MIPs of computing power (for adding services throughout the protocol stack)
- Up to 15 million packets per second transmitted at wire speed
- 17 programmable RISC Cores (for cell/packet forwarding)
- 32 programmable Serial Data Processors (for processing bit streams)
- Up to 133 million table lookups per second
- Three internal buses for 60Gb of aggregate bandwidth

High functional integration

- 838 pin Ball Grid Array (BGA) package
- 16 Channel Processors including:
  - Embedded OC-3c, OC-12, OC-12c SONET framers
  - Programmable MAC interface
  - RISC Cores
  - Programmable pin PHY interfaces
- Embedded coprocessors for table lookup (classification), buffer memory (payload control), and queue management (CoS/QoS implementation)
- Dedicated Fabric Processor and port
- Embedded RISC Executive Processor
- Integrated 32bit/66MHz PCI bus

Stable programming interfaces

- Supports generic communications programming interfaces to simplify programming and allow future reuse of code across generations of the processor
- Network Processing Forum (NPF), (formerly CPIX), Charter member

Third-party support

- Support for virtually any third-party protocol stack, PHY or fabric interface, and industry standard tools
- Smart Networks Alliance Program ensures a wide range of verified solutions

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About This Guide

Data Sheet Description and Organization

This data sheet describes the C-5 Network processor, Version D0. It provides hardware layout specifications including pinouts, memory configuration guidelines, timing diagrams, power and power sequencing guidelines, thermal design guidelines, and mechanical specifications.

The data sheet is divided into the following topics:

- Functional Description
- Signal Descriptions
- Electrical Specifications
- Mechanical Specifications

Revision History

Table 1 shows the revision history for this data sheet, providing a description of the changes.

Table 1 C-5 Network Processor Data Sheet Revision History

Revision Date	Change	Page No.
March 10, 2000	First printing for the C-5 NP.	

Table 1 C-5 Network Processor Data Sheet Revision History

Revision Date	Change	Page No.
June 12, 2000	Chapter 2 contains the following revisions:	
	• LVTTL and LVPECL specifications have been added.	17
	• Several of the tables listing pin configurations have had their descriptions updated. Check each application's configuration table as required.	18 - 39
	• CPn3+1 is RCLKN (5/25/00), not NC (3/10/00)	25
	• Mechanism for EPROM signaling has changed.	31
	• XPUHOT functionality is clarified	
	• QCPA is a NC (5/25/00), not Address Parity (3/10/00)	31
	• The power and ground connections illustration has been updated.	36
	Chapter 3 contains the following revisions:	38
	• Many values listed in individual timing diagrams and specification tables have updated or corrected. Check each specification table as required.	61 - 78
	• Low speed serial interface timing specifications have been added.	71
	• PROM I/F timing specifications are changed	72
June 14, 2000	QMU timing specification for Tqdo has been changed from 2.2 to 1.5.	77
July 17, 2000	Updated BMU section to reflect change to external Pipeline Architecture, Single Data Rate Synchronous DRAM.	12
August 8, 2000	Operating temperatiure range added.	54
	Power sequencing diagram updated.	56
	BMU timing diagram updated.	75
	TLU timing diagram updated.	77
	QMU timing diagram updated.	78

Table 1 C-5 Network Processor Data Sheet Revision History

Revision Date	Change	Page No.
March 26, 2001	Chapter 1 contains the following revisions:	Thru-out
	• Fabric Processor Interface Frequency changed from 100 MHz to 110 MHz thruoughout.	
	• TLU interface memory was incorrectly noted at 64 MBytes. Changed to 32 MBytes. The maximum amount of memory supported by the TLU is 32MBytes in four banks.	18
	Chapter 2 contains the following revisions:	19
	• Buffer Management Unit (BMU) has 161 pins	
	• Added Figure 5. PROM Interface Timing Outline	21
	• Added Figure 7. Observe-Only Cell	37
	• Added Figure 8. Cell Design That Can Be Used for Both Input and Output Pins	57
	• PROM Interface Timing Outline added.	
	• Numerous changes in tables 17, 18 and 19	36
	• Data lines incorrectly noted at 128. The useful configuration is 139 data lines and all 12 address lines.	39, 40
	• The TLU SRAM interface was incorrectly noted at 64 MBytes. Changed to 32 MBytes.	41
	Chapter 3 contains the following revisions:	42
	• Table 40, Gigabit Ethernet (TBI) Timing Description, Tcgr min value of -1.0 removed.	
	• Figure 16, OC 12 Clock Duty Cycle was added	71
	• Tc12d added to Table 42	73
	• Figure 17, Executive Processor PCI Timing Diagram PGNTX is only an input. PGNTX Output removed.	73
	• Tpgo, Tpgz, Tpgv removed from Table 43.	74
	Chapter 4 contains the following revisions:	75
	• Mechanical specs changed.	

Table 1 C-5 Network Processor Data Sheet Revision History

Revision Date	Change	Page No.
October 1, 2001	Chapter 2 contains the following revisions:	
	• LVTTL and LVPECL conform to the JEDEC JESD8-BSpecification	23
	• Table 3 changed to note LVPECL differential signal	23
	• Table 10 LVPECL change	31
	• Table 11 CP*n*_6 and CP*n+1*_6 changed	31
	• Table 21 changed to reflect pin G14 used for signal MDQML	32
	• Table 27 changed to reflect total number of NC pins for D0	42
	• Table 28 changed to reflect G14 receiving signal MDQML	48
	• C-Port web site support address added	61
	Chapter 3 contains the following revisions	
	• Table 32 Storage / max junction temperatures added	63
	• Table 34 LVPECL high and low voltage min / max added	65
	• Table 36 Power dissipation, P_D min, max, typical changed	67
	Chapter 4 contains the following revisions	
	• Added "Marking Codes"	91
	• Added "Reflow" profile	91
January 21, 2002	Chapter 1 contains the following revisions:	
	• Table 2 contain revised TLU SRAM Configuration specifications	19
	Chapter 2 contains the following revisions:	
	• TLU SRAM Interface Signals: Table 22 and Table 23 changed to reflect Memory Bank Selection	44
	Chapter 3 contains the following revisions:	
	• Table 48, Table 49 and Table 51 contain revised timing specifications	84 thru 86

Chapter 1

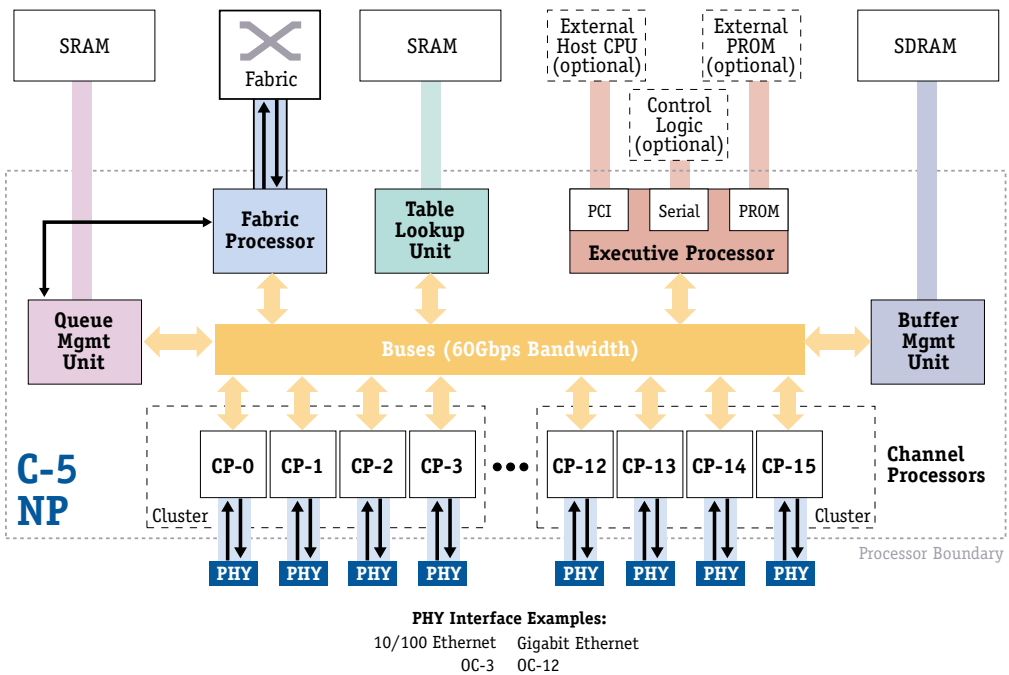
Functional Description

Block Diagram

The C-5™ network processor, has an architecture specifically designed for networking applications. Figure 1 shows a block diagram of the C-5 NP, including its potential external interfaces. The following sections describe each component of the C-5 NP.

For more information about the architecture of the C-5 NP, see the *C-5 Network Processor Architecture Guide*.

Figure 1 C-5 Network Processor Block Diagram



The main components of the C-5 NP are:

- Channel Processors
- Executive Processor
- Fabric Processor
- Buffer Management Unit
- Table Lookup Unit
- Queue Management Unit

Channel Processors

The C-5 NP contains sixteen programmable Channel Processors (CPs) that receive, process, and transmit network data. The number of CPs per port is configurable, depending on the line interface. Typically one CP is assigned to each port for medium bandwidth applications (Fast Ethernet to OC-3). Multiple CPs can be assigned to a port in a configuration called *channel aggregation* in high bandwidth applications (greater than OC-3). Multiple logical ports can be assigned to a single CP, with the addition of an external multiplexor, for low bandwidth applications, such as DS1 to DS3.

The C-5 NP's architecture supports a variety of industry-standard serial and parallel protocols and individual port data rates including:

- 10Mb Ethernet (RMII)
- 100Mb Ethernet (RMII)
- 1Gb Ethernet (GMII and TBI)
- OC-3
- OC-12
- DS1/DS3, supported through the use of external framers/multiplexors

The C-5 NP's programmability can also support a variety of special interfaces, such as various xDSL encapsulations and proprietary protocols.

Key components of each CP are a RISC Core (CPRC) that orchestrates cell/packet processing and a set of microprogrammable, special-purpose processors, called Serial Data Processors (SDPs), that provide features such as Ethernet MAC and SONET framing, multichannel HDLC, and ATM cell delineation. This means you usually only need to include PHYs to complete the system.

Executive Processor

The Executive Processor (XP) serves as a centralized computing resource for the C-5 NP and manages the system interfaces.

The XP performs conventional supervisory tasks in the C-5 NP, including:

- Reset and initialization of the C-5 NP
- Program loading and control of CPs
- Centralized exception handling
- Management of a host interface through the PCI
- Management of system interfaces (PCI, Serial Bus, PROM)

System Interfaces

The system interfaces to the XP are:

- **PCI** — Provides an industry standard 32bit 33/66MHz PCI channel used for chip-level shared resources. The PCI has both *initiator* and *target* capabilities. The PCI interface is typically connected to a host processor.
- **Serial Bus Interface** — Provides a general purpose bi-directional, two-wire serial bus and I/O port that allows the C-5 NP to control external logic with either of two standard protocols:
  - The **MDIO (high-speed) protocol**: uses a 16bit data format with 10bits of addressing and supports transfers up to 25MHz.
  - The **low-speed protocol**: uses an 8bit data format followed by an acknowledge bit and supports transfers up to 400kbps.

  Software is used to select which protocol to use, by setting the appropriate bits in the Serial Bus Configuration Register. When a serial bus transfer is active, an external pin is driven by the C-5 NP to indicate which protocol is being used (SPLD=0 indicates MDIO protocol; SPLD=1 indicates low-speed protocol).

  Both SIDA and SICL are bi-directional lines that are connected, via an external pull-up resistor, to a positive supply voltage. When the bus is free, both lines are HIGH because of the pull-up resistor. The output stages of the devices connected to the bus must have either an open-drain or open-collector in order to perform the wired-AND function required for its arbitration mechanism.
- **PROM Interface** — Allows the XP to boot from nonvolatile, flash memory. The PROM interface is a low-speed, serial I/O port that runs at $^1/_2$ to $^1/_{16}$ the core clock rate. The maximum PROM size is 8MBytes, and a 16bit wide configuration is required. External

board logic is required to perform serial-to-parallel conversion for PROM address outputs and parallel-to-serial conversion for PROM data inputs.

Fabric Processor

The Fabric Processor (FP) acts as a high-speed network interface port with advanced functionality. It allows the C-5 NP to interface to an application-specific switching solution internal to your design. The FP port supports the bidirectional transfer of packets, frames, or cells from the C-5 NP to a hardware interface that provides connectivity to other network processors or other similar line processing hardware. There are numerous parameters that can be configured within the FP to allow the interface to be adapted to different fabric protocols. The FP is Utopia-1, 2 and Utopia-3, IBM PRIZMA, and PowerX (Csix-L0) compatible.

The FP can be configured to run at any frequency up to 110MHz, and the receive and transmit data buses are 16 or 32 bits wide. This allows a wide range of supported bandwidths to and from the switching fabric, all the way up to 3200Mbps full duplex bandwidth.

Buffer Management Unit

The Buffer Management Unit (BMU) interfaces the C-5 NP to external pipeline architecture, Single Data Rate Synchronous DRAM. The external memory is partitioned and used as buffers for receiving and transmitting data between CPs, the FP, and the XP. It is also used as second level storage in the XP memory hierarchy.

The interface to an array of SDRAM chips is 139bits wide, composed of 128 data bits, two internal control bits, and nine SECDED (single error correction-double error detection) ECC (error correction code) bits. The interface is compliant with the PC100 standard and operates at up to 125MHz with 3.3V LVTTL-compatible inputs and outputs. The refresh period, Trcd, Tcas, Trp, Tmrd, and Trc are configurable via boot time configuration (see the *C-5 Network Processor Architecture Guide* for more details).

The C-5 NP uses auto-refresh mode and the interface, (which is not configurable), transfers four bits of data for each read and write using a sequential burst type.

Some of these parameters are programmed into the SDRAMs' mode register and can be applied only once per power cycle. The ECC functionality can be enabled or disabled via configuration register writes.

If needed, the interface can narrowed to 128bits by disabling ECC and providing board pull-ups for the two control bits and nine ECC bits. This is useful if DIMMs are used in the board design. If individual SDRAM parts are used, x16 and x32 are supported. The BMU

supports SDRAM devices that use 12 address lines. Internal address calculation paths limit the maximum memory size to 128MBytes. Only one physical bank of SDRAM is supported.

Table Lookup Unit

The Table Lookup Unit (TLU) performs table lookups in external SRAM. It can also be used for statistics accumulation and retrieval and as general data storage. The TLU simultaneously supports multiple application-defined tables and multiple search strategies, such as those needed for routing, circuit switching, and QoS lookup tasks.

The C-5 NP uses external 64bit wide ZBT Pipelined Bursting Static RAM (SRAM) modules (at frequencies to 133MHz) for storage of its tables. These modules allow implementation of tables with 2^{20} x 64bit entries at a cycle time of up to 7.5 nanoseconds using 4Mbit SRAM technology. The maximum amount of memory supported by the TLU is 32MBytes in four banks.

Table 2 TLU SRAM Configurations

SRAM Technology*	Min Table Size (One Bank)	No. of Parts	Maximum Table Size (Four Banks)	No. of Parts
1Mbit (32k x 32)	256kBytes	2	1MBytes	8
2Mbit (64k x 32)	512kBytes	2	2MBytes	8
4Mbit (256k x 18)	2MBytes	4	8MBytes	16
8Mbit (512k x 18	4MBytes	4	16MBytes	16
16Mbit (1M x 18)	8MBytes	4	32MBytes	16

* For (n x 32) parts, divide total memory and number of parts by two.

External Mode

There is support for external devices. Refer to the *C-5e Archictecture Guide*.

Queue Management Unit

The Queue Management Unit (QMU) autonomously manages a number of application-defined descriptor queues. It handles inter-CP and inter-C-5 NP descriptor flows by providing switching and buffering. It also performs descriptor replication for multicast applications. A number of queues can be assigned to each CPRC for QoS-based services.

The QMU provides a queuing engine internal to the chip and uses external SRAM to store the descriptors. Scheduling is done by the CPs. The QMU supports up to 512 queues and 16, 384 descriptor buffers. A descriptor buffer holds an application-defined "descriptor",

which is a structure that defines the payload buffer handle and other attributes of the forwarded cell or packet.

The QMU's external SRAM interface uses ZBT synchronous SRAMs organized in a single bank of up to 128k, 32bit words. This interface runs at half ($^1/_2$) the core clock frequency.

Chapter 2

Signal Descriptions

Signal Summary

There are ten functional groupings of signals in the C-5 network processor:

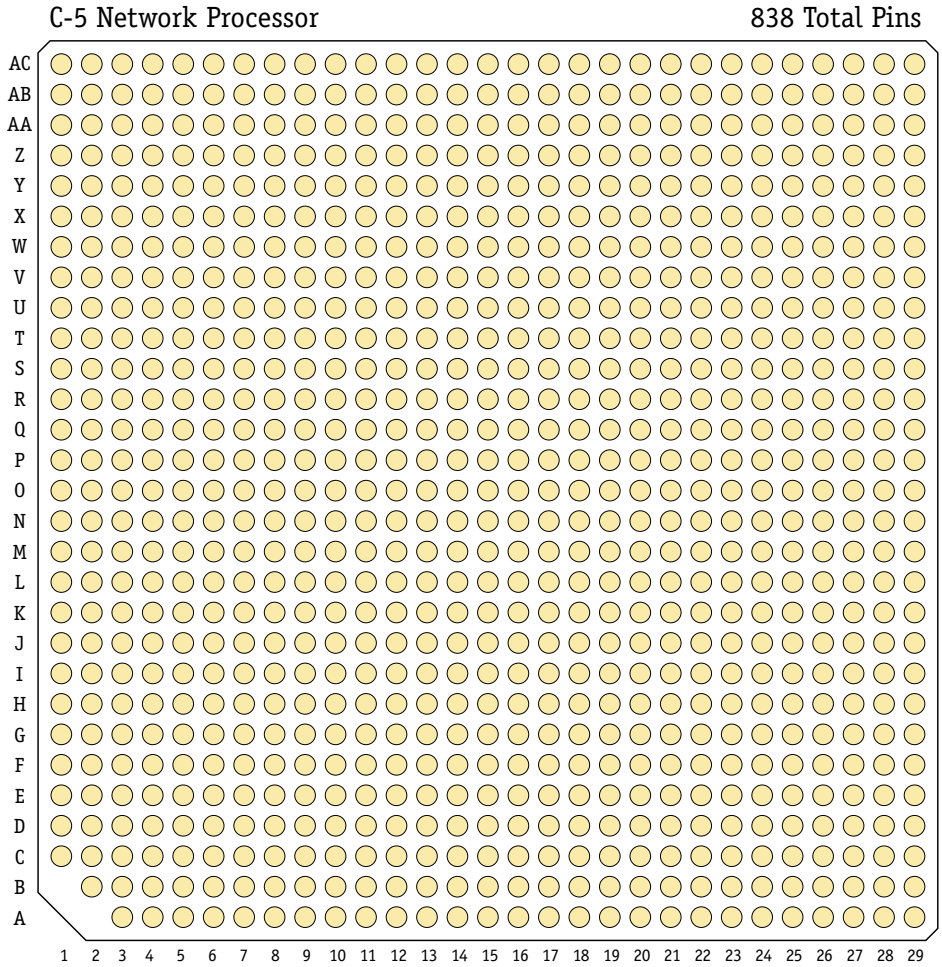
- Clock — 11 pins
- Channel Processors (CP0 - CP15) — 16x7 = 112 pins
- Executive Processor (XP) — 57 pins
  - PCI Interface — 50 pins
  - PROM Interface — 4 pins
  - Serial Bus Interface — 2 pins
  - General System Interface — 1 pin
- Fabric Processor (FP) — 80 pins
- Buffer Management Unit (BMU) — 161 pins
- Table Lookup Unit (TLU) — 100 pins
- Queue Management Unit (QMU) — 55 pins
- Power — 233 pins
- Test — 18 pins
- No connection (NC) — 11 pins

Two of the sections (CPs and FP) are configurable, depending on the type of device being implemented.

Pinout Diagram

The C-5 NP contains 838 pins as shown in Figure 2. These pin numbers are referenced throughout the remaining chapter.

Figure 2 Pin Locations (Bottom View)



Pin Descriptions Grouped by Function

The C-5 NP pins are categorized in groups, reflecting interfaces to the chip:

- Clock Signals
- CP Interface Signals
- Executive Processor System Interface Signals
- Fabric Processor Interface Signals
- BMU SDRAM Interface Signals
- TLU SRAM Interface Signals
- QMU SRAM Interface Signals
- Power Supply Signals
- Test Signals
- No Connection Pins

LVTTL and LVPECL Specifications

C-5 NP pins are the following types:

- Low Voltage TTL-Compatible (LVTTL). The C-5 NP's LVTTL pins conform to the JEDEC JESD8-B specification.
- Low Voltage Positive Emitter Coupled Logic (LVPECL). The C-5 NP's LVPECL pins conform to the JEDEC JESD8-2 specification.

Clock Signals

Table 3 describes the C-5 NP clock signals.

Table 3 Clock and Reference Signals

Signal Name	Pin #	Total	Type	I/O	Signal Description
SCLK* SCLKX*	H15 G15	1 1	LVPECL LVPECL	I I	Core Clock Rate (Differential)
CCLK0	K12	1	LVTTL	I	1_544MHZ_CLK (T1)†
CCLK1	J13	1	LVTTL	I	2_048MHZ_CLK (E1)†
CCLK2	J15	1	LVTTL	I	34_368MHZ_CLK (E3)†
CCLK3	I12	1	LVTTL	I	44_736MHZ_CLK (T3)†
CCLK4	I14	1	LVTTL	I	50MHZ_CLK (100Mbit Ethernet)†
CCLK5	H13	1	LVTTL	I	106_25MHZ_CLK (Fibre Channel)†

Table 3 Clock and Reference Signals (continued)

Signal Name	Pin #	Total	Type	I/O	Signal Description
CCLK6	K14	1	LVTTL	I	125MHZ_CLK (Gigabit Ethernet)†
CCLK7	K16	1	LVTTL	I	155_52MHZ_CLK (OC-3)†
CPREF‡	L13	1	LVPECL	I	Reference
Total		**11**			

* SCLK and SCLKX must not be AC-coupled.

† The frequencies specified for CCLK0 - CCLK7 allow full flexibility for the C-5 NP. Clock inputs associated with a specific protocol should be wired to ground when that protocol is not used by the C-5 NP. It is also possible to use one or more CCLK*n* inputs for other frequencies. Contact your C-Port representative for more information.

‡ If any of the CPs are configured for LVPECL operation (OC3) using the pin mode registers, then CPREF must be wired to an external reference, as specified in Table 34 on page 65. If none of the CPs are configured for LVPECL operation, then the CPREF pin can be left unconnected. It is acceptable to tie the CPREF pin high or low through a resistor, or into the specified reference, but this is not required.

CP Interface Signals

The C-5 NP's 16 CPs support various network physical interfaces, providing a serial interface to the PHY layer. Interfaces are configured via bits in the C-5 NP register set. Many interfaces are possible by programming the configuration registers. CPs can be used individually or in a cluster (four CPs) to implement the various interfaces.

Table 4 provides a quick reference of all the CP pins organized by clusters. There are seven physical I/O pins associated with each CP. All pins are capable of receiving data, with some configurable to be input clocks, output clocks, or data drivers. In addition, pairs of pins can be configured as differential pairs for LVPECL compatibility.

In the case of RMII, OC-3, DS1, and DS3, the drivers and receivers at the pin are locally configured to match the relevant PHY or Framer chip. OC-12 uses the aggregation of four CPs (one cluster), while GMII and Ten Bit Interface (TBI) can use either eight CPs (four for receive and four for transmit) or four CPs that share the transmit and receive functions for non-wire speed applications.

During CP aggregation, all 28 pins associated with a cluster are routed to all of the Serial Data Processors (SDPs) in that cluster. This allows round-robin usage of portions of the SDPs, with each getting access to the necessary I/O pins.

The signals for the following CP physical interfaces are included in this section:

- DS1/T1 Framer Interface Configuration
- 10/100 Ethernet (RMII) Configuration

- Gigabit Ethernet (GMII) Configuration
- Gigabit Ethernet and Fibre Channel TBI Configuration
- SONET OC-3 Transceiver Interface Configuration
- SONET OC-12 Transceiver Interface Configuration

Table 4 CP Physical Interface Signals and Pins (Grouped by Clusters)

CP Cluster 1		CP Cluster 2		CP Cluster 3		CP Cluster 4	
Signal	**Pin #**	**Signal**	**Pin #**	**Signal**	**Pin #**	**Signal**	**Pin #**
CP0_0	AC28	CP4_0	AB22	CP8_0	Z29	CP12_0	Y28
CP0_1	AC26	CP4_1	AB21	CP8_1	Z28	CP12_1	Y26
CP0_2	AC24	CP4_2	AB20	CP8_2	Z27	CP12_2	Y24
CP0_3	AC22	CP4_3	AB19	CP8_3	Z26	CP12_3	Y22
CP0_4	AC20	CP4_4	AB18	CP8_4	Z25	CP12_4	Y20
CP0_5	AC18	CP4_5	AB17	CP8_5	Z24	CP12_5	Y18
CP0_6	AC16	CP4_6	AB16	CP8_6	Z23	CP12_6	Y16
CP1_0	AC02	CP5_0	AB08	CP9_0	Z01	CP13_0	Y02
CP1_1	AC04	CP5_1	AB09	CP9_1	Z02	CP13_1	Y04
CP1_2	AC06	CP5_2	AB10	CP9_2	Z03	CP13_2	Y06
CP1_3	AC08	CP5_3	AB11	CP9_3	Z04	CP13_3	Y08
CP1_4	AC10	CP5_4	AB12	CP9_4	Z05	CP13_4	Y10
CP1_5	AC12	CP5_5	AB13	CP9_5	Z06	CP13_5	Y12
CP1_6	AC14	CP5_6	AB14	CP9_6	Z07	CP13_6	Y14
CP2_0	AB29	CP6_0	AA28	CP10_0	Z22	CP14_0	X29
CP2_1	AB28	CP6_1	AA26	CP10_1	Z21	CP14_1	X28
CP2_2	AB27	CP6_2	AA24	CP10_2	Z20	CP14_2	X27
CP2_3	AB26	CP6_3	AA22	CP10_3	Z19	CP14_3	X26
CP2_4	AB25	CP6_4	AA20	CP10_4	Z18	CP14_4	X25
CP2_5	AB24	CP6_5	AA18	CP10_5	Z17	CP14_5	X24
CP2_6	AB23	CP6_6	AA16	CP10_6	Z16	CP14_6	X23
CP3_0	AB01	CP7_0	AA02	CP11_0	Z08	CP15_0	X01
CP3_1	AB02	CP7_1	AA04	CP11_1	Z09	CP15_1	X02
CP3_2	AB03	CP7_2	AA06	CP11_2	Z10	CP15_2	X03

Table 4 CP Physical Interface Signals and Pins (Grouped by Clusters) (continued)

CP Cluster 1		CP Cluster 2		CP Cluster 3		CP Cluster 4	
Signal	**Pin #**	**Signal**	**Pin #**	**Signal**	**Pin #**	**Signal**	**Pin #**
CP3_3	AB04	CP7_3	AA08	CP11_3	Z11	CP15_3	X04
CP3_4	AB05	CP7_4	AA10	CP11_4	Z12	CP15_4	X05
CP3_5	AB06	CP7_5	AA12	CP11_5	Z13	CP15_5	X06
CP3_6	AB07	CP7_6	AA14	CP11_6	Z14	CP15_6	X07

DS1/T1 Framer Interface Configuration

Table 5 describes the serial framer interface signals. For each CP (0-15), you can implement one serial Framer interface.

Table 5 DS1/T1 Framer Interface Signals

Signal Name*	Pin #†	Total	Type	I/O	Label	Signal Description
CP*n*_0	Table 4	1	LVTTL	O	TCLK	Transmit Clock (1.544MHz)
CP*n*_1	Table 4	1	LVTTL	I	RCLK	Receive Clock (1.544MHz)
CP*n*_2	Table 4	1	LVTTL	O	TData	Transmit Data
CP*n*_3	Table 4	1	LVTTL	O	TFrame	Transmit Frame Synchronization
CP*n*_4	Table 4	1	LVTTL	I	RData	Receive Data
CP*n*_5	Table 4	1	LVTTL	I	RFrame	Receive Frame Synchronization
CP*n*_6	Table 4	1	nc	nc	nc	nc
Total Pins		**7**				

* *n* can be from 0 to 15. See Table 4.

† Reference Table 4 for pin numbers for the actual cluster(s) you are configuring.

10/100 Ethernet (RMII) Configuration

Table 6 describes the 10/100BASE-T Ethernet Reduced Media Independent Interface (RMII) signals. For each CP (0-15), you can implement one 10/100 Ethernet interface.

Table 6 10/100 Ethernet Signals

Signal Name*	Pin #	Total	Type	I/O	Label	Signal Description
CP*n*_0	Table 4	1	LVTTL	O	REF_CLK	Transmit and Receive Clock (50MHz)
CP*n*_1	Table 4	1	LVTTL	I	CRS_DV	Carrier Sense (CRS)/ Receive Data Valid (RX_DV). CRS indicates that traffic is on the link, and is asserted if the signal is a 1 or an alternating 1010... RX_DV indicates that a receive frame is in progress and the data present on the RXD pins is valid. It is asserted if this signal is a 1 for more than one cycle.
CP*n*_2	Table 4	1	LVTTL	O	TXD(0)	Transmit Data 0 (first on wire)
CP*n*_3	Table 4	1	LVTTL	O	TXD(1)	Transmit Data 1 (second on wire)
CP*n*_4	Table 4	1	LVTTL	I	RXD(0)	Receive Data 0 (first on wire)
CP*n*_5	Table 4	1	LVTTL	I	RXD(1)	Receive Data 1 (second on wire)
CP*n*_6	Table 4	1	LVTTL	O	TX_EN	Transmit Enable. When asserted, the data on TXD is encoded and transmitted on the twisted pair cable.
Total Pins		**7**				

* *n* can be from 0 to 15. See Table 4.

Gigabit Ethernet (GMII) Configuration

Gigabit Ethernet Media Independent Interface (GMII) is configured in one of two ways:

1. Use one CP cluster when density is more important than wire-speed performance because you can then implement up to four Gigabit Ethernet ports per C-5 NP.
2. Use two CP clusters for wire-speed performance and additional processing power. You can implement up to two Gigabit Ethernet ports per C-5 NP.

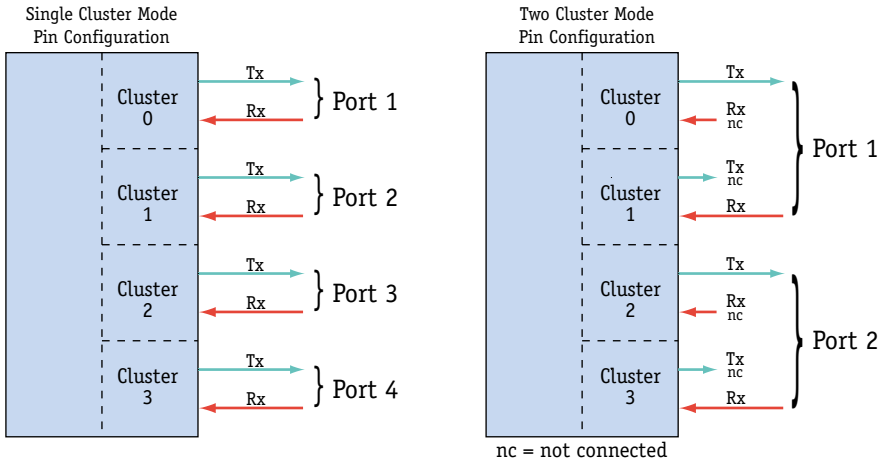
Table 7 lists the possible CP cluster combinations you can use and Figure 3 shows receive and transmit pin configurations by cluster. Table 8 lists the signals and pinouts for Gigabit Ethernet (GMII).

Table 7 Transmit and Receive Pin Combinations for Gigabit Ethernet and Fibre Channel

Cluster	Single Cluster Mode (TBI or GMII)	Two Cluster Mode (GMII)*
0	Port 1 Tx and Rx	Port 1 Tx
1	Port 2 Tx and Rx	Port 1 Rx
2	Port 3 Tx and Rx	Port 2 Tx
3	Port 4 Tx and Rx	Port 2 Rx

* The Two Cluster Mode column lists typical configurations. Any cluster can be set up to either receive or transmit. So you could configure a dual cluster mode where cluster 0 receives and cluster 3 transmits.

Figure 3 GMII/TBI Transmit and Receive Pin Configurations



The unused CP pins in the two cluster configurations should be wired to ground using a resistor.

Table 8 Gigabit Ethernet (GMII/MII) Signals One Cluster Example

Signal Name*	Pin #†	Total	Type	I/O	Label	Signal Description
CP*n*_0	Table 4	1	LVTTL	O	T_CLK	GMII Transmit Clock (125MHz). This clock is used to synchronize the transmit data.
CP*n*_1	Table 4	1	LVTTL	I	TCLKI	MII transmit clock. Transmit data aligned to this clock input from phy in MII mode. 25 Mhz in 100BaseT, 2.5 in Mhz in 10BaseT
CP*n*_2	Table 4	1	LVTTL	O	TXD(0)	Transmit Data (byte-wide data, least significant bit)
CP*n*_3	Table 4	1	LVTTL	O	TXD(1)	Transmit Data
CP*n*_4	Table 4	1	LVTTL	O	TXD(2)	Transmit Data
CP*n*_5	Table 4	1	LVTTL	O	TXD(3)	Transmit Data
CP*n*_6	Table 4	1	LVTTL	O	TX_EN	Transmit Enable. When asserted, the data on TXD is encoded and transmitted on the twisted pair cable.
CP*n+1*_0	Table 4	1	nc	nc	nc	nc
CP*n+1*_1	Table 4	1	LVTTL	I	COL	Collision. Asserted when both RX_DV and TX_EN are valid during half duplex operation.
CP*n+1*_2	Table 4	1	LVTTL	O	TXD(4)	Transmit Data
CP*n+1*_3	Table 4	1	LVTTL	O	TXD(5)	Transmit Data
CP*n+1*_4	Table 4	1	LVTTL	O	TXD(6)	Transmit Data
CP*n+1*_5	Table 4	1	LVTTL	O	TXD(7)	Transmit Data (byte-wide receive data, most significant bit)

Table 8 Gigabit Ethernet (GMII/MII) Signals One Cluster Example (continued)

Signal Name*	Pin #†	Total	Type	I/O	Label	Signal Description
CP*n+1*_6	Table 4	1	LVTTL	O	TX_ER	Transmit Error. Asserting TX_ER when TX_EN is a 1 causes transmission of the designated "bad code" in lieu of the normal encoded data on the twisted pair data.
CP*n+2*_0	Table 4	1	nc		nc	nc
CP*n+2*_1	Table 4	1	LVTTL	I	RCLK	Receive Clock (125MHz)
CP*n+2*_2	Table 4	1	LVTTL	I	RXD(0)	Receive Data (byte-wide receive data, least significant bit)
CP*n+2*_3	Table 4	1	LVTTL	I	RXD(1)	Receive Data
CP*n+2*_4	Table 4	1	LVTTL	I	RXD(2)	Receive Data
CP*n+2*_5	Table 4	1	LVTTL	I	RXD(3)	Receive Data
CP*n+2*_6	Table 4	1	LVTTL	I	RX_DV	Receive Data Valid. Indicates that there is a receive frame in progress and that the data present on the RXD signals is valid.
CP*n+3*_0	Table 4	1	nc	nc	nc	nc
CP*n+3*_1	Table 4	1	LVTTL	I	CRS	Carrier Sense. Indicates traffic is on the link. CRS is asserted when a non-idle condition is detected on the receive data stream. CRS is deasserted when an end of frame or idle condition is detected.
CP*n+3*_2	Table 4	1	LVTTL	I	RXD(4)	Receive Data
CP*n+3*_3	Table 4	1	LVTTL	I	RXD(5)	Receive Data
CP*n+3*_4	Table 4	1	LVTTL	I	RXD(6)	Receive Data
CP*n+3*_5	Table 4	1	LVTTL	I	RXD(7)	Receive Data (most significant bit)
CP*n+3*_6	Table 4	1	LVTTL	I	RX_ER	Receive Error Detected. Indicates that there has been an error received in the receive frame.
Total Pins		**28**				

* n can be 0, 4, 8, or 12.

† Reference Table 4 for pin numbers for the actual cluster(s) you are configuring.

Gigabit Ethernet and Fibre Channel TBI Configuration

1000BASE-T Gigabit Ethernet and Fibre Channel TBI is implemented in much the same way as Gigabit Ethernet (GMII). Table 7 shows the possible CP pin combinations you can use and Figure 3 shows receive and transmit pin configurations by cluster. Table 9 shows the signals and pinouts for a single cluster for Gigabit Ethernet and Fibre Channel TBI.

The unused pins for the two cluster configurations should be wired down using a resistor.

Table 9 Gigabit Ethernet and Fibre Channel TBI Signals Example

Signal Name*	Pin #†	Total	Type	I/O	Label	Signal Description
CP*n*_0	Table 4	1	LVTTL	O	TCLK	Transmit Clock (125MHz). This clock is used to synchronize the transmit data.
CP*n*_1	Table 4	1	nc	nc	nc	nc
CP*n*_2	Table 4	1	LVTTL	O	TXD(9)	Transmit Data (ten bits wide, last on wire)
CP*n*_3	Table 4	1	LVTTL	O	TXD(8)	Transmit Data
CP*n*_4	Table 4	1	LVTTL	O	TXD(7)	Transmit Data
CP*n*_5	Table 4	1	LVTTL	O	TXD(6)	Transmit Data
CP*n*_6	Table 4	1	LVTTL	O	TXD(1)	Transmit Data
CP*n+1*_0	Table 4	1	nc	nc	nc	nc
CP*n+1*_1	Table 4	1	nc	nc	nc	nc
CP*n+1*_2	Table 4	1	LVTTL	O	TXD(5)	Transmit Data
CP*n+1*_3	Table 4	1	LVTTL	O	TXD(4)	Transmit Data
CP*n+1*_4	Table 4	1	LVTTL	O	TXD(3)	Transmit Data
CP*n+1*_5	Table 4	1	LVTTL	O	TXD(2)	Transmit Data
CP*n+1*_6	Table 4	1	LVTTL	O	TXD(0)	Transmit Data (ten bits wide, first on wire)
CP*n+2*_0	Table 4	1	nc	nc	nc	nc
CP*n+2*_1	Table 4	1	LVTTL	I	RCLK	Receive Clock (62.5 MHz)
CP*n+2*_2	Table 4	1	LVTTL	I	RXD(9)	Receive Data (ten bits wide, last on wire)
CP*n+2*_3	Table 4	1	LVTTL	I	RXD(8)	Receive Data
CP*n+2*_4	Table 4	1	LVTTL	I	RXD(7)	Receive Data
CP*n+2*_5	Table 4	1	LVTTL	I	RXD(6)	Receive Data
CP*n+2*_6	Table 4	1	LVTTL	I	RXD(1)	Receive Data
CP*n+3*_0	Table 4	1	nc	nc	nc	nc
CP*n+3*_1	Table 4	1	LVTTL	I	RCLKN	Receive Clock Inverted
CP*n+3*_2	Table 4	1	LVTTL	I	RXD(5)	Receive Data
CP*n+3*_3	Table 4	1	LVTTL	I	RXD(4)	Receive Data

Table 9 Gigabit Ethernet and Fibre Channel TBI Signals Example (continued)

Signal Name*	Pin #†	Total	Type	I/O	Label	Signal Description
CP*n+3*_4	Table 4	1	LVTTL	I	RXD(3)	Receive Data
CP*n+3*_5	Table 4	1	LVTTL	I	RXD(2)	Receive Data
CP*n+3*_6	Table 4	1	LVTTL	I	RXD(0)	Receive Data (ten bits wide, first on wire)
Total Pins		**28**				

* n can be 0, 4, 8, or 12

† Reference Table 4 for pin numbers for the actual cluster(s) you are configuring.

SONET OC-3 Transceiver Interface Configuration

Table 10 describes the SONET Optical Carrier (OC) 3 transceiver interface signals. For each CP (0-15), you can implement a single OC-3 interface.

Table 10 OC-3 Signals

Signal Name*	Pin #†	Total	Type	I/O	Label	Signal Description
CP*n*_0	Table 4	1	LVPECL	I	RCLK_H	Receive Clock noninverted side of pair (155.52MHz)
CP*n*_1	Table 4	1	LVPECL	I	RCLK_L	Receive Clock inverted side of pair (155.52MHz)
CP*n*_2	Table 4	1	LVPECL	O	TXD_H	Transmit Data noninverted side of pair
CP*n*_3	Table 4	1	LVPECL	O	TXD_L	Transmit Data inverted side of pair
CP*n*_4	Table 4	1	LVPECL	I	RXD_H	Receive Data noninverted side of pair
CP*n*_5	Table 4	1	LVPECL	I	RXD_L	Receive Data inverted side of pair
CP*n*_6	Table 4	1	LVPECL	I	SIGNAL_DET	A light level above a certain threshold is present at the optical receiver - single ended LVPECL.
Total Pins		**7**				

* *n* can be from 0 to 15.

† Reference Table 4 for pin numbers for the actual cluster(s) you are configuring.

SONET OC-12 Transceiver Interface Configuration

SONET Optical Carrier (OC) 12 is implemented by using one cluster of CPs. At any time, a CP within a cluster spends half its time performing receive functions, and the other half performing transmit functions. Table 11 shows a CP Cluster configured for one OC-12 interface.

Table 11 OC-12 Signals Example

Signal Name*	Pin #†	Total	Type	I/O	Label	Signal Description
CP*n*_0	Table 4	1	LVTTL	O	TCLK	Deskewed Transmit Clock (77.76MHz). This clock is used to synchronize the transmit data.
CP*n*_1	Table 4	1	LVTTL	I	TCLK1	Transceiver Transmit Clock. This clock sets the frequency of the transmit data and is typically sourced by the PHY chip.
CP*n*_2	Table 4	1	LVTTL	O	TXD(0)	Transmit Data (byte-wide data, least significant bit)
CP*n*_3	Table 4	1	LVTTL	O	TXD(1)	Transmit Data
CP*n*_4	Table 4	1	LVTTL	O	TXD(2)	Transmit Data
CP*n*_5	Table 4	1	LVTTL	O	TXD(3)	Transmit Data
CP*n*_6	Table 4	1	LVTTL	0	00F	Out of Frame
CP*n+1*_0	Table 4	1	nc	nc	nc	nc
CP*n+1*_1	Table 4	1	nc	nc	nc	nc
CP*n+1*_2	Table 4	1	LVTTL	O	TXD(4)	Transmit Data
CP*n+1*_3	Table 4	1	LVTTL	O	TXD(5)	Transmit Data
CP*n+1*_4	Table 4	1	LVTTL	O	TXD(6)	Transmit Data
CP*n+1*_5	Table 4	1	LVTTL	O	TXD(7)	Transmit Data (byte-wide data, most significant bit)
CP*n+1*_6	Table 4	1	nc	nc	nc	nc
CP*n+2*_0	Table 4	1	nc	nc	nc	nc
CP*n+2*_1	Table 4	1	LVTTL	I	RCLK	Receive Clock (77.76MHz)
CP*n+2*_2	Table 4	1	LVTTL	I	RXD(0)	Receive Data (byte-wide receive data, least significant bit)
CP*n+2*_3	Table 4	1	LVTTL	I	RXD(1)	Receive Data
CP*n+2*_4	Table 4	1	LVTTL	I	RXD(2)	Receive Data
CP*n+2*_5	Table 4	1	LVTTL	I	RXD(3)	Receive Data
CP*n+2*_6	Table 4	1	LVTTL	I	FP	Frame Synchronization Pulse. This is valid during the third A2 of the receive SONET frame.
CP*n+3*_0	Table 4	1	nc	nc	nc	nc
CP*n+3*_1	Table 4	1	nc	nc	nc	nc

Table 11 OC-12 Signals Example (continued)

Signal Name*	Pin #†	Total	Type	I/O	Label	Signal Description
CP*n*+3_2	Table 4	1	LVTTL	I	RXD(4)	Receive Data
CP*n*+3_3	Table 4	1	LVTTL	I	RXD(5)	Receive Data
CP*n*+3_4	Table 4	1	LVTTL	I	RXD(6)	Receive Data
CP*n*+3_5	Table 4	1	LVTTL	I	RXD(7)	Receive Data (most significant bit)
CP*n*+3_6	Table 4	1	nc	nc	nc	nc
Total Pins		**28**				

* n can be 0, 4, 8, or 12

† Reference Table 4 for pin numbers for a different cluster.

Executive Processor System Interface Signals

The XP's system interface manages the supervisory controls for the network interfaces, as well as the set of pins that provide interfaces to other components in the system that are not memories or network interfaces. It is also the primary interface used for initializing the C-5 NP after reset. The XP signals include PCI signals, Serial interface signals, and PROM interface signals.

PCI Signals

The PCI can be configured to support a 32bit PCI capable of operating at either 33MHz or 66MHz. The PCI is fully compliant with PCVI Specification revision 2.1. Table 12 describes the PCI signals.

Table 12 PCI Signals

Signal Name	Pin #	Total	Type	I/O	Signal Description
PAD0 - PAD31	T22, R21, P21, T21, R20, P20, T20, R19, Q20, S20, R18, P19, T19, R17, P18, T18, R16, Q18, S18, S16, P17, T17, R15, P16, T16, S14, Q16, T15, R14, P15, T14, Q14	32	PCI	I/O	Multiplexed Address/Data Bus. These signals are multiplexed address and data bits. The C-5 NP receives addresses as target and drives addresses as master. It drives the data and receives read data as master.
PCBEX0 - PCBEX3	N21, N20, M20, O20	4	PCI	I/O	Command byte enables. These signals are multiplexed command and byte enabled signals. The C-5 NP receives byte enables as target and drives byte enables as master.
PPAR	P14	1	PCI	I/O	Parity. This signal carries even parity for AD and CBE# pins. It has the same receive and drive characteristics as the address and data bus, except that it is one PCI cycle later.
PFRAMEX	K20	1	PCI	I/O	Cycle frame

Table 12 PCI Signals (continued)

Signal Name	Pin #	Total	Type	I/O	Signal Description
PTRDYX	L20	1	PCI	I/O	Target ready for data transfer
PIRDYX	L19	1	PCI	I/O	Initiator ready for data transfer
PSTOPX	K18	1	PCI	I/O	Target transaction stop request
PDEVSELX	N18	1	PCI	I/O	Target device selected
PPERRX	M18	1	PCI	I/O	Bus parity error
PSERRX	L18	1	PCI	I/O	System error
PCLK	L15	1	PCI	I	Bus clock
PRSTX	N17	1	PCI	I	Bus reset
PREQX	L17	1	PCI	O	Initiator bus request (arbitration)
PGNTX	N19	1	PCI	I	Initiator bus grant (arbitration)
PIDSEL	O18	1	PCI	I	Initialization device select
PINTA	O16	1	PCI	O	Interrupt
Total Pins		**50**			

Serial Interface Signals

The Serial interface is a bidirectional two-wire serial bus. It can use one of the following formats:

1. An 8bit data format followed by an acknowledge bit, which supports transfers at up to 400kbps (low speed).
2. a 16bit IEEE 802.3 MDIO data format with 10bits of addressing, which supports transfers up to 25MHz (high speed).

The signals and pins are identical for both the high and low speed protocols.

Which of the two data rates used is selected by the state of the PROM interface's SPLD signal that is asserted while the PROM interface is idle. When SPLD is asserted HI *the low speed serial bus protocol is selected and when SPLD is asserted* LOW *the MDIO protocol is selected.*

The bus only supports a single master hierarchy that can operate as either a receiver or a transmitter. The bus also supports collision detection and arbitration, and an integrated addressing and data-transfer protocol.

Both SIDA and SICL are bidirectional lines that are connected, through a pull-up resistor, to a positive supply voltage. When the bus is free, both lines are HIGH. The output stages

of the devices connected to the bus must have either an open-drain or open-collector in order to perform the wired-AND function required for its arbitration mechanism.

Table 13 Serial Port Signals

Signal Name	Pin #	Total	Type	I/O	Signal Description
SICL	O14	1	LVTTL	I/O	Serial Clock line
SIDA	N14	1	LVTTL	I/O	Serial Data line
Total Pins		**2**			

PROM Interface Signals

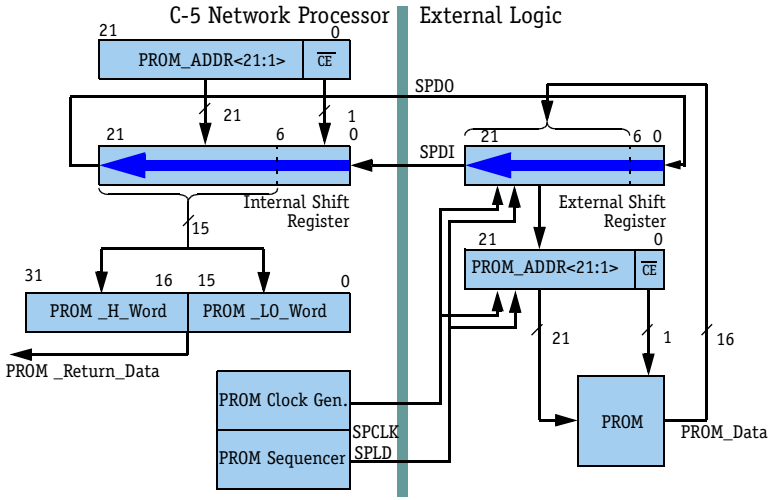
The PROM interface is a low speed I/O port that allows the C-5 NP to communicate through external logic to PROM. The PROM clock is $^1/_2$ to $^1/_{16}$ the core clock rate. The maximum PROM size is 4MBytes x 16, and configuration is required. The PROM signals are listed in Table 14.

Table 14 PROM Interface Signals

Signal Name	Pin #	Total	Type	I/O	Signal Description
SPDO	N15	1	LVTTL	O	Serial Data Out
SPDI	N16	1	LVTTL	I	Serial Data In
SPLD	M16	1	LVTTL	O	When load is asserted on a positive clock edge, the external logic performs a parallel load. On each positive clock edge when load is de-asserted, the shift registers shift. When the PROM interface is idle: • if SPLD is asserted HI it indicates low speed serial protocol, • if asserted LOW it indicates MDIO serial protocol.
SPCK	M14	1	LVTTL	O	Clock
Total Pins		**4**			

Figure 4 shows the connections between the PROM Interface and external board logic. The application is required to provide an external shift register with parallel-in and parallel-out capabilities, and a parallel load register. Both devices should be positive-edge-triggered and perform a parallel load whenever SPLD is asserted. When SPLD is deasserted the shift register shifts.

Figure 4 PROM Interface Diagram



The PROM interface operates in the following manner (Note that two accesses are piplined together to execute one 32-bit fetch). The steps are shown in Figure 5.

1 The PROM_ADDR is loaded into the network processor internal shift register.

2 The PROM_ADDR is shifted into the external shift register for 22 SPCLK cycles.

3 SPLD is asserted for one SPCLK cycle, loading the PROM_ADDR into the external presentation register.

4 SPLD is deasserted for 22 SPCLK cycles. The PROM presents the first 16bit PROM_DATA. At the same time, the next PROM_ADDR is shifted into the external shift register.

5 SPLD is asserted for one SPCLK cycle, loading the PROM_ADDR into the external presentation register and the first PROM_DATA into the external shift register.

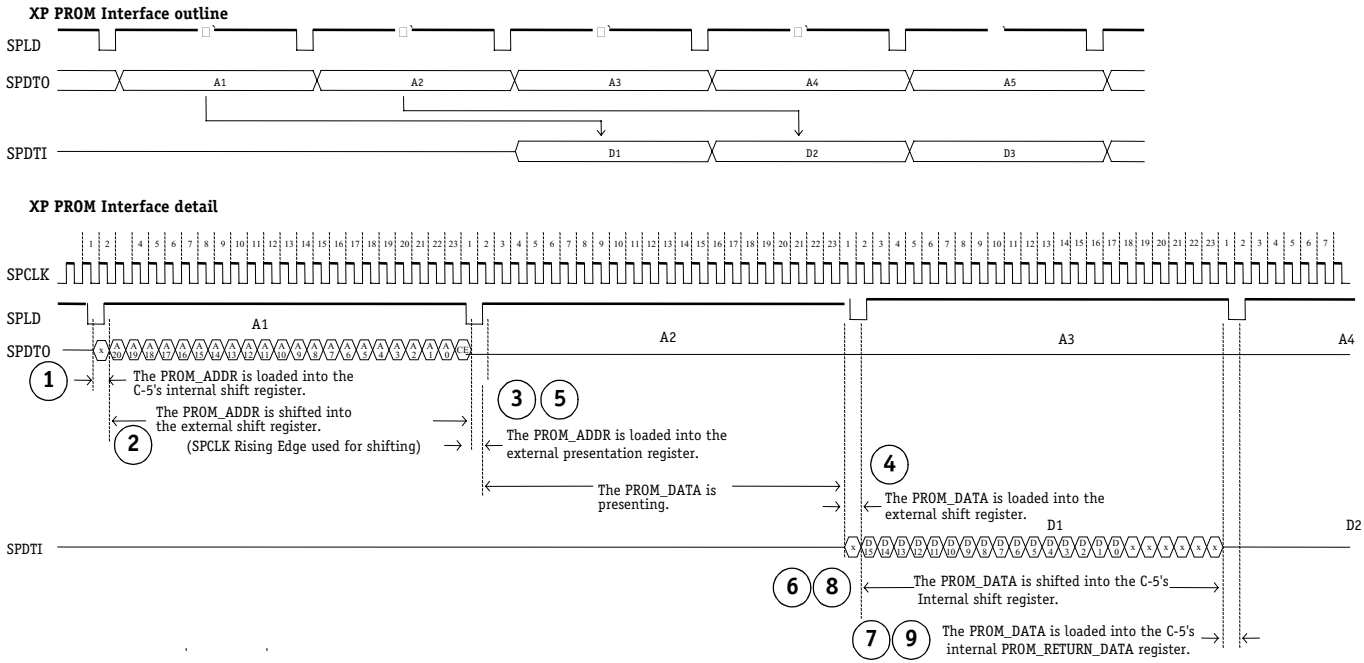
6 SPLD is deasserted for 22 SPCLK cycles, shifting the first PROM_DATA into the network processor internal shift register.

7 SPLD is asserted for one SPCLK cycle, loading the first PROM_DATA into the network processor PROM_RETURN_DATA register and the second PROM_DATA into the external shift register.

8 SPLD is deasserted for 22 SPCLK cycles, shifting the second PROM_DATA into the network processor internal shift register.

9 SPLD is asserted for one SPCLK cycle, loading the second PROM_DATA into the network processor PROM_RETURN_DATA register.

Figure 5 PROM Interface Timing Outline



General System Interface Signal

Table 15 provides the signal for the Executive Processor reset power status and I/O clock. The C-5 NP can be powered up with the XP either running or with the XP in reset mode similar to the CPs. When the XP remains in reset mode, an external host can be used to control the initialization of the C-5 NP.

Table 15 General System Interface Signal

Signal Name	Pin #	Total	Type	I/O	Signal Description
XPUHOT	J19	1	LVTTL	I	Sample at Power On Reset determines if the XP RISC Core is held in reset. Low equals reset and High equals active. During normal operation, this is an external interrupt.
Total Pins		**1**			

Fabric Processor Interface Signals

The FP consists of two logical signal interfaces: a receive data interface and a transmit data interface, each with its own control and clocking signals. The interface has the following characteristics:

- The interface clocks FRXCLK and FTXCLK can have a different frequency from the core C-5 NP clock frequency. The Fabric Data Processor (FDP) has synchronizing FIFOs at its interface boundary to allow for a fabric interface frequency from 10MHz to 110MHz.
- The receive clock FRXCLK and the transmit clock FTXCLK must share the same frequency. The synchronization logic internal to the FP requires related clock domains on the transmit and receive interfaces. Each of the two clocks can have different phase alignment, however, because they are generated externally.

Each data bus can be run at widths of 16 or 32 bits of data (FIN0 - FIN31 and FOUT0 - FOUT31) per clock. The extra data pins in each configuration remain unused. The output pins are driven to a known state, and the input pins should also be pulled to a known state.

Table 16 Fabric Interface Signals

Signal Name	Pin #	Total	Type	I/O	Signal Description
FIN0 - FIN31	W2, V1, T1, V2, U2, V3, T3, T2, W4, V4, V5, U4, T4, W6, V6, U6, T5, T6, V7, T7, X8, W8, V8, V9, U8, X9, V10, U10, X10, W10, X11, V11	32	LVTTL	I	Fabric Data Bus In
FOUT0 - FOUT31	W28, V29, T29, V28, U28, V27, T27, T28, W26, V26, V25, U26, T26, W24, V24, U24, T25, T24, V23, T23, X22, W22, V22, V21, U22, X21, V20, U20, X20, W20, X19, V19	32	LVTTL	O	Fabric Data Bus Out
FRXCLK	W14	1	LVTTL	I	Receive Clock
FTXCLK	W16	1	LVTTL	I	Transmit Clock
FRXCTL0 - FRXCTL6	U12, W12, V12, X12, X13, V13, X14	7	LVTTL	I, O	Receive Control Signals
FTXCTL0 - FTXCTL6	U18, W18, V18, X18, X17, V17, X16	7	LVTTL	I, O	Transmit Control Signals
Total Pins		**80**			

The following tables list the Fabric Interface pin mappings:

- Utopia1, Utopia2, Utopia3 ATM Mode mappings are listed in Table 17
- Utopia1, Utopia2, Utopia3 PHY Mode mappings are listed in Table 18
- PRIZMA Mode mappings are listed in Table 19 (PRIZMA mode is an example of Utopia3 PHY mode)
- Power X Mode mappings are listed in Table 20

Table 17 Utopia1*, 2*, 3 ATM Mode, C-5 Network Processor to Fabric Interface Pin Mapping

Receive Signals				Transmit Signals			
C-5 Network Processor	**I/O**	**Utopia**	**Note**	**C-5 Network Processor**	**I/O**	**Utopia**	**Note**
FRXCTL0	Output	RxEnb*	Pullup or nc	FTXCTL0	Output	TxEnb*	Pullup or nc
FRXCTL1	Input	RxClav	Pulldown	FTXCTL1	Input	TxClav	Pulldown
FRXCTL2	Input	RxSOC	Pulldown	FTXCTL2	Output	TxSOC	Pulldown
FRXCTL3	Input	n/a	Pullup or Pulldown	FTXCTL3	nc	nc	
FRXCTL4	Input	n/a		FTXCTL4	nc	nc	
FRXCTL5	Input	n/a		FTXCTL5	nc	nc	
FRXCTL6	Input	RxPrty		FTXCTL6	Output	TxPrty	

* cell size must be 4Byte aligned.

Table 18 Utopia1*, 2*, 3 PHY Mode, C-5 Network Processor to Fabric Interface Pin Mapping

Receive Signals				Transmit Signals			
C-5 Network Processor	**I/O**	**Utopia**	**Note**	**C-5 Network Processor**	**I/O**	**Utopia**	**Note**
FRXCTL0	Input	TxEnb*	Pullup	FTXCTL0	Input	RxEnb*	Pullup
FRXCTL1	Output	TxClav	Pulldown or nc	FTXCTL1	Output	RxClav	Pulldown or nc
FRXCTL2	Input	TxSOC	Pulldown	FTXCTL2	Output	RxSOC	Pulldown
FRXCTL3	Input	n/a	Pullup or Pulldown	FTXCTL3	nc	nc	
FRXCTL4	Input	n/a	Pullup or Pulldown	FTXCTL4	nc	nc	
FRXCTL5	Input	n/a	Pullup or Pulldown	FTXCTL5	nc	nc	

Table 18 Utopia1*, 2*, 3 PHY Mode, C-5 Network Processor to Fabric Interface Pin Mapping

Receive Signals				Transmit Signals			
C-5 Network Processor	**I/O**	**Utopia**	**Note**	**C-5 Network Processor**	**I/O**	**Utopia**	**Note**
FRXCTL6	Input	TxPrty		FTXCTL6	Output	RxPrty	

* cell size must be 4Byte aligned.

When configuring two C-5 network processors back-to-back using the Fabric Port, set up the transmit side of each C-5 network processor in Utopia ATM mode and the receive side of each C-5 network processor in Utopia PHY mode.

Table 19 PRIZMA Mode, C-5 Network Processor to Fabric Interface Pin Mapping

Receive Signals				Transmit Signals			
C-5 Network Processor	**I/O**	**Utopia**	**Note**	**C-5 Network Processor**	**I/O**	**Utopia**	**Note**
FRXCTL0	Input	TxEnb*	pulldown (not connected to fabric)	FTXCTL0	Input	RxEnb*	pulldown (not connected to fabric)
FRXCTL1	Output	TxClav	nc	FTXCTL1	Output	RxClav	nc
FRXCTL2	Input	TxSOP	Pulldown	FTXCTL2	Output	RxSOP	Pulldown
FRXCTL3	Input	n/a	Pullup or Pulldown	FTXCTL3	nc	nc	
FRXCTL4	Input	n/a	Pullup or Pulldown	FTXCTL4	nc	nc	
FRXCTL5	Input	n/a	Pullup or Pulldown	FTXCTL5	nc	nc	
FRXCTL6	Input	TxPrty or nc		FTXCTL6	Output	RxPrty or nc	

Table 20 Power X Mode, C-5 Network Processor to Fabric Interface Pin Mapping

Receive Signals				Transmit Signals			
C-5 Network Processor	**I/O**	**Power X**	**Note**	**C-5 Network Processor**	**I/O**	**Power X**	**Note**
FRXCTL0	Input	RxCtrl[0]	Pulldown	FTXCTL0	Output	TxCtrl[0]	Pulldown or nc
FRXCTL1	Input	RxCtrl[1]	Pulldown	FTXCTL1	Output	TxCtrl[1]	Pulldown or nc
FRXCTL2	Input	RxCtrl[2]	Pulldown	FTXCTL2	Output	TxCtrl[2]	Pulldown or nc

Table 20 Power X Mode, C-5 Network Processor to Fabric Interface Pin Mapping

Receive Signals				Transmit Signals			
C-5 Network Processor	**I/O**	**Power X**	**Note**	**C-5 Network Processor**	**I/O**	**Power X**	**Note**
FRXCTL3	Input	RxPrty[3]		FTXCTL3	Output	TxPrty[3]	
FRXCTL4	Input	RxPrty[2]		FTXCTL4	Output	TxPrty[2]	
FRXCTL5	Input	RxPrty[1]		FTXCTL5	Output	TxPrty[1]	
FRXCTL6	Input	RxPrty[0]		FTXCTL6	Output	TxPrty[0]	

BMU SDRAM Interface Signals

The BMU and SDRAM interface signals are described in Table 21.

The BMU is designed to support SDRAM devices with 12 address lines. All 139 data lines and all 12 address lines must be connected to the SDRAM in order for the BMU to be able to read and write external SDRAM properly.

Table 21 BMU SDRAM Interface Signals

Signal Name	Pin #	Total	Type	I/O	Signal Description
MD0 - MD129	R29, Q28, P28, S28, R28, P29, R27, Q26, P26, S26, R26, P27, R25, Q24, P24, S24, R24, P25, S22, R23, R22, N29, M28, L28, J29, O28, N28, L29, K28, N27, M26, L26, J28, O26, N26, L27, K26, N25, M24, L24, J27, O24, N24, L25, K24, P22, M22, K22, J23, Q22, N23, L22, J25, O22, L23, J26, J22, P23, N22, L21, J24, B29, D29, F29, A28, C28, E28, G28, B28, D28, F28, B27, D27, F27, A26, C26, E26, B26, D26, F26, G26, B25, D25, F25, A24, C24, E24, B24, D24, F24, B23, D23, F23, G24, A22, C22, E22, B22, D22, F22, B21, D21, F21, A20, C20, E20, G22, B20, D20, F20, B19, D19, F19, A18, C18, E18, B18, D18, F18, G20, B17, D17, F17, A16, C16, E16, B16, D16, F16, B15	130	LVTTL	I/O	Data Lines In
MDECC0 - MDECC8	G16, F15, F14, E14, D15, D14, C14, B14, A14	9	LVTTL	I/O	Stored as data, ECC bits
MA0 - MA11	H22, I22, H23, H24, I24, H25, H26, I26, H27, H28, I28, H29	12	LVTTL	O	Address Outputs: A0-A11 are sampled during the ACTIVE command and READ/WRITE to select one location out of the memory array in the respective bank. The address inputs also provide the op-code during a LOAD MODE REGISTER command
MBA0 - MBA1	G18, H19	2	LVTTL	O	Bank Address Outputs: BA0 and BA1 define which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied
MCLK	I16	1	nc	nc	Reserved
MCASX	J21	1	LVTTL	O	Command Outputs: MRASX, MCASX, MWEX and MCSX define the command being entered. *NOTE: MCSX is considered part of the command code.*

Table 21 BMU SDRAM Interface Signals (continued)

Signal Name	Pin #	Total	Type	I/O	Signal Description
MRASX	I20	1	LVTTL	O	Command Outputs: MRASX, MCASX, MWEX and MCSX define the command being entered. MCSX is considered part of the command code.
MWEX	J20	1	LVTTL	O	Command Outputs: MRASX, MCASX, MWEX and MCSX define the command being entered. MCSX is considered part of the command code.
MCSX	H20	1	LVTTL	O	Chip Select: MCSX enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when MCSX is registered HIGH. MCSX provides the external bank selection on systems with multiple banks. MCSX is considered part of the command code.
MDQM MDQML	H21 G14	1 1	LVTTL LVTTL	O O	Input/Output Mask: MDQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when MDQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a high Z state (two-clock latency) when MDQM is sampled HIGH during the READ cycle. *NOTE: MDQML is an identical copy of MDQM used to drive the loading on SDRAM configurations with 2 DQM pins.*
MDCLK	J17	1	LVTTL	I	Clock: MDCLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of the MDCLK. MDCLK also increments the internal burst counter and controls the output registers.
Total Pins		**161**			

TLU SRAM Interface Signals

The TLU SRAM interface supports up to 32MBytes of SRAM at frequencies to 133MHz using LVTTL signaling levels (in single bank-mode only) and SRAM technologies up to 64Mbits. The TLU SRAM interface signals are described in Table 22.

Table 22 TLU SRAM Interface Signals

Signal Name	Pin #	Total	Type	I/O	Signal Description
TD0 - TD63	N1, L1, J1, H1, M2, K2, I2, G2, N2, L2, J2, H2, L3, J3, H3, G4, 04, M4, K4, I4, L4, J4, H4, G6, N5, L5, J5, H5, N6, L6, I6, H6, K6, J6, M6, H7, L7, J7, H8, N8, M8, K8, I8, G8, N7, L8, J8, H9, L9, J9, J10, G10, P9, O8, L10, H10, O10, N9, L11, I10, M10, K10, J11, H11	64	LVTTL	I/O	TLU Memory Data
TA0 - TA21	R1, P1, S2, Q2, O2, R2, P2, R3, P3, N3, S4, Q4, R4, P4, N4, R5, P5, S6, R6, Q6, P6, O6	22	LVTTL	O	TLU Memory Address
TA18x - TA21x	T8, Q8, R7, P7	4	LVTTL	O	Data Parity
TCE0X - TCE3X	P8, R8, S8, T9	4	LVTTL	O	TLU Memory Chip Enable
TWE0X - TWE3X	Q10, R9, S10, T10	4	LVTTL	O	TLU Memory Write Enable
TCLKI	M12	1	LVTTL	I	TLU Clock Input
Total Pins		**99**			

Table 23 Memory Bank Selection

		Chip Select (Signals TA18x through TA21x)						
Size	**Bank 1**		**Bank 2**		**Bank 3**		**Bank 4**	
	CE2	**CE2x**	**CE2**	**CE2x**	**CE2**	**CE2x**	**CE2**	**CE2x**
4Mbit	TA18x	TA19	TA18	TA19	TA18x	TA19x	TA18	TA19x
8Mbit	TA19x	TA20	TA19	TA20	TA19x	TA20x	TA19	TA20x
16Mbit	TA20x	TA21	TA20	TA21	TA20x	TA21x	TA20	TA21x

QMU SRAM Interface Signals

The QMU signals are described in Table 24. The QMU's clock frequency is $^1/_2$ the internal core clock frequency.

Table 24 QMU SRAM Interface Signals

Signal Name	Pin #	Total	Type	I/O*	Signal Description
QCPAR	A10	1	nc	nc	Not used
QCLK	G12	1	LVTTL	O	Clock Signal to the memory ICs
QCMD0 - QCMD15	B10, C10, D10, E10, F10, B11, D11, F11, A12, B12, C12, D12, E12, B13, D13, F13	16	LVTTL	O	Memory Address [15: 0] to the memory ICs
QDPAR	A8	1	LVTTL	I/O	Data parity
QDATA0 - QDATA31	D1, F1, F2, B2, C2, D2, E2, B3, D3, F3, A4, B4, C4, D4, E4, F4, B5, D5, F5, A6, B6, C6, D6, E6, F6, B7, D7, F7, C8, D8, E8, F8	32	LVTTL	I/O	Memory Data
QSFLOW	B9	1	LVTTL	O	Not Used
QXCTRL0	D9	1	LVTTL	O	Rd/Wr (Read is true high, write is true low)
QXCTRL1	F9	1	LVTTL	O	Memory Address [16] to the memory ICs
QXRQST	B8	1	nc	nc	Reserved *Note: Requires Pullup or Pulldown.*
Total Pins		**55**			

*During normal (non-scan) operation.

Power Supply Signals

Power supply and ground signals are described in Table 25 and their pinouts are shown in Figure 6.

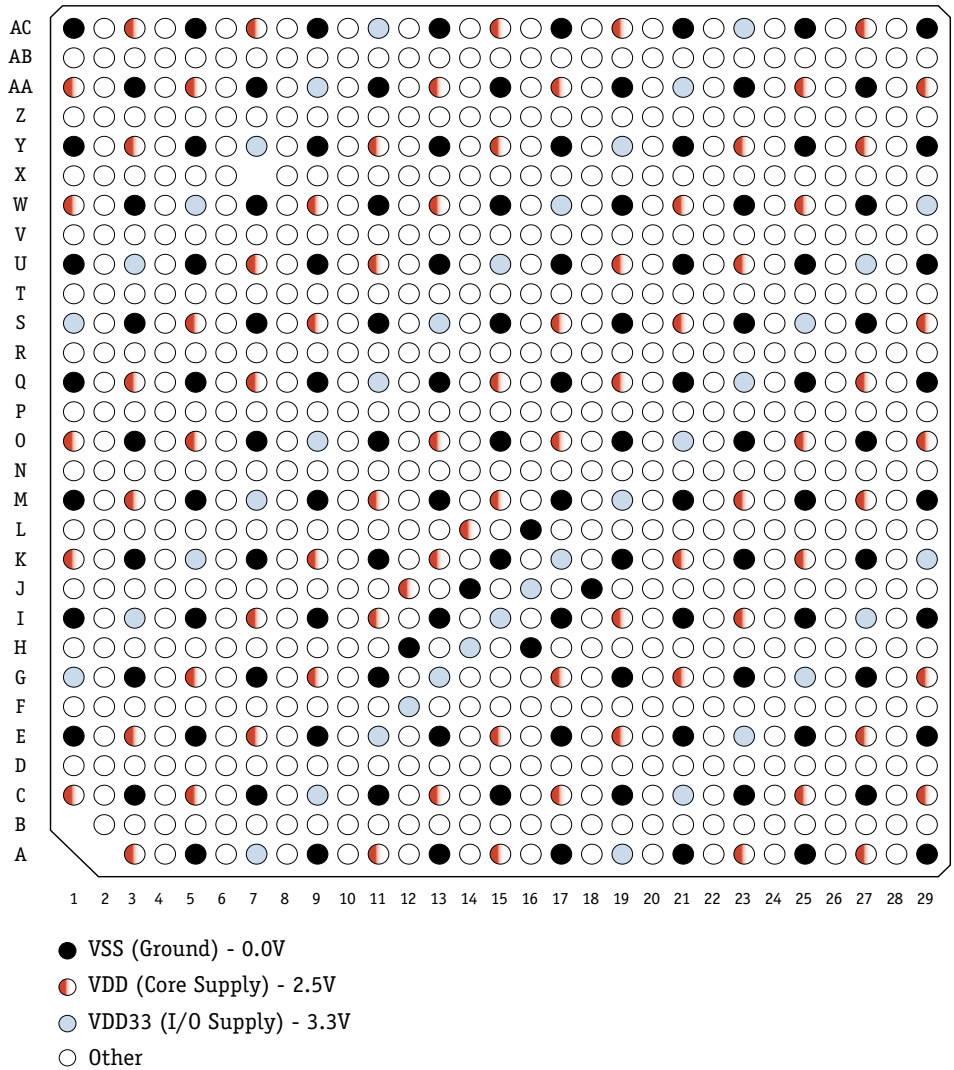
Table 25 Power Supply Signals

Signal Name	Pin #	Total	Type	Signal Description
VDD	A3, A11, A15, A23, A27, C1, C5, C13, C17, C25, C29, E3, E7, E15, E19, E27, G5, G9, G17, G21, G29, I7, I11, I19, I23, J12, K1, K9, K13, K21, K25, L14, M3, M11, M15, M23, M27, O1, O5, O13, O17, O25, O29, Q3, Q7, Q15, Q19, Q27, S5, S9, S17, S21, S29, U7, U11, U19, U23, W1, W9, W13, W21, W25, Y3, Y11, Y15, Y23, Y27, AA1, AA5, AA13, AA17, AA25, AA29, AC3, AC7, AC15, AC19, AC27	78	P	Core Supply Voltage (1.8V Input)
VDD33	A7, A19, C9, C21, E11, E23, F12, G1, G13, G25, H14, I3, I15, I27, J16, K5, K17, K29, M7, M19, O9, O21, Q11, Q23, S1, S13, S25, U3, U15, U27, W5, W17, W29, Y7, Y19, AA9, AA21, AC11, AC23	39	P	I/O Supply Voltage (3.3V Input)

Table 25 Power Supply Signals (continued)

Signal Name	Pin #	Total	Type	Signal Description
VSS	A5, A9, A13, A17, A21, A25, A29, C3, C7, C11, C15, C19, C23, C27, E1, E5, E9, E13, E17, E21, E25, E29, G3, G7, G11, G19, G23, G27, H12, H16, I1, I5, I9, I13, I17, I21, I25, I29, J14, J18, K3, K7, K11, K15, K19, K23, K27, L16, M1, M5, M9, M13, M17, M21, M25, M29, O3, O7, O11, O15, O19, O23, O27, Q1, Q5, Q9, Q13, Q17, Q21, Q25, Q29, S3, S7, S11, S15, S19, S23, S27, U1, U5, U9, U13, U17, U21, U25, U29, W3, W7, W11, W15, W19, W23, W27, Y1, Y5, Y9, Y13, Y17, Y21, Y25, Y29, AA3, AA7, AA11, AA15, AA19, AA23, AA27, AC1, AC5, AC9, AC13, AC17, AC21, AC25, AC29	116	P	Ground
Total Pins		**234**		

Figure 6 Power and Ground Connections (Bottom View)



Test Signals

Test signals are described in Table 26 and their pinouts are shown in Figure 6.

Table 26 Miscellaneous Test Signals For JTAG, Scan, and Internal Test Routines

Signal Name	Pin #	Total	Type	Signal Description
JTCK	T11	1	LVTTL	Test Clock
JTMS*	Z15	1	LVTTL	Test Mode Select. High selects modes as defined in the IEEE 1149.1 JTAG specification.
JTRSTX†	X15	1	LVTTL	Test Reset (low active)
JTDI†	AB15	1	LVTTL	Test Data In
JTDO	V15	1	LVTTL	Test Data Out
JHIGHZ	T12	1	LVTTL	Turns off all output drivers when High
JCLKBYP	T13	1	LVTTL	1X or 2X Clock Mode Select. Low selects 1X, High selects 2X.
JSE	S12	1	LVTTL	Scan Enable. High enables scan test.
JS00-JS09	L12, N13, N12, P13, P12, Q12, R13, R12, R11, R10	10	LVTTL	Scan Out Pins
Total Pins		**18**		

* According to the IEEE 1149.1 specification, the JTMS, JTRST, and JTDI pins must have internal pullups. While the C-5 NP does not currently have pads with pullups, customers can pull up these three pins on the board.

During JTAG, SCLK and SCLKX must remain as differential inputs.

No Connection Pins

No connection pins are listed in Table 27.

Table 27 No Connection Pins

Signal Name	Pin #	Total	Type	Signal Description
NC1 - NC11	I18, H17, H18, N10, P10, N11, P11, U14, V14, U16, V16	11	nc	Reserved for future functionality
Total Pins		**11**		

Signals Grouped by Pin Number

The C-5 NP signals are listed by pin number in Table 28.

Table 28 Signals Listed by Pin Number

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A 1-29							
A1	Not present	A9	VSS	A17	VSS	A25	VSS
A2	Not present	A10	QCPAR	A18	MD113	A26	MD74
A3	VDD	A11	VDD	A19	VDD33	A27	VDD
A4	QDATA10	A12	QCMD8	A20	MD103	A28	MD64
A5	VSS	A13	VSS	A21	VSS	A29	VSS
A6	QDATA19	A14	MECC8	A22	MD94		
A7	VDD33	A15	VDD	A23	VDD		
A8	QDPAR	A16	MD123	A24	MD84		
B 1-29							
B1	Not present	B9	QSFLOW	B17	MD120	B25	MD81
B2	QDATA3	B10	QCMD0	B18	MD116	B26	MD77
B3	QDATA7	B11	QCMD5	B19	MD110	B27	MD71
B4	QDATA11	B12	QCMD9	B20	MD107	B28	MD68
B5	QDATA16	B13	QCMD13	B21	MD100	B29	MD61
B6	QDATA20	B14	MECC7	B22	MD97		
B7	QDATA25	B15	MD129	B23	MD90		
B8	QXRQST	B16	MD126	B24	MD87		
C 1-29							
C1	VDD	C9	VDD33	C17	VDD	C25	VDD
C2	QDATA4	C10	QCMD1	C18	MD114	CB26	MD75
C3	VSS	C11	VSS	C19	VSS	C27	VSS
C4	QDATA12	C12	QCMD10	C20	MD104	C28	MD65
C5	VDD	C13	VDD	C21	VDD33	C29	VDD
C6	QDATA21	C14	MECC6	C22	MD95		

Table 28 Signals Listed by Pin Number (continued)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
C7	VSS	C15	VSS	C23	VSS		
C8	QDATA28	C16	MD124	C24	MD85		
D 1-29							
D1	QDATA0	D9	QXCTRL0	D17	MD121	D25	MD82
D2	QDATA5	D10	QCMD2	D18	MD117	D26	MD78
D3	QDATA8	D11	QCMD6	D19	MD111	D27	MD72
D4	QDATA13	D12	QCMD11	D20	MD108	D28	MD69
D5	QDATA17	D13	QCMD14	D21	MD101	D29	MD62
D6	QDATA22	D14	MECC5	D22	MD98		
D7	QDATA26	D15	MECC4	D23	MD91		
D8	QDATA29	D16	MD127	D24	MD88		
E 1-29							
E1	VSS	E9	VSS	E17	VSS	E25	VSS
E2	QDATA6	E10	QCMD3	E18	MD115	E26	MD76
E3	VDD	E11	VDD33	E19	VDD	E27	VDD
E4	QDATA14	E12	QCMD12	E20	MD105	E28	MD66
E5	VSS	E13	VSS	E21	VSS	E29	VSS
E6	QDATA23	E14	MECC3	E22	MD96		
E7	VDD	E15	VDD	E23	VDD33		
E8	QDATA30	E16	MD125	E24	MD86		
F 1-29							
F1	QDATA1	F9	QXCTRL1	F17	MD122	F25	MD83
F2	QDATA2	F10	QCMD4	F18	MD118	F26	MD79
F3	QDATA9	F11	QCMD7	F19	MD112	F27	MD73
F4	QDATA15	F12	VDD33	F20	MD109	F28	MD70
F5	QDATA18	F13	QCMD15	F21	MD102	F29	MD63
F6	QDATA24	F14	MECC2	F22	MD99		
F7	QDATA27	F15	MECC1	F23	MD92		

Table 28 Signals Listed by Pin Number (continued)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
F8	QDATA31	F16	MD128	F24	MD89		
G 1-29							
G1	VDD33	G9	VDD	G17	VDD	G25	VDD33
G2	TD7	G10	TD51	G18	MBA0	G26	MD80
G3	VSS	G11	VSS	G19	VSS	G27	VSS
G4	TD15	G12	QCLK	G20	MD119	G28	MD67
G5	VDD	G13	VDD33	G21	VDD	G29	VDD
G6	TD23	G14	MDQML	G22	MD106		
G7	VSS	G15	SCLKX	G23	VSS		
G8	TD43	G16	MECC0	G24	MD93		
H 1-29							
H1	TD3	H9	TD47	H17	NC2	H25	MA5
H2	TD11	H10	TD55	H18	NC3	H26	MA6
H3	TD14	H11	TD63	H19	MBA1	H27	MA8
H4	TD22	H12	VSS	H20	MCSX	H28	MA9
H5	TD27	H13	CCLK5	H21	MDQM	H29	MA11
H6	TD31	H14	VDD33	H22	MA0		
H7	TD35	H15	SCLK	H23	MA2		
H8	TD38	H16	VSS	H24	MA3		
I 1-29							
I1	VSS	I9	VSS	I17	VSS	I25	VSS
I2	TD6	I10	TD59	I18	NC1	I26	MA7
I3	VDD33	I11	VDD	I19	VDD	I27	VDD33
I4	TD19	I12	CCLK3	I20	MRASX	I28	MA10
I5	VSS	I13	VSS	I21	VSS	I29	VSS
I6	TD30	I14	CCLK4	I22	MA1		
I7	VDD	I15	VDD33	I23	VDD		
I8	TD42	I16	MCLK	I24	MA4		

Table 28 Signals Listed by Pin Number (continued)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
J 1-29							
J1	TD2	J9	TD49	J17	MDCLK	J25	MD52
J2	TD10	J10	TD50	J18	VSS	J26	MD55
J3	TD13	J11	TD62	J19	XPUHOT	J27	MD40
J4	TD21	J12	VDD	J20	MWEX	J28	MD32
J5	TD26	J13	CCLK1	J21	MCASX	J29	MD24
J6	TD33	J14	VSS	J22	MD56		
J7	TD37	J15	CCLK2	J23	MD48		
J8	TD46	J16	VDD33	J24	MD60		
K 1-29							
K1	VDD	K9	VDD	K17	VDD33	K25	VDD
K2	TD5	K10	TD61	K18	PSTOPX	K26	MD36
K3	VSS	K11	VSS	K19	VSS	K27	VSS
K4	TD18	K12	CCLK0	K20	PFRAMEX	K28	MD28
K5	VDD33	K13	VDD	K21	VDD	K29	VDD33
K6	TD32	K14	CCLK6	K22	MD47		
K7	VSS	K15	VSS	K23	VSS		
K8	TD41	K16	CCLK7	K24	MD44		
L 1-29							
L1	TD1	L9	TD48	L17	PREQX	L25	MD43
L2	TD9	L10	TD54	L18	PSERRX	L26	MD31
L3	TD12	L11	TD58	L19	PIRDYX	L27	MD35
L4	TD20	L12	JSO0	L20	PTRDYX	L28	MD23
L5	TD25	L13	CPREF	L21	MD59	L29	MD27
L6	TD29	L14	VDD	L22	MD51		
L7	TD36	L15	PCLK	L23	MD54		
L8	TD45	L16	VSS	L24	MD39		

Table 28 Signals Listed by Pin Number (continued)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
M 1-29							
M1	VSS	M9	VSS	M17	VSS	M25	VSS
M2	TD4	M10	TD60	M18	PPERRX	M26	MD30
M3	VDD	M11	VDD	M19	VDD33	M27	VDD
M4	TD17	M12	TCLKI	M20	PCBEX2	M28	MD22
M5	VSS	M13	VSS	M21	VSS	M29	VSS
M6	TD34	M14	SPCK	M22	MD46		
M7	VDD33	M15	VDD	M23	VDD		
M8	TD40	M16	SPLD	M24	MD38		
N 1-29							
N1	TD0	N9	TD57	N17	PRSTX	N25	MD37
N2	TD8	N10	NC4	N18	PDEVSELX	N26	MD34
N3	TA9	N11	NC6	N19	PGNTX	N27	MD29
N4	TA14	N12	JSO2	N20	PCBEX1	N28	MD26
N5	TD24	N13	JSO1	N21	PCBEX0	N29	MD21
N6	TD28	N14	SIDA	N22	MD58		
N7	TD44	N15	SPDO	N23	MD50		
N8	TD39	N16	SPDI	N24	MD42		
O 1-29							
O1	VDD	O9	VDD33	O17	VDD	O25	VDD
O2	TA4	O10	TD56	O18	PIDSEL	O26	MD33
O3	VSS	O11	VSS	O19	VSS	O27	VSS
O4	TD16	O12	TCLKO	O20	PCBEX3	O28	MD25
O5	VDD	O13	VDD	O21	VDD33	O29	VDD
O6	TA21	O14	SICL	O22	MD53		
O7	VSS	O15	VSS	O23	VSS		
O8	TD53	O16	PINTA	O24	MD41		

Table 28 Signals Listed by Pin Number (continued)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
P 1-29							
P1	TA1	P9	TD52	P17	PAD20	P25	MD17
P2	TA6	P10	NC5	P18	PAD14	P26	MD8
P3	TA8	P11	NC7	P19	PAD11	P27	MD11
P4	TA13	P12	JSO4	P20	PAD5	P28	MD2
P5	TA16	P13	JSO3	P21	PAD2	P29	MD5
P6	TA20	P14	PPAR	P22	MD45		
P7	TA21X	P15	PAD29	P23	MD57		
P8	TCE0X	P16	PAD23	P24	MD14		
Q 1-29							
Q1	VSS	Q9	VSS	Q17	VSS	Q25	VSS
Q2	TA3	Q10	TWE0X	Q18	PAD17	Q26	MD7
Q3	VDD	Q11	VDD33	Q19	VDD	Q27	VDD
Q4	TA11	Q12	JSO5	Q20	PAD8	Q28	MD1
Q5	VSS	Q13	VSS	Q21	VSS	Q29	VSS
Q6	TA19	Q14	PAD31	Q22	MD49		
Q7	VDD	Q15	VDD	Q23	VDD33		
Q8	TA19X	Q16	PAD26	Q24	MD13		
R 1-29							
R1	TA0	R9	TWE1X	R17	PAD13	R25	MD12
R2	TA5	R10	JSO9	R18	PAD10	R26	MD10
R3	TA7	R11	JSO8	R19	PAD7	R27	MD6
R4	TA12	R12	JSO7	R20	PAD4	R28	MD4
R5	TA15	R13	JSO6	R21	PAD1	R29	MD0
R6	TA18	R14	PAD28	R22	MD20		
R7	TA20X	R15	PAD22	R23	MD19		
R8	TCE1X	R16	PAD16	R24	MD16		

Table 28 Signals Listed by Pin Number (continued)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
S 1-29							
S1	VDD33	S9	VDD	S17	VDD	S25	VDD33
S2	TA2	S10	TWE2X	S18	PAD18	S26	MD9
S3	VSS	S11	VSS	S19	VSS	S27	VSS
S4	TA10	S12	JSE	S20	PAD9	S28	MD3
S5	VDD	S13	VDD33	S21	VDD	S29	VDD
S6	TA17	S14	PAD25	S22	MD18		
S7	VSS	S15	VSS	S23	VSS		
S8	TCE2X	S16	PAD19	S24	MD15		
T 1-29							
T1	FIN2	T9	TCE3X	T17	PAD21	T25	FOUT16
T2	FIN7	T10	TWE3X	T18	PAD15	T26	FOUT12
T3	FIN6	T11	JTCK	T19	PAD12	TT27	FOUT6
T4	FIN12	T12	JHIGHZ	T20	PAD6	T28	FOUT7
T5	FIN16	T13	JCLKBYP	T21	PAD3	T29	FOUT2
T6	FIN17	T14	PAD30	T22	PAD0		
T7	FIN19	T15	PAD27	T23	FOUT19		
T8	TA18X	T16	PAD24	T24	FOUT17		
U 1-29							
U1	VSS	U9	VSS	U17	VSS	U25	VSS
U2	FIN4	U10	FIN27	U18	FTXCTL0	U26	FOUT11
U3	VDD33	U11	VDD	U19	VDD	U27	VDD33
U4	FIN11	U12	FRXCTL0	U20	FOUT27	U28	FOUT4
U5	VSS	U13	VSS	U21	VSS	U29	VSS
U6	FIN15	U14	NC8	U22	FOUT24		
U7	VDD	U15	VDD33	U23	VDD		
U8	FIN24	U16	NC10	U24	FOUT15		

Table 28 Signals Listed by Pin Number (continued)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
V 1-29							
V1	FIN1	V9	FIN23	V17	FTXCTL5	V25	FOUT10
V2	FIN3	V10	FIN26	V18	FTXCTL2	V26	FOUT9
V3	FIN5	V11	FIN31	V19	FOUT31	V27	FOUT5
V4	FIN9	V12	FRXCTL2	V20	FOUT26	V28	FOUT3
V5	FIN10	V13	FRXCTL5	V21	FOUT23	V29	FOUT1
V6	FIN14	V14	NC9	V22	FOUT22		
V7	FIN18	V15	JTDO	V23	FOUT18		
V8	FIN22	V16	NC11	V24	FOUT14		
W 1-29							
W1	VDD	W9	VDD	W17	VDD33	W25	VDD
W2	FIN0	W10	FIN29	W18	FTXCTL1	W26	FOUT8
W3	VSS	W11	VSS	W19	VSS	W27	VSS
W4	FIN8	W12	FRXCTL1	W20	FOUT29	W28	FOUT0
W5	VDD33	W13	VDD	W21	VDD	W29	VDD33
W6	FIN13	W14	FRXCLK	W22	FOUT21		
W7	VSS	W15	VSS	W23	VSS		
W8	FIN21	W16	FTXCLK	W24	FOUT13		
X 1-29							
X1	CP15_0	X9	FIN25	X17	FTXCTL4	X25	CP14_4
X2	CP15_1	X10	FIN28	X18	FTXCTL3	X26	CP14_3
X3	CP15_2	X11	FIN30	X19	FOUT30	X27	CP14_2
X4	CP15_3	X12	FRXCTL3	X20	FOUT28	X28	CP14_1
X5	CP15_4	X13	FRXCTL4	X21	FOUT25	X29	CP14_0
X6	CP15_5	X14	FRXCTL6	X22	FOUT20		
X7	CP15_6	X15	JTRSTX	X23	CP14_6		
X8	FIN20	X16	FTXCTL6	X24	CP14_5		

Table 28 Signals Listed by Pin Number (continued)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
Y 1-29							
Y1	VSS	Y9	VSS	Y17	VSS	Y25	VSS
Y2	CP13_0	Y10	CP13_4	Y18	CP12_5	Y26	CP12_1
Y3	VDD	Y11	VDD	Y19	VDD33	Y27	VDD
Y4	CP13_1	Y12	CP13_5	Y20	CP12_4	Y28	CP12_0
Y5	VSS	Y13	VSS	Y21	VSS	Y29	VSS
Y6	CP13_2	Y14	CP13_6	Y22	CP12_3		
Y7	VDD33	Y15	VDD	Y23	VDD		
Y8	CP13_3	Y16	CP12_6	Y24	CP12_2		
Z 1-29							
Z1	CP9_0	Z9	CP11_1	Z17	CP10_5	Z25	CP8_4
Z2	CP9_1	Z10	CP11_2	Z18	CP10_4	Z26	CP8_3
Z3	CP9_2	Z11	CP11_3	Z19	CP10_3	Z27	CP8_2
Z4	CP9_3	Z12	CP11_4	Z20	CP10_2	Z28	CP8_1
Z5	CP9_4	Z13	CP11_5	Z21	CP10_1	Z29	CP8_0
Z6	CP9_5	Z14	CP11_6	Z22	CP10_0		
Z7	CP9_6	Z15	JTMS	Z23	CP8_6		
Z8	CP11_0	Z16	CP10_6	Z24	CP8_5		
AA 1-29							
AA1	VDD	AA9	VDD33	AA17	VDD	AA25	VDD
AA2	CP7_0	AA10	CP7_4	AA18	CP6_5	AA26	CP6_1
AA3	VSS	AA11	VSS	AA19	VSS	AA27	VSS
AA4	CP7_1	AA12	CP7_5	AA20	CP6_4	AA28	CP6_0
AA5	VDD	AA13	VDD	AA21	VDD33	AA29	VDD
AA6	CP7_2	AA14	CP7_6	AA22	CP6_3		
AA7	VSS	AA15	VSS	AA23	VSS		
AA8	CP7_3	AA16	CP6_6	AA24	CP6_2		
AB 1-29							

Table 28 Signals Listed by Pin Number (continued)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
AB1	CP3_0	AB9	CP5_1	AB17	CP4_5	AB25	CP2_4
AB2	CP3_1	AB10	CP5_2	AB18	CP4_4	AB26	CP2_3
AB3	CP3_2	AB11	CP5_3	AB19	CP4_3	AB27	CP2_2
AB4	CP3_3	AB12	CP5_4	AB20	CP4_2	AB28	CP2_1
AB5	CP3_4	AB13	CP5_5	AB21	CP4_1	AB29	CP2_0
AB6	CP3_5	AB14	CP5_6	AB22	CP4_0		
AB7	CP3_6	AB15	JTDI	AB23	CP2_6		
AB8	CP5_0	AB16	CP4_6	AB24	CP2_5		
AC 1-29							
AC1	VSS	AC9	VSS	AC17	VSS	AC25	VSS
AC2	CP1_0	AC10	CP1_4	AC18	CP0_5	AC26	CP0_1
AC3	VDD	AC11	VDD33	AC19	VDD	AC27	VDD
AC4	CP1_1	AC12	CP1_5	AC20	CP0_4	AC28	CP0_0
AC5	VSS	AC13	VSS	AC21	VSS	AC29	VSS
AC6	CP1_2	AC14	CP1_6	AC22	CP0_3		
AC7	VDD	AC15	VDD	AC23	VDD33		
AC8	CP1_3	AC16	CP0_6	AC24	CP0_2		

JTAG Support

The C-5 NP contains JTAG test logic compliant with the IEEE 1149.1 specification. All required public instructions are implemented, as well as some optional instructions. This section contains information regarding the pinout, instructions, identification codes, and boundary scan cell types.

Pinout

The C-5 NP uses the standard JTAG pins including the optional test reset pin. Table 26 describes the pins and their functions. Note that pins for JTRSTX, JTDI, and JTMS require external pullups on the board. These ports do not have internal pullups as required by the 1149.1 specification.

JTAG Data Registers

The C-5 NP contains the standard internal registers as specified in IEEE 1149.1. These registers are described in Table 29.

Table 29 JTAG Internal Register Descriptions

Register Name	Register Length	Description
Bypass	1	Standard JTAG bypass register
Boundary	1807	Boundary Scan Register
Device Identification	32	Standard JTAG IDCODE Register

Boundary Scan Cell Types

The C-5 NP boundary scan register contains only two cell types. All input cells are *observe only* cells of type BC_4. All enable and output cells are standard cells of type BC_1. In IEEE 1149.1-1990 specification, the BC_4 cell is shown in Figure 7 and the BC_1 cell is shown in Figure 8.

Figure 7 Observe-Only Cell

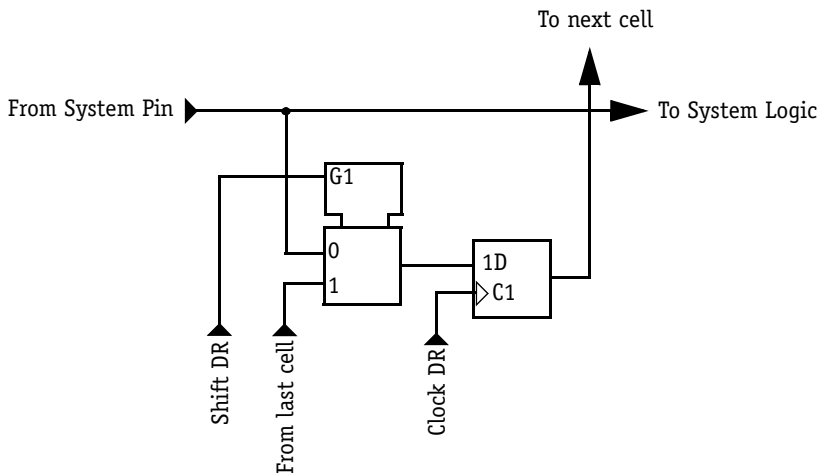
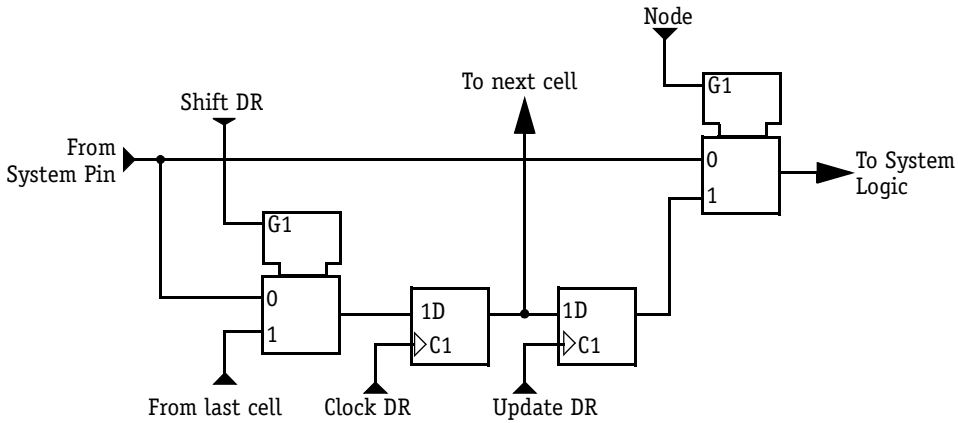


Figure 8 Cell Design That Can Be Used for Both Input and Output Pins



IDcode Register

The C-5 NP implements a standard 32bit JTAG identification register. Table 30 lists the value of the code for full identification and its sub-components.

Table 30 JTAG Identification Code and Its Sub-components

Field Name	Width	Bit Positions	Binary Value
Version	4	31-28	0000
Part Number	16	27-12	0000_0000_0000_0010
Manufacturer Identity	11	11-1	001_1001_0110
LSB	1	0	1

The concatenated 32bit value is hexidecimal 0000232d.

JTAG Instruction Register

The C-5 NP contains a 4bit instruction register. Table 31 lists the instructions that are supported.

Table 31 Instruction Register Instructions

Instruction Mnemonic	Selected Register	Instruction Opcode
Extest	Boundary Scan	0000
Idcode	Identification Register	0001
Sample/Preload	Boundary Scan	0010
Highz	Bypass Register	0011
Clamp	Bypass Register	0100
Bypass	Bypass Register	0101
Reserved*	Bypass Register	0110
Reserved*	Bypass Register	0111
Bypass	Bypass Register	1000
Bypass	Bypass Register	1001
Bypass	Bypass Register	1010
Bypass	Bypass Register	1011
Bypass	Bypass Register	1100
Bypass	Bypass Register	1101
Bypass	Bypass Register	1110
Bypass	Bypass Register	1111

* There are two reserved instructions intended for C-Port Corporation's internal use. These should not be programmed by users.

Boundary Scan Description Language

In order to simplify board test, C-Port Corporation has provided a boundary scan description language (BSDL) file in the C-Port web site support area that describes the complete set of instructions, boundary scan order, and identification code value in an industry standard format. This information can be found at: http://e-www.motorola.com/webapp/sps/site/homepage.jsp?nodeId=03M0ylgx1Ks.

Chapter 3

Electrical Specifications

Absolute Maximum Ratings

Table 32 lists the absolute maximum ratings for the C-5 network processor. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those listed under "Recommended Operating Conditions" (Table 33) is possible.

Exposure to conditions beyond Table 32 can:Reduce device reliability

- Result in premature device failure, even with no immediate sign of failure

Prolonged exposure to conditions at or near the absolute maximum ratings could also result in reduced useful life and reliability of the C-5 NP.

Table 32 C-5 Network Processor Absolute Maximum Ratings

Parameter	Min	Max	Unit
V_{DD33} Supply Voltage (3.3V input)*†	-0.5	+5	V
V_{DD} Supply Voltage (1.8V input)*	-0.5	+2.8	V
Voltage on any pin	-0.5	V_{DD33} + 0.5	V
Static Discharge Voltage	2000/500		V
Storage Temperature	-40	+125	°C
Absolute Maximum Junction Temperature	-40	+125	°C

* Voltages are relative to Ground

† Not to exceed V_{DD} + 2.5V

Recommended Operating Conditions

The recommended operating conditions describe an environment the C-5 NP network processor is expected to encounter during normal operation. Table 33 delineates the recommended operating parameters for the C-5 NP.

Table 33 C-5 Network Processor Recommended Operating Conditions

Parameter	Min	Max	Unit
V_{DD33} Supply Voltage	3.135	3.465	V
V_{DD} Supply Voltage	1.7	1.9	V
I_{DD33} - V_{DD33} Supply Current		1.5*	A
I_{DD} - V_{DD} Supply Current		14*	A
T_j Junction Temperature	-40	100	°C

* Peak values to be used by power supply designer.

DC Characteristics

The DC electrical characteristics define the input operating conditions for proper operation and the output responses to applied DC signals and switch characteristics over specified voltage and temperature ranges. The DC electrical characteristics are specified within the *recommended operating conditions* including operating temperature and power supply range as stated in this data sheet. Table 34 outlines the C-5 NP DC characteristics.

Table 34 C-5 Network Processor DC Characteristics

Parameter*	Min	Max	Unit	Notes
LVTTL Input High Voltage	2.0	V_{DD33}+.3	V	
LVTTL Input Low Voltage	-0.3	0.8	V	
LVTTL Output High Voltage	2.4		V	@I_{OH} = -2mA
LVTTL Output Low Voltage		0.4	V	@I_{OL} = +2mA
LVTTL Input Current	-5	+5	µA	V_{IN} = 0V or V_{DD33}
LVPECL Input High Voltage	V_{DD33} -1.165	V_{DD33}+.3V	V	
LVPECL Input Low Voltage	-0.3	V_{DD33} -1.475	V	
LVPECL Output High Voltage	V_{DD33} -1.025	V_{DD33} -0.880	V	Load = 50ohm to V_{DD33} - 2V
LVPECL Output Low Voltage	V_{DD33} -1.810	V_{DD33} -1.620	V	Load = 50ohm to V_{DD33} - 2V
LVPECL Input Current	-5	+5	µA	
CPREF	V_{DD33} -1.38	V_{DD33} -1.26	V	Single-ended LVPECL reference

* All voltages are relative to Ground unless otherwise indicated.

Each control input pin has a capacitance associated with it. The capacitance at the control input is due to the package and the input circuitry connected to the pin. Capacitance is based on these conditions: T_A = 25°C; V_{DD33} = 3.3V; f = 1MHz. Table 35 provides capacitance data.

Table 35 C-5 Network Processor Capacitance Data

Parameter	Typical	Max	Unit
Input/Output Pins	7	8	pF
Input Pins	6	7	pF
Clock Pins	6	7	pF

Power Sequencing

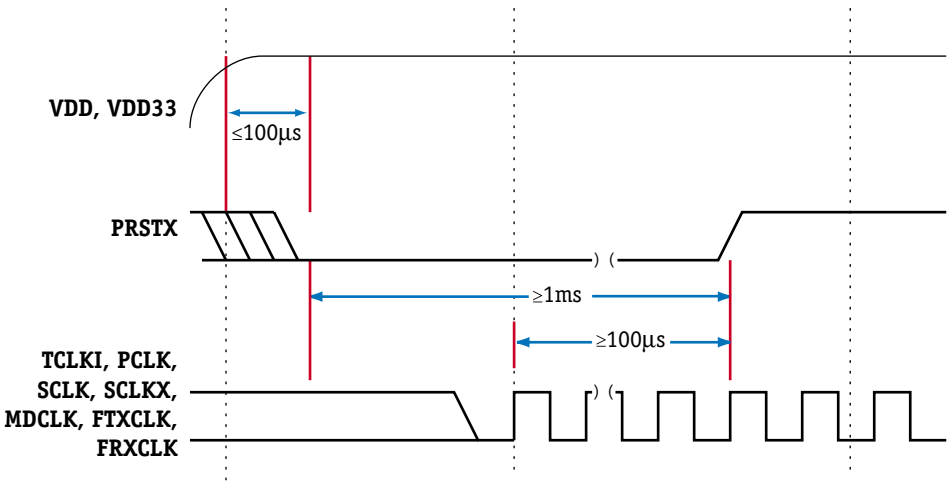
The VDD rail must be kept within 2.5V of the VDD33 rail. However, this rule can be violated for periods up to one second, as is typical during power sequencing, as long as:

- The VDD is not clamped to ground or some other low voltage.
- The number of power cycling events averages to less than once per day over the lifetime of the product.

It is intended that the VDD and VDD33 rail be sequenced to their final value together for most applications.

It is also required that SCLK, SCLKX, TCLKI, PCLK, MDCLK, FTXCLK, and FRXCLK be running or begin running during power sequencing to propagate reset inside the C-5 NP. Figure 9 indicates the relationship between the clocks and PRSTX. There is no requirement that the asserting and deasserting edges of PRSTX be synchronous to the clocks. Reset must be asserted within 100µs of power initiation. Typically, reset is held low during power initiation.

Figure 9 Bringup Clock Timing Diagram



Power and Thermal Characteristics

Table 36 provides the derived power and thermal characteristics for the production version (Revision D0) of the C-5 NP.

Table 36 C-5 Network Processor Power and Thermal Characteristics

Parameter	Min	Typ	Max	Units	Test Conditions
Power Dissipation, P_D	10.5 11.5 12.5 14.5	15.0 16.0 17.5 20.0	18.0 19.0 20.5 23.0	W	166MHz core clock (See Note 1) 180MHz core clock (See Note 1) 200MHz core clock (See Note 1) 233MHz core clock (See Note 1)
Maximum Junction Temperature, T_J			100	°C	
Thermal Resistance, junction to case, ϕ_{JC}		0.24		°C/W	See Note 2
Thermal Resistance, junction to ambient, ϕ_{JA}		1.87		°C/W	See Note 2
Thermal Resistance, junction to printed circuit board, ϕ_{JB}		4.8		°C/W	See Note 2
Thermal Resistance, Junction through Board to Ambient, ϕ_{JBA}		6.0			See Note 2
Effective Thermal Resistance, $\phi_{effective}$		1.43		°C/W	See Note 3

Notes for Table 36:

1 Estimated power dissipation (+/-10%) is derived from measurements on the C-5 NP Revision D00 under following conditions:

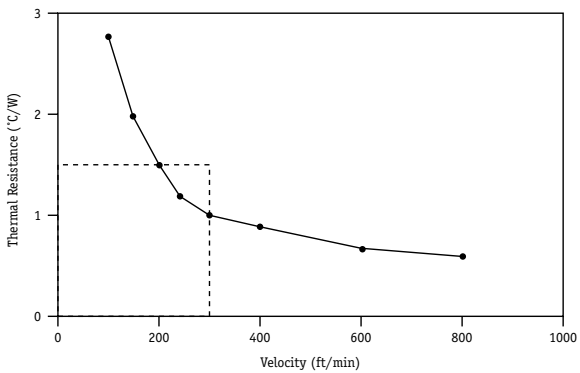
- BMU memory operating at 125MHz.
- TLU memory operating at 133MHz.
- V_{DD} = 1.8V, V_{DD33} = 3.3V, T_J at approximately 50° C.
- "Minimum" P_D based on idle condition (clocks running and no programs executing).
- "Typical" P_D based on test application that implements Fast Ethernet forwarding actively running on all CPs.
- "Maximum" P_D based on projected maximum consumption for any high-bandwidth communications application executing on all CPs, FP, and XP.

2 Thermal performance specifications based on following conditions:

- Printed circuit board is based on the C-Ware Development System's C-5 NP Switch Module reference design, with specifications of:
  - 14 total layers (5 planes). Planes at least 100mm x 100mm below the C-5 NP before any interruptions.
  - FR4 board material, Cu signal and plane material.
  - 0.5mils signal layer thickness, 1.4mils plane layer thickness.
  - Thermal resistance, board to ambient (ϕ_{BA}) of 1.2 °C/W.
- Custom heat sink design has the following characteristics:
  - Dimensions: 100mm x 80mm x 10mm (height)
  - Thermal resistance heat sink to ambient (ϕ_{SA}) of 1.6 °C/W @200 LFM. Figure 10 provides the characteristic thermal resistance curve for this head sink for various airflow rates.
  - Thermal resistance case to heat sink (ϕ_{CS}) of 0.03 °C/W (Chomerics T705 thermal material).
  - Note that target heat sink design is for low profile (10mm height) applications. Significantly better thermal performance is possible with taller and/or wider designs. Contact your C-Port representative for heat sink options.

3 Effective Thermal Resistance ($\phi_{effective} = \phi_{JA}\phi_{JB} / (\phi_{JA} + \phi_{JB})$) reflects the total thermal performance of the heat sink and board, as outlined in Note 2 above.

Figure 10 Thermal Performance for C-5 Network Processor Heat Sink (see step 2 above)



Theoretical calculation of thermal resistance as a function of airflow velocity across heat sink

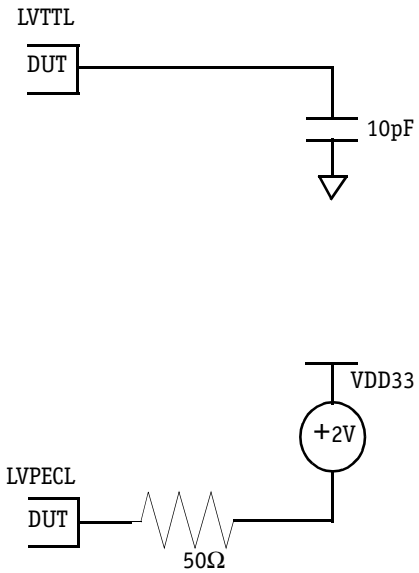
AC Timing Specifications

AC timing specifications consist of input requirements and output responses. The input requirements include setup and hold times, pulse widths, and high and low times. The output responses include delays from clock to signal. The AC timing specifications are defined separately for each interface to the C-5 NP

Unless otherwise noted, all AC specifications were tested within the functional operating range.

See Figure 11. Output timing specifications for LVTTL pins are given with a 10pF load on the output. Other loads can be simulated with the IBIS model available from C-Port. The LVPECL driver is specified into a 50Ω load terminated to a (VDD33 - 2V) reference.

Figure 11 Test Loading Conditions



Clock Timing Specifications

The system clock timing is shown in Figure 12 and described in Table 37.

Figure 12 System Clock Timing Diagram

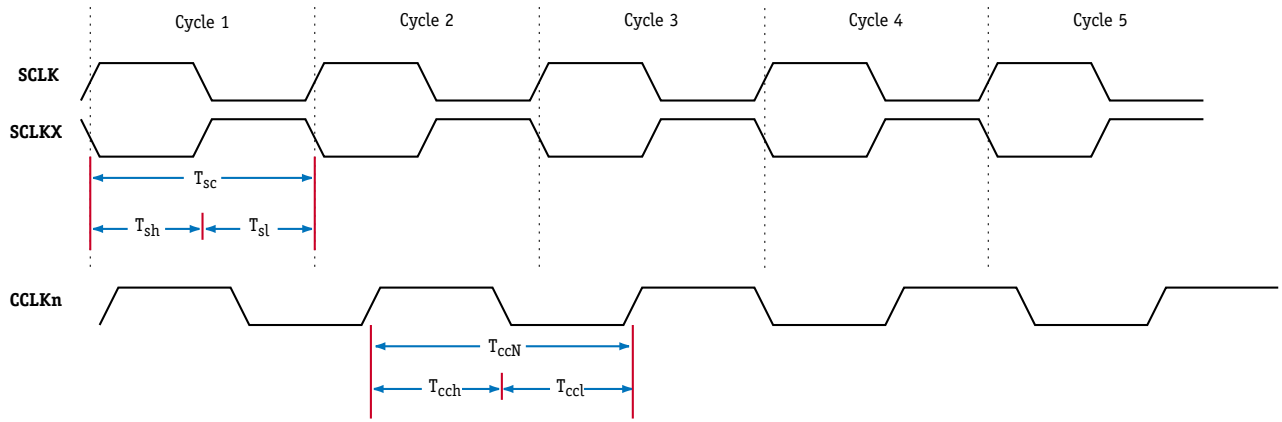


Table 37 System Clock Timing Description

Symbol	Parameter	Min 1X Clk Mode	Min 2X Clk Mode	Typ	Max 1X Clk Mode	Max 2X Clk Mode	Unit	Comment
Tsc	System Cycle Time	6.0 5.0 4.3	3.0 2.5 2.14				ns	166MHz core clock 200MHz core clock 233MHz core clock
Tsh	Sys Clk High Pulse	45	30		55	70		Duty cycle*
Tsl	Sys Clk Low Pulse	45	30		55	70		Duty cycle†
Tcc0	CCLK0 Cycle Time			647.67			ns	T1†
Tcc1	CCLK1 Cycle Time			488.28			ns	E1†
Tcc2	CCLK2 Cycle Time			29.097			ns	E3†
Tcc3	CCLK3 Cycle Time			22.353			ns	T3†
Tcc4	CCLK4 Cycle Time			20.00			ns	RMII†
Tcc5	CCLK5 Cycle Time			9.412			ns	Fibre Channel†
Tcc6	CCLK6 Cycle Time			8.00			ns	GMII†
Tcc7	CCLK7 Cycle Time			6.43			ns	OC-3†
Tcch	CCLKm High Time	40%	40%		60%	60%		% cycle pulse is high
Tccl	CCLKm Low Time	40%	40%		60%	60%		% cycle pulse is low

* Pulse duty cycle measured at crossing voltage of SCLK/SCLKX

† The frequencies specified for CCLK0 - CCLK7 allow full flexibility for the C-5 NP . Clock inputs associated with a specific protocol should be tied to ground when that protocol is not used by the C-5 NP . It is also possible to use one or more CCLK*n* inputs for other frequencies; contact your C-Port representative for more information.

Unused clocks should be pulled to a known state (ground) through a resistor. If you are using a clock generator, disabling the output should not cause a tristate. If it does, then the line should be pulled down.

CP Timing Specifications

This section describes the timing for the following CP interfaces:

- DS1/DS3
- 10/100 Ethernet
- Gigabit Ethernet
- OC-3
- OC-12

DS1/DS3 Timing Specifications

The DS1/DS3 interface timing is shown in Figure 13 and described in Table 38.

Figure 13 DS1/DS3 Ethernet Timing Diagram

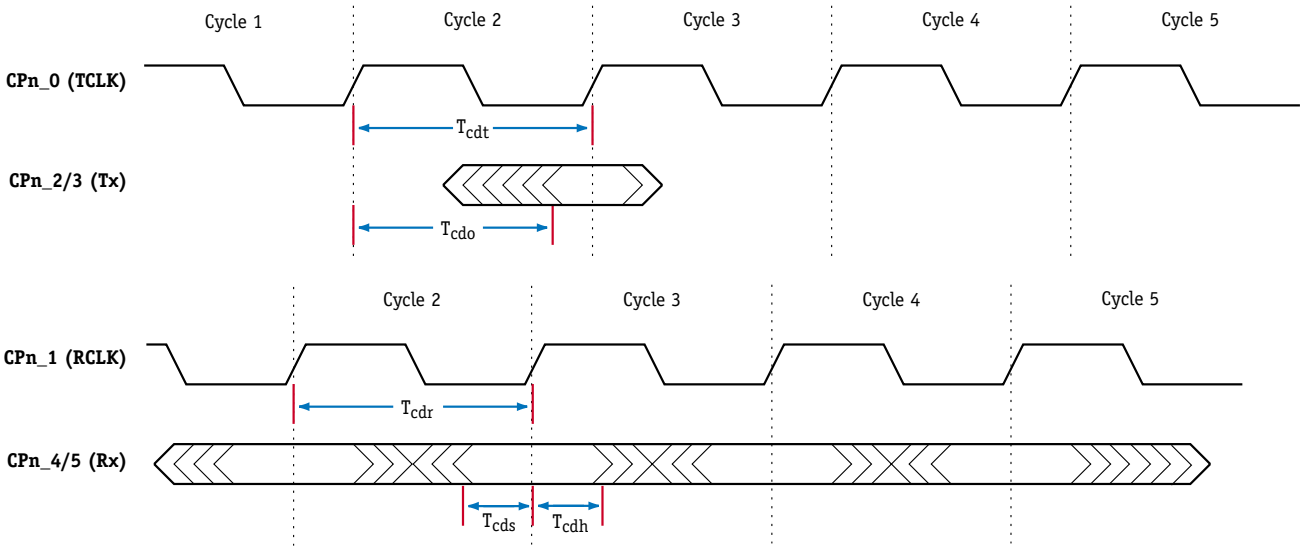


Table 38 DS1/DS3 Ethernet Timing Description

Symbol	Parameter	Min	Typ	Max	Unit
Tcdt	DS1/DS3 Transmit Cycle Time		647/22.4		ns
Tcdo	DS1/DS3 Output Time	3.0/3.0		400/15.0	ns
Tcdr	DS1/DS3 Receive Cycle Time		647/22.4		ns
Tcds	DS1/DS3 Setup Time	2.0			ns
Tcdh	DS1/DS3 Hold Time	2.5			ns

10/100 Ethernet Timing Specifications

The 10/100 Ethernet interface timing is shown in Figure 14 and described in Table 39.

Figure 14 10/100 Ethernet Timing Diagram

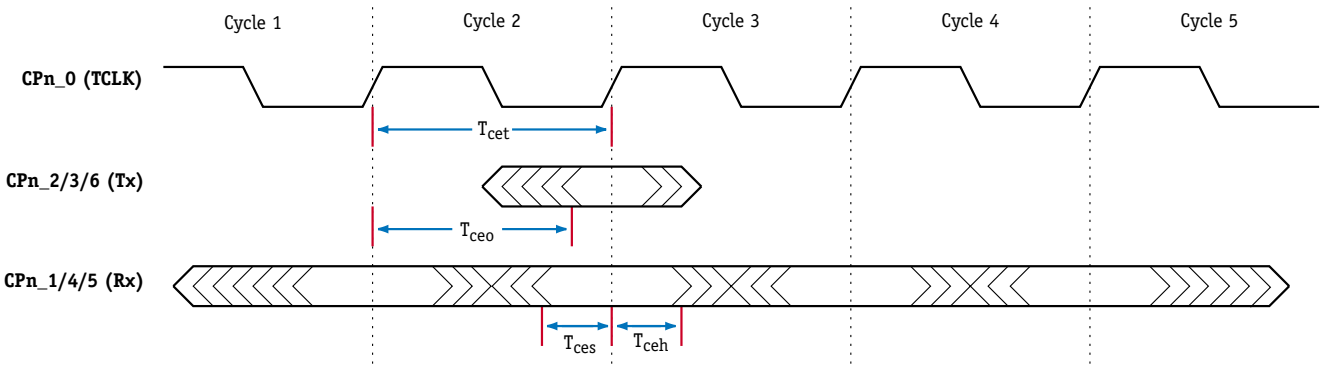


Table 39 10/100 Ethernet Timing Description

Symbol	Parameter	Min	Typ	Max	Unit
Tcet	Transmit Cycle Time*		20		ns
Tceo	Output Time	3.0		15.0	ns
Tces	Setup Time	2.0			ns
Tceh	Hold Time	2.5			ns

* STD/Fast Ethernet

Gigabit GMII Ethernet, TBI and MII Interface Timing Specifications

The Gigabit GMII Ethernet interface timing is shown in Figure 15 and described in Table 40. The TBI interface timing is shown in Figure 15 and described in Table 41.

Figure 15 Gigabit Ethernet and TBI Interface Timing Diagram

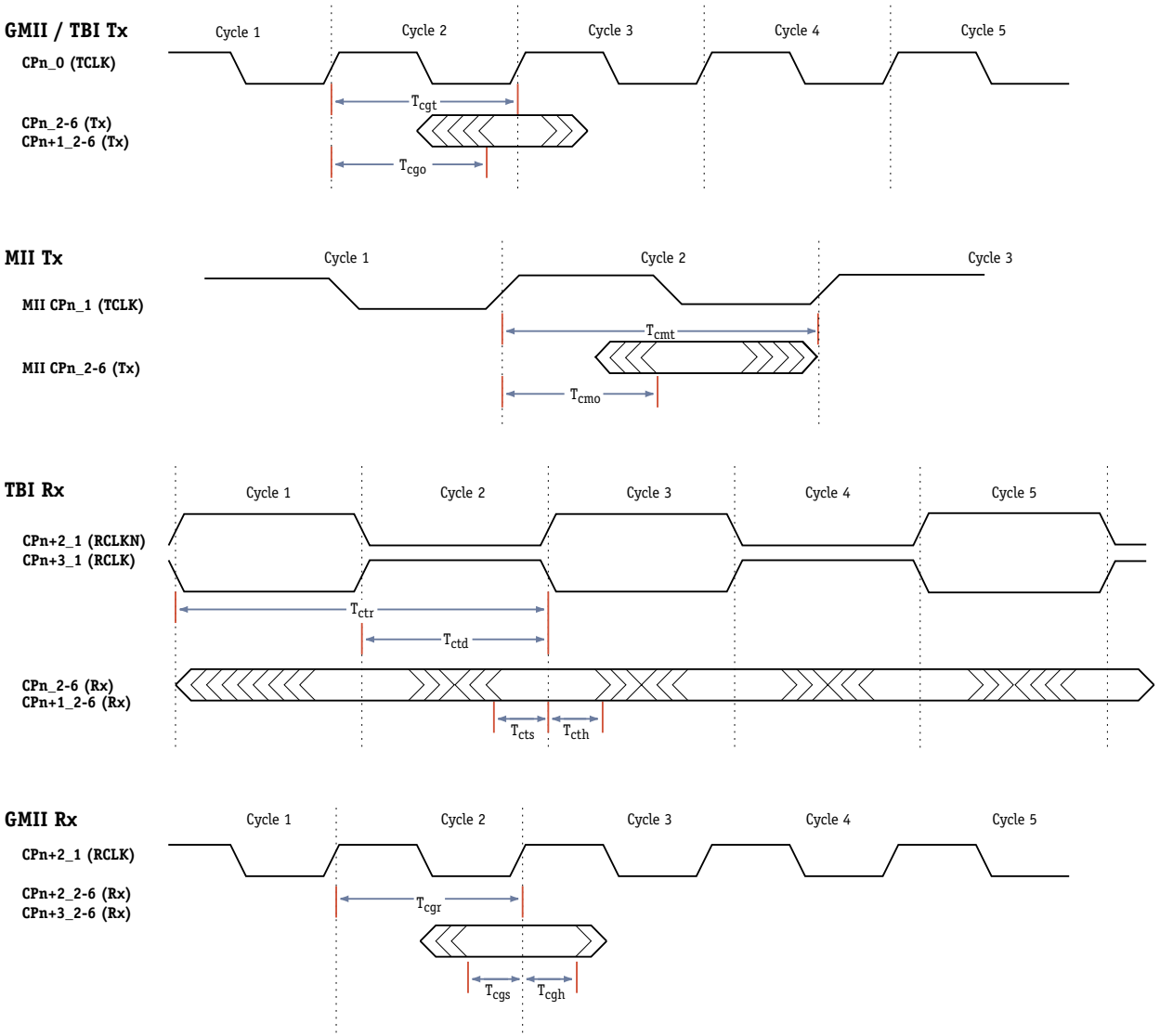


Table 40 Gigabit GMII/MII Ethernet Interface Timing Description

Symbol Gigabit	Parameter	Min	Typ	Max	Unit	Comment
Tcgt	Transmit Cycle Time, GMII		8.0		ns	
Tcgo	Output Time, GMII	3.0		6.0	ns	
Tcgr	Receive Cycle Time		8.0		ns	
Tcgs	Setup Time	1.5			ns	
Tcgh	Hold Time	0.5			ns	
Tcmt	Transmit Cycle Time, MII		40/400		ns	100BaseT/10BaseT
Tcmo	Output Time, MII	2		12	ms	

Table 41 Gigabit TBI Interface Timing Description

Symbol TBI	Parameter	Min	Typ	Max	Unit
Tctt	Transmit Cycle Time		8.0		ns
Tcto	Output Time	3.0		6.0*	ns
Tctr	Receive Cycle Time		16.0		ns
Tctd	Rclk/Rclkn Deviation			1.0	ns
Tcts	Setup Time	1.5			ns
Tcth	Hold Time	0.5			ns

* For Fibre Channel applications this value is 7.0ns for a transmit cycle time of 9.4ns.

OC-3 Timing Specifications

The OC-3 interface timing is shown in Figure 16 and described in Table 42.

Figure 16 OC-3 Timing Diagram

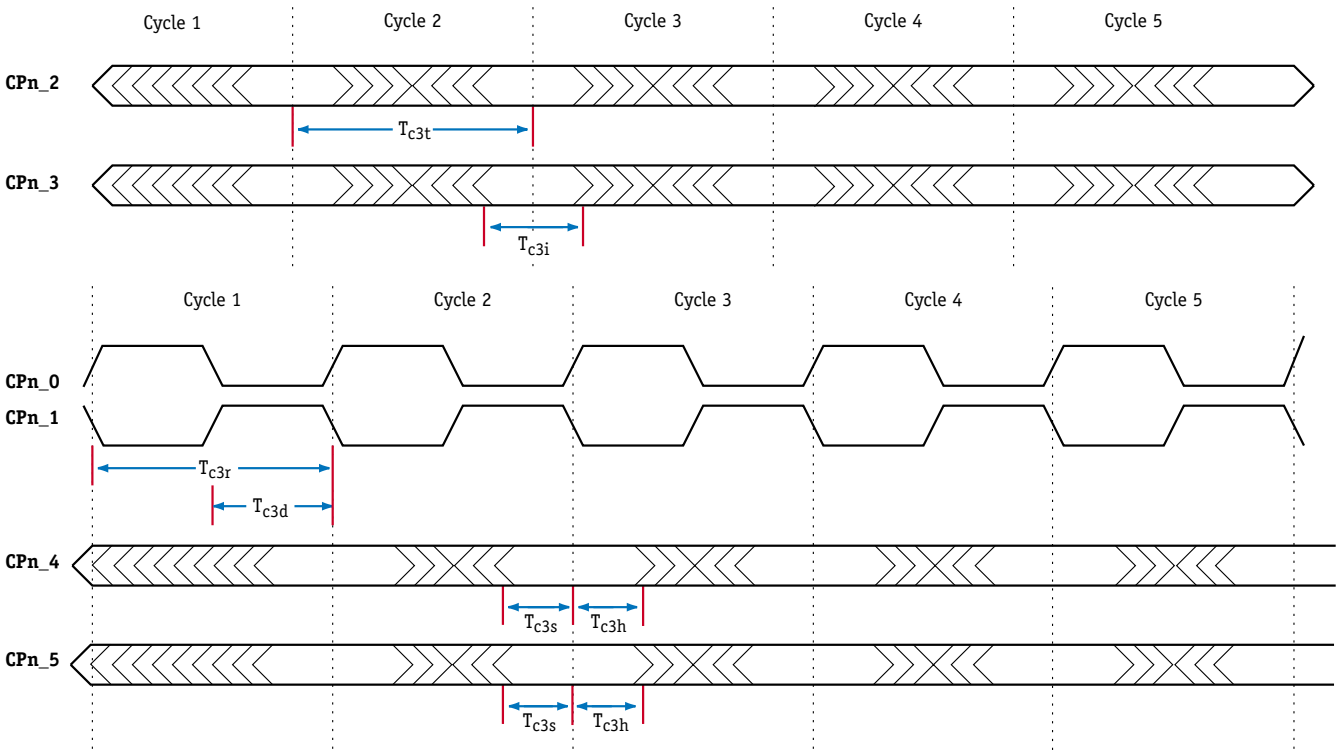


Table 42 OC-3 Timing Description

Symbol	Parameter	Min	Typ	Max	Unit
Tc3t	OC-3 Transmit Cycle Time		6.43		ns
Tc3i	OC-3 Pulse Width	2.0			ns
Tc3r	OC-3 Receive Cycle Time*	6.0			ns
Tc3d	OC-3 Clock Duty Cycle	40		60	%
Tc3s	OC-3 Setup Time	2.0			ns
Tc3h	OC-3 Hold Time	2.5			ns

* 155.52MHz

OC-12 Timing Specifications

The OC-12 interface timing is shown in Figure 17 and described in Table 43.

Figure 17 OC-12 Timing Diagram

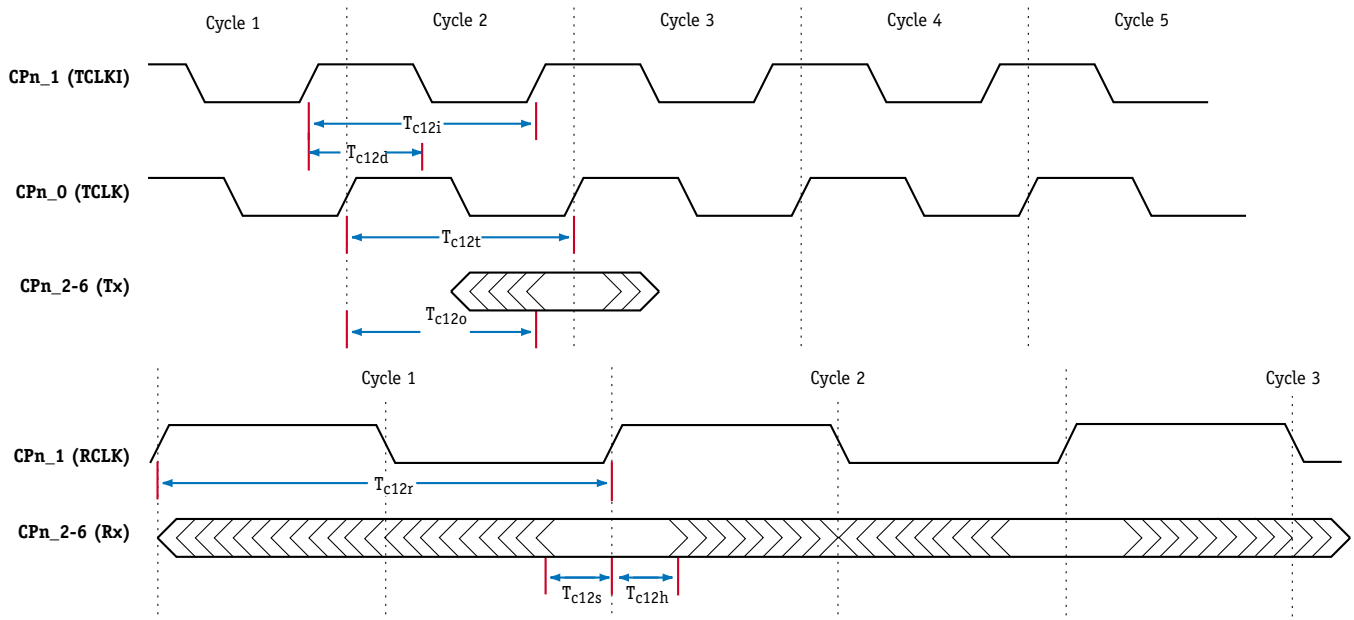


Table 43 OC-12 Timing Description

Symbol	Parameter	Min	Typ	Max	Unit
Tc12i	OC-12 Transmit Cycle Time*		12.86		ns
Tc12d	OC-3 Clock Duty Cycle	40		60	%
Tc12t	OC-12 Transmit Cycle Time†		12.86		ns
Tc12o	OC-12 Output Time‡	3.0		10.0	ns
Tc12r	OC-12 Receive Cycle Time	12.0	12.86		ns
Tc12s	OC-12 Setup Time	2.0			ns
Tc12h	OC-12 Hold Time	2.5			ns

* Input from PHY
† Output from C-5 NP
‡ Aligned to TCLK

Executive Processor Timing Specifications

The XP timing specifications include:

- PCI Timing Specifications
- MDIO Serial Interface Timing Specifications
- Low Speed Serial Interface Timing Specifications
- PROM Interface Timing Specifications

PCI Timing Specifications

The PCI timing is shown in Figure 18 and described in Table 44.

Figure 18 PCI Timing Diagram

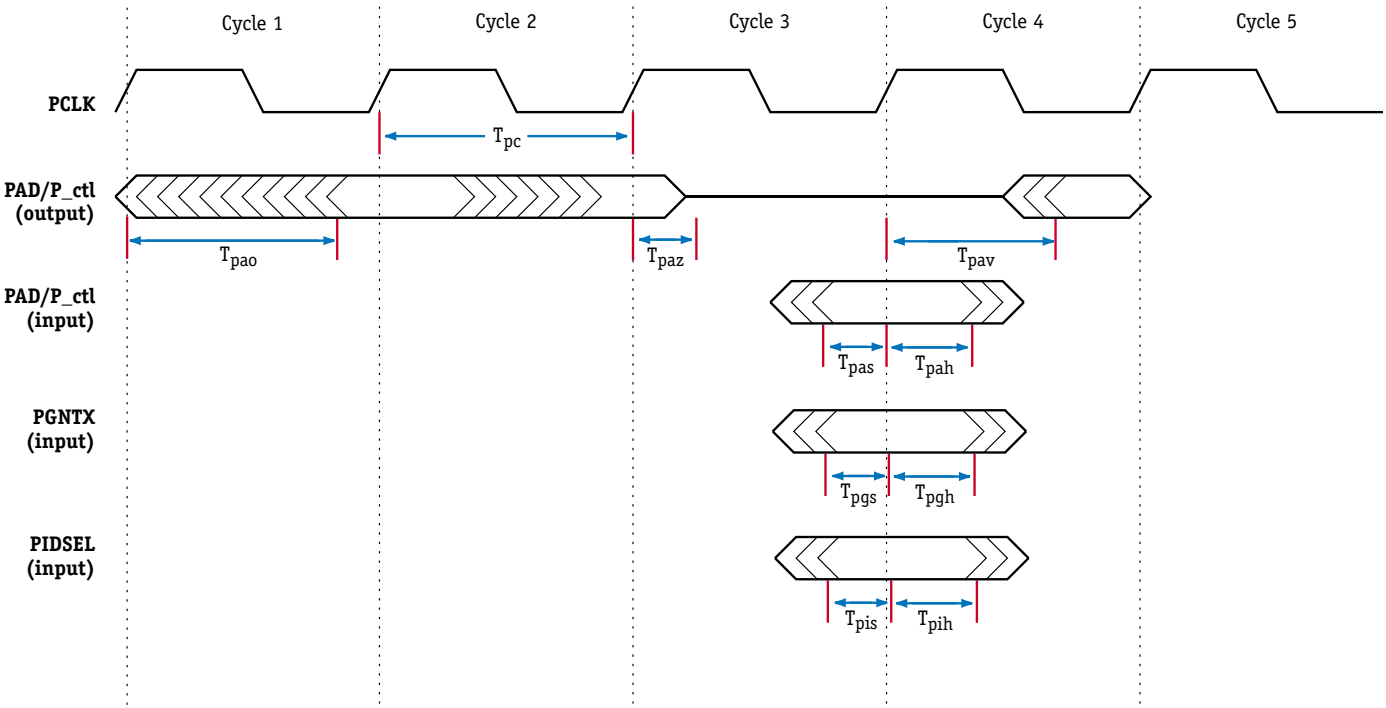


Table 44 PCI Timing Description

Symbol	Parameter	Min	Typ	Max	Unit
Tpc	PCI Cycle Time*	15.0			ns
Tpas	PAD/P_ctl† Setup	3.0			ns
Tpah	PAD/P_ctl Hold	0.0			ns
Tpao	PAD/P_ctl Output	2.0		6.0	ns
Tpaz	PAD/P_ctl Clk to Tri‡	1.8		5.5	ns
Tpav	PAD/P_ctl Clk to Driven‡	1.3		5.5	ns
Tpgs	PGNTX Setup	5.1			ns
Tpgh	PGNTX Hold	0.0			ns
Tpis	PIDSEL Setup	5.0			ns
Tpih	PIDSEL Hold	0.0			ns
	PRSTX**				ns
	PINTA**				ns

* 66MHz PCI

† P_ctl includes all PCI control parameters including: PPAR, PFRAMEX, PTRDYX, PIRDYX, PSTOPX, PDEVSELX, PPERRX, PSERRX

‡ Not fully tested, values based on design/characterization.

** Asynchronous

MDIO Serial Interface Timing Specifications

The MDIO serial interface timing is shown in Figure 19 and described in Table 45.

Figure 19 MDIO Serial Interface Timing Diagram

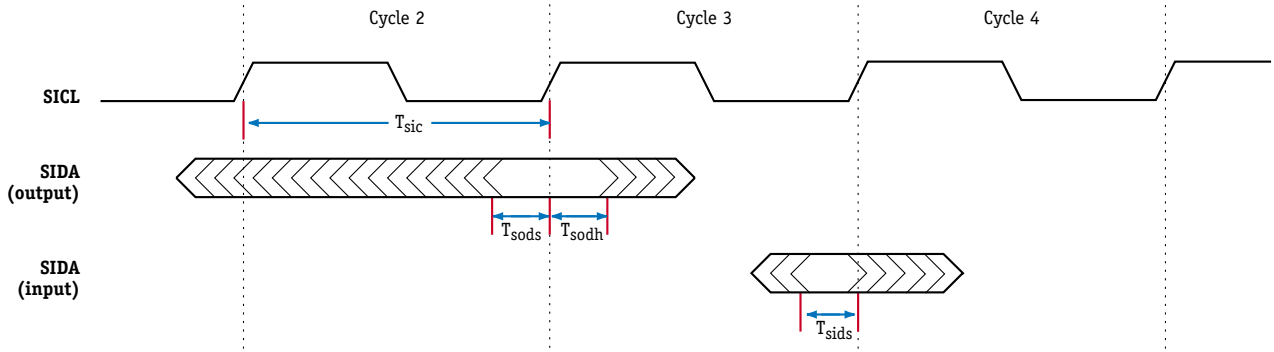


Table 45 MDIO Serial Interface Timing Description

Symbol	Parameter	Min	Typ	Max	Unit
Tsic	SICL Cycle Time	40			ns
Tsids	SIDA Input Setup	10			ns
Tsidh	SIDA Input Hold	0.0			ns
Tsods	SIDA Output Setup	10			ns
Tsodh	SIDA Output Hold	10			ns

Low Speed Serial Interface Timing Specifications

The low speed serial interface timing is shown in Figure 20 and described in Table 46.

Figure 20 Low Speed Serial Interface Timing Diagram

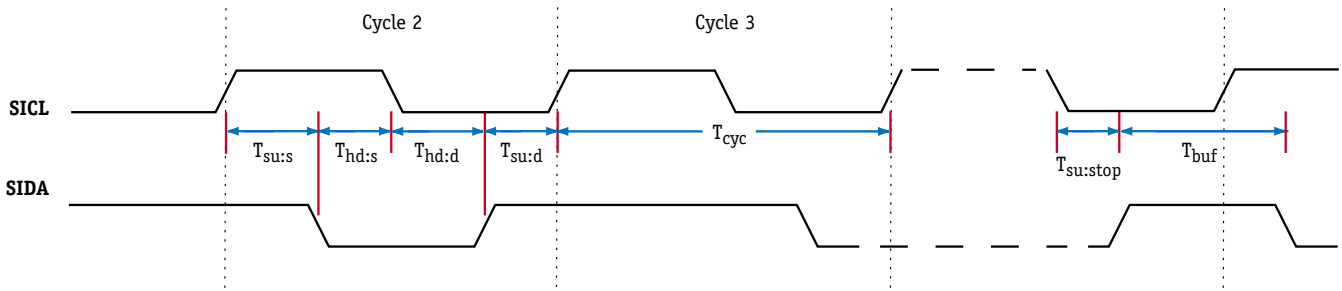


Table 46 Low Speed Serial Interface Timing Description

Symbol	Parameter	Min	Max	Unit
Tcycle	SICL Cycle Time	2500		ns
Tsu:s	Set-up Time for Repeated START Condition	600		ns
Thd:s	Hold Time START Condition	600		ns
Tsu:d	Data Set-up Time	250		ns
Thd:d	Data Hold Time	0.0		ns
Tsu:stop	Set-up Time for STOP Condition	600		ns
Tbuf	Bus Free Time Between a STOP and START Condition	1250		ns
Cmax	Capacitive load for each line of the bus		400	pF

PROM Interface Timing Specifications

The PROM interface timing is shown in Figure 21 and described in Table 47.

Figure 21 PROM Interface Timing Diagram

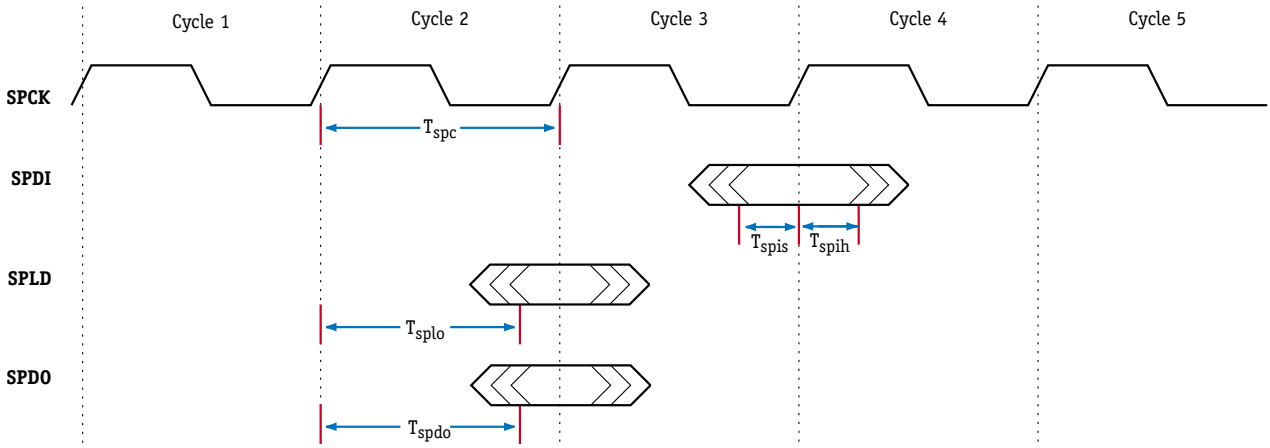


Table 47 PROM Interface Timing Description

Symbol	Parameter	Clock Mode	Min	Typ	Max	Unit
Tspc	SPCK Cycle Time		40.0			ns
Tspis	SPDI Setup		10.0			ns
Tspih	SPDI Hold		0.0			ns
Tsplo	SPLD Output	1X	Tsc*		Tsc + 3.0	ns
		2X	2 x Tsc*		2 x Tsc + 3.0	ns
Tspdo	SPDO Output	1X	Tsc*		Tsc + 3.0	ns
		2X	2 x Tsc*		2 x Tsc + 3.0	ns

* Tsc is the System Cycle Time. See Table 37 on page 70

Fabric Processor Timing Specifications

The FP timing specifications are shown in Figure 22 and described in Table 48.

Figure 22 Fabric Processor Timing Diagram

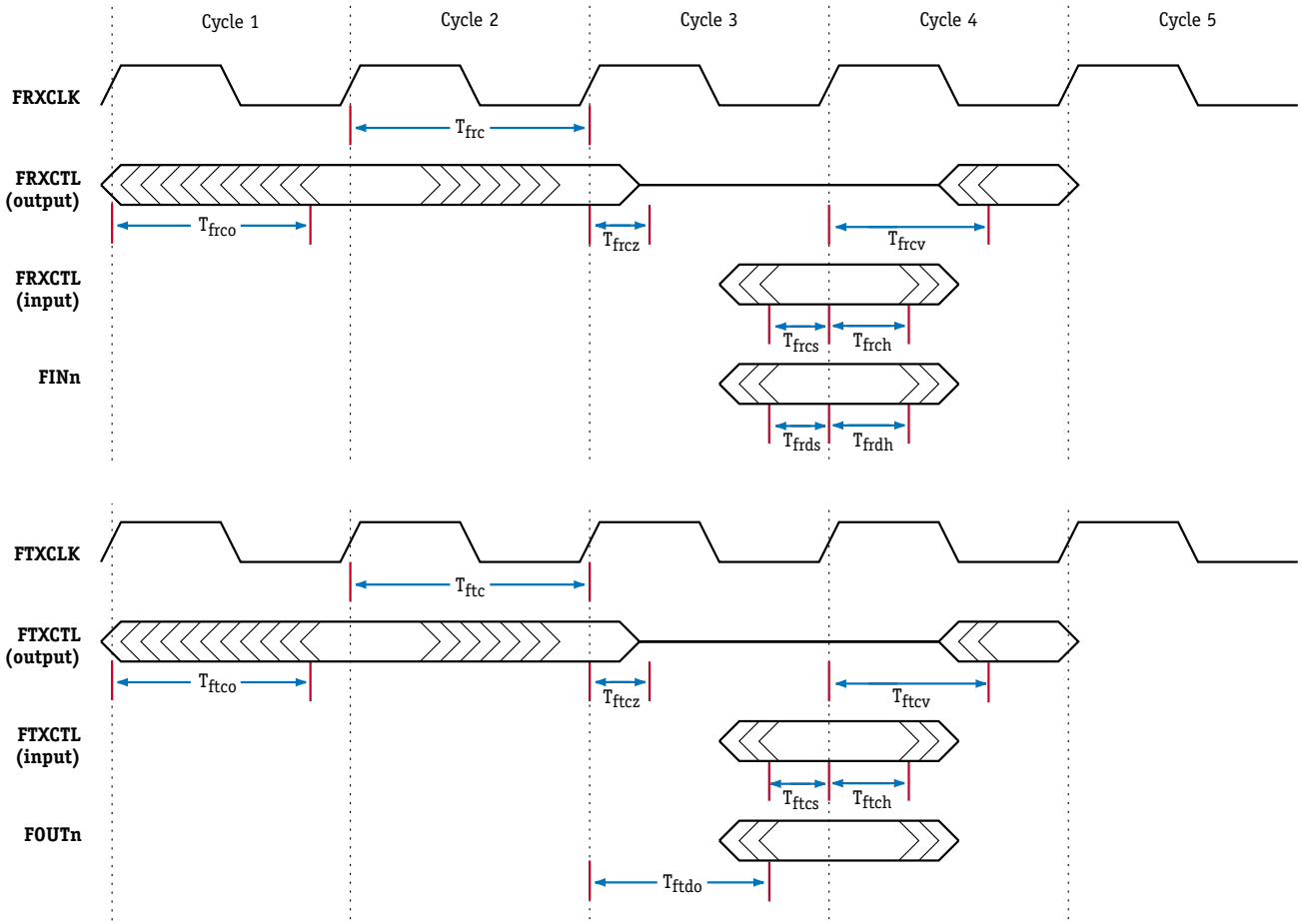


Table 48 Fabric Processor Timing Description

Symbol	Parameter	Min	Typ	Max	Unit	Comment
Tfrc	FRX Cycle Time	9.0			ns	
Tfrcs	FRXCTL Setup	4.0 1.5			ns	Utopia2 Mode All other modes
Tfrch	FRXCTL Hold	0.5			ns	
Tfrco	FRXCTL Output	1.0		3.4	ns	
Tfrcz	FRXCTL Clk to Tri*	1.8		5.5	ns	
Tfrcv	FRXCTL Clk to Driven*	1.3		5.5	ns	
Tfrds	FIN Setup	4.0 1.5			ns	Utopia2 Mode All other modes
Tfrdh	FIN Hold	0.5			ns	
Tftc	FTX Cycle Time	9.0			ns	
Tftcs	FTXCTL Setup	4.0 1.5			ns	Utopia2 Mode All other modes
Tftch	FTXCTL Hold	0.5			ns	
Tftco	FTXCTL Output	1.0		3.6	ns	
Tftcz	FTXCTL Clk to Tri*	1.7		5.5	ns	
Tftcv	FTXCTL Tri to Driven*	1.3		5.5	ns	
Tftdo	FOUT Output	1.0		3.6	ns	

* Not fully tested, values based on design/characterization.

BMU Timing Specifications

The BMU timing specifications are shown in Figure 23 and described in Table 49.

The BMU synchronous DRAM interface is PC100-compliant and designed to work with industry standard SDRAM components with 12 or fewer address lines. The information below is intended to provide the output, setup, and hold data required to design this interface without duplicating the transaction waveform diagrams in SDRAM data sheets.

Figure 23 BMU Timing Diagram

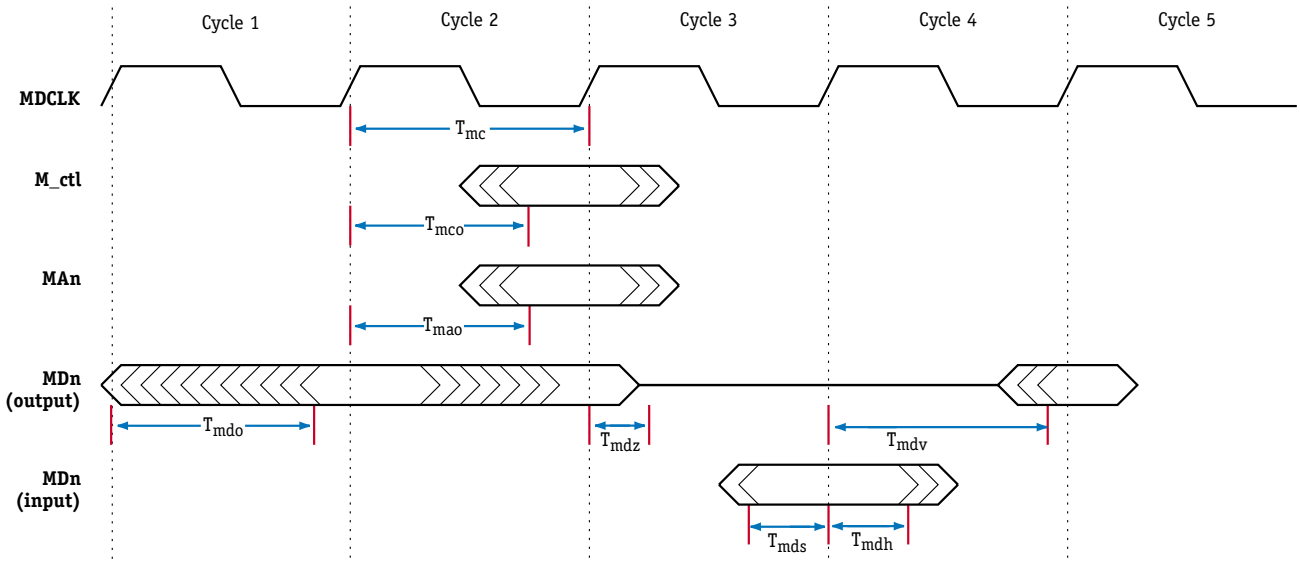


Table 49 BMU Timing Description

Symbol	Parameter	Min	Typ	Max	Unit
Tmc	BMU Cycle Time	8.0			ns
Tmco	BMU Ctrl Output	1.2		3.7	ns
Tmao	BMU Addr Output	1.2		3.8	ns
Tmds	BMU Data Setup	0.5			ns
Tmdh	BMU Data Hold	1.0			ns
Tmdo	BMU Data Output	1.2		4.0	ns
Tmdz	BMU Data Clk to Tri*	1.8		4.0	ns
Tmdv	BMU Data Clk to Driven*	1.4		4.0	ns

* Not fully tested, values based on design/characterization.

Table 50 Signal Groups in BMU Timing Diagrams

Signal Group	Included Signals
Control (M_ctl)	MBA0, MBA1, MCASX, MRASX, MWEX, MCSX, MDQM
Address (MAn)	MA0 - MA11
Data (MDn)	MD0 - MD129, MDECC0 - MDECC8

TLU Timing Specifications

The TLU timing specifications are shown in Figure 24 and described in Table 51.

Figure 24 TLU Timing Diagram

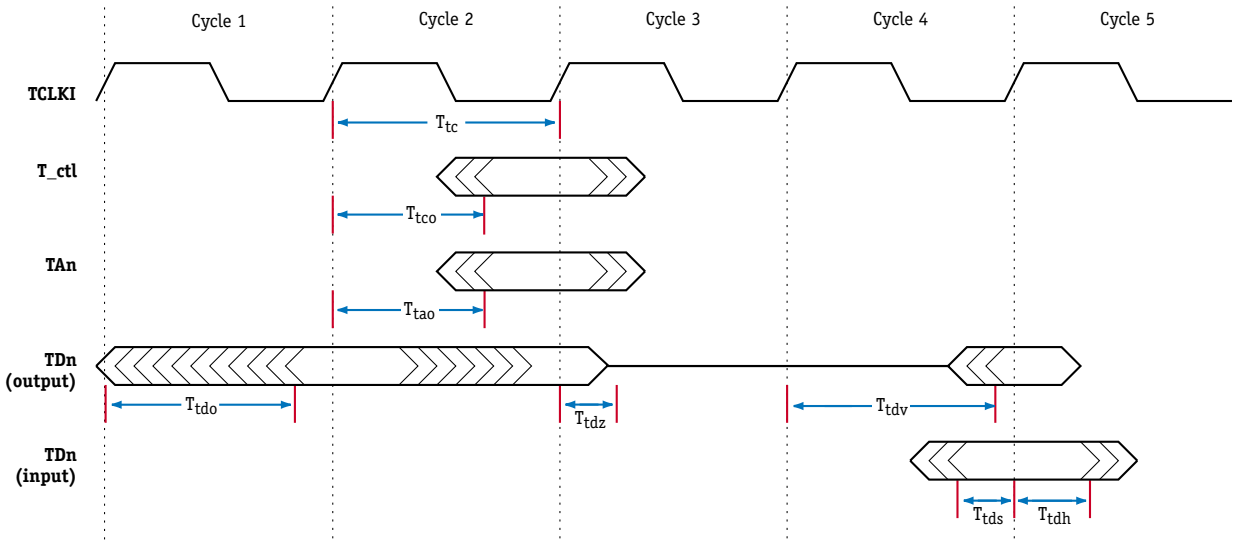


Table 51 TLU Timing Description

Symbol	Parameter	Min	Typ	Max	Unit
Ttc	TLU Cycle Time	7.5			ns
Ttco	TLU Ctrl Output	1.2		3.4	ns
Ttao	TLU Addr Output	1.2		3.4	ns
Ttds	TLU Data Setup	0.5			ns
Ttdh	TLU Data Hold	1.0			ns
Ttdo	TLU Data Output	1.2		3.5	ns
Ttdz	TLU Data Clk to Tri*	2.0		3.5	ns
Ttdv	TLU Data Clk to Driven*	1.5		3.5	ns

* Not fully tested, values based on design/characterization.

Table 52 Signal Groups in TLU Timing Diagrams

Signal Group	Included Signals
Control (T_ctl)	TA18X - TA21X, TCE0X - TCE3X, TWE0X - TWE3X
Address (TAn)	TA0 - TA21
Data (TDn)	TD0 - TD63

QMU Timing Specifications

The QMU timing specifications are shown in Figure 25 and described in Table 53.

Figure 25 QMU Timing Diagram

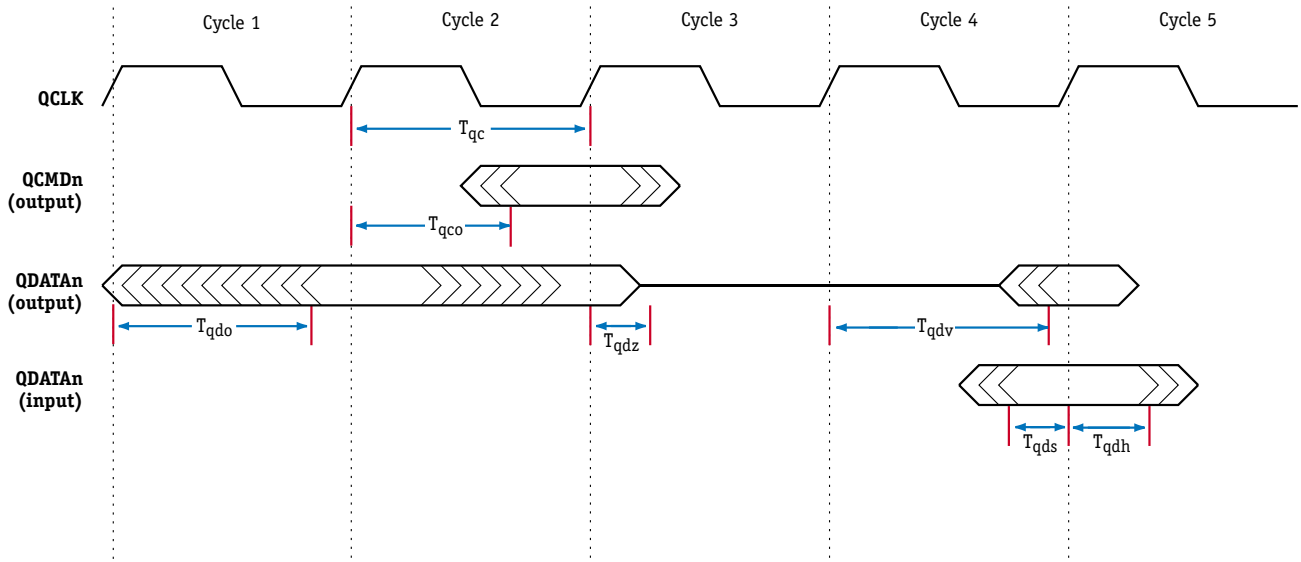


Table 53 QMU Timing Description

Symbol	Parameter	Min	Typ	Max	Unit	Comment
Tqc	QMU Cycle Time	2 x Tsc 4 x Tsc			ns ns	1X Clock Mode 2X Clock Mode
Tqco	QMU Ctrl Output	1.5		1/2 Tsc + 1.0 Tsc + 1.0	ns	1X Clock Mode 2X Clock Mode
Tqds	QMU Data Setup	3.1			ns	
Tqdh	QMU Data Hold	1.3		3.5	ns	
Tqdo	QMU Data Output	1.5		1/2 Tsc + 1.0 Tsc + 1.0	ns	1X Clock Mode 2X Clock Mode

Table 53 QMU Timing Description (continued) (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comment
Tqdz	QMU Data Clk to Tri*	1.1		5.5	ns	
Tqdv	QMU Data Clk to Driven*	0.6		5.5	ns	

* Not fully tested, values based on design/characterization.

Table 54 Signal Groups in QMU Timing Diagrams

Signal Group	Included Signals
QCMDn	QCMD0 - QCMD15, QSFLOW, QXCTRL0, QXCTRL1, QXRQST
QDATAn	QDATA0 - QDATA31, QDPAR

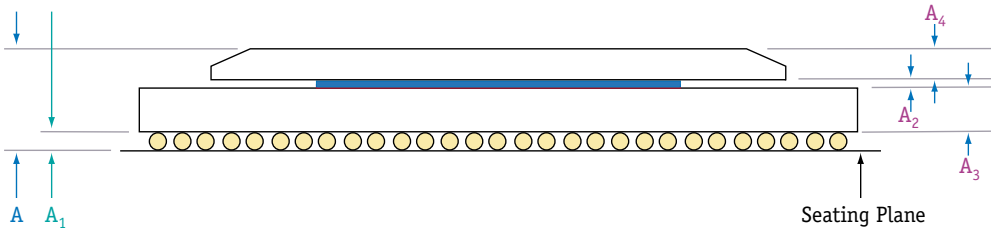
Chapter 4

Mechanical Specifications

Package Views

The C-5 network processor is an 838 pin (29 pins x 29 pins) Ball Grid Array (BGA) package as shown in the following illustrations. Table 55 defines the package measurements.

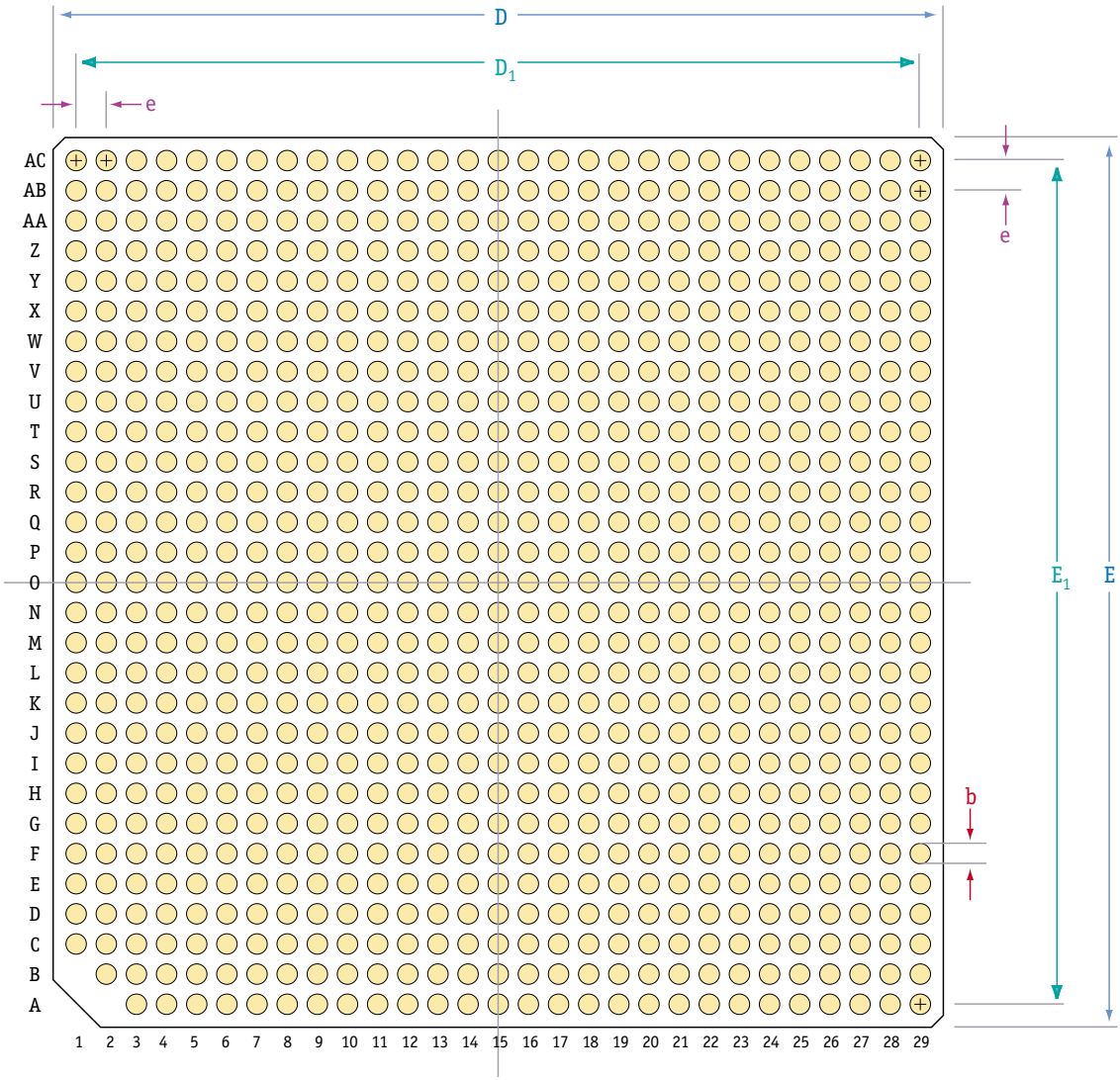
Figure 26 C-5 Network Processor BGA Package Side View



HiTCE: Green ceramic is thermally matched to FR4 circuit board.

The aluminum lid is electrically connected to the grounded substrate of the C-5 NP. Neither the lid nor any heat sink connected to the lid should be part of a current-carrying path. It is acceptable, however, to connect the lid or heatsink to ground if necessary (through the standoff screws for the heat sink).

Figure 27 C-5 Network Processor BGA Package (Bottom View)



Package Measurements

Table 55 defines the C-5 NP package measurements, providing nominal, minimum, and maximum sizes where appropriate.

Table 55 Package Measurements (Reference Figure 26 and Figure 27 for Symbols)

Symbol	Definition	Nom. (mm)	Min. (mm)	Max. (mm)
A	Overall	5.63	5.31	5.95
A_1	Ball height	0.89		
A_2	C4 and Die	0.88		
A_3	Body thickness	2.26	2.07	2.53
A_4	Lid thickness	1.6		
D	Body size	37.50		
D_1	Ball footprint (X)	35.56		
E	Body size	37.50		
E_1	Ball footprint (Y)	35.56		
e	Ball pitch	1.27		
b	Ball diameter	0.89		

Marking Codes

Table 56 explains the marking on the C-5 NP.

Table 56 C-5 Network Processor Marking Codes

Marking (Explanation of Codes)	
Top	Logo/Part#/Country of Origin/Date Code
Bottom	N/A
Pin 1 Marking	Chamfered Corner

Reflow

Typical Reflow Profile for the C-5 Switch Module

1 Follow the guidelines recommended by your solder paste supplier.

Flux requirements must be met for best solderability.

2 The temperature profile should be carefully characterized to ensure uniform temperature across the board and package.

Solder ball voiding may be affected by ramp rates and dwell times below and above liquidus.

3 A nitrogen atmosphere is not required, but will make the process more robust. It can make a difference for marginally solderable PC board pads.

4 Full convection forced air furnaces work best, but IR, Convection/IR, or vapor phase can be used.

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