100-Pin TQFP
Commercial Temp
Industrial Temp

1M x 18, 512K x 32, 512K x 36 16Mb Sync Burst SRAMs

225 MHz–133 MHz
2.5 V V_{DD}
2.5 V or 3.3 V I/O

Features

- $\overline{FT}$ pin for user-configurable flow through or pipeline operation
- Single Cycle Deselect (SCD) operation
- 2.5 V +10%/–5% core power supply
- 2.5 V or 3.3 V I/O supply
- $\overline{LBO}$ pin for Linear or Interleaved Burst mode
- Internal input resistors on mode pins allow floating mode pins
- Default to Interleaved Pipeline mode
- Byte Write ($\overline{BW}$) and/or Global Write ($\overline{GW}$) operation
- Internal self-timed write cycle
- Automatic power-down for portable applications
- JEDEC-standard 100-lead TQFP package

		-225	-200	-180	-166	-150	-133	Unit
Pipeline 3-1-1-1	t_{KQ}	2.5	3.0	3.2	3.5	3.8	4.0	ns
	tCycle	4.4	5.0	5.5	6.0	6.6	7.5	ns
	Curr (x18)	350	315	290	270	250	230	mA
	Curr (x32)	410	370	340	315	290	260	mA
	Curr (x36)	410	370	340	315	290	260	mA
Flow Through 2-1-1-1	t_{KQ}	7.0	7.5	8	8.5	10	11	ns
	tCycle	8.5	10	10	10	10	15	ns
	Curr (x18)	205	185	185	185	185	140	mA
	Curr (x32)	240	210	210	210	210	160	mA
	Curr (x36)	240	210	210	210	210	160	mA

Functional Description

Applications

The GS816018/32/36T is a 18,874,368-bit (16,777,216-bit for x32 version) high performance synchronous SRAM with a 2-bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPUs, the device now finds application in synchronous SRAM application,s ranging from DSP main store to networking chip set support.

Controls

Addresses, data I/Os, chip enables ($\overline{E1}$, E2, $\overline{E3}$), address burst control inputs ($\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$), and write control inputs ($\overline{Bx}$, $\overline{BW}$, $\overline{GW}$) are synchronous and are controlled by a positive-edge-triggered clock input (CK). Output enable ($\overline{G}$) and power down control (ZZ) are asynchronous inputs. Burst cycles can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ inputs. In Burst mode, subsequent burst addresses are generated internally and are controlled by $\overline{ADV}$. The burst address counter may be configured to count in either linear or interleave order with the Linear Burst Order ($\overline{LBO}$) input. The Burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

Flow Through/Pipeline Reads

The function of the Data Output register can be controlled by the user via the $\overline{FT}$ mode pin (Pin 14). Holding the $\overline{FT}$ mode pin low places the RAM in Flow Through mode, causing output data to bypass the Data Output Register. Holding $\overline{FT}$ high places the RAM in Pipeline mode, activating the rising-edge-triggered Data Output Register.

SCD Pipelined Reads

The GS816018/32/36T is a SCD (Single Cycle Deselect) pipelined synchronous SRAM. DCD (Dual Cycle Deselect) versions are also available. SCD SRAMs pipeline deselect commands one stage less than read commands. SCD RAMs begin turning off their outputs immediately after the deselect command has been captured in the input registers.

Byte Write and Global Write

Byte write operation is performed by using Byte Write enable ($\overline{BW}$) input combined with one or more individual byte write signals ($\overline{Bx}$). In addition, Global Write ($\overline{GW}$) is available for writing all bytes at one time, regardless of the Byte Write control inputs.

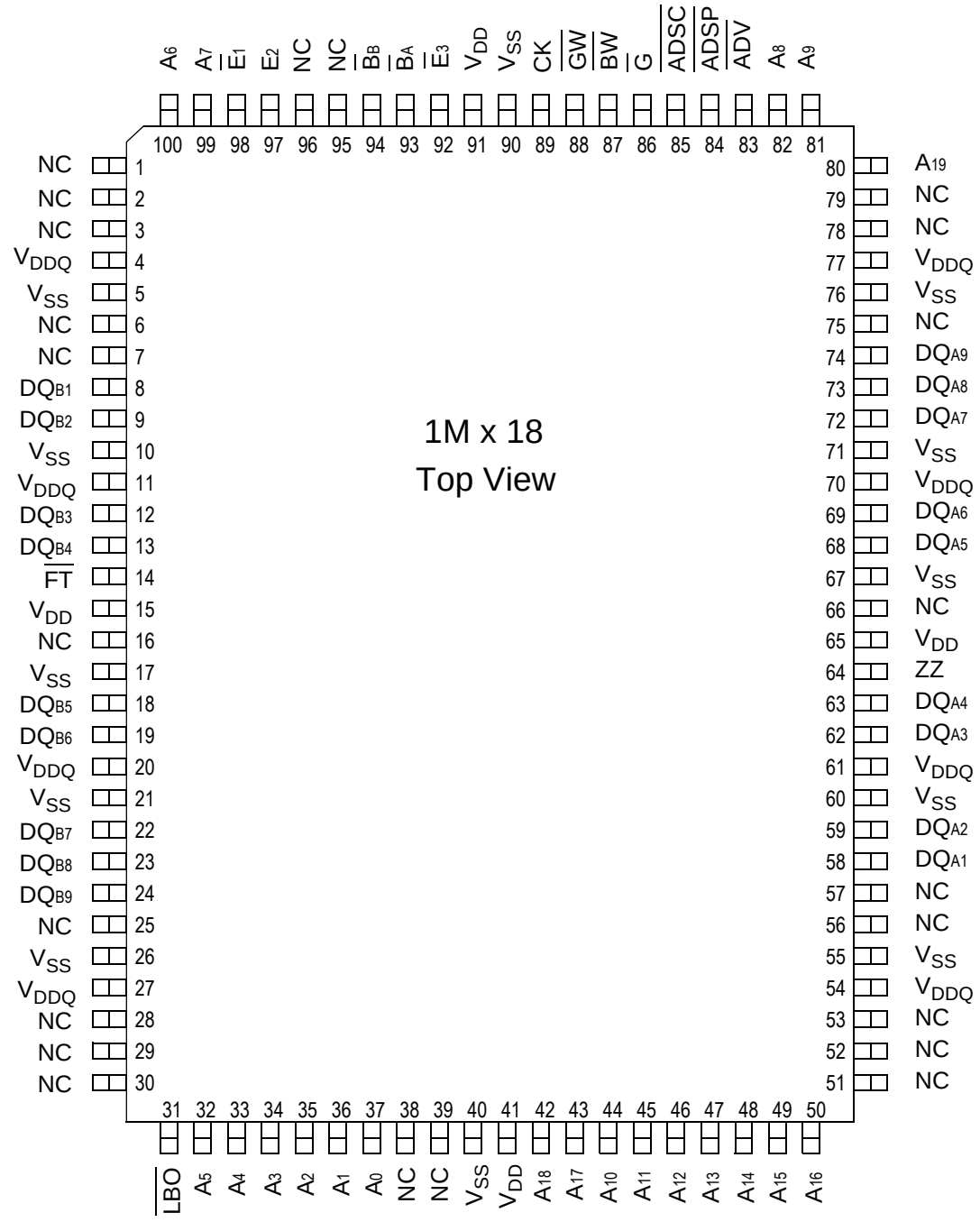
Sleep Mode

Low power (Sleep mode) is attained through the assertion (High) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Sleep mode.

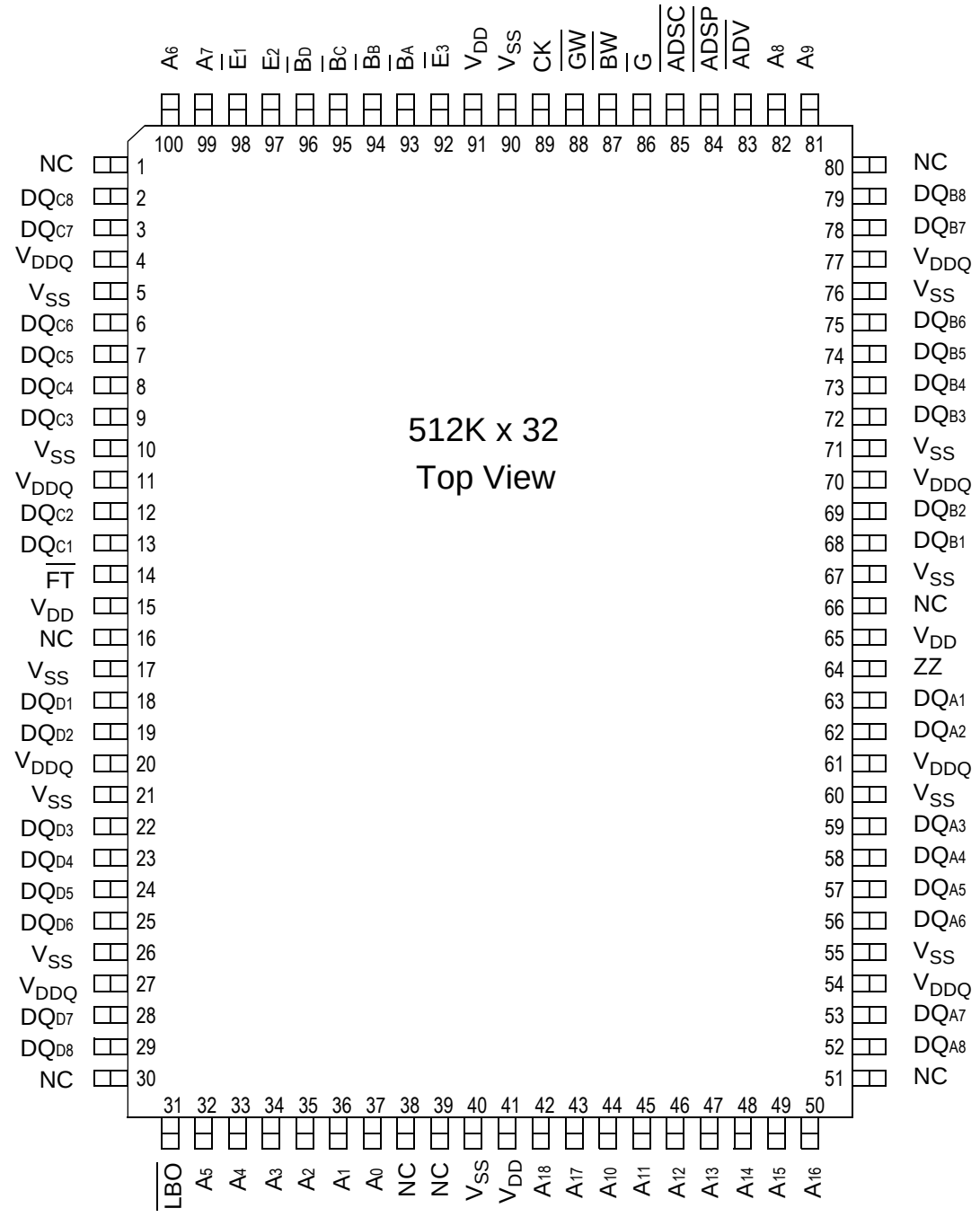
Core and Interface Voltages

The GS816018/32/36T operates on a 2.5 V power supply. All input are 3.3 V- and 2.5 V-compatible. Separate output power (V_{DDQ}) pins are used to decouple output noise from the internal circuits and are 3.3 V- and 2.5 V-compatible.

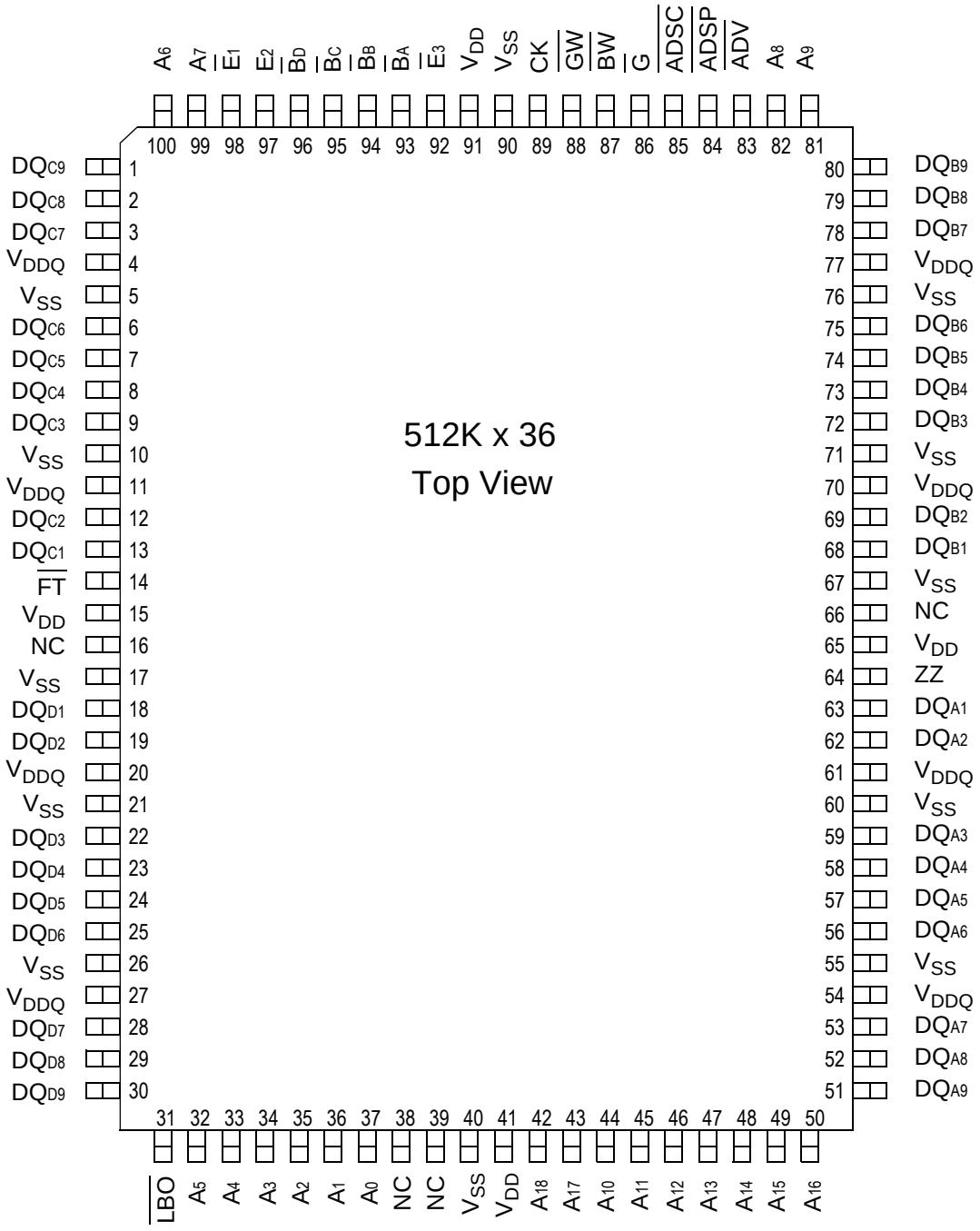
GS816018 100-Pin TQFP Pinout



GS816032 100-Pin TQFP Pinout



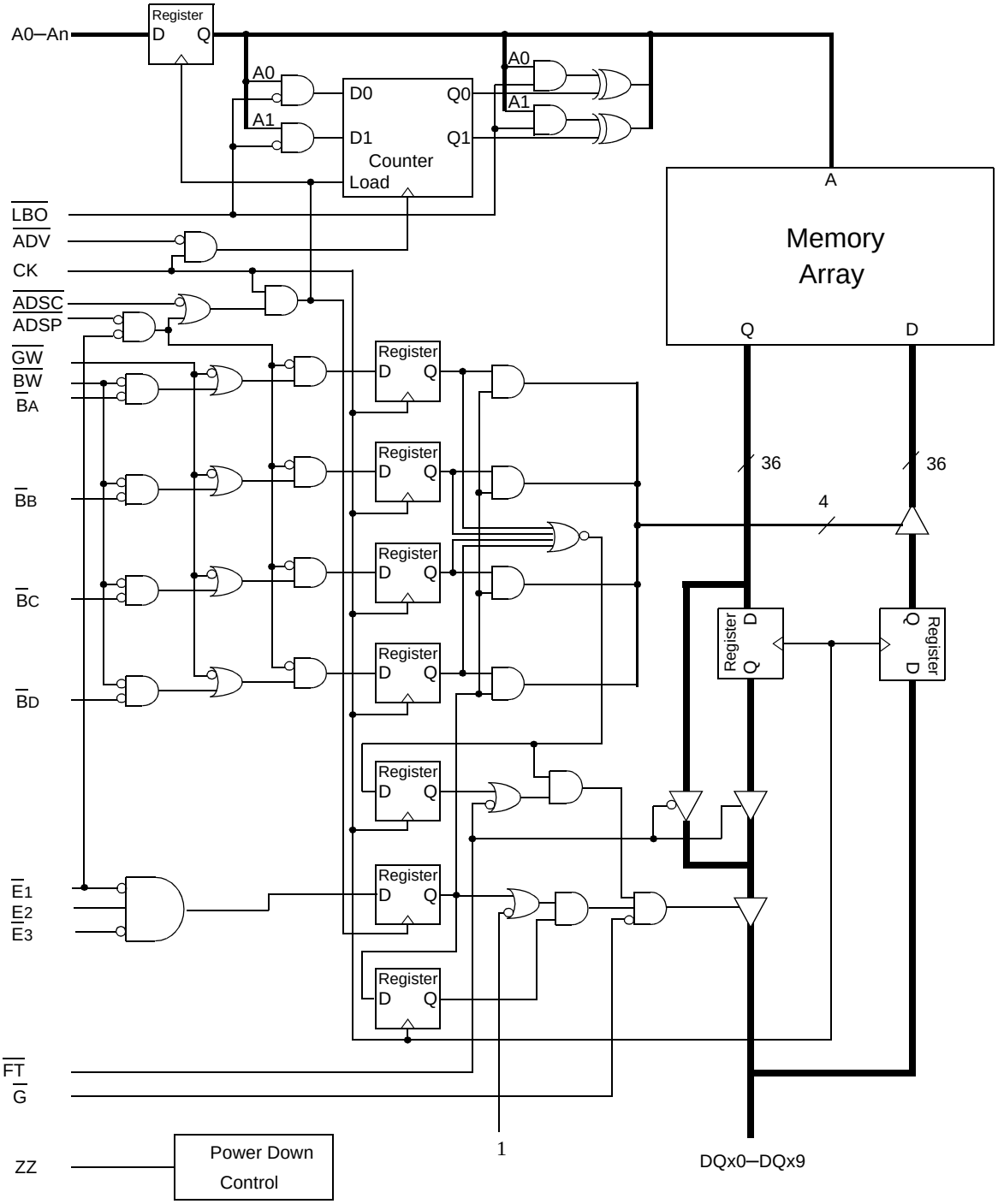
GS816036 100-Pin TQFP Pinout



TQFP Pin Description

Pin Location	Symbol	Type	Description
37, 36	A_0, A_1	I	Address field LSBs and Address Counter preset Inputs
35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50, 43, 42,	A_2–A_{18}	I	Address Inputs
80	A_{19}	I	Address Inputs (x18 versions)
63, 62, 59, 58, 57, 53, 52 68, 69, 72, 73, 74, 75, 78, 79 13, 12, 9, 8, 7, 6, 3, 2 18, 19, 22, 23, 24, 25, 28, 29	DQ_{A1}–DQ_{A8} DQ_{B1}–DQ_{B8} DQ_{C1}–DQ_{C8} DQ_{D1}–DQ_{D8}	I/O	Data Input and Output pins (x32, x36 Version)
51, 80, 1, 30	DQ_{A9}, DQ_{B9}, DQ_{C9}, DQ_{D9}	I/O	Data Input and Output pins (x36 Version)
51, 80, 1, 30	NC		No Connect (x32 Version)
58, 59, 62, 63, 68, 69, 72, 73, 74 8, 9, 12, 13, 18, 19, 22, 23, 24	DQ_{A1}–DQ_{A9} DQ_{B1}–DQ_{B9}	I/O	Data Input and Output pins (x18 Version)
51, 52, 53, 56, 57 75, 78, 79, 1, 2, 3, 6, 7, 25, 28, 29, 30	NC	—	No Connect (x18 Version)
87	$\overline{BW}$	I	Byte Write—Writes all enabled bytes; active low
93, 94	$\overline{B}_A$, $\overline{B}_B$	I	Byte Write Enable for DQ_A, DQ_B Data I/Os; active low
95, 96	$\overline{B}_C$, $\overline{B}_D$	I	Byte Write Enable for DQ_C, DQ_D Data I/Os; active low (x32, x36 Version)
95, 96	NC	—	No Connect (x18 Version)
89	CK	I	Clock Input Signal; active high
88	$\overline{GW}$	I	Global Write Enable—Writes all bytes; active low
98, 92	$\overline{E}_1$, $\overline{E}_3$	I	Chip Enable; active low
97	E_2	I	Chip Enable; active high
86	$\overline{G}$	I	Output Enable; active low
83	$\overline{ADV}$	I	Burst address counter advance enable; active low
84, 85	$\overline{ADSP}$, $\overline{ADSC}$	I	Address Strobe (Processor, Cache Controller); active low
64	ZZ	I	Sleep Mode control; active high
14	$\overline{FT}$	I	Flow Through or Pipeline mode; active low
31	$\overline{LBO}$	I	Linear Burst Order mode; active low
15, 41, 65, 91	V_{DD}	I	Core power supply
5,10,17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	I	I/O and Core Ground
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	I	Output driver power supply
16, 38, 39, 66	NC	—	No Connect

GS816018/32/36 Block Diagram



Note: Only x36 version shown for simplicity.

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{LBO}$	L	Linear Burst
		H	Interleaved Burst
Output Register Control	$\overline{FT}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$

Note:
There is a pull-up device on the and $\overline{FT}$ pin and a pull-down device on the ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above tables.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note: The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note: The burst counter wraps to initial state on the 5th clock.

BPR 1999.05.18

Byte Write Truth Table

Function	$\overline{GW}$	$\overline{BW}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$	Notes
Read	H	H	X	X	X	X	1
Read	H	L	H	H	H	H	1
Write byte a	H	L	L	H	H	H	2, 3
Write byte b	H	L	H	L	H	H	2, 3
Write byte c	H	L	H	H	L	H	2, 3, 4
Write byte d	H	L	H	H	H	L	2, 3, 4
Write all bytes	H	L	L	L	L	L	2, 3, 4
Write all bytes	L	X	X	X	X	X	

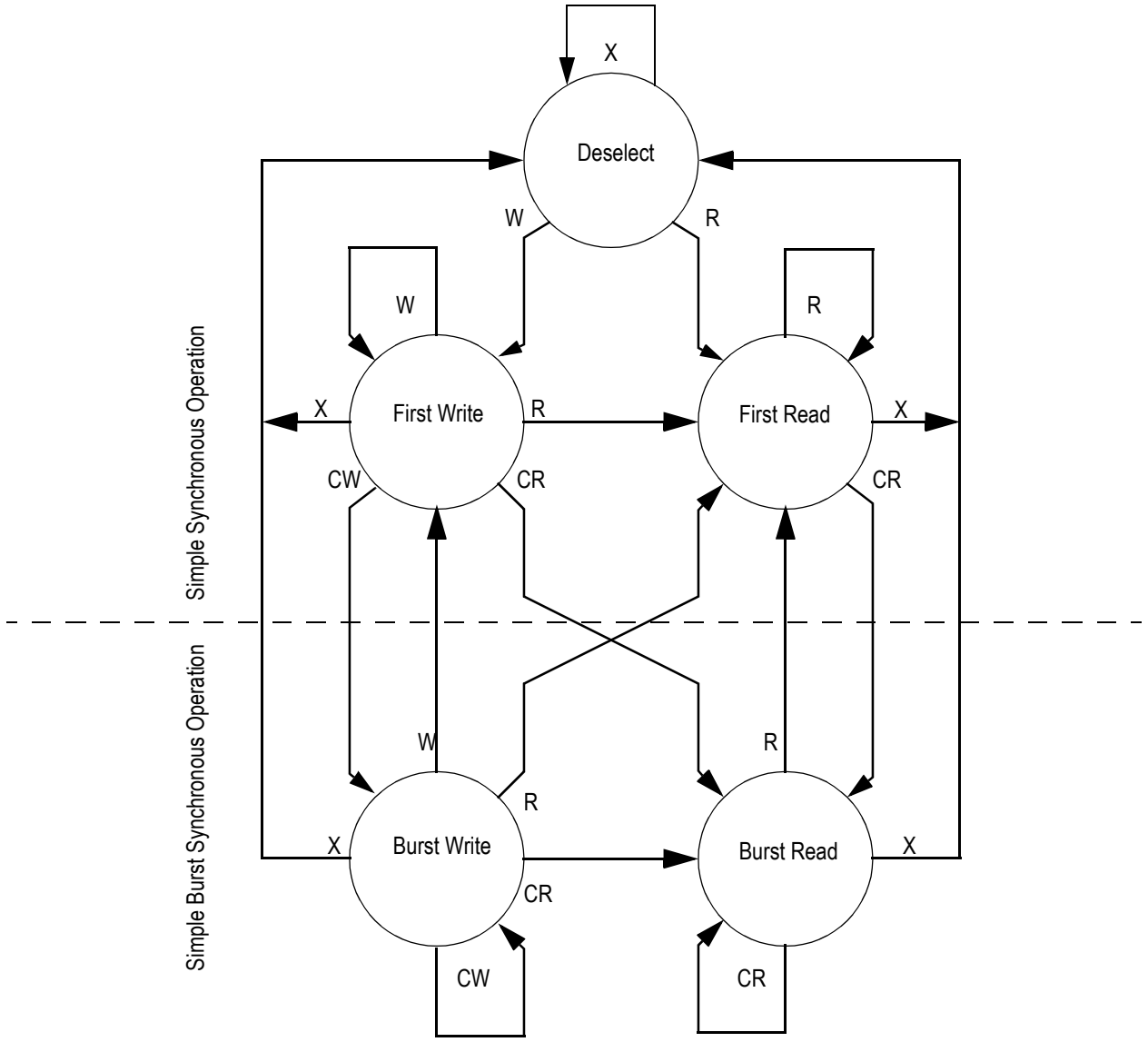
Notes:
1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs.
2. Byte Write Enable inputs $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$ and/or $\overline{B}_D$ may be used in any combination with $\overline{BW}$ to write single or multiple bytes.
3. All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
4. Bytes C and D are only available on the x32 and x36 versions.

Synchronous Truth Table

Operation	Address Used	State Diagram Key[5]	$\overline{E}_1$	E^2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{W}^3$	DQ[4]
Deselect Cycle, Power Down	**None**	**X**	**H**	**X**	**X**	**L**	**X**	**X**	**High-Z**
Deselect Cycle, Power Down	None	X	L	F	L	X	X	X	High-Z
Deselect Cycle, Power Down	**None**	**X**	**L**	**F**	**H**	**L**	**X**	**X**	**High-Z**
Read Cycle, Begin Burst	External	R	L	T	L	X	X	X	Q
Read Cycle, Begin Burst	**External**	**R**	**L**	**T**	**H**	**L**	**X**	**F**	**Q**
Write Cycle, Begin Burst	**External**	**W**	**L**	**T**	**H**	**L**	**X**	**T**	**D**
Read Cycle, Continue Burst	*Next*	*CR*	*X*	*X*	*H*	*H*	*L*	*F*	*Q*
Read Cycle, Continue Burst	Next	CR	H	X	X	H	L	F	Q
Write Cycle, Continue Burst	*Next*	*CW*	*X*	*X*	*H*	*H*	*L*	*T*	*D*
Write Cycle, Continue Burst	Next	CW	H	X	X	H	L	T	D
Read Cycle, Suspend Burst	Current		X	X	H	H	H	F	Q
Read Cycle, Suspend Burst	Current		H	X	X	H	H	F	Q
Write Cycle, Suspend Burst	Current		X	X	H	H	H	T	D
Write Cycle, Suspend Burst	Current		H	X	X	H	H	T	D

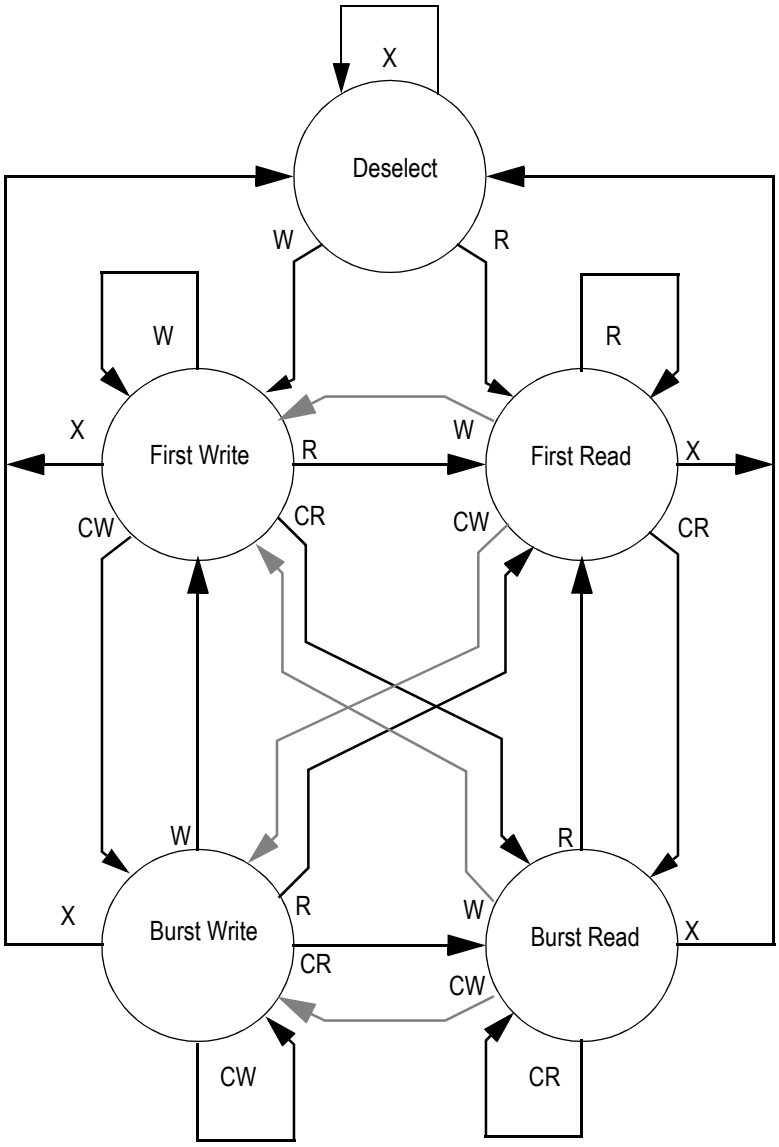
Notes:
1. X = Don t Care, H = High, L = Low
2. E = T (True) if E_2 = 1 and $\overline{E}_3$ = 0; E = F (False) if E_2 = 0 or $\overline{E}_3$ = 1
3. $\overline{W}$ = T (True) and F (False) is defined in the Byte Write Truth Table preceding.
4. $\overline{G}$ is an asynchronous input. $\overline{G}$ can be driven high at any time to disable active output drivers. $\overline{G}$ low can only enable active drivers (shown as Q in the Truth Table above).
5. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
6. Tying ADSP high and ADSC low allows simple non-burst synchronous operations. See **BOLD** items above.
7. Tying ADSP high and ADV low while using ADSC to load new addresses allows simple burst operations. See *ITALIC* items above.

Simplified State Diagram



Notes:
1. The diagram shows only supported (tested) synchronous state transitions. The diagram presumes $\overline{G}$ is tied low.
2. The upper portion of the diagram assumes active use of only the Enable ($\overline{E1}$, E2, and $\overline{E3}$) and Write ($\overline{BA}$, $\overline{BB}$, $\overline{BC}$, $\overline{BD}$, $\overline{BW}$, and $\overline{GW}$) control inputs, and that $\overline{ADSP}$ is tied high and $\overline{ADSC}$ is tied low.
3. The upper and lower portions of the diagram together assume active use of only the Enable, Write, and $\overline{ADSC}$ control inputs, and assumes $\overline{ADSP}$ is tied high and $\overline{ADV}$ is tied low.

Simplified State Diagram with $\overline{G}$



Notes:
1. The diagram shows supported (tested) synchronous state transitions plus supported transitions that depend upon the use of $\overline{G}$.
2. Use of Dummy Reads (Read Cycles with $\overline{G}$ High) may be used to make the transition from Read cycles to Write cycles without passing through a Deselect cycle. Dummy Read cycles increment the address counter just like normal read cycles.
3. Transitions shown in gray tone assume $\overline{G}$ has been pulsed high long enough to turn the RAM s drivers off and for incoming data to meet Data Input Set Up Time.

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 3.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to 3.6	V
V_{CK}	Voltage on Clock Input Pin	–0.5 to 6	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ}+0.5 (≤ 3.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to 3.6	V
I_{IN}	Input Current on Any Pin	+/–20	mA
I_{OUT}	Output Current on Any I/O Pin	+/–20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	–55 to 125	°C
T_{BIAS}	Temperature Under Bias	–55 to 125	°C

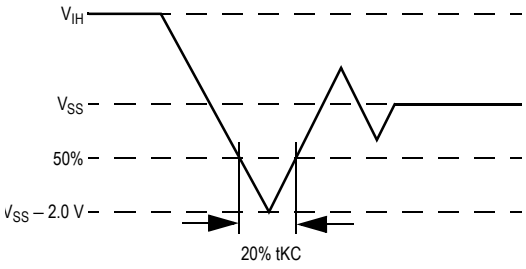
Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Recommended Operating Conditions

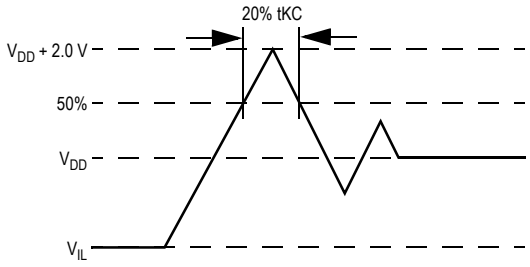
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	V_{DD}	2.375	2.5	2.7	V	
I/O Supply Voltage	V_{DDQ}	2.375	2.5	3.6	V	
Input High Voltage	V_{IH}	0.7 * V_{DD}	—	3.6	V	1
Input Low Voltage	V_{IL}	–0.3	—	0.3 * VDD	V	1
Ambient Temperature (Commercial Range Versions)	T_A	0	25	70	°C	2
Ambient Temperature (Industrial Range Versions)	T_A	–40	25	85	°C	2

Note:
1. The part number of Industrial Temperature Range versions end the character I . Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be –2 V > Vi < V_{DD}+2 V with a pulse width not to exceed 20% tKC.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 2.5 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0 V	6	7	pF

Note: These parameters are sample tested.

Package Thermal Characteristics

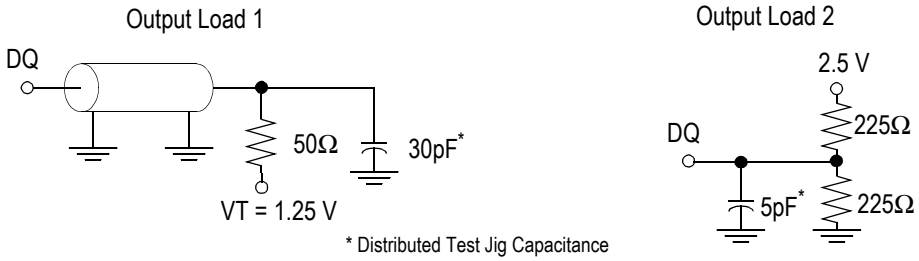
Rating	Layer Board	Symbol	Max	Unit	Notes
Junction to Ambient (at 200 lfm)	single	$R_{\Theta JA}$	40	°C/W	1,2
Junction to Ambient (at 200 lfm)	four	$R_{\Theta JA}$	24	°C/W	1,2
Junction to Case (TOP)	—	$R_{\Theta JC}$	9	°C/W	3

Notes:
1. Junction temperature is a function of SRAM power dissipation, package thermal resistance, mounting board temperature, ambient. Temperature air flow, board density, and PCB thermal resistance.
2. SCMI G-38-87
3. Average thermal resistance between die and top surface, MIL SPEC-883, Method 1012.1

AC Test Conditions

Parameter	Conditions
Input high level	2.3 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	1.25 V
Output reference level	1.25 V
Output load	**Fig. 1& 2**

Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Output Load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}
4. Device is deselected as defined by the Truth Table.



DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–1 uA	1 uA
ZZ Input Current	I_{INZZ}	$V_{DD} \geq V_{IN} \geq V_{IH}$ 0 V ≤ V_{IN} ≤ V_{IH}	–1 uA –1 uA	1 uA 300 uA
Mode Pin Input Current	I_{INM}	$V_{DD} \geq V_{IN} \geq V_{IL}$ 0 V ≤ V_{IN} ≤ V_{IL}	–300 uA –1 uA	1 uA 1 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH}	I_{OH} = –8 mA, V_{DDQ} = 2.375 V	1.7 V	—
Output High Voltage	V_{OH}	I_{OH} = –8 mA, V_{DDQ} = 3.135 V	2.4 V	—
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	0.4 V

Operating Currents

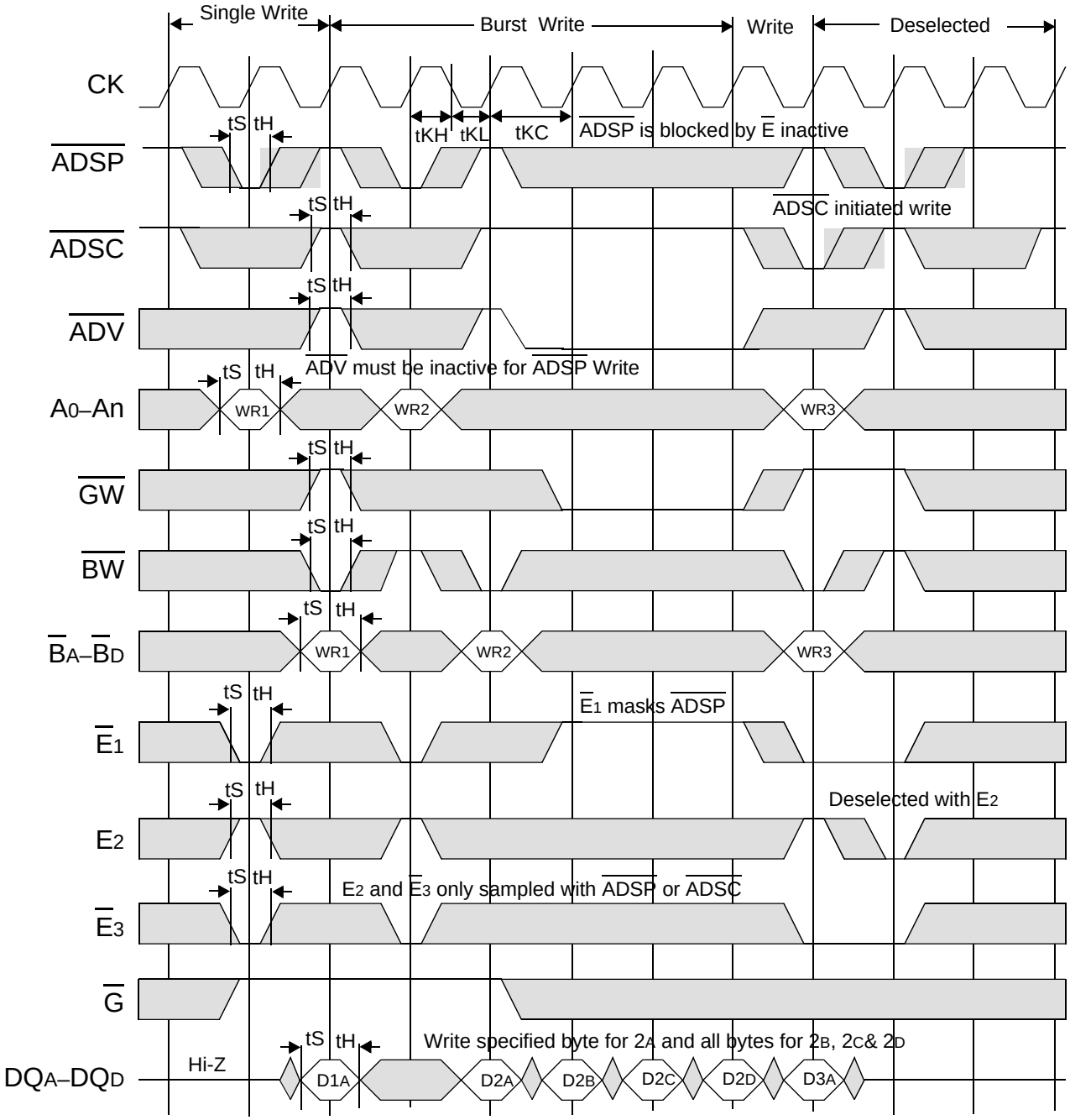
Parameter	Test Conditions		Mode	Symbol	-225		-200		-180		-166		-150		-133		Unit
					0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	
Operating Current	Device Selected; All other inputs ≥V_{IH} or ≤ V_{IL} Output open	(x36)	Pipeline	I_{DD}	335	345	303	313	278	288	260	270	240	250	218	228	mA
				I_{DDQ}	74	84	66	76	59	69	55	65	50	60	44	54	
			Flow Through	I_{DD}	199	209	177	187	177	187	177	187	177	187	134	144	mA
				I_{DDQ}	39	49	33	43	33	43	33	43	33	43	22	32	
		(x18)	Pipeline	I_{DD}	310	320	281	291	258	268	242	252	223	233	204	214	mA
				I_{DDQ}	37	47	33	43	30	40	27	37	25	35	22	32	
			Flow Through	I_{DD}	186	196	166	176	166	176	166	176	166	176	127	137	mA
				I_{DDQ}	19	29	17	27	17	27	17	27	17	27	11	21	
Standby Current	ZZ ≥ V_{DD} – 0.2 V	—	Pipeline	I_{SB}	10	20	10	20	10	20	10	20	10	20	10	20	mA
			Flow Through	I_{SB}	10	20	10	20	10	20	10	20	10	20	10	20	mA
Deselect Current	Device Deselected; All other inputs ≥ V_{IH} or ≤ V_{IL}	—	Pipeline	I_{DD}	80	85	75	80	70	75	64	70	60	65	50	55	mA
			Flow Through	I_{DD}	60	65	50	55	50	55	50	55	50	55	45	50	mA

AC Electrical Characteristics

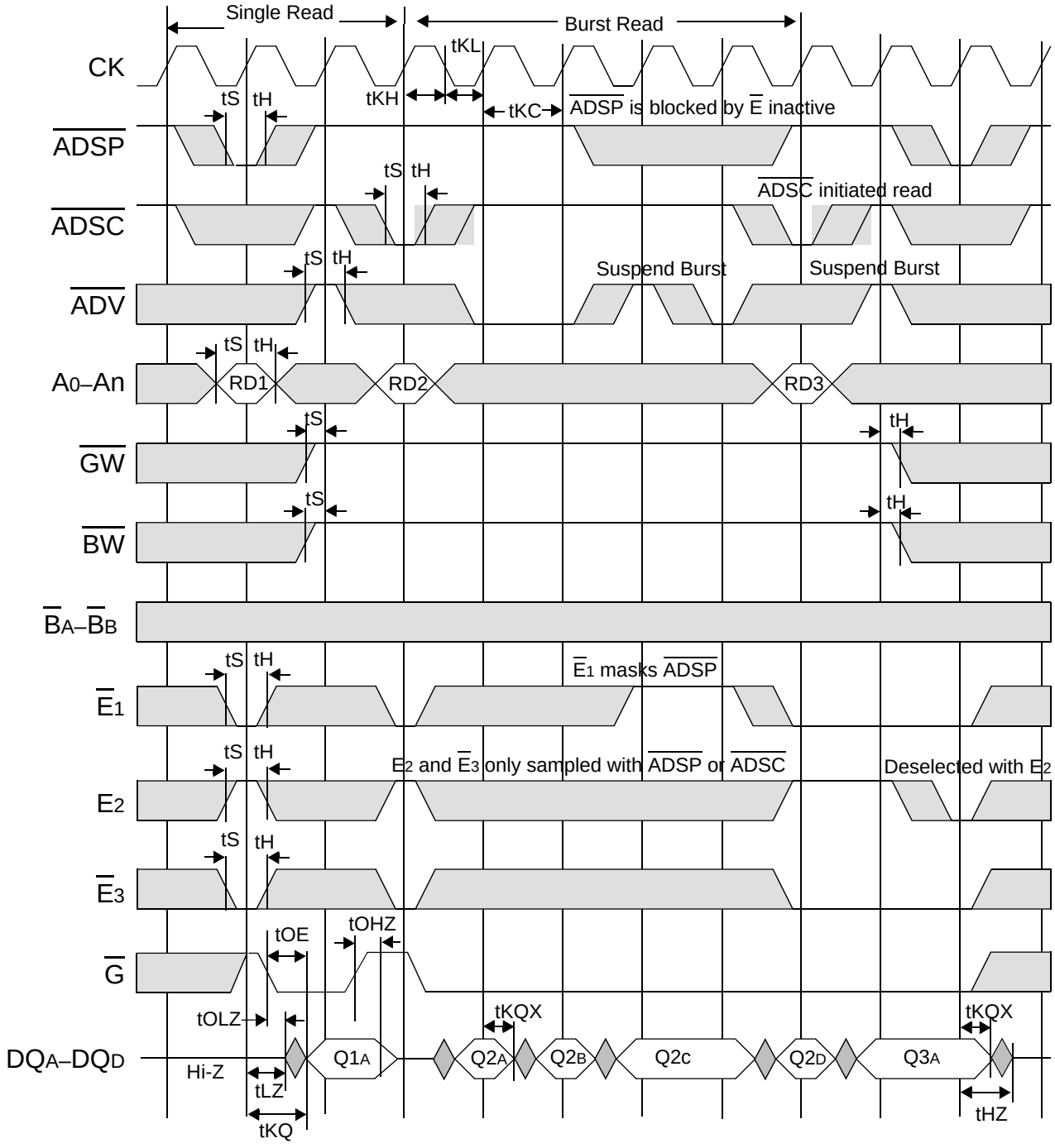
	Parameter	Symbol	-225		-200		-180		-166		-150		-133		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	tKC	4.4	—	5.0	—	5.5	—	6.0	—	6.7	—	7.5	—	ns
	Clock to Output Valid	tKQ	—	2.5	—	3.0	—	3.2	—	3.5	—	3.8	—	4.0	ns
	Clock to Output Invalid	tKQX	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	tLZ[1]	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
Flow Through	Clock Cycle Time	tKC	8.5	—	10.0	—	10.0	—	10.0	—	10.0	—	15.0	—	ns
	Clock to Output Valid	tKQ	—	7.0	—	7.5	—	8.0	—	8.5	—	10.0	—	11.0	ns
	Clock to Output Invalid	tKQX	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock to Output in Low-Z	tLZ[1]	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock HIGH Time	tKH	1.3	—	1.3	—	1.3	—	1.3	—	1.5	—	1.7	—	ns
	Clock LOW Time	tKL	1.5	—	1.5	—	1.5	—	1.5	—	1.7	—	2	—	ns
	Clock to Output in High-Z	tHZ[1]	1.5	2.5	1.5	3.0	1.5	3.2	1.5	3.5	1.5	3.8	1.5	4.0	ns
	$\overline{G}$ to Output Valid	tOE	—	2.5	—	3.2	—	3.2	—	3.5	—	3.8	—	4.0	ns
	$\overline{G}$ to output in Low-Z	tOLZ[1]	0	—	0	—	0	—	0	—	0	—	0	—	ns
	$\overline{G}$ to output in High-Z	tOHZ[1]	—	2.5	—	3.0	—	3.2	—	3.5	—	3.8	—	4.0	ns
	Setup time	tS	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Hold time	tH	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
	ZZ setup time	tZZS[2]	5	—	5	—	5	—	5	—	5	—	5	—	ns
	ZZ hold time	tZZH[2]	1	—	1	—	1	—	1	—	1	—	1	—	ns
	ZZ recovery	tZZR	100	—	100	—	100	—	100	—	100	—	100	—	ns

Notes:
1. These parameters are sampled and are not 100% tested.
2. ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

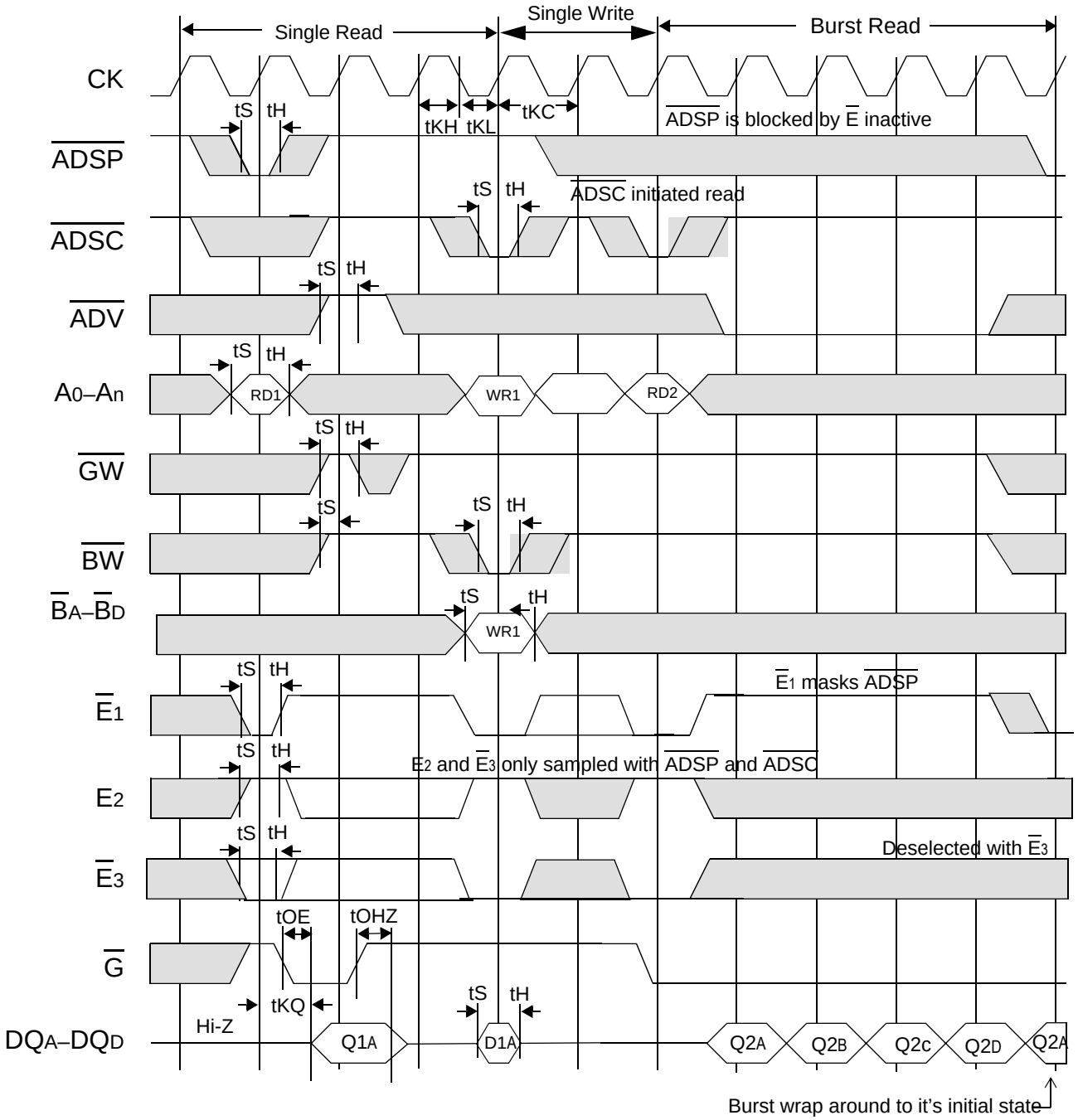
Write Cycle Timing



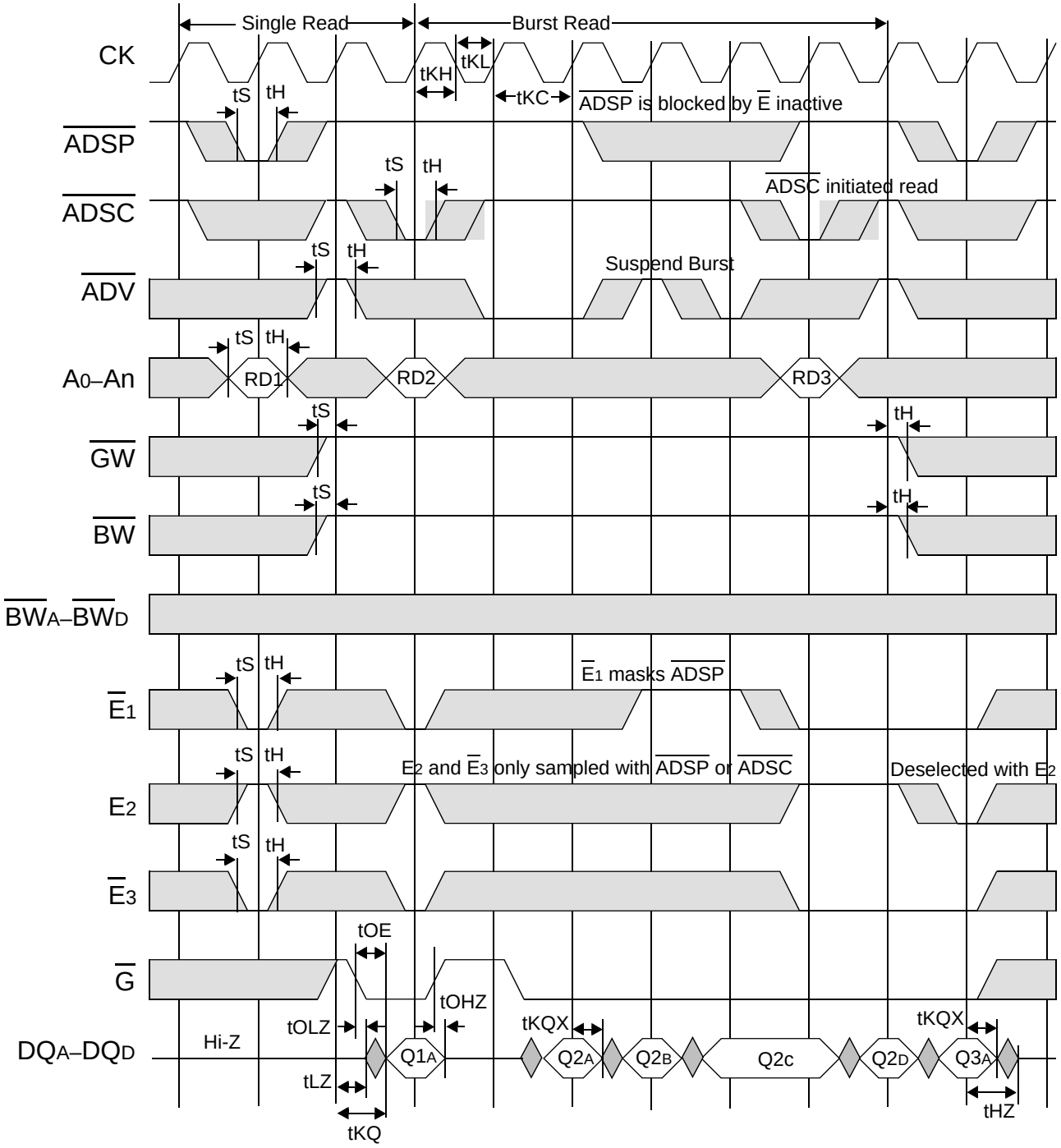
Flow Through Read Cycle Timing



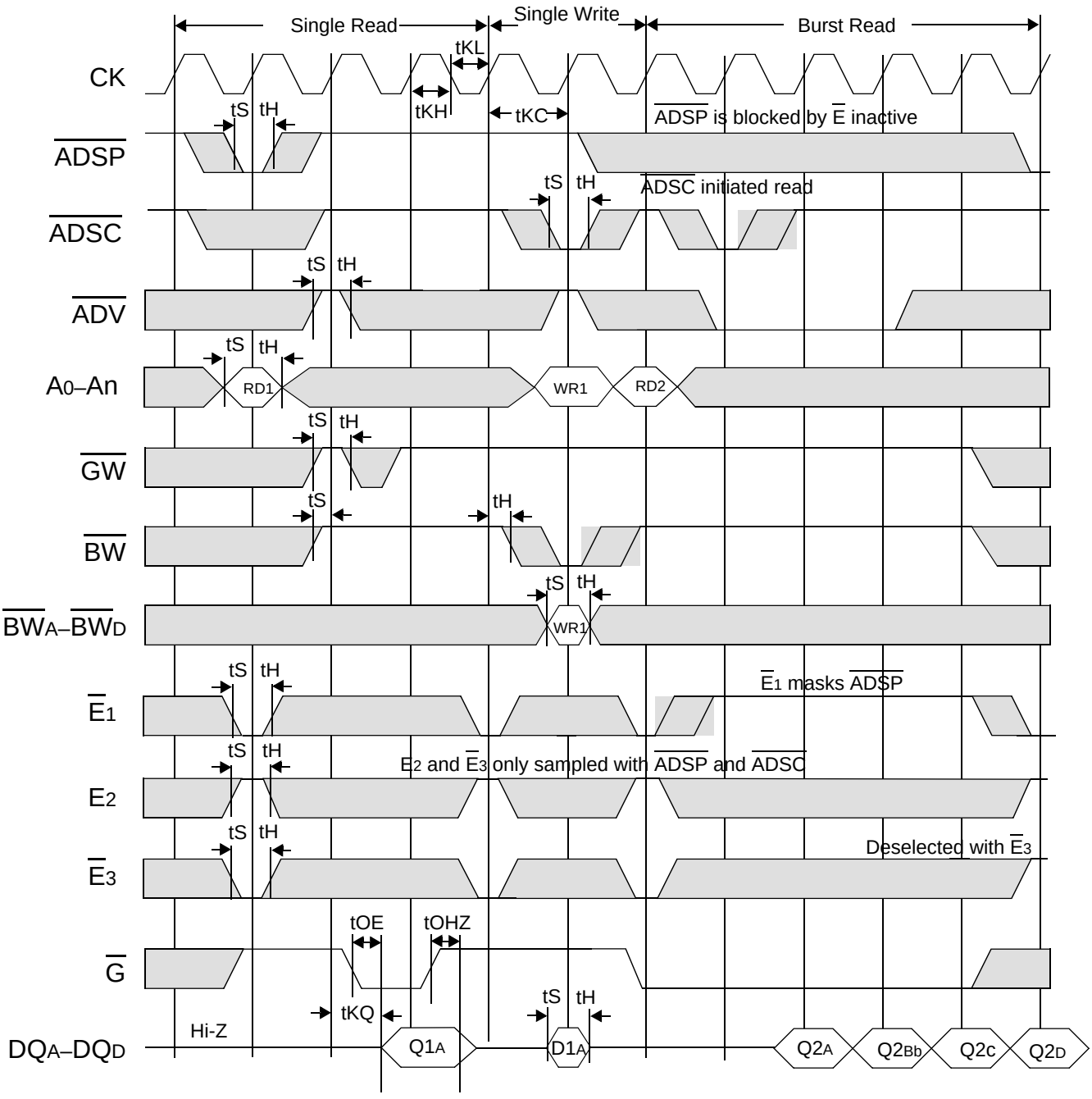
Flow Through Read-Write Cycle Timing



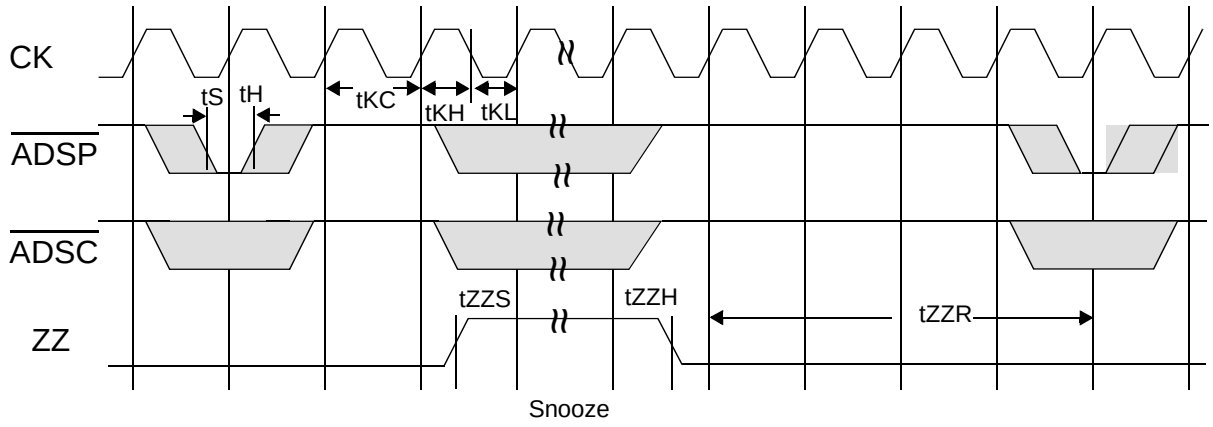
Pipelined SCD Read Cycle Timing



Pipelined SCD Read-Write Cycle Timing



Sleep Mode Timing Diagram



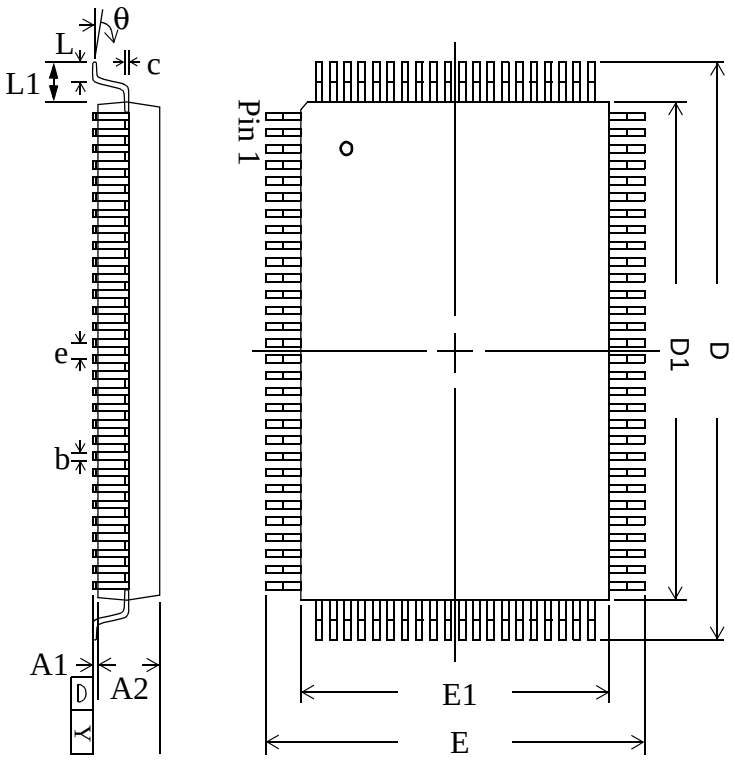
Application Tips

Single and Dual Cycle Deselect

SCD devices force the use of "dummy read cycles" (read cycles that are launched normally but that are ended with the output drivers inactive) in a fully synchronous environment. Dummy read cycles waste performance but their use usually assures there will be no bus contention in transitions from reads to writes or between banks of RAMs. DCD SRAMs do not waste bandwidth on dummy cycles and are logically simpler to manage in a multiple bank application (wait states need not be inserted at bank address boundary crossings) but greater care must be exercised to avoid excessive bus contention.

TQFP Package Drawing

Symbol	Description	Min.	Nom.	Max
A1	Standoff	0.05	0.10	0.15
A2	Body Thickness	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40
c	Lead Thickness	0.09	—	0.20
D	Terminal Dimension	21.9	22.0	22.1
D1	Package Body	19.9	20.0	20.1
E	Terminal Dimension	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1
e	Lead Pitch	—	0.65	—
L	Foot Length	0.45	0.60	0.75
L1	Lead Length	—	1.00	—
Y	Coplanarity			0.10
θ	Lead Angle	0°	—	7°



Notes:
1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.

Ordering Information for GSI Synchronous Burst RAMs

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_A[3]	Status
1M x 18	GS816018T-225	Pipeline/Flow Through	TQFP	225/7	C	
1M x 18	GS816018T-200	Pipeline/Flow Through	TQFP	200/7.5	C	
1M x 18	GS816018T-180	Pipeline/Flow Through	TQFP	180/8	C	
1M x 18	GS816018T-166	Pipeline/Flow Through	TQFP	166/8.5	C	
1M x 18	GS816018T-150	Pipeline/Flow Through	TQFP	150/10	C	
1M x 18	GS816018T-133	Pipeline/Flow Through	TQFP	133/11	C	
512K x 32	GS816032T-225	Pipeline/Flow Through	TQFP	225/7	C	
512K x 32	GS816032T-200	Pipeline/Flow Through	TQFP	200/7.5	C	
512K x 32	GS816032T-180	Pipeline/Flow Through	TQFP	180/8	C	
512K x 32	GS816032T-166	Pipeline/Flow Through	TQFP	166/8.5	C	
512K x 32	GS816032T-150	Pipeline/Flow Through	TQFP	150/10	C	
512K x 32	GS816032T-133	Pipeline/Flow Through	TQFP	133/11	C	
512K x 36	GS816036T-225	Pipeline/Flow Through	TQFP	225/7	C	
512K x 36	GS816036T-200	Pipeline/Flow Through	TQFP	200/7.5	C	
512K x 36	GS816036T-180	Pipeline/Flow Through	TQFP	180/8	C	
512K x 36	GS816036T-166	Pipeline/Flow Through	TQFP	166/8.5	C	
512K x 36	GS816036T-150	Pipeline/Flow Through	TQFP	150/10	C	
512K x 36	GS816036T-133	Pipeline/Flow Through	TQFP	133/11	C	
1M x 18	GS816018T-225I	Pipeline/Flow Through	TQFP	225/7	I	Not Available
1M x 18	GS816018T-200I	Pipeline/Flow Through	TQFP	200/7.5	I	Not Available
1M x 18	GS816018T-180I	Pipeline/Flow Through	TQFP	180/8	I	
1M x 18	GS816018T-166I	Pipeline/Flow Through	TQFP	166/8.5	I	
1M x 18	GS816018T-150I	Pipeline/Flow Through	TQFP	150/10	I	
1M x 18	GS816018T-133I	Pipeline/Flow Through	TQFP	133/11	I	
512K x 32	GS816032T-225I	Pipeline/Flow Through	TQFP	225/7	I	Not Available
512K x 32	GS816032T-200I	Pipeline/Flow Through	TQFP	200/7.5	I	Not Available
512K x 32	GS816032T-180I	Pipeline/Flow Through	TQFP	180/8	I	
512K x 32	GS816032T-166I	Pipeline/Flow Through	TQFP	166/8.5	I	
512K x 32	GS816032T-150I	Pipeline/Flow Through	TQFP	150/10	I	
512K x 32	GS816032T-133I	Pipeline/Flow Through	TQFP	133/11	I	

Notes:

1. Customers requiring delivery in Tape and Reel should add the character T to the end of the part number. Example: GS816018T-150IT.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow through mode-selectable by the user.
3. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings.

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_A[3]	Status
512K x 36	GS816036T-225I	Pipeline/Flow Through	TQFP	225/7	I	Not Available
512K x 36	GS816036T-200I	Pipeline/Flow Through	TQFP	200/7.5	I	Not Available
512K x 36	GS816036T-180I	Pipeline/Flow Through	TQFP	180/8	I	
512K x 36	GS816036T-166I	Pipeline/Flow Through	TQFP	166/8.5	I	
512K x 36	GS816036T-150I	Pipeline/Flow Through	TQFP	150/10	I	
512K x 36	GS816036T-133I	Pipeline/Flow Through	TQFP	133/11	I	

Notes:
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0.18u 16M Sync SRAM Data Sheet Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page;Revisions;Reason
GS816018T-150IT 1.00 9/ 1999A;GS816018T-150IT 2.00 1/1999B	Content	• Converted from 0.25u 3.3V process to 0.18u 2.5V process. Master File Rev B • Added x72 Pinout. • Added GSI Logo.
GS816018T- 2.00 11/ 1999B;GS816018T 2.01 1/ 2000C	Format	• Changed Flow-Through Read-Write cycle Timing Diagram for accuracy
GS816018T 2.01 1/ 2000C;GS816018 T 2.02 1/ 2000D		• Changed pin description in TQFP to match order of pins in pinout.
GS18/362.0 1/2000DGS18/ 362.03 2/2000E		• Front page; Features - changed 2.5V I/O supply to 2.5V or3.3V I/O supply; Core and Interface voltages - Changed paragraph to include information for 3.3V;Completeness • Absolute Maximum Ratings; Changed VDDQ - Value: From: - .05 to VDD : to : -.05 to 3.6; Completeness. • Recommended Operating Conditions;Changed: I/O Supply Voltage- Max. from VDD to 3.6; Input High Voltage- Max. from VDD +0.3 to 3.6; Same page - took out Note 1;Completeness • Electrical Characteristics - Added second Output High Voltage line to table; completeness. • Note: There was not a Rev 2.02 for the 8160Z or the 8161Z.
GS18/362.03 2/2000E; 816018_r2_04	Content	• Input High Voltage (p. 11) changed to 0.7* V_{DD} • Input Low Voltage (p.11) changed to 0.3* V_{DD}
816018_r2_04; 816018_r2_05	Content	• Changed the value of ZZ recovery in the AC Electrical Characteristics table on page 15 from 20 ns to 100 ns
816018_r2_05; 816018_r2_06	Content/Format	• Added 225 MHz speed bin • Updated Pg. 1 table, AC Characteristics table, and Operating Currents table to match 815xxx • Updated format to comply with Technical Publications standards
816018_r2_06; 816018_r2_07	Content	• Updated Capitance table—removed Input row and changed Output row to I/O
816018_r2_07; 816018_r2_08	Content	• Updated Features list on page 1 • Completely reworked table on page 1 • Updated Mode Pin Functions tableon page 7

