# PCD3316

Caller-ID on Call Waiting (CIDCW) receiver

**11 March 1999** **Product specification**

## 1. General description

The PCD3316 is a low power mixed signal CMOS integrated circuit for receiving physical layer signals like Bellcore's 'CPE[1] Alerting Signal (CAS)' and the signals used in similar services. The device is capable of a very high precision detection of the dual tone (2130 and 2750 Hz) by using a patented digital algorithm. The PCD3316 can be used for on-hook and off-hook Caller-ID (CID), Caller-ID on Call Waiting (CIDCW) and Caller-Name (CNAM) applications.

For timing purposes the PCD3316 can be programmed to generate an interrupt signal to the microcontroller every second or every minute. These timings are derived from an on-chip 32.768 kHz oscillator.

Also incorporated in the device are a Frequency Shift Keying (FSK) receiver/demodulator and a 'Ring or polarity change detector'. The status of the PCD3316, the received FSK data bytes and the ringer period can be read and many options can be selected via the I$^2$C-bus serial interface. Two on-chip oscillators are available. One 3.58 MHz oscillator for all internal functions and a low frequency 32.768 kHz oscillator for the 1 second or 1 minute timing.

In Power-down mode only the polarity comparators and the 32.768 kHz oscillator are active. The CAS detection, the FSK receiver and the 3.58 MHz oscillator can be enabled separately. Detection of a polarity change on the inputs POL0 or POL1, the reception of an FSK data byte, the detection of a CAS tone or a timebase interrupt is signalled to the microcontroller by an interrupt request signal (IRQ). The microcontroller can communicate with the PCD3316 device via the serial interface.

The PCD3316 is designed for use in a microcontroller controlled system. The device is available in a SO16 package.

A demonstration board OM5843 and an application note *AN98071* are available.

1. CPE = Customer Premises Equipment.

PHILIPS

## 2. Features

- Bellcore's 'CPE Alerting Signal (CAS)' and British Telecom's (BT) 'Loop State Tone Alert Signal' detection
- BT's 'Idle State Tone Alert Signal' by means of monitoring the input signal level
- 1200 baud FSK demodulator conform Bell 202 and CCITT V23 standards
- Ring or polarity change detector
- Ring period measurement
- Low battery comparator
- Signal level detector
- On-hook and off-hook applications according to *Bellcore TR-NWT-000030* and *SR-TSV-002476* specifications
- Receive sensitivity of –37.8 dBm (in 600 Ω) for CAS
- 2.5 to 3.6 V supply; low power standby mode
- Selectable 1 second or 1 minute timebase interrupt
- 3.58 MHz and 32.768 kHz crystal oscillators
- SO16 package.

## 3. Applications

- Analog Display Services Interface (ADSI) phones
- Feature phones and adjunct boxes with Bellcore CID, CIDCW and CNAM systems
- Computer Telephony Integrated (CTI) systems.

## 4. Ordering information

**Table 1: Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PCD3316T | SO16 | plastic small outline package; 16 leads; body width 7.5 mm | SOT162-1 |

# 5. Block diagram

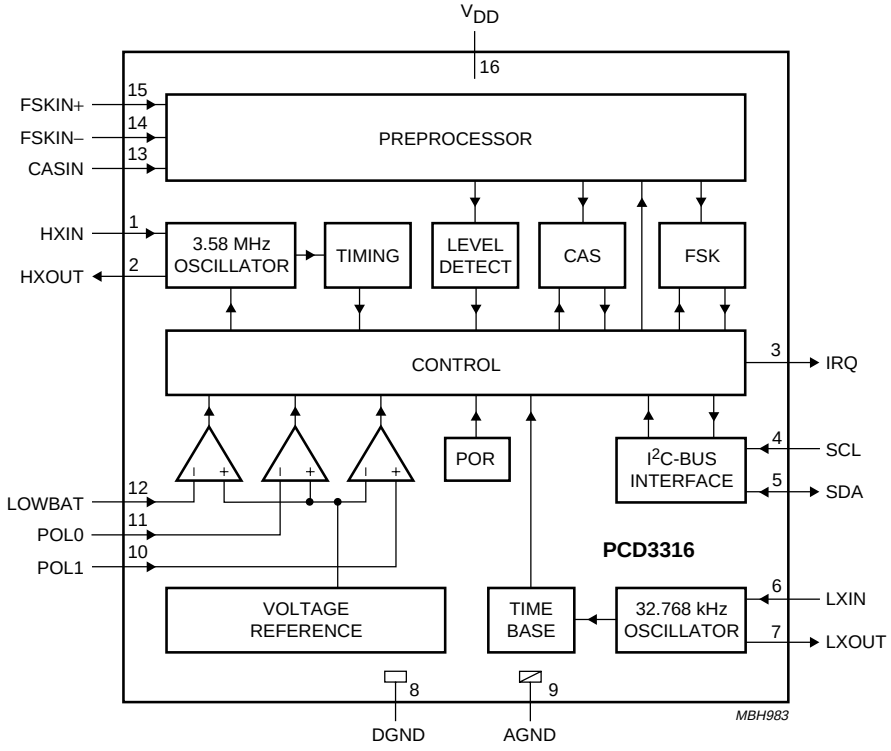



**Fig 1. Block diagram.**

# 6. Pinning information

## 6.1 Pinning

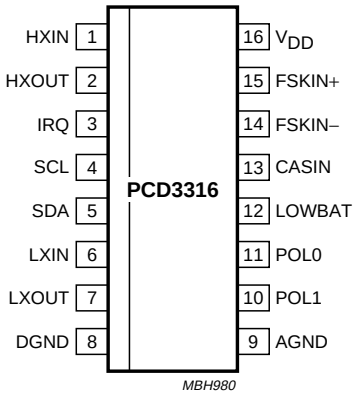



**Fig 2. Pin configuration.**

### 6.2 Pin description

**Table 2: Pin description**

| Symbol | Pin | I/O | Description |
|---|---|---|---|
| HXIN | 1 | I | 3.58 MHz crystal oscillator input |
| HXOUT | 2 | O | 3.58 MHz crystal oscillator output |
| IRQ | 3 | O | interrupt output; programmable active HIGH or active LOW |
| SCL | 4 | I | serial clock line of $I^2C$-bus |
| SDA | 5 | I/O | serial data line of $I^2C$-bus |
| LXIN | 6 | I | 32.768 kHz crystal oscillator input |
| LXOUT | 7 | O | 32.768 kHz crystal oscillator output |
| DGND | 8 | – | digital ground |
| AGND | 9 | – | analog ground |
| POL1 | 10 | I | polarity detector input 1 |
| POL0 | 11 | I | polarity detector input 0 |
| LOWBAT | 12 | I | low battery detector input |
| CASIN | 13 | I | input pin for CAS signal |
| FSKIN– | 14 | I | negative input for FSK signal |
| FSKIN+ | 15 | I | positive input for FSK signal |
| $V_{DD}$ | 16 | – | supply |

## 7. Functional description

### 7.1 Preprocessor and analog inputs

The preprocessor for the CAS detection and the FSK receiver incorporates an Analog-to-Digital Converter (ADC) and a digital bandpass filter.

The LOWBAT input of the PCD3316 can be used for low battery detection. The voltage on the LOWBAT pin is compared with an internal voltage reference circuit. When the LOWBAT voltage drops below the reference voltage, the Status register, bit 5 is set to logic 1.

The PCD3316 can be forced in a Power-down state by switching off the 3.58 MHz system clock and the ADC. This is done by setting Mode register 2, bit 7 (CIDMD2.7) to logic 0. To guarantee correct operation the following order of actions must be performed (see also Section 7.8 about interrupts):

1. Switch off CAS and FSK detection (if turned on)
2. Read the interrupt register (thus clearing pending interrupts generated by the CAS and FSK detector)
3. Switch off the 3.58 MHz oscillator by clearing bit 7 of Mode register 2.

The two low power comparators (inputs POL0 and POL1) and the 32.768 kHz clock are always active.

They can be used for ring or line polarity reversal detection. The POL on/off bit (Mode register 1, bit 4) must be set to enable generation of an interrupt when a polarity change occurs. The result of the two comparators can be read in bits 7 and 6 (POL0 and POL1) of the Status register (see Section 7.4). The 3.58 MHz clock is not needed for the generation of a polarity interrupt.

## 7.2 CAS detection

After a power-on reset or after enabling the CAS detector the internal registers of the CAS detection function are initialized. The initialization takes a maximum of 100 periods of the 3.58 MHz clock.

If the CAS detection is enabled the PCD3316 will generate an interrupt (Interrupt register, bit 1 is set) when a correct dual tone (2130 and 2750 Hz) is detected. Interrupts will be blocked when the signal level on the CAS input is below the threshold in the level detector.

## 7.3 FSK reception

The FSK receiver function can be enabled by setting the FSK on/off bit (Mode register 1, bit 7).

In the FSK transmission specification of BT and Bellcore a channel seizure is transmitted first (sequence of 1010..). After the channel seizure a block of marks and finally the data pattern are sent (see Figure 3). These mark bits are detected by the PCD3316 which sets the FSK-BOM Indication bit (Status register, bit 4). The FSK-BOM Indication bit is reset when the FSK receiver is disabled.

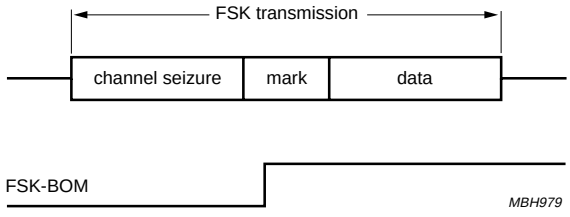



**Fig 3. FSK transmission specification.**

If the FSK-BOM Indication bit is set, the FSK receiver will generate an interrupt after it has received a complete data word. An FSK data word consists of one start bit (space), followed by eight data bits and one stop bit (mark). Interrupts will therefore not be generated during the channel seizure and during the block of marks. When a valid data word has been received, FSK data is available in the FSK data register.

By clearing the FSK-BOM-mask on/off bit (Mode register 1, bit 6), the FSK receiver will not wait with the generation of interrupts until a Begin Of Mark (BOM) has been detected but will handle the channel seizure as normal data. The block of marks which is a string of logic 1 will still not generate interrupts because there are no start bits.

After the generation of an interrupt the IRQ pin will become active (see Figure 4), and the FSK Interrupt bit is set (Interrupt register, bit 5). The received data is available in the FSK data register.

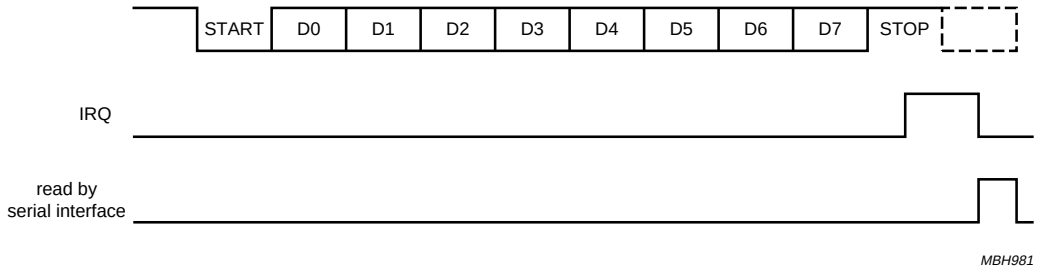



**Fig 4. IRQ generation after reading a valid data byte.**

The FSK-OVR Error bit (Status register, bit 3) indicates that a previous byte is lost due to an overrun. The FSK-FRM Error bit (Status register, bit 2) indicates an incorrect start- or stop-bit. These frame errors indicate that there are synchronization problems. The on-chip level detector can be used to detect a carrier loss during FSK transmission. FSK data can be rejected when the signal level is below the reference level, this to avoid that noise is interpreted as data (Interrupt register, bit 4 is logic 1).

## 7.4 Ring or polarity change detector

For ring and polarity change detection two comparators are available in the PCD3316. The reference level of the comparators is set internally by the reference voltage generator. The voltage levels on the two polarity comparator inputs, POL0 and POL1, are compared with the reference voltage $V_{ref}$. If POL0 < $V_{ref}$ or POL1 > $V_{ref}$, POL0 and POL1 (Status register, bit 7 and 6) are set respectively and reset if POL0 > $V_{ref}$ and POL1 < $V_{ref}$. Every time the POL0 status bit changes from logic 1 to logic 0, a POL0 interrupt is generated. Every time the POL1 status bit changes from logic 0 to logic 1, a POL1 interrupt is generated.

The period time of a POL1-POL0-POL1 sequence is available in the Ringer period register. It is preset to 255 on power-on and updated every time a POL1 interrupt is generated. The sequence is:

1. Power-on: Ringer period register = 255
2. First POL1 interrupt: Ringer period register = 255
3. First POL1 interrupt after a POL0 interrupt: Ringer period register = new time
4. First POL1 interrupt after more than $^{255}/_{2048}$ s: Ringer period register = 255.

The period is given in multiples of $^{1}/_{2048}$ s. The maximum value is 255.

The POL1-POL0-POL1 sequence is recognized when one or more POL1 interrupts are generated followed by one or more POL0 interrupts, followed by a POL1 interrupt. The 32.768 kHz clock is needed for the generation of a polarity interrupt.

## 7.5 Low battery detection

The low battery voltage detection input (pin LOWBAT) is connected to the positive input of a comparator. The negative input is connected to the internal reference voltage. If the voltage on the LOWBAT input pin is less than the reference voltage $V_{ref}$, the LOW-BAT Indication (Status register, bit 5) is set. If the LOWBAT input rises above $V_{ref}$ again, the LOW-BAT Indication is cleared.

The 32.768 kHz clock signal must be available. The LOW-BAT Indication bit does not generate interrupts, thus the bit should be polled.

## 7.6 Level detect

When the input signal level on the FSK or the CAS input (the one that is selected) is below a threshold of typically −40 dBm, the Low Level Status bit will be set (Interrupt register, bit 4). The level detector can be used to observe a carrier loss during FSK transmission and to detect the 'Idle State Tone Alert Signal' for British Telecom. The signal power on the input can be monitored by polling the register bit since it will not generate an interrupt. Signal power is measured in a frequency band corresponding to the selected operation mode, FSK (1000 to 2200 Hz) or CAS (2000 to 2800 Hz).

The Low Level Status bit will be updated every 8 ms. When FSK and CAS are both disabled the signal level on the FSK input is measured. The 32.768 kHz clock signal must be available.

## 7.7 Time base

The 32.768 kHz oscillator is used to generate either a 1 second or a 1 minute interrupt signal. If the TB on/off bit is set (Mode register 2, bit 6) every second or minute an interrupt is generated and MIN Interrupt and/or SEC Interrupt bits (Interrupt register, bit 7 and 6) are set. After reading the Interrupt register the interrupt is cleared.

The SEC/MIN (Mode register 2, bit 5) selects whether every second (SEC/MIN is set) or every minute (SEC/MIN is cleared) an interrupt is generated. All possible selections are shown in Table 3. Resetting bit TB on/off in Mode register 2 (bit 6) will only disable time base interrupts, and the 32.768 kHz oscillator will continue to run.

## 7.8 Interrupt

The interrupt request output (IRQ) is active HIGH by default. The polarity of the IRQ output can be made active LOW by the INT Polarity HIGH/LOW bit (Mode register 1, bit 3). The IRQ pin is in 3-state when not active, so an external pull-up or pull-down resistor is required. The interrupt cause is indicated by the flags in the Interrupt register. Interrupt flags are set by hardware but must be reset by software. All flags of the Interrupt register are reset when the register is read via $I^2C$-bus interface.

The IRQ pin is deactivated at the positive edge of SCL which reads the first data bit of the Interrupt register. The IRQ pin will stay inactive for one SCL cycle. IRQ can handle a next interrupt after the next positive edge of SCL.

**Table 3: Selection of interrupt modes**

| Mode register 2 (CIDMD2) | | Interrupt register (CIDINT) | | Interrupt |
|---|---|---|---|---|
| TB on/off (CIDMD2.6) | SEC/MIN (CIDMD2.5) | MIN Interrupt (CIDINT.7) | SEC Interrupt (CIDINT.6) | |
| 0 | X [1] | 0 | 0 | no time base interrupt (time base is reset) |
| 1 | 0 | 1 | 0 | every minute an interrupt is generated; no second interrupt |
| 1 | 1 | 1 | 1 | every second an interrupt is generated; every minute an interrupt is generated |

[1] X = don't care.

## 7.9 The internal Power-on reset (POR)

The device contains an on-chip Power-on reset circuitry which activates a reset as long as $V_{DD}$ is below a predefined level $V_{POR(H)}$. If $V_{DD}$ exceeds $V_{POR(H)}$, the 3.58 MHz oscillator will start. The PCD3316 is initialized and the internal registers are set to the default value (see Section 7.13). It takes a maximum of 100 cycles of the 3.58 MHz clock to initialize all internal functions. The POR circuitry also ensures, that the chip will be switched off as soon as a falling $V_{DD}$ reaches a predefined level ($V_{POR(L)}$).

## 7.10 3.58 MHz oscillator circuitry

The 3.58 MHz oscillator is needed for the FSK receiver and the CAS detection. This on-chip Amplitude Controlled Oscillator (ACO) circuitry is a single-stage inverting amplifier biased by an internal feedback resistor $R_{fb}$. The oscillator circuit is shown in Figure 5. When using a quartz resonator to drive the oscillator, normally no external components are needed.

When using ceramic resonators to drive the oscillator, in some cases external components are needed; refer to the ceramic resonator product specifications. Two different configurations are shown in Figure 6a and Figure 6b.

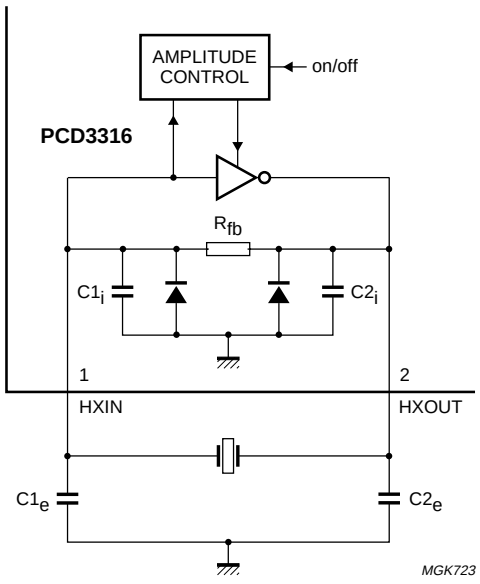
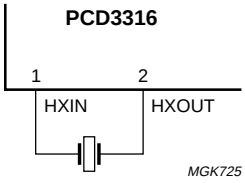


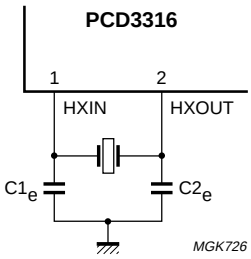

**Fig 5. Oscillator.**

To drive the device with an external clock source, apply the external clock signal to HXIN, and leave HXOUT to float, as shown in Figure 6c. If the amplitude of the input signal is less than $V_{DD}$ to DGND or a sine wave is applied, capacitive decoupling is needed as shown in Figure 6d.

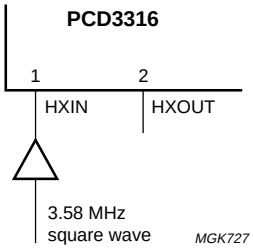
In the Power-down mode (Mode register 2, bit 7 = 0), the oscillator is stopped and HXIN and HXOUT are internally pulled LOW. The current of the whole oscillator is switched off.



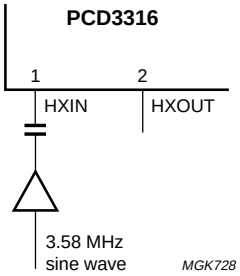

a. Standard oscillator: quartz or PXE.




b. Oscillator: quartz or PXE with external capacitors.

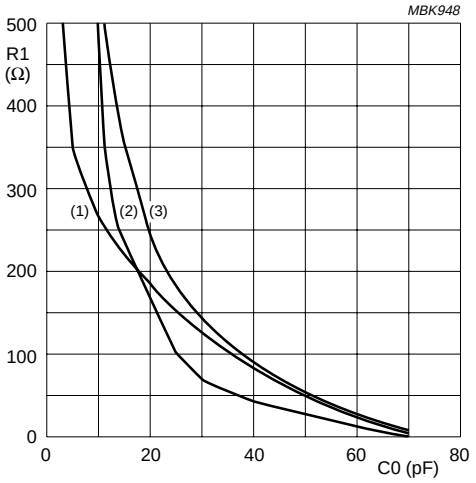



c. External clock: square wave.




d. External clock: sine wave.

**Fig 6. 3.58 MHz oscillator configurations.**



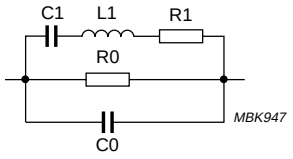

$C1_e$ and $C2_e$ are the external load capacitances (see Figure 6b). Normally, they are not needed due to integrated load capacitances of 10 pF; see curve (2).

(1) $C1_e = C2_e = 22$ pF.

(2) $C1_e = C2_e = 0$ pF.

(3) $C1_e = C2_e = 12$ pF.

a. Resonator requirements for the ACO.




For correct function of the oscillator, the values of R1 and C0 of the chosen resonator (quartz or PXE) must be below the related curve lines shown in Figure 7a. The value of the parallel resistor R0 must be less than 47 kΩ.

The wiring between chip and resonator should be kept as short as possible.

b. Resonator equivalent circuit.

**Fig 7. Resonator requirements and equivalent circuit.**

## 7.11 32 kHz oscillator

The 32.768 kHz oscillator is enabled permanently and is used to generate either a 1 second or 1 minute interrupt. The 32.768 kHz clock is also used for the ‘Ring or polarity change detector’, the ‘Low battery detection’ and the ‘Level detect’ function.

An external 32.768 kHz signal may be applied to pin LXIN while leaving pin LXOUT not connected.

The 32 kHz oscillator requires an external 32.768 kHz quartz crystal and an external feedback resistor (4.7 MΩ) between the LXIN and LXOUT pins (see Figure 8).

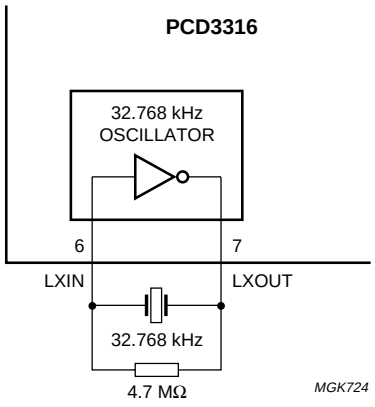



**Fig 8. Connections of the 32 kHz oscillator.**

## 7.12 Serial interface

The serial interface of the PCD3316 is the I²C-bus. A detailed description of the I²C-bus specification, including applications, is given in the brochure: *The I²C-bus and how to use it*, order no. 9398 393 40011 or *I²C Peripherals Data Handbook IC12*.

### 7.12.1 Characteristics of the I²C-bus

For the I²C-bus configuration see Figure 9. A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are called the ‘slaves’. The PCD3316 operates in the slave transmitter/receiver mode only.

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

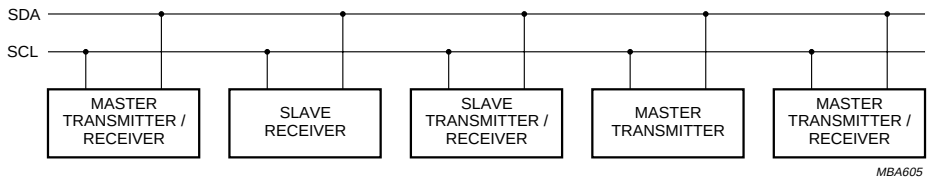



**Fig 9. I²C-bus configuration.**

### 7.12.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as a STOP condition (P); see Figure 10.

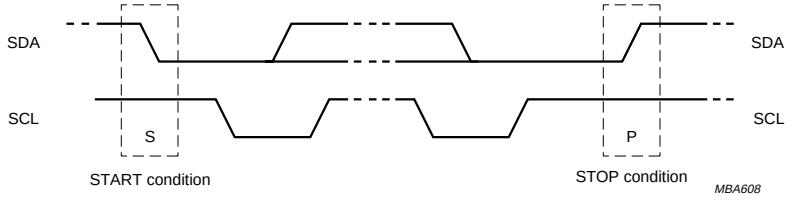



**Fig 10. START and STOP conditions for the I²C-bus.**

### 7.12.3 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal; see Figure 11.

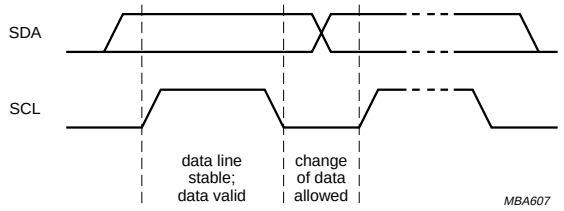



**Fig 11. I²C-bus bit transfer.**

### 7.12.4 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from the transmitter to the receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge-related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock period immediately after the 8th SCL pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

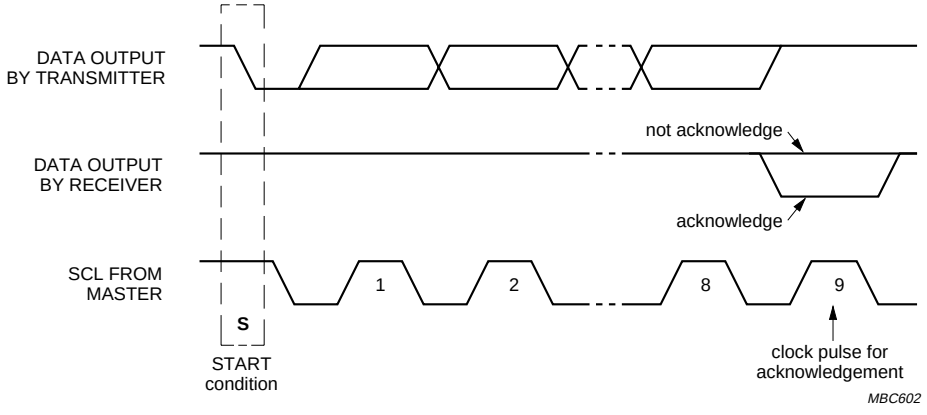



**Fig 12. I²C-bus acknowledge.**

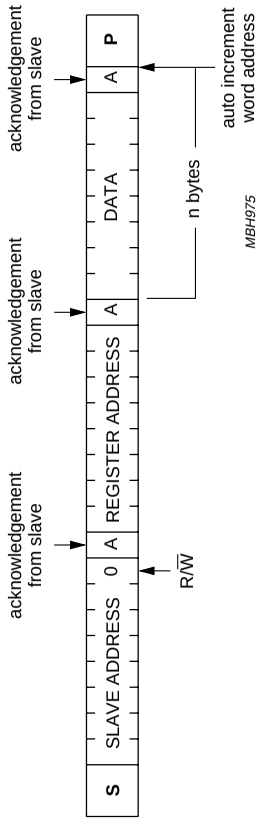
### 7.12.5 I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with first byte transmitted after the START procedure. One I²C-bus slave address is reserved for the PCD3316, E0H (1110 0000 for write and 1110 0001 for read).

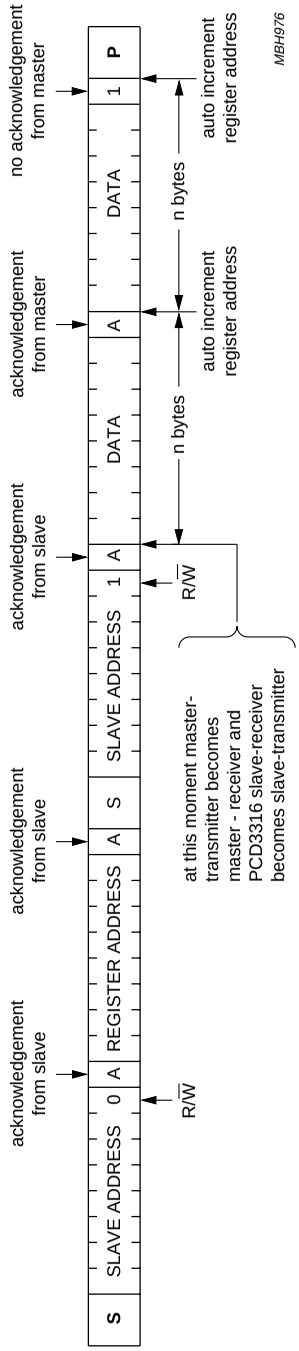
The I²C-bus protocol is shown in Figure 13. Two different sequences are considered, the write sequence and the read sequence. Both sequences are initiated with a START condition (S) from the I²C-bus master which is followed by the PCD3316 slave address with the read bit cleared. The first byte after the I²C-bus address is interpreted as the address of a PCD3316 register.During the write sequence the register address of the PCD3316 is auto-incremented on each acknowledge. The write sequence is ended with a STOP condition from the master. If the addressed register is read-only or non-existent, nothing will be changed.

For the read sequence the bus master issues a repeated START condition followed by the PCD3316 slave address with the read bit set. Then data is read from previously set address and sent out. When the master responds with an acknowledge the address of the register is auto incremented and the slave will put the data from the next register on the bus. The read sequence is stopped when the master stops giving an acknowledge and generates a STOP condition.

When a non-existing register is addressed the PCD3316 will return FFH. Existing register addresses are shown in Section 7.13. An additional register address (73H) is reserved for test purposes. This address cannot be reached with the auto-increment function of the I²C-bus interface.




a. I²C-bus write sequence.




b. I²C-bus read sequence.

**Fig 13. I²C-bus write and read sequence.**

### 7.12.6 I²C-bus bit rate

When a microcontroller is used that implements an I²C-bus in software, the bit rate of the I²C-bus can be critical during reception of FSK. The collection of the interrupt data and FSK-data from the PCD3316 takes 48 bits on the I²C-bus. With an FSK baud rate of 1200 (corresponds to 1200 bits per second) the minimal speed of the I²C-bus should be 5.76 kbits/s. Additional interrupts generated by the time base of the PCD3316 will cause the processor to collect extra information from the PCD3316.

As a consequence, the FSK-data can be overrun in the PCD3316 and one data byte will be lost. In this case, the time base interrupt should be suppressed while FSK is active. This can be done by setting the ‘INT-SUP on/off’ bit (bit 4 in Mode register 2). The ‘TB on/off’ bit (bit 6 in Mode register 2) will still be set but the IRQ output will not be activated by the time base interrupt. Any time base interrupt can be detected by the microcontroller when an FSK interrupt is processed by reading the Interrupt register.

## 7.13 Registers

**Table 4: Register overview**

| Address | Name | Function | Read/Write | Default value |
|---|---|---|---|---|
| 00H | CIDINT | Interrupt register | read only | 0000 0000 |
| 01H | CIDFSK | FSK data register | read only | – |
| 02H | CIDSTA | Status register | read only | – |
| 03H | CIDRNG | Ringer period register | read only | – |
| 04H | CIDMD1 | Mode register 1 | read/write | 0101 1000 |
| 05H | CIDMD2 | Mode register 2 | read/write | 1101 0000 |

### 7.13.1 Interrupt register (CIDINT)

**Table 5: Interrupt register**

*Address: 00H; read only.*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MIN Interrupt | SEC Interrupt | FSK Interrupt | Low Level Status | POL1 Interrupt | POL0 Interrupt | CAS Interrupt | – |

**Table 6: Description of CIDINT bits**

| Bit | Symbol | Description |
|---|---|---|
| CIDINT.7 | MIN Interrupt | MIN Interrupt = 0: no interrupt request;<br>MIN Interrupt = 1: one minute interrupt request |
| CIDINT.6 | SEC Interrupt | SEC Interrupt = 0: no interrupt request;<br>SEC Interrupt = 1: one second interrupt request |
| CIDINT.5 | FSK Interrupt | FSK Interrupt = 0: no FSK interrupt or FSK disabled;<br>FSK Interrupt = 1: FSK interrupt, one byte received |
| CIDINT.4 | Low Level Status | Low Level Status = 0: signal level on selected input above power reference (no interrupt);<br>Low Level Status = 1: signal level on selected input below power reference (no interrupt) |
| CIDINT.3 | POL1 Interrupt | POL1 Interrupt = 0: no zero to one changes on POL1 input or polarity interrupt disabled;<br>POL1 Interrupt = 1: a one to zero input change on the POL1 input is detected |
| CIDINT.2 | POL0 Interrupt | POL0 Interrupt = 0: no one to zero changes on POL0 input or polarity interrupt disabled;<br>POL0 Interrupt = 1: a zero to one input change on the POL0 input is detected |
| CIDINT.1 | CAS Interrupt | CAS Interrupt = 0: no CAS signal detected or CAS disabled;<br>CAS Interrupt = 1: CAS signal detected |
| CIDINT.0 | – | reserved bit |

### 7.13.2 FSK data register (CDFSK)

**Table 7: Interrupt register**

*Address: 01H; read only.*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 8: Description of CDFSK bits**

| Bit | Symbol | Description |
|---|---|---|
| CDFSK.7 to CDFSK.0 | D7 to D0 | If an FSK interrupt has occurred and no FSK error is detected, the FSK data register contains valid data. |

### 7.13.3 Status register (CIDSTA)

**Table 9: Status register**

*Address: 02H; read only.*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| POL1 | POL0 | LOW-BAT Indication | FSK-BOM Indication | FSK-OVR Error | FSK-FRM Error | – | – |

**Table 10: Description of CIDSTA bits**

| Bit | Symbol | Description |
|---|---|---|
| CIDSTA.7 | POL1 | POL1 = 0: voltage on input POL1 < $V_{ref}$; POL1 = 1: voltage on input POL1 > $V_{ref}$ |
| CIDSTA.6 | POL0 | POL0 = 0: voltage on input POL0 > $V_{ref}$; POL0 = 1: voltage on input POL0 < $V_{ref}$ |
| CIDSTA.5 | LOW-BAT Indication | LOW-BAT Indication = 0: voltage on input LOWBAT > $V_{ref}$;<br>LOW-BAT Indication = 1: voltage on input LOWBAT < $V_{ref}$ |
| CIDSTA.4 | FSK-BOM Indication | FSK-BOM Indication = 0: begin of mark period not yet detected;<br>FSK-BOM Indication = 1: begin of mark period detected |
| CIDSTA.3 | FSK-OVR Error | FSK-OVR Error = 0: no FSK overrun error;<br>FSK-OVR Error = 1: FSK overrun error, data byte(s) lost |
| CIDSTA.2 | FSK-FRM Error | FSK-FRM Error = 0: no FSK frame error;<br>FSK-FRM Error = 1: FSK frame error, stop bit was wrong |
| CIDSTA.1 and CIDSTA.0 | – | reserved bits |

### 7.13.4 Ringer period register (CIDRNG)

**Table 11: Register format**

*Address: 03H; read only.*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 12: Description of CIDRNG bits**

| Bit | Symbol | Description |
|---|---|---|
| CIDRNG.7 to CIDRNG.0 | D7 to D0 | The value held in this byte denotes the time between two positive edges of the POL1 comparator output (between two positive edges of POL1 one positive edge of POL0 must have been detected). |

### 7.13.5 Mode register 1 (CIDMD1)

**Table 13: Mode register 1**

*Address: 04H; read/write.*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FSK on/off | FSK-BOM-mask on/off | CAS on/off | POL on/off | INT polarity HIGH/LOW | – | – | – |

**Table 14: Description of CIDMD1 bits**

| Bit | Symbol | Description |
|---|---|---|
| CIDMD1.7 | FSK on/off | FSK on/off = 0: FSK receiver disabled; FSK on/off = 1: FSK receiver enabled |
| CIDMD1.6 | FSK-BOM-mask on/off | FSK-BOM-mask on/off = 0: FSK interrupts will be generated when a data word was received even before mark period (data from channel seizure);<br>FSK-BOM-mask on/off = 1: FSK interrupts will only be generated after the mark period was detected (no interrupts from channel seizure) |
| CIDMD1.5 | CAS on/off | CAS on/off = 0: CAS detector disabled; CAS on/off = 1: CAS detector enabled |
| CIDMD1.4 | POL on/off | POL on/off = 0: disable interrupts due to polarity change;<br>POL on/off = 1: enable interrupts due to polarity change |
| CIDMD1.3 | INT polarity HIGH/LOW | INT polarity HIGH/LOW = 0: interrupt pin active LOW;<br>INT polarity HIGH/LOW = 1: interrupt pin active HIGH |
| CIDMD1.2 to CIDMD1.0 | – | reserved bits |

### 7.13.6 Mode register 2 (CIDMD2)

**Table 15: Mode register 2**

*Address: 05H; read/write.*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| XTAL on/off | TB on/off | SEC/MIN | INT-SUP on/off | – | – | – | – |

**Table 16: Description of CIDMD2 bits**

| Bit | Symbol | Description |
|---|---|---|
| CIDMD2.7 | XTAL on/off | XTAL on/off = 0: disable 3.58 MHz oscillator;<br>XTAL on/off = 1: enable 3.58 MHz oscillator |
| CIDMD2.6 | TB on/off | TB on/off = 0: disable 32.768 kHz timebase;<br>TB on/off = 1: enable 32.768 kHz timebase |
| CIDMD2.5 | SEC/MIN | SEC/MIN = 0: every minute a timebase interrupt;<br>SEC/MIN = 1: every second a timebase interrupt |
| CIDMD2.4 | INT-SUP on/off | INT-SUP on/off = 0: enable SEC/MIN interrupts during FSK reception;<br>INT-SUP on/off = 1: disable SEC/MIN interrupts during FSK reception |
| CIDMD2.3 to CIDMD2.0 | – | reserved bits |

# 8. Limiting values

**Table 17: Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | –0.5 | +5.0 | V |
| $I_{DD}$ | supply current | | – | 50 | mA |
| $I_I$ | DC input current at any input | | –10 | +10 | mA |
| $I_O$ | DC output current at any output | | –10 | +10 | mA |
| $V_I$ | input voltage on all inputs | | –0.5 | $V_{DD}$ + 0.5 [1] | V |
| $P_{tot}$ | total power dissipation | | – | 300 | mW |
| $P_O$ | power dissipation per output | | – | 10 | mW |
| $T_{amb}$ | operating ambient temperature | | –25 | +70 | °C |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |

[1] $V_{I(max)}$ = 5.0 V.

# 9. Characteristics

**Table 18: Characteristics**

*$V_{DD}$ = 2.5 to 3.6 V; $T_{amb}$ = –25 to +70 °C; HXIN = 3.579545 MHz ±0.05%; LXIN = 32.768 kHz ±0.1%; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | [1] | 2.5 | 3.3 | 3.6 | V |
| $V_{POR(H)}$ | power-on reset HIGH voltage | | | 1.85 | 2.05 | 2.25 | V |
| $V_{hys(POR)}$ | power-on reset hysteresis voltage | | [2] | 50 | 100 | 150 | mV |
| $I_{DD}$ | supply currents | $V_{DD}$ = 2.5 V | | | | | |
| | Power-down mode | | [3] | – | 30 | 70 | µA |
| | operating | | [3] [4] | – | 2.0 | 2.3 | mA |
| **Low voltage and polarity comparators (pins LOWBAT, POL0 and POL1)** | | | | | | | |
| $V_{hys}$ | hysteresis voltage | | | – | 20 | – | mV |
| $I_{LI}$ | input leakage current | | [5] | – | – | 1 | µA |
| **Internal reference** | | | | | | | |
| $V_{ref}$ | reference voltage level | | | 1.125 | 1.25 | 1.375 | V |
| $P_{i(ref)}$ | input signal reference power for Low Level Status bit | in 600 Ω load | [6] | –43.8 | – | –37.8 | dBm |
| $t_{r(level)}$ | input signal to Low Level Status bit rise time | input signal power < $P_{i(ref)}$ | | – | – | 8 | ms |
| $t_{f(level)}$ | input signal to Low Level Status bit fall time | input signal power > $P_{i(ref)}$ | | – | – | 8 | ms |
| **Logical output (pin IRQ)** [7] | | | | | | | |
| $I_{OL}$ | LOW-level output current | $V_{IRQ}$ = 0.4 V | | 2 | – | – | mA |
| $I_{OH}$ | HIGH-level output current | $V_{IRQ}$ = $V_{DD}$ – 0.4 V | | 2 | – | – | mA |

**Table 18: Characteristics** *...continued*

*$V_{DD}$ = 2.5 to 3.6 V; $T_{amb}$ = −25 to +70 °C; HXIN = 3.579545 MHz ±0.05%; LXIN = 32.768 kHz ±0.1%; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **FSK receiver (pins FSKIN+ and FSKIN−)** | | | | | | | |
| $Z_i$ | input impedance FSKIN+ to FSKIN− | | | – | 1.4 | – | MΩ |
| $Z_{source(max)}$ | maximum source impedance | | | – | – | 200 | kΩ |
| $P_{i(FSKIN)}$ | input signal power | in 600 Ω load | [8] | −50 | – | 0 | dBm |
| $S/N_{FSK}$ | signal-to-noise ratio | 200 to 3400 Hz | | 20 | – | – | dB |
| $\|V_{dif}\|$ | differential voltage between mark and space (twist) | | | – | – | 10 | dB |
| $f_{(D)}$ | data transmission rate frequency | | | 1180 | 1200 | 1212 | bits/s |
| $f_s$ | space frequency | | | 2068 | – | 2222 | Hz |
| $f_m$ | mark frequency | | | 1188 | – | 1320 | Hz |
| **CAS detector (pin CASIN)** | | | | | | | |
| $Z_i$ | input impedance CASIN to $V_{ref}$ | | | – | 1.4 | – | MΩ |
| $Z_{source(max)}$ | maximum source impedance | | | – | – | 200 | kΩ |
| $P_i$ | input signal power | in 600 Ω load | [8] | −37.8 | – | 0 | dBm |
| $TH_{ns(CAS)}$ | no signal threshold (CAS) | in 600 Ω load | | −43.8 | – | −37.8 | dBm |
| $f_l$ | low tone frequency | | | – | 2130 | – | Hz |
| $f_h$ | high tone frequency | | | – | 2750 | – | Hz |
| $\Delta f_{max}$ | maximum frequency deviation | | [9] | −0.5 | – | +0.5 | % |
| $V_{dif}$ | differential voltage level (twist) | | [9] | – | – | 6 | dB |
| $t_{dt}$ | dual tone detection time | | | 60 | – | – | ms |
| **$I^2C$-bus interface (pins SCL and SDA) [10]; see Figure 14** | | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | [11] | 0 | – | $0.3V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | [11] | $0.7V_{DD}$ | – | $V_{DD}$ | V |
| $I_{OL1}$ | LOW-level output current for pin SDA | $V_{O(SDA)}$ = 0.4 V | | 2 | – | – | mA |
| $C_i$ | input capacitance for each I/O pin | | | – | – | 10 | pF |
| $f_{SCL}$ | SCL clock frequency | | | – | – | 100 | kHz |
| $t_{BUF}$ | bus free time | | | 4.7 | – | – | µs |
| $t_{SU;STA}$ | START condition set-up time | | | 4.7 | – | – | µs |
| $t_{HD;STA}$ | START condition hold time | | | 4.0 | – | – | µs |
| $t_{LOW}$ | SCL LOW time | | | 4.7 | – | – | µs |
| $t_{HIGH}$ | SCL HIGH time | | | 4.0 | – | – | µs |
| $t_r$ | maximum SCL and SDA rise time | | [12] | – | – | 1000 | ns |
| $t_f$ | maximum SCL and SDA fall time | | [12] | – | – | 300 | ns |
| $t_{SU;DAT}$ | data set-up time | | | 250 | – | – | ns |
| $t_{HD;DAT}$ | data hold time | | | 0 | – | – | ns |
| $t_{VD;DAT}$ | SCL LOW to data out valid time | | | – | – | 3.4 | µs |
| $t_{SU;STO}$ | STOP condition set-up time | | | 4.0 | – | – | µs |

**Table 18: Characteristics** *...continued*

*$V_{DD}$ = 2.5 to 3.6 V; $T_{amb}$ = −25 to +70 °C; HXIN = 3.579545 MHz ±0.05%; LXIN = 32.768 kHz ±0.1%; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **3.58 MHz oscillator (pins HXIN and HXOUT)** | | | | | | |
| $V_{HXIN(p-p)}$ | external clock signal amplitude (peak-to-peak value) on pin HXIN | | 0.5 | – | $V_{DD}$ | V |
| $Z_{i(HXIN)}$ | input impedance on pin HXIN | | 300 | 1000 | – | kΩ |
| $C1_i$; $C2_i$ | input capacitance on pins HXIN and HXOUT [13] | | – | 10 | – | pF |
| **32 kHz oscillator (pins LXIN and LXOUT)** | | | | | | |
| $g_m$ | transconductance | $V_{i(p-p)}$ < 50 mV | 2 | 4 | 10 | µS |
| $C_{i(LXIN)}$ | LXIN input capacitance | | – | 13 | – | pF |
| $C_{o(LXOUT)}$ | LXOUT output capacitance | | – | 10 | – | pF |

[1] Except for FSK and CAS detection, all circuitry works already when $V_{DD} > V_{POR(H)}$. Since the $I^2C$-bus interface will work (starts to acknowledge), the application can start reading the LOW-BAT Indication bit (Status register, bit 5) to check whether the supply voltage has reached the operating voltage level. A voltage divider network can be connected to pins $V_{DD}$, LOWBAT and AGND/DGND such that $V_{LOWBAT} = V_{ref}$ if $V_{DD} = V_{DD(min)}$.

[2] The power-on reset LOW level is defined as $V_{POR(L)} = V_{POR(H)} - V_{hys(POR)}$. By design $V_{POR(L)}$ is always lower than $V_{POR(H)}$.

[3] 32 kHz oscillator on (MIN Interrupt, SEC Interrupt, Polarity change, Low battery and Level detect available).

[4] 3.58 MHz oscillator on (device fully operational).

[5] $GND < V_I < V_{DD}$. The leakage currents are generally very small, <1 nA. The value given here, 1 µA, is a maximum that can occur after an Electrostatic Stress on the pin.

[6] When FSK is selected the signal power is measured between 1000 and 2200 Hz. When CAS is selected signal levels are measured between 2000 and 2800 Hz.

[7] The IRQ pin is implemented as a 3-state pin which is only active (either HIGH or LOW) when an interrupt occurs. A pull-up or pull-down has to be connected to define the line when no interrupt is generated.

[8] Verified on sampling basis.

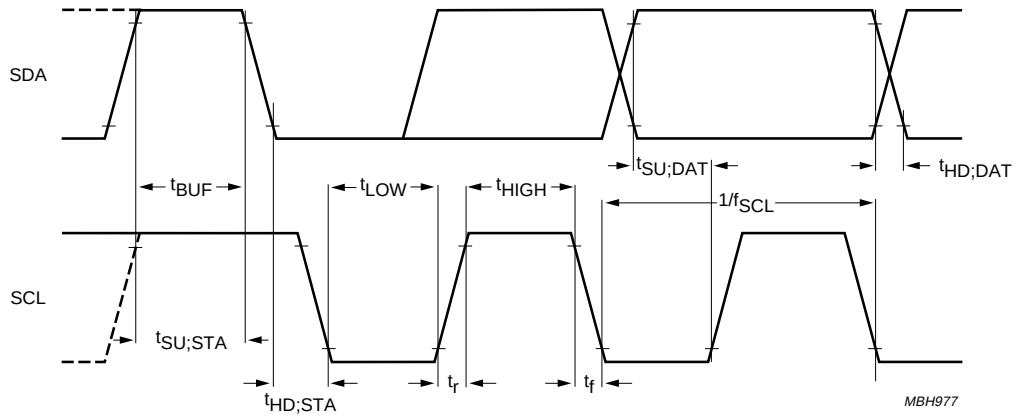
[9] According to Bellcore specification: near end speech level ≤ −7 dBm ASL (ASL = Active Speech Level), referenced to 600 Ω, according to method B of recommendation P.56.

[10] Pins SCL and SDA are equipped with an open-drain output buffer. The pins have no clamp diode to $V_{DD}$.

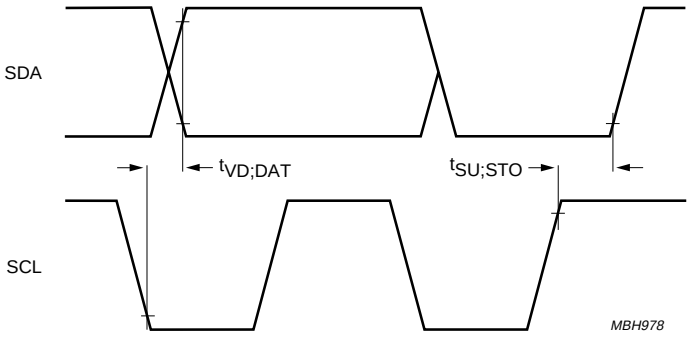
[11] The input threshold voltage of SCL and SDA meet the $I^2C$-bus specification. Therefore, an input voltage below $0.3V_{DD}$ will be recognized as a logic 0 and an input voltage above $0.7V_{DD}$ will be recognized as a logic 1

[12] Maximum capacitive load for each bus line is 400 pF.

[13] $C1_i$ and $C2_i$ are the total internal capacitances (including gate capacitance and leadframe capacitance).



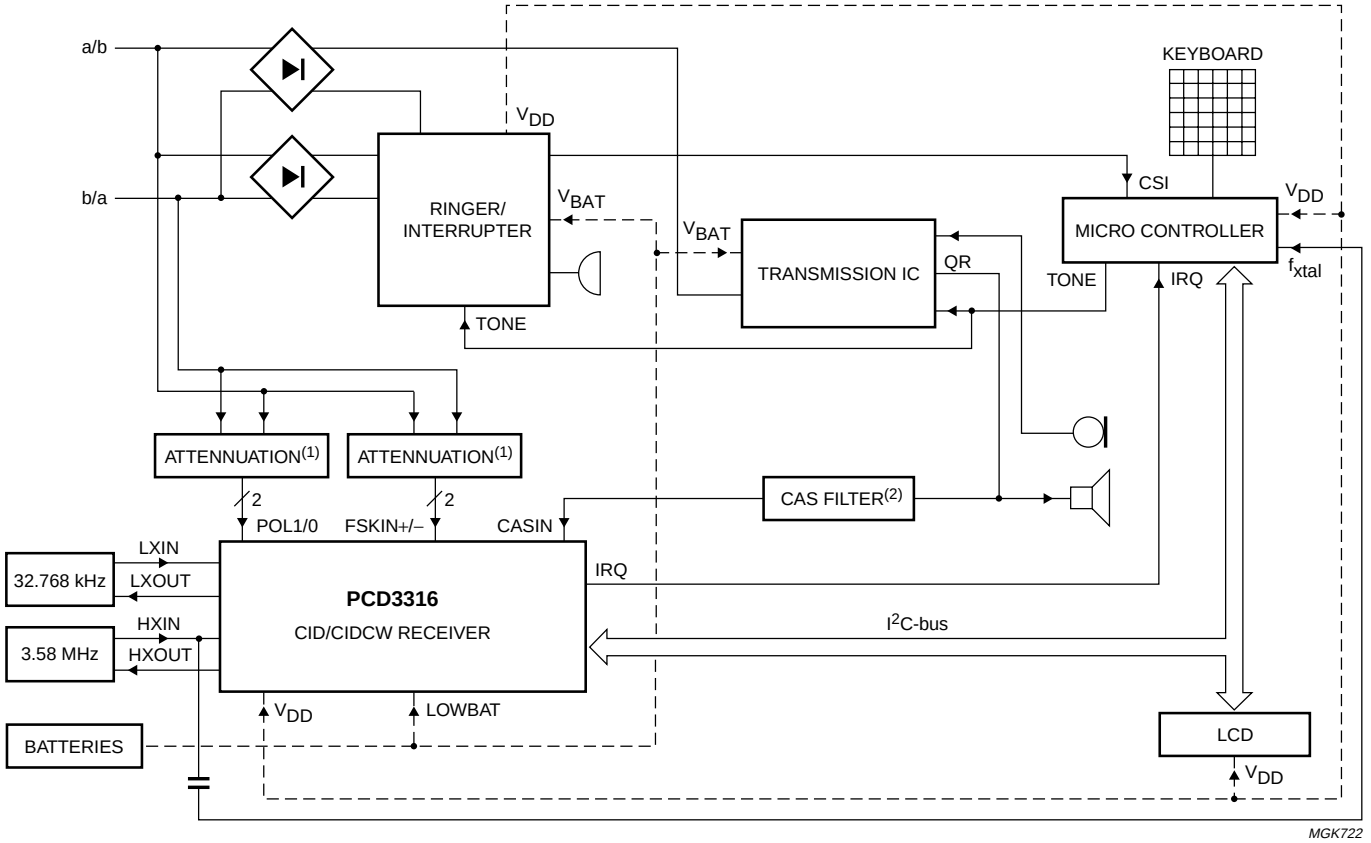

a. Timing diagram 1.




b. Timing diagram 2.

**Fig 14. $I^2C$-bus timing.**

## 10. Application information




A demo-board (OM5843) of this configuration is available. Please contact your Philips sales office.

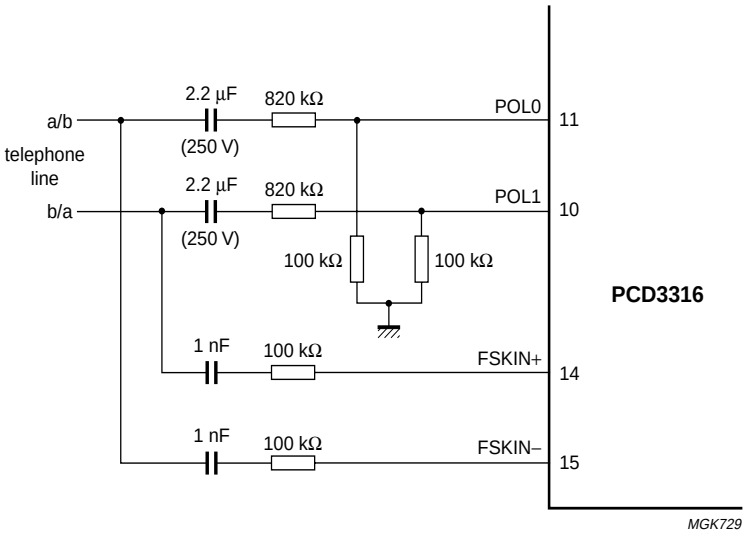
(1) See Figure 16a.

(2) See Figure 16b.

**Fig 15. Application diagram for a telephone with CID/CIDCW functionality.**

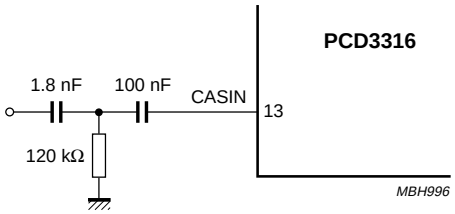


9397 750 04824




Attenuation networks to connect the polarity and FSK inputs to the telephone line.

a. Attenuation networks.




High-pass filter (cut-off frequency ≈ 1 kHz) to improve performance of CAS detection.

b. High-pass filter.

**Fig 16. Application diagrams.**

# 11. Test information

## 11.1 Application note on Customer Premises Equipment (CPE) testing

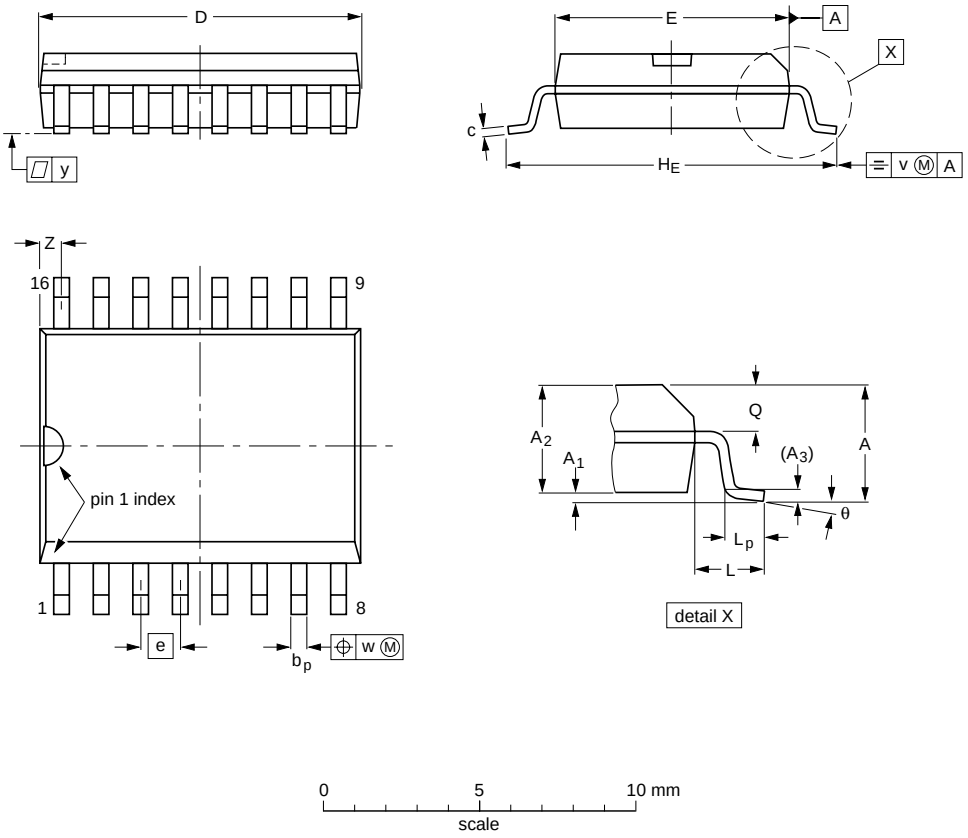
Under certain circumstances, some external CIDCW test equipment may generate incorrect pulses after the ringing signal becomes inactive. These pulses may cause the FSK detector of the PCD3316 to respond. Note that this is by no means an incorrect behaviour of the PCD3316 chip, but a correct detection of incorrect test stimuli. However, if not known, it may lead to confusing results during testing of the CPE.

To avoid the issue described above, following work-around can be used:

1. Disable the FSK detection of PCD3316, before and during the ringing signal detection.
2. Switch on the FSK detection only after a certain period, e.g. 100 ms after the ringing signal goes inactive.
3. When the first FSK data is detected, e.g ‘55H’ (possible part of channel seizure), switch off the FSK detection and on again. This will force the FSK detector to resynchronize and detect the normal FSK data correctly. It may be necessary to repeat this sequence a number of times to ensure that the data detected really comes from the channel seizure. Thus, it is recommended to wait for a multiple number of bytes ‘55H’ to be detected to validate a correct channel seizure.

## 12. Package outline

**SO16: plastic small outline package; 16 leads; body width 7.5 mm** **SOT162-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.30<br>0.10 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 10.5<br>10.1 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | $8^o$<br>$0^o$ |
| inches | 0.10 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.41<br>0.40 | 0.30<br>0.29 | 0.050 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT162-1 | 075E03 | MS-013AA | | | | ~~95-01-24~~<br>97-05-22 |

**Fig 17. SOT162-1.**

# 13. Soldering

## 13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

## 13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

## 13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

## 13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## 13.5 Package related soldering information

**Table 19: Suitability of surface mount IC packages for wave and reflow soldering methods**

| Package | Soldering method | |
|---|---|---|
| | Wave | Reflow [1] |
| BGA, SQFP | not suitable | suitable |
| HLQFP, HSQFP, HSOP, HTSSOP, SMS | not suitable [2] | suitable |
| PLCC, SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended [3] [4] | suitable |
| SSOP, TSSOP, VSO | not recommended [5] | suitable |

[1] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[2] These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

[3] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[4] Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[5] Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

## 14. Revision history

| Rev | Date | CPCN | Description |
|---|---|---|---|
| 01 | 990311 | - | **This data sheet supersedes the version of 1998 May 14 (9397 750 03525):**<br>• The format of this specification has been redesigned to comply with Philips Semiconductors' new presentation and information standard<br>• Section 1 "General description" on page 1: reference to application note AN98701 added<br>• Section 7.6 "Level detect" on page 7: Added text regarding the frequency band for signal power measurement<br>• Section 7.10 "3.58 MHz oscillator circuitry" on page 8: recommended resonator indication removed<br>• Section 7.13 "Registers" on page 15: new register presentation in this section<br>• Table 14 " Description of CIDMD1 bits" on page 17: Description of bit CIDMD1.6 and CIDMD1.5 adjusted<br>• Application diagram Figure 16a on page 23: diodes removed<br>• Added Section 11.1 "Application note on Customer Premises Equipment (CPE) testing" on page 23. |

## Data sheet status

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|---|---|---|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

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# Contents


| | | |
|---|---|---|
| **1** | **General description** | 1 |
| **2** | **Features** | 2 |
| **3** | **Applications** | 2 |
| **4** | **Ordering information** | 2 |
| **5** | **Block diagram** | 3 |
| **6** | **Pinning information** | 3 |
| 6.1 | Pinning | 3 |
| 6.2 | Pin description | 4 |
| **7** | **Functional description** | 4 |
| 7.1 | Preprocessor and analog inputs | 4 |
| 7.2 | CAS detection | 5 |
| 7.3 | FSK reception | 5 |
| 7.4 | Ring or polarity change detector | 6 |
| 7.5 | Low battery detection | 6 |
| 7.6 | Level detect | 7 |
| 7.7 | Time base | 7 |
| 7.8 | Interrupt | 7 |
| 7.9 | The internal Power-on reset (POR) | 8 |
| 7.10 | 3.58 MHz oscillator circuitry | 8 |
| 7.11 | 32 kHz oscillator | 10 |
| 7.12 | Serial interface | 10 |
| 7.12.1 | Characteristics of the $I^2C$-bus | 10 |
| 7.12.2 | START and STOP conditions | 11 |
| 7.12.3 | Bit transfer | 11 |
| 7.12.4 | Acknowledge | 11 |
| 7.12.5 | $I^2C$-bus protocol | 12 |
| 7.12.6 | $I^2C$-bus bit rate | 14 |
| 7.13 | Registers | 15 |
| 7.13.1 | Interrupt register (CIDINT) | 15 |
| 7.13.2 | FSK data register (CDFSK) | 16 |
| 7.13.3 | Status register (CIDSTA) | 16 |
| 7.13.4 | Ringer period register (CIDRNG) | 16 |
| 7.13.5 | Mode register 1 (CIDMD1) | 17 |
| 7.13.6 | Mode register 2 (CIDMD2) | 17 |
| **8** | **Limiting values** | 18 |
| **9** | **Characteristics** | 18 |
| **10** | **Application information** | 22 |
| **11** | **Test information** | 23 |
| 11.1 | Application note on Customer Premises Equipment (CPE) testing | 23 |
| **12** | **Package outline** | 24 |
| **13** | **Soldering** | 25 |
| 13.1 | Introduction to soldering surface mount packages | 25 |
| 13.2 | Reflow soldering | 25 |
| 13.3 | Wave soldering | 25 |
| 13.4 | Manual soldering | 26 |
| 13.5 | Package related soldering information | 26 |
| **14** | **Revision history** | 27 |




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