

User's Manual

V854™

32/16-Bit Single-Chip Microcontroller

Hardware

μPD703006

μPD703008

μPD70F3008

μPD703008Y

μPD70F3008Y

[MEMO]

① **PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② **HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ **STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Major Revisions in This Edition

Page	Contents
Throughout	Deletion of BV _{DD} and BV _{SS} Modification of voltage of V _{PP} Addition of μ PD703006 to the target devices
p.44	Modification of description in 2.3 (19) MODE0 to MODE2 (Mode 0 to 2)
p.47	Modification of recommended connection method for pins P40/AD0 to P47/AD7, P50/AD8 to P57/AD15, P60/A16 to P67/A23, P90/LBEN/WRL, P91/UBEN, P92/R/W/WRH, P93/DSTB/RD, P94/ASTB, P95/HLDAK, P96/HLDRQ, WAIT, and MODE0 to MODE2 in 2.4 Pin I/O Circuit Type and Connection of Unused Pins
p.53	Modification of description of EP flag in Figure 3-3 Program Status Word (PSW)
p.54	Modification of description in 3.3.2 Specifying operation mode
p.140	Addition of Caution in 6.5.1 (2) IDLE mode
p.140	Modification of description in 6.5.1 (3) (a) PLL mode
p.140	Modification of description in 6.5.1 (3) (b) Direct mode
p.142	Modification of description of CESEL bit in 6.5.2 (1) Power save control register (PSC)
p.149	Modification of description in 6.6 (1) Securing time using internal time base counter (NMI pin input)
p.150	Modification of description in 6.6 (2) Securing time by signal level width (RESET pin input)
p.159	Addition of Note in 7.2 (1) Timer 0 (24-bit timer/event counter)
p.161	Addition of description in 7.2.1 (1) Timers 0, 0L (TM0, TM0L)
p.206	Addition to the item Transfer rate in 8.2.1 Features
p.220	Addition to the item High transfer speed in 8.3.1 Features
p.241	Addition of Note to bits 4 and 5 in 8.4.4 (3) IIC clock selection register (IICCL)
p.242	Addition of Caution to 8.4.4 (4) IIC shift register (IIC)
p.276	Addition of 8.4.6 (15) (b) Operation during communication reservation (when a multi-master is used), (c) Start operation after communication reservation (when a multi-master is used), and (d) STT setting timing (when a multi-master is used)
p.299	Modification of description of function of bits FR2 to FR0 in the table in 9.3 (2) A/D converter mode register 1 (ADM1)
p.301	Modification of setting value of ADM1 register in the table of operation and trigger modes in 9.4.2 Operation mode and trigger mode
pp.308 to 310, 312 to 318	Addition of Tables 9-1 to 9-9 and Figures 9-6 to 9-14
p.319	Modification of description in 9.8.2 Interval of the external/timer trigger
p.379	Addition of description in 13.2 (2) Power-ON reset
p.380	Modification of initial values after reset of timer registers (TM0, TM1, TM0L, TM1L, TM20 to TM24, TM3) in Table 13-2 Initial Values after Reset of Each Register (1/2)
p.384	Deletion of CSI2 in 14.3 Programming Environment
p.385	Deletion of CSI2, SO2, SI2, and $\overline{\text{SCK2}}$ in 14.4 Communication System
p.388	Deletion of CSI2 and the pin used by CSI2 in the table of pins used by each serial interface in 14.5.2 Serial interface pin
p.392	Deletion of CSI2 in Table 14-1 List of Communication Systems
p.393	Modification of the table of flash memory control commands in 14.6.4 Communication command

The mark ★ shows major revised points in this edition.

INTRODUCTION

Readers This manual is intended for users who understand the functions of the V854 (μ PD703006, 703008, 70F3008, 703008Y, 70F3008Y) and design application systems using the V854.

Purpose This manual is intended to enable users to understand the hardware functions described in the Organization below.

Organization The V854 User's Manual is divided into two parts: hardware (this manual) and architecture (V850 Family™ Architecture User's Manual) manuals.

Hardware	Architecture
<ul style="list-style-type: none">• Pin function• CPU function• Internal peripheral function• Flash memory programming mode	<ul style="list-style-type: none">• Data type• Register set• Instruction format and instruction set• Interrupt and exception• Pipeline operation

How to Read This Manual It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- To find out the details of a register whose the name is known:
→ Refer to **APPENDIX A REGISTER INDEX**.
- To find out the details of a function whose name is known:
→ Refer to **APPENDIX C INDEX**.
- To understand the details of an instruction function:
→ Refer to the **V850 Family Architecture User's Manual** available separately.
- To understand the overall functions of the V854:
→ Read this manual according to the Table of Contents.

Conventions	Data significance:	Higher digits on the left and lower digits on the right
	Active low:	$\overline{\text{xxx}}$ (overscore over pin or signal name)
	Memory map address:	High order at high stage and low order at low stage
	Note:	Footnote for items marked with Note in the text
	Caution:	Information requiring particular attention
	Remark:	Supplementary information
	Number representation:	Binary ... xxxx or xxxxB Decimal ... xxxx Hexadecimal ... xxxxH
	Prefixes indicating power of 2 (address space, memory capacity):	K (kilo): $2^{10} = 1024$ M (mega): $2^{20} = 1024^2$ G (giga): $2^{30} = 1024^3$

Related documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

• Documents related to devices

Document Name	Document No.
V850 Family Architecture User's Manual	U10243E
V850 Family Instruction Table	U10229E
μPD703008 Data Sheet	To be prepared
μPD703008Y Data Sheet	To be prepared
μPD70F3008 Data Sheet	U12756E
μPD70F3008Y Data Sheet	U12755E
V854 Hardware User's Manual	This manual

• Documents related to development tools (User's Manual)

Document Name		Document No.
IE-703002-MC (In-circuit emulator)		U11595E
IE-703008-MC-EM1 (In-circuit emulator option board)		U12420E
CA850 (C Compiler Package)	Operation (UNIX™ based)	U12839E
	Operation (Windows™ based)	U12827E
	C Language	U12840E
	Assembly Language	U10543E
ID850 (Ver.1.31) (Integrated Debugger)	Operation Windows based	U13716E
RX850 (Real Time OS)	Basics	U13430E
	Technical	U13431E
	Installation	U13410E
RX850 Pro (Real Time OS)	Fundamental	U13773E
	Technical	U13772E
	Installation	U13774E
RD850 (Task Debugger) ^{Note}		U11158E
RD850 (Ver.3.0) (Task Debugger)		U13737E
AZ850 (System Performance Analyzer)		U11181E
SM850 (Ver.2.0) (System Simulator) Operation Windows based.		Under preparation

Note Supports ID850 (Ver.1.31)

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[MEMO]

CHAPTER 1 INTRODUCTION

The V854 is a product of NEC's V850 Family single-chip microcontrollers for real-time control applications. This chapter briefly outlines the V854.

1.1 General

The V854 is a 32-/16-bit single-chip microcontroller that employs the CPU core of the V850 Family of high-performance 32-bit single-chip microcontrollers for real-time control applications, and integrates peripheral functions such as ROM/RAM, real-time pulse unit, serial interface, A/D converter, and PWM.

The V854 is provided with multiplication instructions that are executed with a hardware multiplier, saturated operation instructions, and bit manipulation instructions that are ideal for digital servo control applications, in addition to the basic instructions that have a high real-time response speed and can be executed in 1 clock cycle. This microcontroller can be employed for many applications including real-time control systems such as AV applications including digital still cameras and camera built-in VCRs; communication applications including portable telephones and portable information terminals. In any of these applications, the V854 demonstrates an extremely high cost effectiveness. Especially, the real-time pulse unit that can realize VCR software servo control is provided; therefore, the system/servo/camera control of camera built-in VCR is realized by one chip.

1.2 Features

- Number of instructions : 74
- Minimum instruction execution time : 30 ns (at internal 33 MHz)
- General register : 32 bits x 32
- Instruction set : Signed multiply (16 bits x 16 bits → 32 bits): 1 to 2 clocks
Saturated operation instructions (with overflow/underflow detection function)
32-bit shift instructions: 1 clock
Bit manipulation instructions
Load/store instructions with long/short format
- Memory space : 16 Mbytes linear address space (common program/data)
Memory block division function: 2 Mbytes/block
Programmable wait function
Idle state insertion function
- External bus interface : 16-bit data bus (address/data multiplexed)
Bus hold function
External wait function

★ ○ Internal memory

Part Number	Internal ROM	Internal RAM
μPD703006	None	4 Kbytes
μPD703008, 703008Y	128 K (Mask ROM)	4 Kbytes
μPD70F3008, 70F3008Y	128 K (Flash memory)	4 Kbytes

- Interrupt/exception : External interrupt: 22 (including NMI)
Internal interrupt : 31 sources
Exception : 1 source
Eight levels of priorities can be set.

- I/O line : Input port: 16
I/O port : 96

- Real-time pulse unit : 24-bit timer/event counter: 2 ch
16-bit interval timer: 6 ch

- Serial interface : Asynchronous serial interface (UART)
Synchronous or clocked serial interface (CSI)
I²C bus interface (I²C) (μPD703008Y and 70F3008Y only)
UART/CSI: 1 ch
CSI: 2 ch
CSI/I²C: 1 ch
Dedicated baud rate generator: 4 ch

- PWM (Pulse Width Modulation) : 12- to 16-bit resolution PWM: 4 ch
- A/D converter : 8-bit resolution A/D converter: 16 ch
- Clock generator : Multiplication function by PLL clock synthesizer (multiplication by one or five)
2-frequency division function by external clock
- Power save function : HALT/IDLE/software STOP mode
Clock output stop function
- Package : 144-pin plastic LQFP: pin pitch: 0.5 mm
- CMOS technology : Complete static circuit

1.3 Application Fields

- System/servo/camera control of camera built-in VCRs, etc.
- Portable cameras such as digital still cameras, etc.
- Portable telephones and portable information terminals, etc.

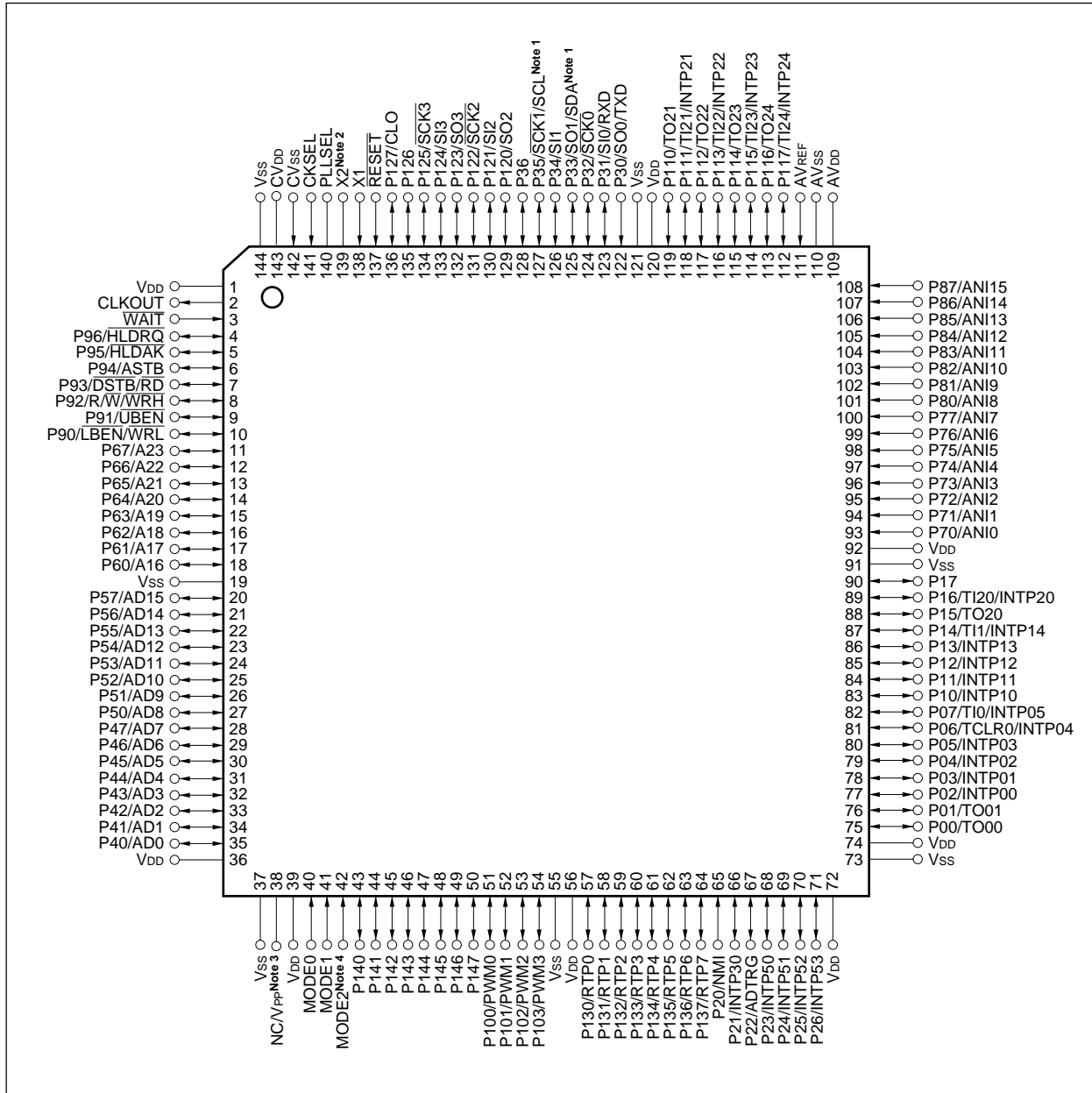
★ 1.4 Ordering Information

Part number	Package	Internal ROM
μ PD703006GJ-33-8EU	144-pin plastic LQFP (fine pitch) (20 × 20 mm)	None
μ PD703008GJ-25-xxx-8EU	144-pin plastic LQFP (fine pitch) (20 × 20 mm)	Mask ROM
μ PD703008YGJ-25-xxx-8EU	144-pin plastic LQFP (fine pitch) (20 × 20 mm)	Mask ROM
μ PD703008YGJ-33-xxx-8EU	144-pin plastic LQFP (fine pitch) (20 × 20 mm)	Mask ROM
μ PD70F3008GJ-16-8EU ^{Note}	144-pin plastic LQFP (fine pitch) (20 × 20 mm)	Flash memory
μ PD70F3008YGJ-16-8EU ^{Note}	144-pin plastic LQFP (fine pitch) (20 × 20 mm)	Flash memory

Note Under development

Remark xxx indicates ROM code suffix.

★ 1.5 Pin Identification (Top View)

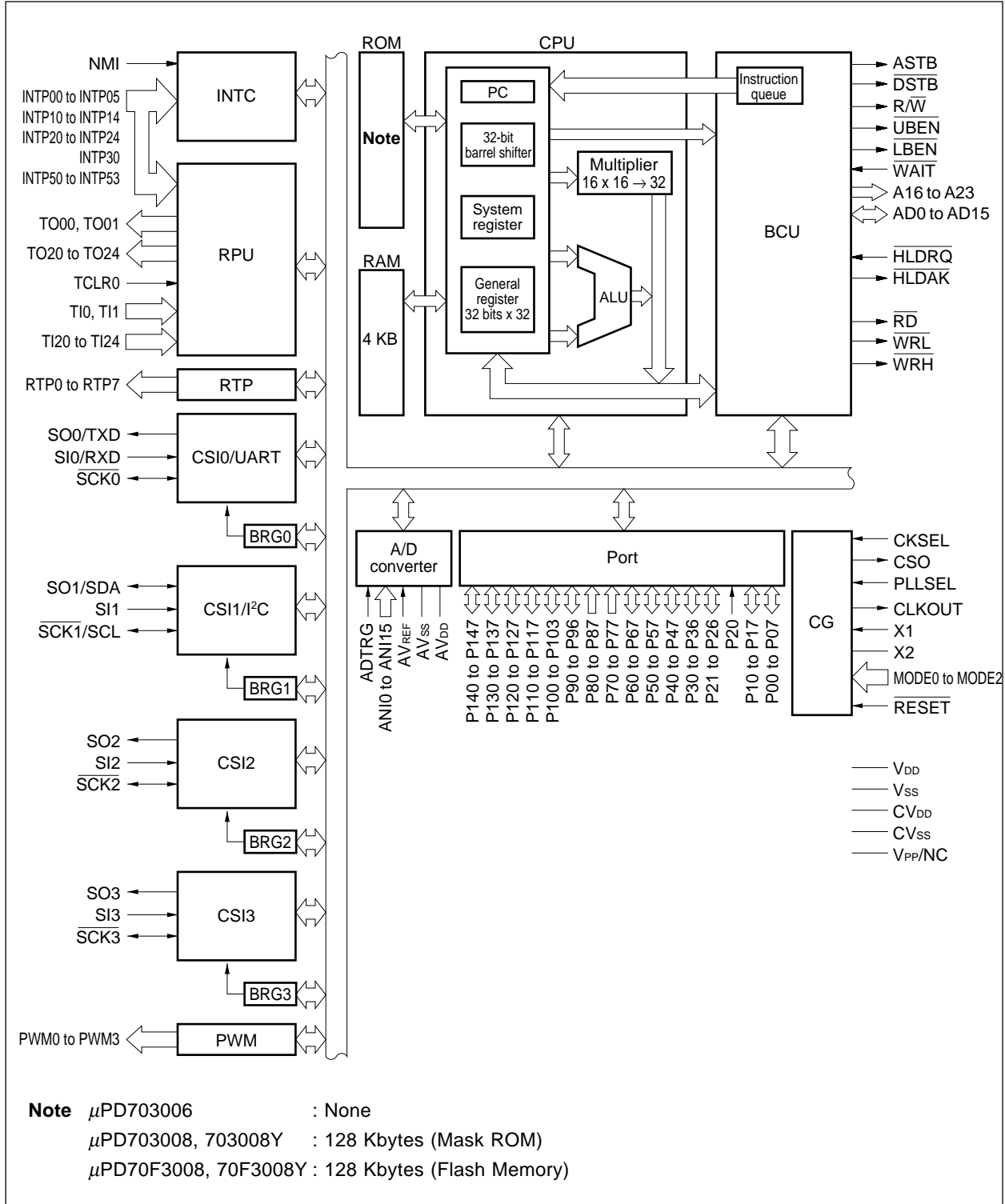


- Notes**
1. SCL and SDA are available only for μ PD703008Y and 70F3008Y.
 2. Leave open when external clock is connected to X1 pin.
 3. μ PD703006, 703008, 703008Y : NC
 μ PD70F3008, 70F3008Y : V_{PP} (Connect to V_{SS} via a resistor (R_{VPP}) in normal operating mode)
 4. Connect directly to V_{SS} in the normal operation mode.

Pin name		P00 to P07	: Port0
		P10 to P17	: Port1
A16 to A23	: Address Bus	P20 to P26	: Port2
AD0 to AD15	: Address/Data Bus	P30 to P36	: Port3
ADTRG	: AD Trigger Input	P40 to P47	: Port4
ANI0 to ANI15	: Analog Input	P50 to P57	: Port5
ASTB	: Address Strobe	P60 to P67	: Port6
AV _{DD}	: Analog V _{DD}	P70 to P77	: Port7
AV _{REF}	: Analog Reference Voltage	P80 to P87	: Port8
AV _{SS}	: Analog V _{SS}	P90 to P96	: Port9
CKSEL	: Clock Select	P100 to P103	: Port10
CLKOUT	: Clock Output	P110 to P117	: Port11
CLO	: Clock Output (Divided)	P120 to P127	: Port12
CV _{DD}	: Power Supply for Clock Generator	P130 to P137	: Port13
CV _{SS}	: Ground for Clock Generator	P140 to P147	: Port14
<u>DSTB</u>	: Data Strobe	PLLSEL	: PLL Select
<u>HLDAK</u>	: Hold Acknowledge	PWM0 to PWM3	: Pulse Width Modulation
<u>HLDRQ</u>	: Hold Request	<u>RD</u>	: Read
INTP00 to	: Interrupt Request from Peripherals	RESET	: Reset
INTP05,		RTP0 to RTP7	: Real-time Port
INTP10 to		R/ <u>W</u>	: Read/Write Status
INTP14,		RXD	: Receive Data
INTP20 to		<u>SCK0</u> to <u>SCK3</u>	: Serial Clock
INTP24,		SCL	: Serial Clock
INTP30,		SDA	: Serial Data
INTP50 to		SI0 to SI3	: Serial Input
INTP53		SO0 to SO3	: Serial Output
<u>LBEN</u>	: Lower Byte Enable	TCLR0	: Timer Clear
MODE0 to	: Mode	TI0, TI1,	: Timer Input
MODE2		TI20 to TI24	
NC	: No Connection	TO00, TO01,	: Timer Output
NMI	: Non-maskable Interrupt Request	TO20 to TO24	
		TXD	: Transmit Data
		<u>UBEN</u>	: Upper Byte Enable
		V _{DD}	: Power Supply
		V _{PP}	: Programming Power Supply
		V _{SS}	: Ground
		<u>WAIT</u>	: Wait
		<u>WRH</u>	: Write Strobe High Level Data
		<u>WRL</u>	: Write Strobe Low Level Data
		X1, X2	: Crystal

1.6 Function Block Configuration

★ 1.6.1 Internal block diagram



1.6.2 Internal units

(1) CPU

Executes almost all instruction processing such as address calculation, arithmetic/logic operation, and data transfer in 1 clock by using a 5-stage pipeline.

Dedicated hardware devices such as a multiplier (16 bits × 16 bits → 32 bits) and a barrel shifter (32 bits) are provided to increase the speed of processing complicated instructions.

- ★ **(2) Bus control unit (BCU)**
Initiates the necessary number of external bus cycles based on the physical address obtained by the CPU. If the CPU does not issue a request to start a bus cycle when an instruction is fetched from external memory area, it generates a prefetch address to prefetch an instruction code. The prefetched instruction code is loaded into the internal instruction queue.

- ★ **(3) Internal ROM**
The μ PD703008 and 703008Y incorporate mask ROM (128 Kbytes) and the μ PD70F3008 and 70F3008Y incorporate flash memory (128 Kbytes). They are each mapped starting from address 00000000H. The μ PD703006 does not contain internal ROM.
Access is enabled/disabled by the MODE0 to MODE2 pins. With the internal flash memory device, the programming mode is specified by these two pins.
This internal ROM is accessed in 1 clock by the CPU when an instruction is fetched.

- (4) Internal RAM**
4 Kbytes RAM is mapped starting from address FFFFE000H. This RAM can be accessed in 1 clock by the CPU when data is accessed.

- (5) Interrupt controller (INTC)**
Processes interrupt requests (NMI, INTP00 to INTP05, INTP10 to INTP14, INTP20 to INTP24, INTP30, and INTP50 to INTP53) from the internal peripheral hardware and external sources. Eight levels of priorities can be specified for these interrupt requests, and multiplexed processing control can be performed on an interrupt source.

- (6) Clock generator (CG)**
By the internal PLL, supplies the CPU clock whose frequency is five times, one time (when internal PLL is used), or 1/2 times (when internal PLL is not used) the frequency of the oscillator connected across the X1 and X2 pins. Input from an external clock source can also be referenced instead of using the oscillator.

- (7) Real-time pulse unit (RPU)**
Provides two 24-bit timer/event counter channels, six 16-bit interval timer channels, and capabilities for measuring pulse width and generation of programmable pulse outputs.

- (8) Serial interface (SIO)**
The serial interface consists of 4 channels in total of asynchronous serial interfaces (UART) and synchronous or clocked serial interfaces (CSI). One of these channels can be switched between UART and CSI, one channel can be switched between CSI and I²C (μ PD703008Y and 70F3008Y only), and the other two channels are fixed to CSI.
UART transfers data by using the TXD and RXD pins.
CSI transfers data by using the SO, SI, and $\overline{\text{SCK}}$ pins.
I²C transfers data by using the SDA and SCL pins.
The serial clock source can be selected from the baud rate generator output and system clock.

(9) Ports

The ports have functions as general ports and functions as control pins as shown below.

Port	I/O	Port Function	Control Function
Port0	8-bit I/O	General port	Timer I/O, external interrupt
Port1			
Port2	1-bit input, 6-bit I/O		NMI, A/D converter trigger, external interrupt
Port3	7-bit I/O		Serial interface
Port4	8-bit I/O		External address/data bus
Port5			
Port6			External address bus
Port7	8-bit input		A/D converter analog input
Port8			
Port9	7-bit I/O		External bus interface control signal I/O
Port10	4-bit I/O		PWM output
Port11	8-bit I/O		Timer I/O, external interrupt
Port12			Serial interface
Port13			Real time output port
Port14			—

(10) PWM (Pulse Width Modulation)

The V854 is provided with four channels of PWM signal output for which the 12- to 16-bit resolutions can be selected. The PWM output can be used as a D/A converter output by connecting an external low pass filter. It is suitable for controlling the actuator of motors, etc.

(11) A/D converter

This is a high speed, high resolution 8-bit A/D converter with 16 analog input pins. Converts with a sequential conversion method.

(12) RTP

Real time output function which transfers the 8-bit data previously set to output latch with the coincidence signal of compare register. RTP can output data to port at the accurate timing specified with timer.

CHAPTER 2 PIN FUNCTIONS

The following table shows the names and functions of the V854's pins. These pins can be divided by function into port pins and other pins.

2.1 Pin Function List

(1) Port pins

(1/2)

Pin Name	I/O	Function	Alternate Function
P00	I/O	Port 0. 8-bit I/O port. Can be specified in input/output mode in 1-bit units.	TO00
P01			TO01
P02			INTP00
P03			INTP01
P04			INTP02
P05			INTP03
P06			TCLR0/INTP04
P07			TI0/INTP05
P10	I/O	Port 1. 8-bit I/O port. Can be specified in input/output mode in 1-bit units.	INTP10
P11			INTP11
P12			INTP12
P13			INTP13
P14			TI1/INTP14
P15			TO20
P16			TI20/INTP20
P17			—
P20	Input	Port 2. P20 is input-only port. This pin operates as NMI input when valid edge is input. Bit 0 in P2 register signifies NMI input state. P21 to P26 are 6-bit input/output port pins. Can be specified in input/output mode in 1-bit units.	NMI
P21	I/O		INTP30
P22			ADTRG
P23			INTP50
P24			INTP51
P25			INTP52
P26			INTP53
P30	I/O	Port 3. 7-bit I/O port. Can be specified in input/output mode in 1-bit units.	SO0/TXD
P31			SI0/RXD
P32			$\overline{\text{SCK0}}$
P33			SO1/SDA
P34			SI1
P35			$\overline{\text{SCK1/SCL}}$
P36			—
P40 to P47	I/O	Port 4. 8-bit I/O port. Can be specified in input/output mode in 1-bit units.	AD0 to AD7

(2/2)

Pin Name	I/O	Function	Alternate Function
P50 to P57	I/O	Port 5. 8-bit I/O port. Can be specified in input/output mode in 1-bit units.	AD8 to AD15
P60 to P67	I/O	Port 6. 8-bit I/O port. Can be specified in input/output mode in 1-bit units.	A16 to A23
P70 to P77	Input	Port 7. 8-bit input only port.	ANI0 to ANI7
P80 to P87	Input	Port 8. 8-bit input only port.	ANI8 to ANI15
P90	I/O	Port 9. 7-bit I/O port. Can be specified in input/output mode in 1-bit units.	$\overline{\text{LBEN}}/\overline{\text{WRL}}$
P91			$\overline{\text{UBEN}}$
P92			$\overline{\text{R/W}}/\overline{\text{WRH}}$
P93			$\overline{\text{DSTB}}/\overline{\text{RD}}$
P94			ASTB
P95			$\overline{\text{HLD AK}}$
P96			$\overline{\text{HLD RQ}}$
P100	I/O	Port 10. 4-bit I/O port. Can be specified in input/output mode in 1-bit units.	PWM0
P101			PWM1
P102			PWM2
P103			PWM3
P110	I/O	Port 11. 8-bit I/O port. Can be specified in input/output mode in 1-bit units.	TO21
P111			TI21/INTP21
P112			TO22
P113			TI22/INTP22
P114			TO23
P115			TI23/INTP23
P116			TO24
P117			TI24/INTP24
P120	I/O	Port 12. 8-bit I/O port. Can be specified in input/output mode in 1-bit units.	SO2
P121			SI2
P122			$\overline{\text{SCK2}}$
P123			SO3
P124			SI3
P125			$\overline{\text{SCK3}}$
P126			—
P127			CLO
P130 to P137	I/O	Port 13. 8-bit I/O port. Can be specified in input/output mode in 1-bit units.	RTP0 to RTP7
P140 to P147	I/O	Port 14. 8-bit I/O port. Can be specified in input/output mode in 1-bit units.	—

(2) Pins other than port pins

(1/3)

Pin Name	I/O	Function	Alternate Function
TO00	Output	Pulse signal output from timer 0 and 2.	P00
TO01			P01
TO20			P15
TO21			P110
TO22			P112
TO23			P114
TO24			P116
TCLR0	Input	External clear signal input to timer 0.	P06/INTP04
TI0	Input	External count clock input to timer 0, 1, and 2.	P07/INTP05
TI1			P14/INTP14
TI20			P16/INTP20
TI21			P111/INTP21
TI22			P113/INTP22
TI23			P115/INTP23
TI24			P117/INTP24
INTP00 to INTP03	Input	External capture trigger input to timer 0. Also used to input external maskable interrupt request.	P02 to P05
INTP04	Input	External maskable interrupt request input.	P06/TCLR0
INTP05			P07/TI0
INTP10 to INTP13	Input	External capture trigger input to timer 1. Also used to input external maskable interrupt request.	P10 to P13
INTP14	Input	External maskable interrupt request input.	P14/TI1
INTP20	Input	External maskable interrupt request input.	P16/TI20
INTP21			P111/TI21
INTP22			P113/TI22
INTP23			P115/TI23
INTP24			P117/TI24
INTP30	Input	External capture trigger input to timer 3. Also used to input external maskable interrupt request.	P21
INTP50 to INTP53	Input	External maskable interrupt request input.	P23 to P26
NMI	Input	Non-maskable interrupt request input.	P20

(2/3)

Pin Name	I/O	Function	Alternate Function
SO0	Output	Serial transmit data output from CSI0 to CSI3 (3-wire).	P30/TXD
SO1			P33/SDA
SO2			P120
SO3			P123
SI0	Input	Serial receive data input to CSI0 to CSI3 (3-wire).	P31/RXD
SI1			P34
SI2			P121
SI3			P124
$\overline{\text{SCK0}}$	I/O	Serial clock I/O from/to CSI0 to CSI3 (3-wire).	P32
$\overline{\text{SCK1}}$			P35/SCL
$\overline{\text{SCK2}}$			P122
$\overline{\text{SCK3}}$			P125
SDA	I/O	Serial transmit/receive data I/O from/to I ² C.	P33/SO1
SCL		Serial clock I/O from/to I ² C.	P35/ $\overline{\text{SCK1}}$
TXD	Output	Serial transmit data output from UART.	P30/SO0
RXD	Input	Serial receive data input to UART.	P31/SI0
PWM0 to PWM3	Output	Pulse signal output from PWM.	P100 to P103
AD0 to AD7	I/O	16-bit multiplexed address/data bus when external memory is used.	P40 to P47
AD8 to AD15			P50 to P57
A16 to A19	Output	Higher address bus when external memory is used.	P60 to P67
$\overline{\text{LBEN}}$	Output	Lower byte enable signal output of external data bus.	P90/ $\overline{\text{WRL}}$
$\overline{\text{UBEN}}$		Higher byte enable signal output of external data bus.	P91
R/ $\overline{\text{W}}$		External read/write status output.	P92/ $\overline{\text{WRH}}$
$\overline{\text{DSTB}}$		External data strobe signal output.	P93/ $\overline{\text{RD}}$
ASTB		External address strobe signal output.	P94
$\overline{\text{HLD\!AK}}$	Output	Bus hold acknowledge output.	P95
$\overline{\text{HLDRQ}}$	Input	Bus hold request input.	P96
$\overline{\text{WRL}}$	Output	Lower byte write strobe signal output to external data bus.	P90/ $\overline{\text{LBEN}}$
$\overline{\text{WRH}}$		Higher byte write strobe signal output to external data bus.	P92/ $\overline{\text{R/\!W}}$
$\overline{\text{RD}}$	Output	Read strobe signal output to external data bus.	P93/ $\overline{\text{DSTB}}$
ANI0 to ANI7	Input	Analog input to A/D converter.	P70 to P77
ANI8 to ANI15			P80 to P87
RTP0 to RTP7	Output	Real time output port.	P130 to P137
CLO	Output	System clock output (with frequency division function).	P127
CKSEL	Input	Input to specify clock generator operation mode.	–
PLLSEL	Input	Input to specify the number of PLL multiplication.	–
CLKOUT	Output	System clock output.	–

(3/3)

Pin Name	I/O	Function	Alternate Function
$\overline{\text{WAIT}}$	Input	Control signal input inserting wait state to bus cycle.	—
MODE0 to MODE2	Input	Specifies operation mode.	—
$\overline{\text{RESET}}$	Input	System reset input.	—
X1	Input	System clock oscillator connecting pins. Supply external clock to X1.	—
X2	—		—
ADTRG	Input	A/D converter external trigger input.	P22
AV _{REF}	Input	Reference voltage input for A/D converter.	—
AV _{DD}	—	Positive power supply for A/D converter.	—
AV _{SS}	—	Ground for A/D converter.	—
CV _{DD}	—	Positive power supply for clock generator.	—
CV _{SS}	—	Ground for clock generator.	—
V _{DD}	—	Positive power supply.	—
V _{SS}	—	Ground.	—
V _{PP}	—	High voltage applying pin for program write/verify. (μPD70F3008, 70F3008Y only)	—
NC	—	Internally unconnected (μPD703006, 703008, 703008Y only)	—

★

2.2 Pin Status

The operating status of each pin in each operation mode is as follows:

Operating Status Pin	Reset	Software STOP Mode	IDLE Mode	Bus Hold	Idle State	HALT Mode
AD0 to AD15	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
A16 to A23	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Retained ^{Note 1}	Retained
$\overline{\text{LBEN}}$, $\overline{\text{UBEN}}$	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Retained ^{Note 1}	Retained
$\overline{\text{R/W}}$	Hi-Z	Hi-Z	Hi-Z	Hi-Z	H	H
$\overline{\text{DSTB}}$, $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, $\overline{\text{RD}}$	Hi-Z	Hi-Z	Hi-Z	Hi-Z	H	H
$\overline{\text{ASTB}}$	Hi-Z	Hi-Z	Hi-Z	Hi-Z	H	H
$\overline{\text{HLDRQ}}$	–	–	–	Operates	Operates	Operates
$\overline{\text{HLDK}}$	Hi-Z	Hi-Z	Hi-Z	L	Operates	Operates
$\overline{\text{WAIT}}$	–	–	–	–	–	–
CLKOUT	Operates ^{Note 2}	L	–	Operates ^{Note 2}	Operates ^{Note 2}	Operates ^{Note 2}

Hi-Z : high-impedance

Retained : Retains status in external bus cycle immediately before

L : low-level output

H : high-level output

– : input not sampled

Notes 1. Undefined immediately after the bus hold end.

2. Low-level output in single chip mode 1, flash memory programming mode, and clock output inhibit mode.

2.3 Pin Function

(1) P00 to P07 (Port0) ... 3-state I/O

These pins constitute an 8-bit I/O port, port 0. They also serve as control signal pins.

P00 to P07 function not only as I/O port pins, but also as the I/O pins of the real-time pulse unit (RPU) and external interrupt request input pins. Each bit of port 0 can be specified in the port or control mode, by using port 0 mode control register (PMC0).

(a) Port mode

P00 to P07 can be set in the input or output mode in 1-bit units by using port 0 mode register (PM0).

(b) Control mode

P00 to P07 can be set in the port or control mode in 1-bit units by the PMC0 register.

(i) TO00, TO01 (Timer Output) ... output

These are pulse signals output pins for timer 0.

(ii) TCLR0 (Timer Clear) ... input

This pin inputs an external clear signal to timer 0.

(iii) TI0 (Timer Input) ... input

This pin inputs an external count clock to timer 0.

(iv) INTP00 to INTP05 (Interrupt Request from Peripherals) ... input

These pins are the external interrupt request input pins.

(2) P10 to P17 (Port 1) ... 3-state I/O

These pins constitute an 8-bit I/O port, port 1, which can be set in the input or output mode in 1-bit units.

P10 to P17 function as ports, as well as RPU inputs/outputs and external interrupt request inputs. In the operation mode, port control can be selected in 1-bit units, and is specified by the port 1 mode control register (PMC1).

(a) Port mode

P10 to P17 can be set in the input or output mode in 1-bit units by using port 1 mode register (PM1).

(b) Control mode

P10 to P17 can be set in the port or control mode in 1-bit units by the PMC1 register.

(i) TO20 (Timer Output) ... output

This is pulse signal output pin for timer 2.

(ii) TI1, TI20 (Timer Input) ... input

These pins are external count clock input pins of timer 1 and timer 2.

(iii) INTP10 to INTP14 (Interrupt Request from Peripherals) ... input

These pins are the external interrupt request input pins and capture trigger input pins of timer 1.

(iv) INTP20 (Interrupt Request from Peripherals) ... input

This pin is the external interrupt request input pin.

(3) P20 to P26 (Port 2) ... 3-state I/O

These pins constitute an I/O port, port 2, which can be set in the input or output mode in 1-bit units, except P20, which is an input only pin. These pins function not only as port pins but also as NMI input, external interrupt request input, and A/D converter external trigger.

Each bit of this port can be specified in the port or control mode by using port 2 mode control register (PMC2).

(a) Port mode

P21 to P26 can be set in the input or output mode in 1-bit units by port 2 mode register (PM2).

P20 is the input-only port and operates as NMI input when a valid edge is input.

(b) Control mode

P21 to P26 can be set in the port or control mode in 1-bit units by the PMC2 register.

P20 is fixed to control mode.

(i) NMI (Non-maskable Interrupt Request) ... input

This is an input pin for the non-maskable interrupt request signal.

(ii) INTP30, INTP50 to INTP53 (Interrupt Request from Peripherals) ... input

These pins are the external interrupt request input pins.

(iii) ADTRG (AD Trigger Input) ... input

This pin is external trigger input pin of A/D converter.

(4) P30 to P36 (Port 3) ... 3-state I/O

These pins constitute an 7-bit I/O port, port 3. They also function as control signal pins. P30 to P36 function not only as I/O port pins but also as serial interface I/O pins in the control mode.

Each bit of port 3 can be specified in the port or control mode in 1-bit units by using port 3 mode control register (PMC3).

(a) Port mode

P30 to P36 can be set in the input or output mode in 1-bit units by port 3 mode register (PM3).

(b) Control mode

P30 to P36 can be set in the port or control mode in 1-bit units by the PMC3 register.

(i) TXD (Transmit Data) ... output

This is a serial transmit data output pin for the UART.

When transmission is disabled: High impedance

When transmission is enabled: High level

(ii) RXD (Receive Data) ... input

This is a serial receive data input pin for the UART.

(iii) SDA (Serial Data)...I/O

This pin is I²C serial receive data I/O pin. Since this pin is open drain output, connect external pull-up resistor. (μ PD703008Y and 70F3008Y only)

(iv) SCL (Serial Clock) ... I/O

This pin is I²C serial clock I/O pin. Since this pin is the open-drain output, connect external pull-up resistor. (μ PD703008Y and 70F3008Y only)

(v) **SO0, SO1 (Serial Output 0, 1) ... output**

These are serial transmit data output pin for the CSI.

Since SO1 is open drain output, connect external pull-up resistor.

(vi) **SI0, SI1 (Serial Input 0, 1) ... input**

These are serial receive data input pin for the CSI.

(vii) **$\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$ (Serial Clock 0, 1) ... 3-state I/O**

These pins input/output the serial clock of CSI.

Since $\overline{\text{SCK1}}$ is open drain output, connect external pull-up resistor to output.

★

(5) **P40 to P47 (Port 4) ... 3-state I/O**

These pins constitute an 8-bit I/O port, port 4. They also form a portion of the address/data bus connected to external memory.

P40 to P47 function not only as I/O port pins but also as time sharing address/data bus pins (AD0 to AD7) in the control mode (external expansion mode) when an external memory is connected.

Operation mode is specified by the mode specification pin (MODE) and the memory expansion mode register (MM).

(a) **Port mode**

P40 to P47 can be set in the input or output port mode in 1-bit units by using port 4 mode register (PM4).

(b) **Control mode (External Expansion Mode)**

P40 to P47 can be specified as AD0 to AD7 by using the MODE pin and MM register.

(i) **AD0 to AD7 (Address/Data 0 to 7) ... 3-state I/O**

These pins constitute a multiplexed address/data bus when the external memory is accessed. They function as the A0 to A7 output pins of a 24-bit address in the address timing (T1 state), and as the lower 8-bit data I/O bus pins of 16-bit data in the data timing (T2, TW, T3).

The output status of these pins changes in synchronization with the rising edge of the clock in each state of the bus cycle. AD0 to AD7 go into a high-impedance state in the idle state (T1).

Since SO1 is open drain output, connect external pull-up resistor to output.

★

(6) **P50 to P57 (Port 5) ... 3-state I/O**

These pins constitute an 8-bit I/O port, port 5. They also form a portion of the address/data bus connected to external memory.

P50 to P57 function not only as I/O port pins but also as multiplexed address/data bus pins (AD8 to AD15) in the control mode (external expansion mode) when an external memory is connected.

Operation mode is specified by the mode specification pin (MODE) and memory expansion mode register (MM).

(a) **Port mode**

P50 to P57 can be set in the input or output port mode in 1-bit units by using port 5 mode register (PM5).

(b) **Control mode (External Expansion Mode)**

P50 to P57 can be specified as AD8 to AD15 by using the MODE pin and MM register.

(i) AD8 to AD15 (Address/Data 8 to 15) ... 3-state I/O

These pins constitute a multiplexed address/data bus when the external memory is accessed. They function as the A8 to A15 output pins of a 24-bit address in the address timing (T1 state), and as the higher 8-bit data I/O bus pins of 16-bit data in the data timing (T2, TW, T3).

The output status of these pins changes in synchronization with the rising of the clock in each state of the bus cycle. AD8 to AD15 go into a high-impedance state in the idle state (Tl).

★ **(7) P60 to P67 (Port 6) ... 3-state I/O**

These pins constitute an 8-bit I/O port, port 6. They also form a portion of the address/data bus connected to external memory.

P60 to P67 function not only as I/O port pins but also as address bus pins (A16 to A23) in the control mode (external expansion mode) when an external memory is connected. This port can be set in the port or control mode in 2-bit units by using mode specification pin (MODE) and memory expansion mode register (MM).

(a) Port mode

P60 to P67 can be set in the input or output port mode in 1-bit units by using port 6 mode register (PM6).

(b) Control mode (External Expansion Mode)

P60 to P67 can be specified as A16 to A23 by using the MODE pin and MM register.

(i) A16 to A23 (Address 16 to 23) ... output

These pins constitute the higher 8 bits of a 24-bit address bus when the external memory is accessed.

The output status of these pins changes in synchronization with the rising edge of the clock in the T1 state. During the idle state (Tl), the address of the bus cycle immediately before entering the idle state is retained.

(8) P70 to P77 (Port 7), P80 to P87 (Port 8) ... input

Port 7 and port 8 each are an 8-bit input-only port whose pins are all fixed to input.

P70 to P77 and P80 to P87 function as input ports, as well as A/D converter analog inputs in the control mode. However, the input port and analog input pin cannot be switched.

(a) Port mode

P70 to P77 and P80 to P87 are dedicated input ports.

(b) Control mode

P70 to P77 also function as ANI0 to ANI7 pins and P80 to P87 also function as ANI8 to ANI15 pins, and cannot be switched.

(i) ANI0 to ANI15 (Analog Input) ... input

These pins are analog input pins to A/D converter.

To prevent erroneous operation due to noise, connect a capacitor between these pins and AV_{SS}. Make sure that voltage other than the range of AV_{SS} and AV_{REF} should not be applied to the input pin used for A/D converter input. If there should be the possibility that noise whose voltage is AV_{REF} or more or noise whose voltage is AV_{SS} or less is generated, clamp the voltage using a diode with small V_F.

★

(9) P90 to P96 (Port 9) ... 3-state I/O

These pins constitute a 7-bit I/O port, port 9, and are also used to output control signals.

P90 to P96 function not only as I/O port pins but also as control signal output pins and bus hold control signal output pins in the control mode (external expansion mode) when an external memory is used.

If port 9 is accessed in 8-bit units, the higher 1-bit is ignored if the access is write, and undefined if the access is read.

Operation mode is specified by the mode specification pin (MODE) and memory expansion mode register (MM).

(a) Port mode

P90 to P96 can be set in the input or output port mode in 1-bit units by using port 9 mode register (PM9).

(b) Control mode (External Expansion Mode)

P90 to P96 can be used to output control signals when so specified by the MODE pin and MM register when an external memory is used.

(i) $\overline{\text{LBEN}}$ (Lower Byte Enable) ... output

This is the lower byte enable signal of the 16-bit external data bus.

This signal changes in synchronization with the rising edge of the clock in the T1 state of the bus cycle. The status of the bus signal remains unchanged in the idle state (TI).

(ii) $\overline{\text{UBEN}}$ (Upper Byte Enable) ... output

This is the upper byte enable signal of the 16-bit external data bus. It becomes active (low) in byte access to an odd address. It becomes inactive (high) in byte access to an even address.

This signal changes in synchronization with the rising of the clock in the T1 state of the bus cycle. The status of the bus signal remains unchanged in the idle state (TI).

Access		$\overline{\text{UBEN}}$	$\overline{\text{LBEN}}$	A0
Word Access		0	0	0
Half-word Access		0	0	0
Byte Access	Even address	1	0	0
	Odd address	0	1	1

(iii) $\overline{\text{R/W}}$ (Read/Write Status) ... output

This is a status signal output pin that indicates whether the bus cycle for external access is a read or write cycle. It goes high in the read cycle and low in the write cycle.

This signal changes in synchronization with the rising edge of the clock in the T1 state of the bus cycle. It goes high in the idle state (TI).

(iv) $\overline{\text{DSTB}}$ (Data Strobe) ... output

This is the access strobe signal of the external data bus.

It becomes active (low) in the T2 or TW state of the bus cycle, and becomes inactive (high) in the idle state (TI).

(v) $\overline{\text{ASTB}}$ (Address Strobe) ... output

This is the latch strobe signal of the external address bus.

It becomes active (low) in synchronization with the falling edge of the clock in the T1 state of the bus cycle, and becomes inactive (high) in synchronization with the falling edge of the clock in the T3 state. It goes high in the idle state (TI).

(vi) $\overline{\text{HLD\!AK}}$ (Hold Acknowledge) ... output

This is an acknowledge signal output pin that indicates that the V854 has set the address bus, data bus, and control bus in the high-impedance state in response to a bus hold request.

As long as this signal is active, the address bus, data bus, and control bus remain in a high impedance state.

(vii) $\overline{\text{HLDRQ}}$ (Hold Request) ... input

This input pin is used by an external device to request that the V854 relinquish control of the address bus, data bus, and control bus. This pin can be input asynchronously with CLKOUT. When this signal becomes active, the V854 sets the address bus, data bus, and control bus in the high-impedance state, after the current bus cycle completes. If there is no current bus activity, the address bus, data bus, and control bus are immediately set to high-impedance. $\overline{\text{HLD\!AK}}$ is then made active and the bus and control lines are released.

(viii) $\overline{\text{WRL}}$ (Write Strobe Low Byte Data) ... output

This is a write strobe signal output pin for the lower byte of the external 16-bit data bus.

(ix) $\overline{\text{WRH}}$ (Write Strobe High Byte Data) ... output

This is a write strobe signal output pin for the upper byte of the external 16-bit data bus.

(x) $\overline{\text{RD}}$ (Read Strobe)... output

This is a read strobe signal output pin for the external 16-bit data bus.

(10) P100 to P103 (Port 10) ... 3-state I/O

Port 10 is a 4-bit I/O port that can be set in the input or output mode in 1-bit units.

In addition to the function as a port, the pins constituting port 10 are used as output of PWM in the control mode.

If port 10 is accessed in 8-bit units, the higher 4-bit is ignored if the access is write, and undefined if the access is read.

(a) Port mode

P100 to P103 can be set in the input or output mode, in 1-bit units, by the port 10 mode register (PM10).

(b) Control mode

P100 to P103 function as output pins for PWM control signals when the function is enabled by the port 10 mode control register (PMC10).

(i) PWM0 to PWM 3 (Pulse Width Modulation 0 to 3) ... output

These are pulse signals output pins for the PWM.

(11) P110 to P117 (Port 11) ... 3-state I/O

Port 11 is an 8-bit I/O port that can be set in the input or output mode in 1-bit units. In addition to the function as a port, the pins constituting port 11 are used as input/output of RPU or external interrupt request input.

(a) Port mode

P110 to P117 can be set in the input or output mode, in 1-bit units, by the port 11 mode register (PM11).

(b) Control mode

P110 to P117 function as input and output pins for timer 2 when the function is enabled by the port 11 mode control register (PMC11).

(i) TO21 to TO24 (Timer Output) ... output

These are pulse signals output pins for timer 2.

(ii) TI21 to TI24 (Timer Input) ... input

This pin inputs an external counter clock to timer 2.

(iii) INTP21 to INTP24 (Interrupt Request from Peripherals) ... input

These pins are the external interrupt request input pins.

(12) P120 to P127 (Port 12) ... 3-state I/O

Port 12 is an 8-bit I/O port that can be set in the input or output mode in 1-bit units. In addition to the function as a port, the pins constituting port 12 are used as serial interface I/O in the control mode.

(a) Port mode

P120 to P127 can be set in the input or output mode, in 1-bit units, by the port 12 mode register (PM12).

(b) Control mode

P120 to P127 function as input and output of serial interface control signal and output of clock signal by setting of port 12 mode control register (PMC12). However, P126 pin functions only as a port.

(i) SO2, SO3 (Serial Output 2, 3) ... output

These are serial transmit data output pins for the CSI.

(ii) SI2, SI3 (Serial Input 2, 3) ... input

These are serial receive data input pins for the CSI.

(iii) $\overline{\text{SCK2}}$, $\overline{\text{SCK3}}$ (Serial Clock 2, 3) ... 3-state I/O

These are the serial clock I/O pins of CSI.

(iv) CLO (Clock Output (Divided)) ... output

This is an output pin for the system clock (with frequency division function).

(13) P130 to P137 (Port 13) ... 3-state I/O

Port 13 is an 8-bit I/O port that can be set in the input or output mode in 1-bit units. In addition to the function as a port, it is used as real-time output port in the control mode.

(a) Port mode

P130 to P137 can be set in the input or output mode, in 1-bit units, by the port 13 mode register (PM13).

(b) Control mode

P130 to P137 function as real-time output port by setting of port 13 mode control register (PMC13).

(i) RTP0 to RTP7 (Real-time Port 0 to 7) ... output

These pins are real-time output port.

(14) P140 to P147 (Port 14) ... 3-state I/O

Port 14 is an 8-bit I/O port that can be set in the input or output mode in 1-bit units. Port 14 functions only as a port.

(15) CKSEL (Clock Select) ... input

This is the input pin that specifies the operation mode of the clock generation circuit. The input value of this pin cannot be changed during normal operation.

CKSEL	Operation Mode
0	PLL mode
1	Direct mode

(16) PLLSEL (PLL Select) ... input

This is the input pin that specifies the number of PLL multiplication in the PLL mode (CKSEL = 0). The input value of this pin cannot be changed during normal operation.

This pin has no function in the direct mode (CKSEL = 1) and should be treated as an unused pin.

PLLSEL	PLL Multiplication
0	Multiplication by 1
1	Multiplication by 5

★ **(17) CLKOUT (Clock Output) ... output**

This pin outputs the system clock, even during reset in the ROM-less mode. In the single-chip mode 1, the CLKOUT signal is not output until the PSC register is set (low level output). However, in the single-chip mode 2, the CLKOUT signal is output.

★ **(18) $\overline{\text{WAIT}}$ (Wait) ... input**

This control signal input pin inserts a data wait state to the bus cycle, and can be activated asynchronously to CLKOUT. This pin is sampled at the falling edge of the clock in the T2 and TW states of the bus cycle. If the set/hold time for the sampling timing is not satisfied, the wait state may not be inserted.

★ **(19) MODE0 to MODE2 (Mode 0 to 2) ... input**

These pins specify the operation mode of the V854. Operation modes are roughly classified as normal operation mode and flash memory programming mode. Normal operation modes are further classified as single-chip mode and ROM-less mode. The input value of these pins cannot be changed during normal operation. For details, refer to **3.3 Operation Modes**.

(a) μ PD703006

MODE2	MODE1	MODE0	Operation Mode	
0	0	0	Normal operation mode	ROM-less mode 1
0	0	1		ROM-less mode 2
Other than above			Setting prohibited	

(b) μ PD703008, 703008Y

MODE2	MODE1	MODE0	Operation Mode	
0	0	0	Normal operation mode	ROM-less mode 1
0	0	1		ROM-less mode 2
0	1	0		Single-chip mode 1
0	1	1		Single-chip mode 2
Other than above			Setting prohibited	

(c) μ PD70F3008, 70F3008Y

MODE2	MODE1	MODE0	Operation Mode	
0	0	0	Normal operation mode	ROM-less mode 1
0	0	1		ROM-less mode 2
0	1	0		Single-chip mode 1
0	1	1		Single-chip mode 2
1	1	1	Flash memory programming mode	
Other than above			Setting prohibited	

(20) $\overline{\text{RESET}}$ (Reset) ... input

The $\overline{\text{RESET}}$ signal is an asynchronous input signal. A valid low-level signal on the $\overline{\text{RESET}}$ pin initiates a system reset, regardless of the clock operation. In addition to normal system initialization/start functions, the $\overline{\text{RESET}}$ signal is also used for exiting processor power save modes (HALT, IDLE, or STOP).

(21) X1, X2 (Crystal) ... input

An oscillator for internal system clock generation is connected across these pins.

An external clock source can also be referenced by connecting the external clock input to the X1 pin and leaving the X2 pin open.

(22) CV_{DD} (Power Supply for Clock Generator)

This pin supplies positive power to the clock generator.

(23) CV_{SS} (Ground for Clock Generator)

This is the ground pin of the clock generator.

(24) V_{DD} (Power Supply)

This pin supplies positive power. Connect all the V_{DD} pins to a positive power supply.

(25) V_{SS} (Ground)

This is a ground pin. Connect all the V_{SS} pins to ground.

(26) AV_{DD} (Analog V_{DD})

Analog power supply pin for A/D converter.

(27) AV_{SS} (Analog V_{SS})

Ground pin for A/D converter.

(28) AV_{REF} (Analog Reference Voltage) ... input

This is a reference voltage input pin for the A/D converter.

(29) V_{PP} (Programming Power Supply)

This pin supplies positive power for the PROM mode.

This is for μ PD70F3008 or 70F3008Y.

(30) NC (No Connection)

This pin is not connected internally.

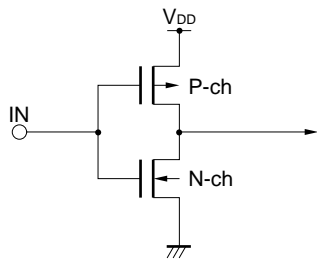
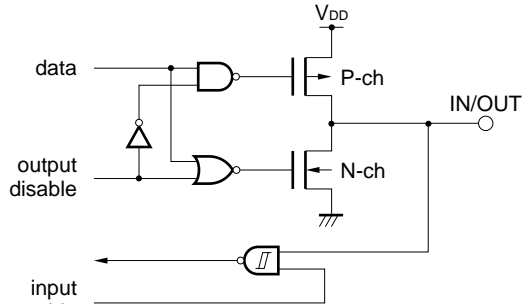
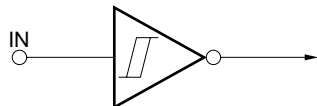
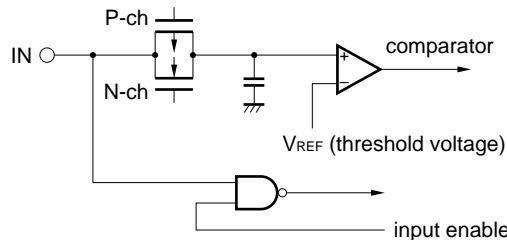
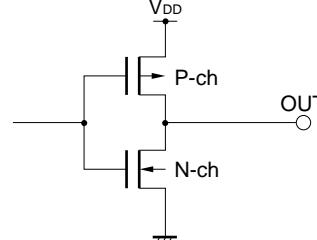
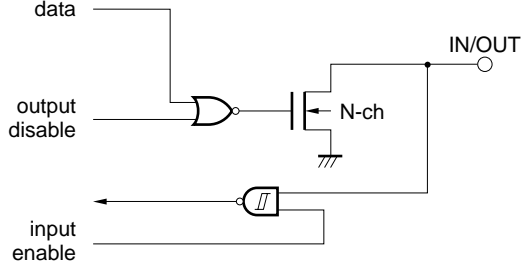
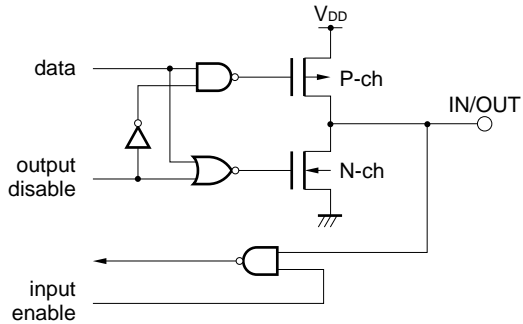
★ This is for the μ PD703006, 703008, and 703008Y.

2.4 Pin I/O Circuit Type and Connection of Unused Pins

When connecting to V_{DD} or V_{SS} via resistor, it is recommended to use 1 to 10-k Ω resistor.

Pin	I/O Circuit Type	Recommended Connection
P00/TO00, P01/TO01	5	Independently connect to V_{DD} or V_{SS} via resistor.
P02/INTP00 to P05/INTP03, P06/TCLR0/INTP04, P07/TI0/INTP05	5-K	
P10/INTP10 to P13/INTP13, P14/TI1/INTP14, P16/TI20/INTP20		
P15/TO20, P17	5	
P20/NMI	2	Connect directly to V_{SS} .
P21/INTP30, P22/ADTRG, P23/INTP50 to P26/INTP53	5-K	Independently connect to V_{DD} or V_{SS} via resistor.
P30/TXD/SO0	5	
P31/RXD/SI0, P32/ $\overline{SCK0}$, P34/SI1	5-K	
P33/SO1/SDA, P35/ $\overline{SCK1}$ /SCL	13-G	
P36	5	
P40/AD0 to P47/AD7	5	Input state: Independently connect to V_{DD} or V_{SS} via resistor. Output state: Leave open.
P50/AD8 to P57/AD15		
P60/A16 to P67/A23		
P70/ANI0 to P77/ANI7	9	Connect directly to V_{SS} .
P80/ANI8 to P87/ANI15		
P90/ \overline{LBEN} /WRL, P91/ \overline{UBEN} , P92/R/W/WRH, P93/DSTB/RD, P94/ASTB, P95/HLDAK, P96/HLDRQ	5	Input state: Independently connect to V_{DD} or V_{SS} via resistor. Output state: Leave open.
P100/PWM0 to P103/PWM3	5	Independently connect to V_{DD} or V_{SS} via resistor.
P110/TO21, P112/TO22, P114/TO23, P116/TO24		
P111/TI21/INTP21, P113/TI22/INTP22, P115/TI23/INTP23, P117/TI24/INTP24	5-K	
P120/SO2	5	
P121/SI2, P122/ $\overline{SCK2}$	5-K	
P123/SO3	5	
P124/SI3, P125/ $\overline{SCK3}$	5-K	
P126, P127/CLO	5	
P130/RTP0 to P137/RTP7		
P140 to P147		
WAIT	1	Connect directly to V_{DD} .
CLKOUT	3	Leave open.
MODE0 to MODE2	2	—
RESET		
AV _{REF} , AV _{SS} , CV _{SS}	—	Connect directly to V_{SS} .
AV _{DD} , CV _{DD}	—	Connect directly to V_{DD} .
PLLSEL	1	Connect directly to V_{DD} or V_{SS} .
CKSEL		
V _{PP} /NC	—	Connect to V_{SS} via resistor (R_{VPP}).

2.5 I/O Circuits of Pins

<p>Type 1</p> 	<p>Type 5-K</p> 
<p>Type 2</p>  <p>Schmitt trigger input with hysteresis characteristics</p>	<p>Type 9</p> 
<p>Type 3</p> 	<p>Type 13-G</p> 
<p>Type 5</p> 	

CHAPTER 3 CPU FUNCTIONS

The CPU of the V854 is based on the RISC architecture and executes most instructions in one clock cycle by using a 5-stage pipeline.

3.1 Features

- Minimum instruction cycle: 30 ns (at internal 33-MHz operation)
- Address space: 16 Mbytes linear
- General registers: Thirty-two 32-bit registers
- Internal 32-bit architecture
- Five-stage pipeline control
- Multiplication/division instructions
- Saturated operation instructions
- Single-clock 32-bit shift instruction
- Long/short instruction format
- Four types of bit manipulation instructions
 - Set
 - Clear
 - Not
 - Test

3.2 CPU Register Set

The registers of the V854 can be classified into two categories: a general-purpose program register set and a dedicated system register set. All the registers are 32 bits wide. For details, refer to **V850 Family User's Manual Architecture**.

Program register set

31		0
r0	Zero Register	
r1	Reserved for Address Generation	
r2	Interrupt Stack Pointer	
r3	Stack Pointer (SP)	
r4	Global Pointer (GP)	
r5	Text Pointer (TP)	
r6		
r7		
r8		
r9		
r10		
r11		
r12		
r13		
r14		
r15		
r16		
r17		
r18		
r19		
r20		
r21		
r22		
r23		
r24		
r25		
r26		
r27		
r28		
r29		
r30	Element Pointer (EP)	
r31	Link Pointer (LP)	
31		0
PC	Program Counter	

System register set

31		0
EIPC	Exception/Interrupt PC	
EIPSW	Exception/Interrupt PSW	
31		0
FEPC	Fatal Error PC	
FEPSW	Fatal Error PSW	
31		0
ECR	Exception Cause Register	
31		0
PSW	Program Status Word	

3.2.1 Program register set

The program register set includes general registers and a program counter.

(1) General registers

Thirty-two general registers, r0 to r31, are available. Any of these registers can be used as a data variable or address variable.

However, r0 and r30 are implicitly used by instructions, and care must be exercised when using these registers. Also, r1 to r5 and r31 are implicitly used by the assembler and C compiler. Therefore, before using these registers, their contents must be saved so that they are not lost. The contents must be restored to the registers after the registers have been used.

Table 3-1. Program Registers

Name	Usage	Operation
r0	Zero register	Always holds 0
r1	Assembler-reserved register	Working register for generating immediate
r2	Interrupt stack pointer	Stack pointer for interrupt handler
r3	Stack pointer	Used to generate stack frame when function is called
r4	Global pointer	Used to access global variable in data area
r5	Text pointer	Register to indicate the start of the text area ^{Note}
r6 to r29	–	Address/data variable registers
r30	Element pointer	Base pointer register when memory is accessed
r31	Link pointer	Used by compiler when calling function
PC	Program counter	Holds instruction address during program execution

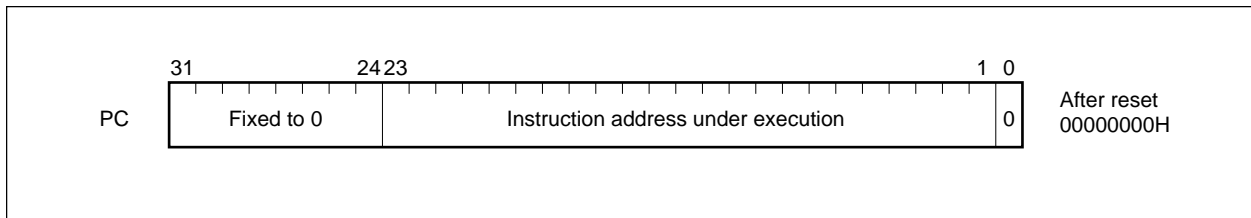
Note Area in which program code is mapped.

(2) Program counter

This register holds the address of the instruction under execution. The lower 24 bits of this register are valid, and bits 31 to 24 are fixed to 0. If a carry occurs from bit 23 to 24, it is ignored.

Bit 0 is fixed to 0, and branching to an odd address cannot be performed.

Figure 3-1. Program Counter (PC)



3.2.2 System register set

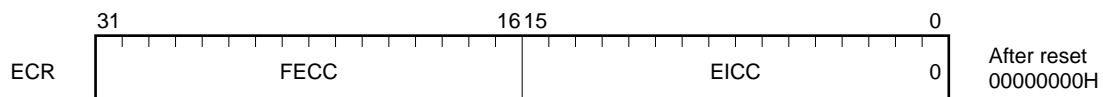
System registers control the status of the CPU and hold interrupt information.

Table 3-2. System Register Numbers

No.	System Register Name	Usage	Operation
0	EIPC	Status saving registers during interrupt	These registers save the PC and PSW when an exception or interrupt occurs. Because only one set of these registers is available, their contents must be saved when multiple interrupts are enabled.
1	EIPSW		
2	FEPC	Status saving registers for NMI	These registers save PC and PSW when NMI occurs.
3	FEPSW		
4	ECR	Interrupt source register	If exception, maskable interrupt, or NMI occurs, this register will contain information referencing the interrupt source. The high-order 16 bits of this register are called FECC, to which exception code of NMI is set. The low-order 16 bits are called EICC, to which exception code of exception/interrupt is set (refer to Figure 3-2).
5	PSW	Program status word	Program status word is collection flags that indicate program status (instruction execution result) and CPU status (refer to Figure 3-3).
6 to 31	Reserved		

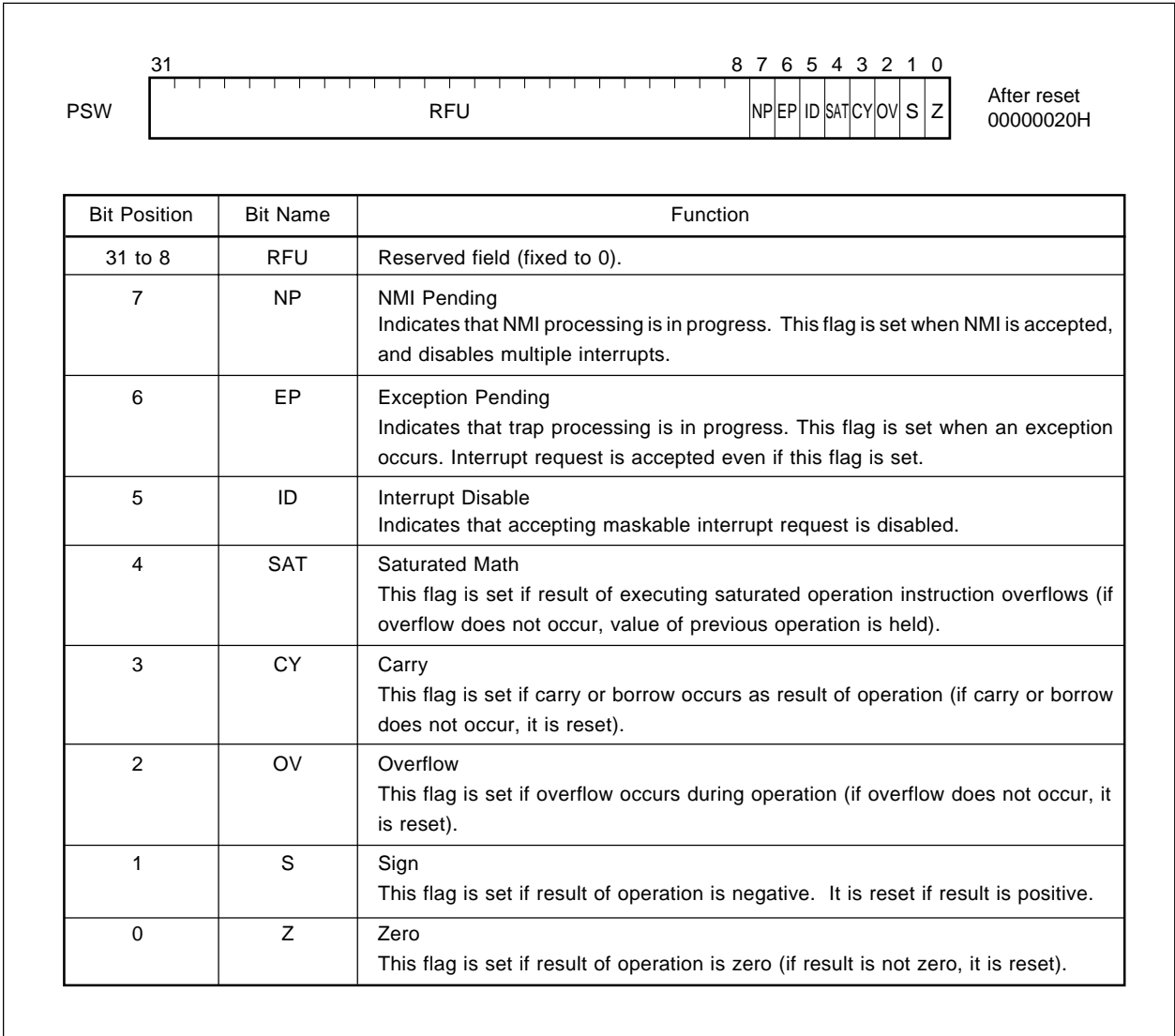
To read/write these system registers, specify a system register number indicated by the system register load/store instruction (LDSR or STSR instruction).

Figure 3-2. Interrupt Source Register (ECR)



Bit Position	Bit Name	Function
31 to 16	FECC	Fatal Error Cause Code Exception code of NMI. (For exception code, refer to Table 5-1 .)
15 to 0	EICC	Exception/Interrupt Cause Code Exception code of exception/interrupt.

Figure 3-3. Program Status Word (PSW)



			Indicates that trap processing is in progress. This flag is set when an exception
--	--	--	---

3.3 Operation Modes

3.3.1 Operation modes

The V854 has the following operations modes. These modes are selected by the MODE pin (n = 0 to 2).

(1) Normal operation modes

(a) Single-chip mode (μ PD703008, 70F3008, 703008Y, 70F3008Y only)

After the system has been released from the reset status, the pins related to the bus interface are set for port mode, execution branches to the reset entry address of the internal ROM, and instruction processing is started. However, access to external memory and peripheral devices can be enabled by setting in the external memory expansion mode register by instruction (MM: refer to **3.4.6 (1)**).

CLKOUT signal output is disabled when reset in the single-chip mode 1. However, it is input in the single-chip mode 2.

(b) ROM-less mode

After the system has been released from the reset status, the pins related to bus interface are set for control mode, execution branches to the reset address of external memory, and instruction processing is started. Instruction fetch and data access to internal ROM are disabled.

\overline{UBEN} , \overline{LBEN} , R/\overline{W} , and \overline{DSTB} signal are output when reset in the ROM-less mode. \overline{UBEN} , \overline{WRL} , \overline{WRH} , and \overline{RD} signal are output in the ROM-less mode 2.

(2) Flash memory programming mode (μ PD70F3008, 70F3008Y only)

- ★ This mode is provided only to on-chip flash memory model. If flash memory write voltage (7.8 V) is input to V_{PP} pin, the program operation to internal flash memory by flash writer is possible.

★ 3.3.2 Specifying operation mode

The operation mode of the V854 is specified depending on the status of the MODE pin. Set these pins in the application system (n = 0 to 2).

If the setting is changed during operation, the operation is not guaranteed.

(a) μ PD703006

MODE2	MODE1	MODE0	Operation Mode	
0	0	1	Normal operation mode	ROM-less mode 1
0	0	1		ROM-less mode 2
Other than above			Setting prohibited	

(b) μ PD703008, 703008Y

MODE2	MODE1	MODE0	Operation Mode	
0	0	0	Normal operation mode	ROM-less mode 1
0	0	1		ROM-less mode 2
0	1	0		Single-chip mode 1
0	1	1		Single-chip mode 2
Other than above			Setting prohibited	

(c) μ PD70F3008, 70F3008Y

Pin Status				Operation Mode	
V _{PP}	MODE2	MODE1	MODE0		
0 V	0	0	0	Normal operation mode	ROM-less mode 1
0 V	0	0	1		ROM-less mode 2
0 V	0	1	0		Single-chip mode 1
0 V	0	1	1		Single-chip mode 2
7.8 V	1	1	1	Flash memory programming mode	
Other than above				Setting prohibited	

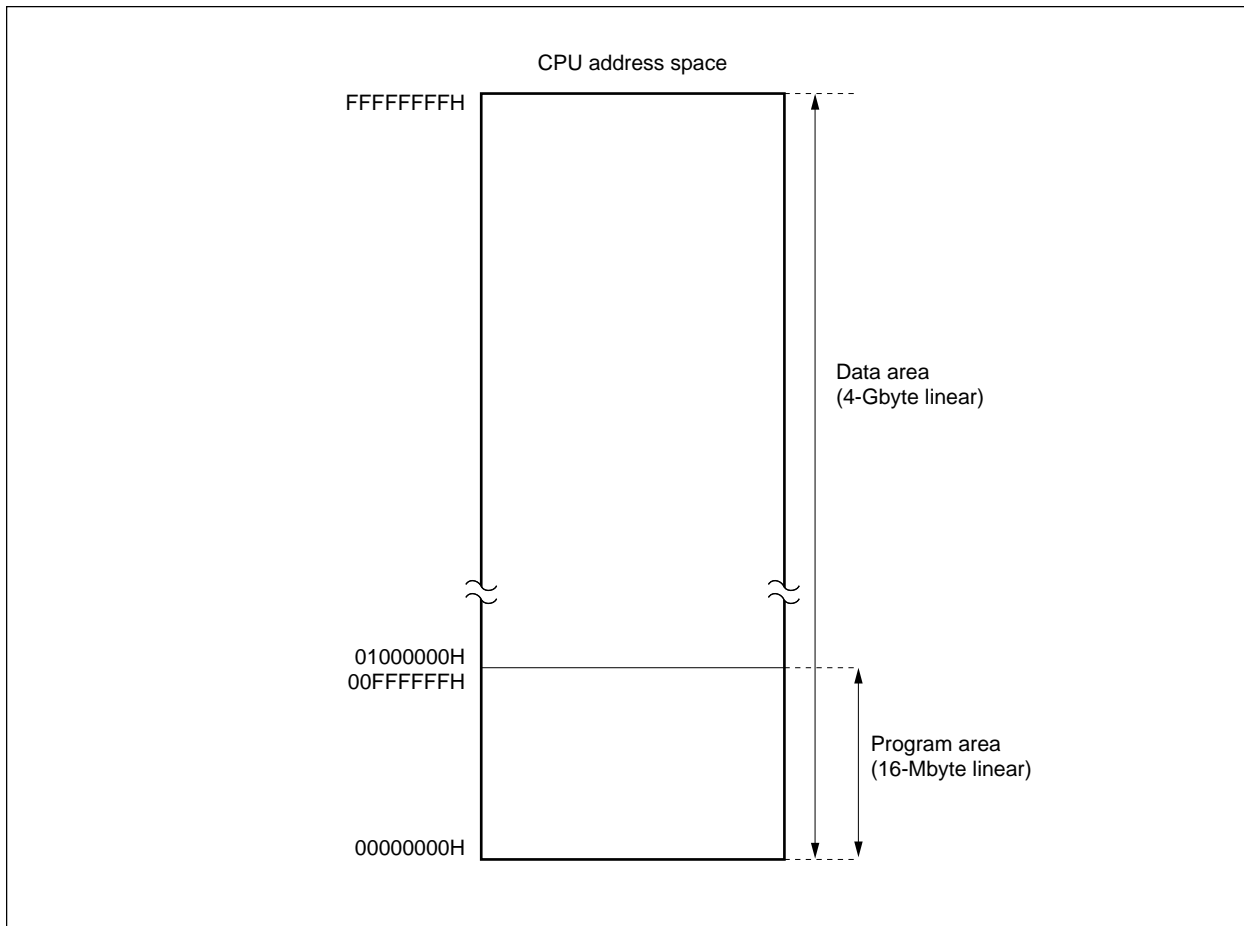
3.4 Address Space

3.4.1 CPU address space

The CPU of the V854 is of 32-bit architecture and supports up to 4 Gbytes of linear address space (data space) during operand addressing (data access). When referencing instruction addresses, a linear address space (program space) of up to 16 Mbytes is supported.

Figure 3-4 shows the CPU address space.

Figure 3-4. CPU Address Space

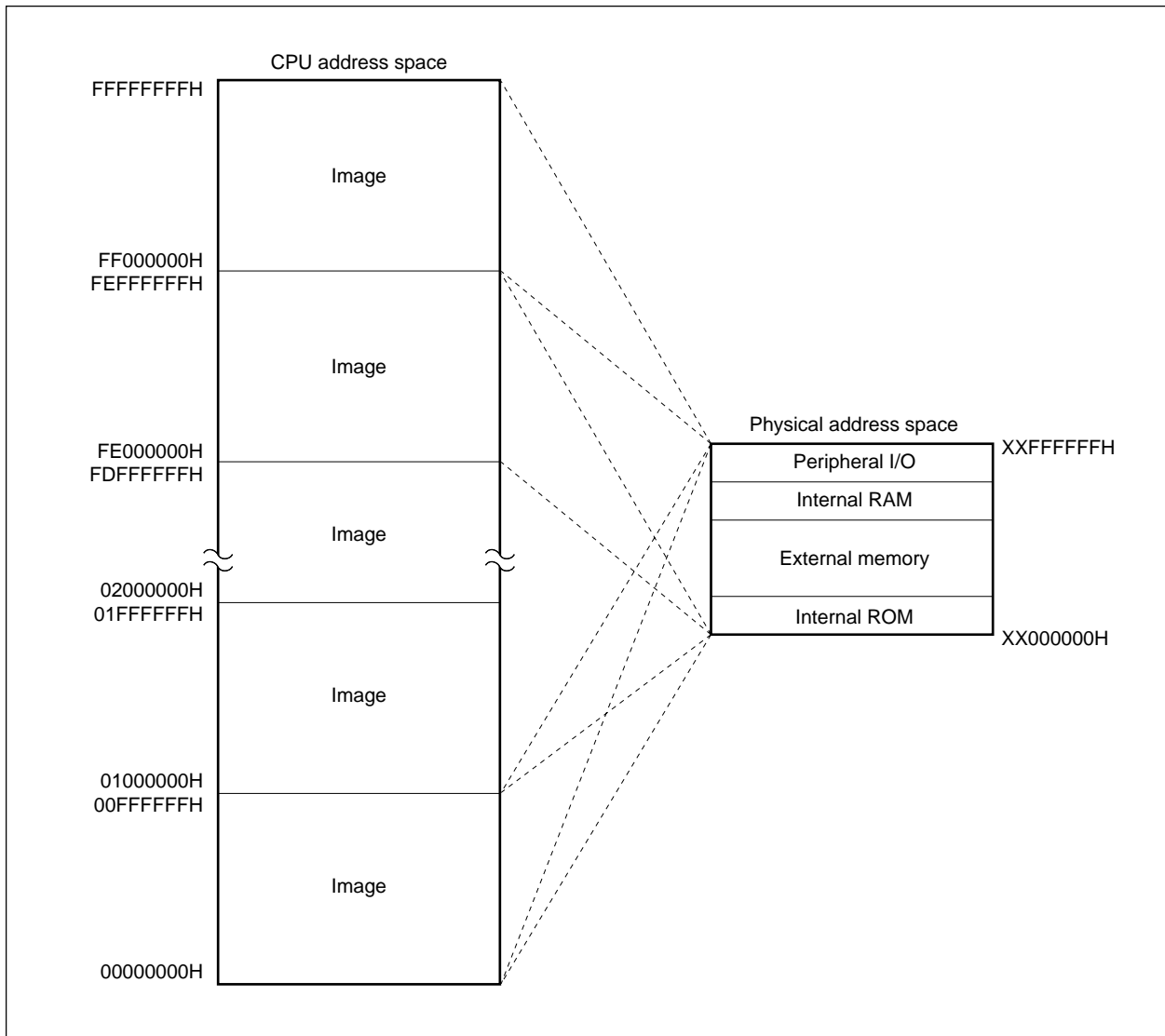


3.4.2 Image (Virtual Address Space)

The core CPU supports 4 Gbytes of “virtual” addressing space, or 256 memory blocks, each containing 16-Mbyte memory locations. In actuality, the same 16-Mbyte block is accessed regardless of the values of bits 31 to 24 of the CPU address. Figure 3-5 shows the image of the virtual addressing space.

Because the higher 8 bits of a 32-bit CPU address are ignored and the CPU address is only seen as a 24-bit external physical address, the physical location XX000000H is equally referenced by multiple address values 00000000H, 01000000H, 02000000H... through FF000000H.

Figure 3-5. Image on Address Space



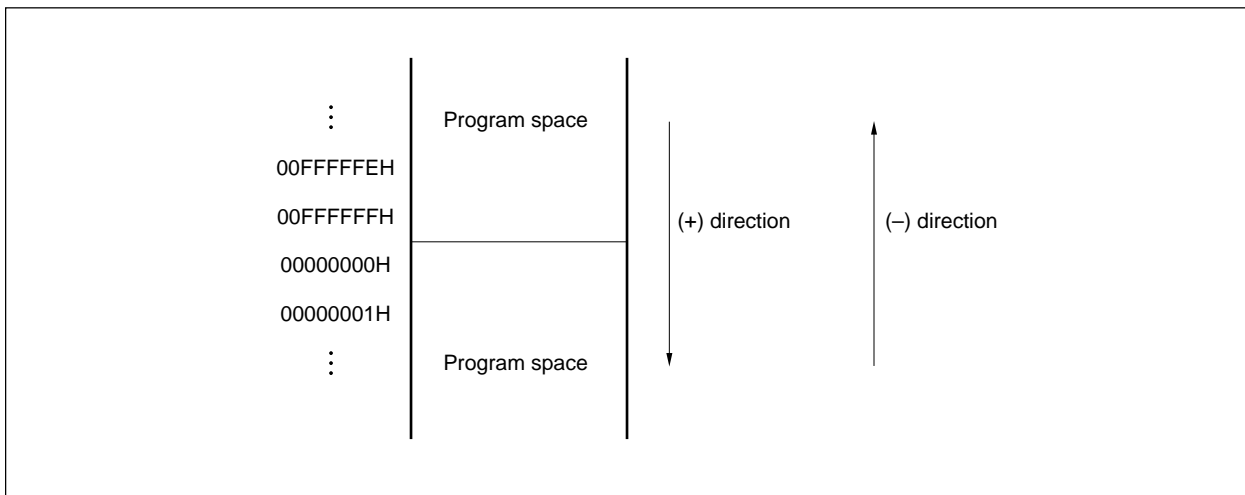
3.4.3 Wrap-around of CPU address space

(1) Program space

Of the 32 bits of the PC (program counter), the higher 8 bits are set to “0”, and only the lower 24 bits are valid. Even if a carry or borrow occurs from bit 23 to bit 24 as a result of branch address calculation, the higher 8 bits ignore the carry or borrow and remain “0”.

Therefore, the lower-limit address of the program space, address 00000000H, and the upper-limit address 00FFFFFFH are contiguous addresses. The above-mentioned state in which the lower-limit and the upper-limit addresses of the memory space are contiguous addresses is called wraparound.

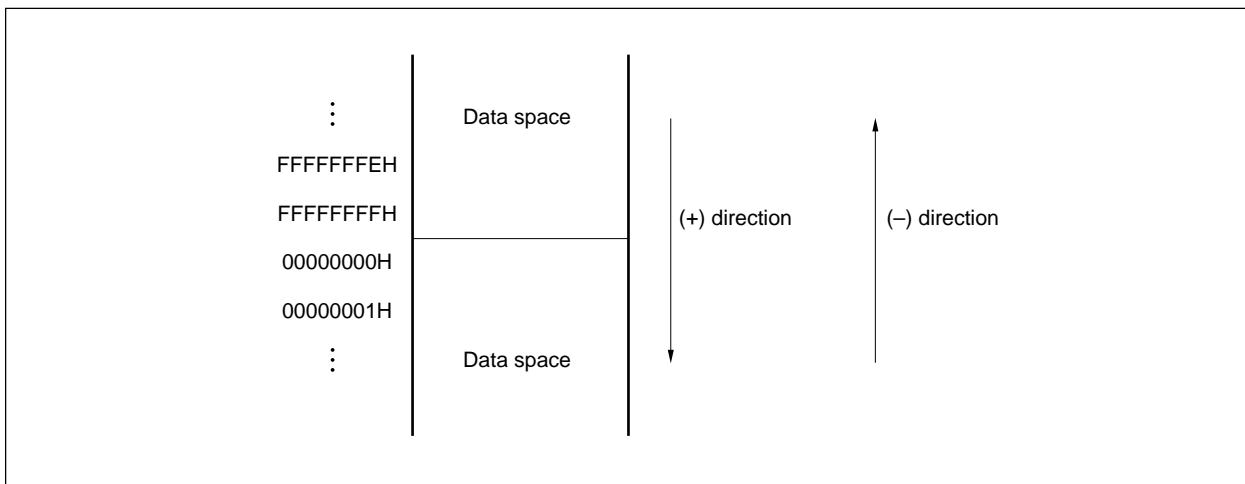
Caution No instruction can be fetched from the 4-Kbyte area of 00FFF000H to 00FFFFFFFH because this area is defined as peripheral I/O area. Therefore, do not execute any branch operation instructions in which the destination address will reside in any part of this area.



(2) Data space

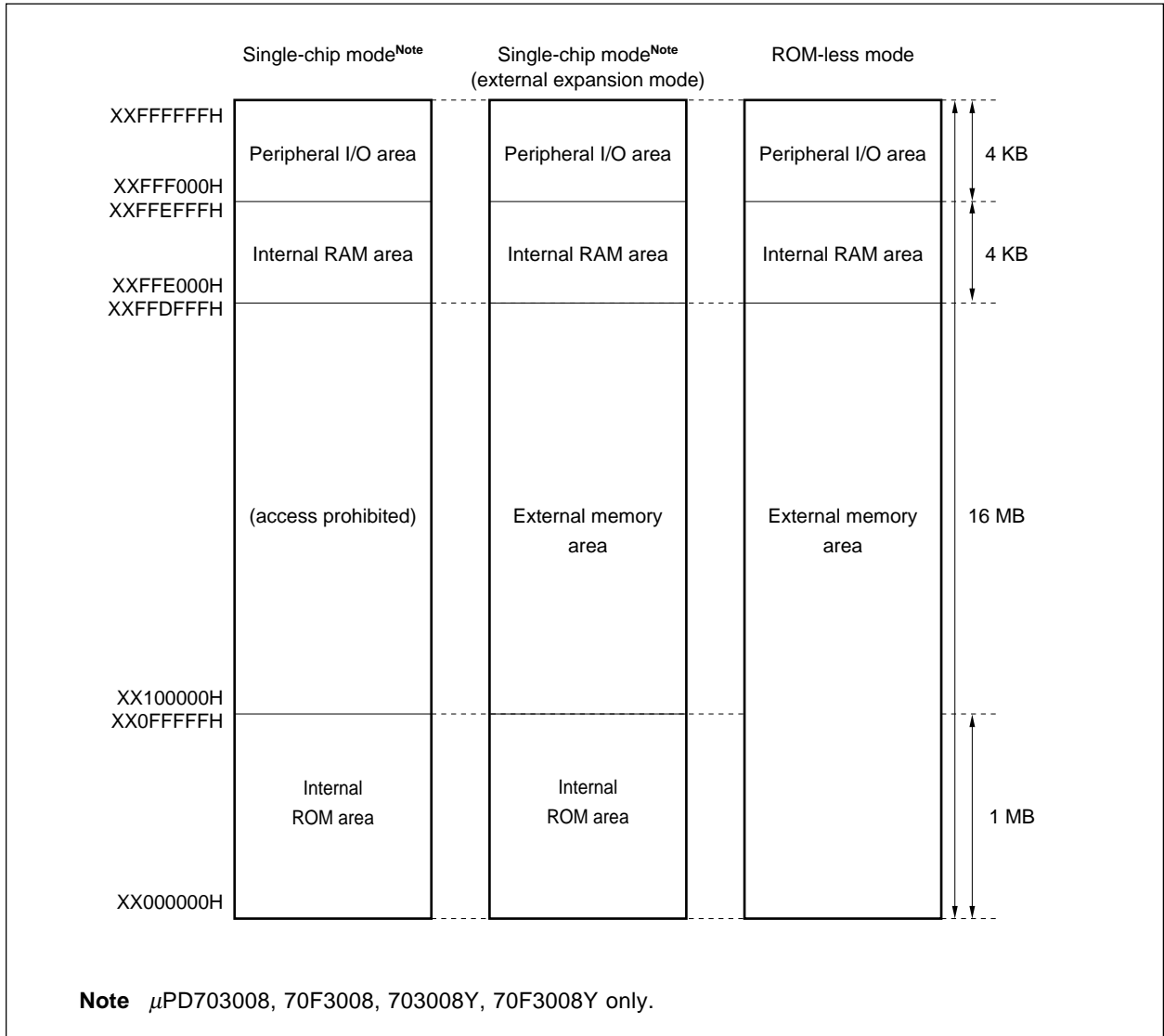
The result of operand address calculation that exceeds 32 bits is ignored.

Therefore, the lower-limit address of the program space, address 00000000H, and the upper-limit address FFFFFFFFH are contiguous addresses, and the data space is wrapped around at the boundary of these addresses.



3.4.4 Memory map

The V854 reserves areas as shown below. Each mode is specified by using the MODEn pin at reset (n = 0 to 2).



3.4.5 Area

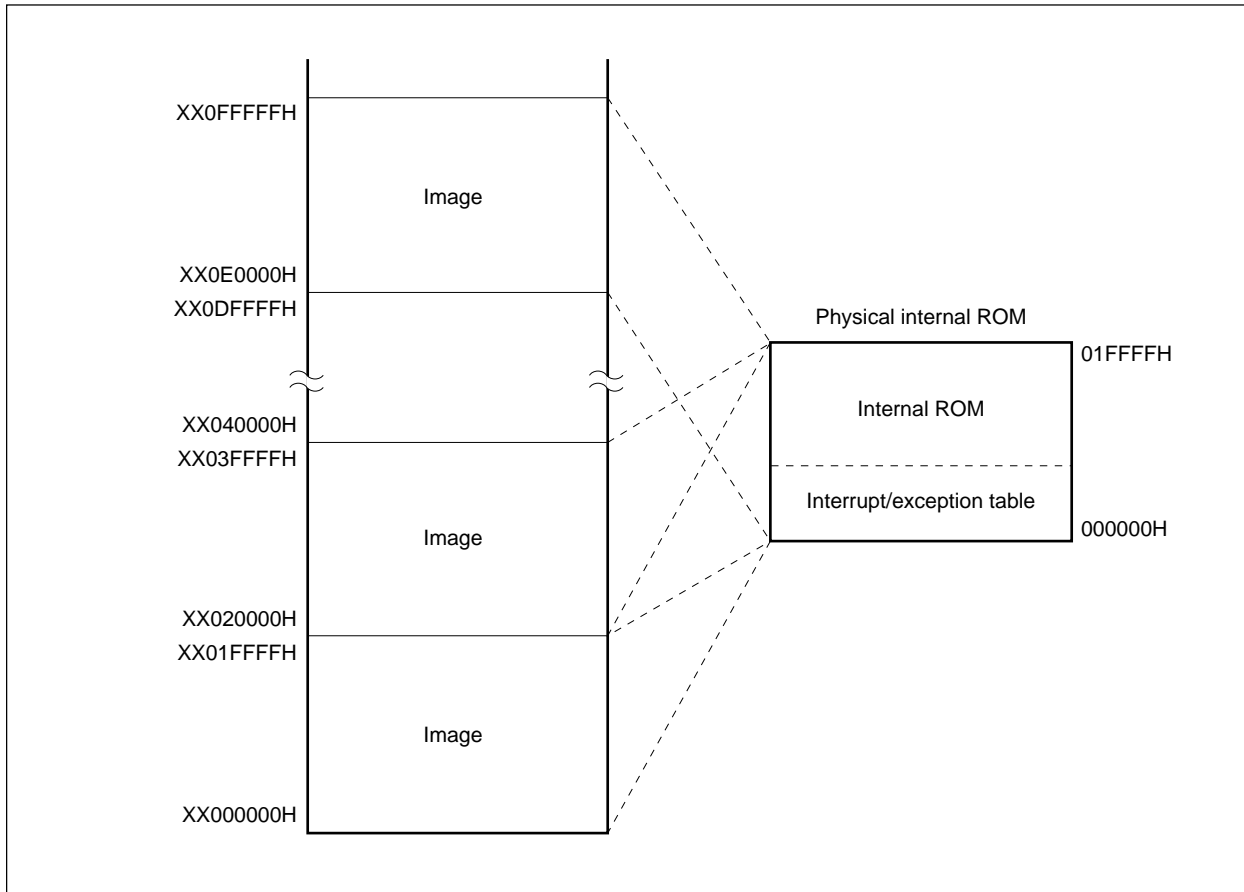
(1) Internal ROM area

A 1-Mbyte area corresponding to addresses 000000H to 0FFFFFFH is reserved for the internal ROM area. The V854 is provided with physical internal ROM as follows:

Caution Internal ROM products are μ PD703008, 70F3008, 703008Y and 70F3008Y only.

- Physical internal ROM: 000000H to 01FFFFH (128 Kbytes)

The image of 000000H to 01FFFFH is seen in the rest of the area (020000H to 0FFFFFFH).



Interrupt/exception table

The V854 increases the interrupt response speed by assigning destination addresses corresponding to interrupts/exceptions.

The collection of these destination addresses is called an interrupt/exception table, which is located in the internal ROM area. When an interrupt/exception request is granted, execution jumps to the corresponding destination address, and the program written at that memory address is executed. Table 3-3 shows the sources of interrupts/exceptions, and the corresponding addresses.

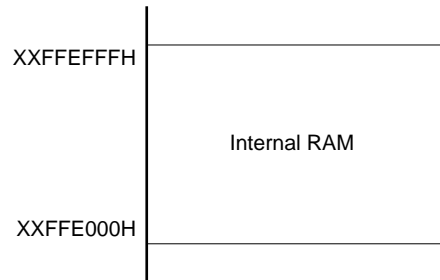
Table 3-3. Interrupt/Exception Table

Start Address of Interrupt/Exception Table	Interrupt/Exception Source
00000000H	RESET
00000010H	NMI
00000040H	TRAP0n (n = 0 to FH)
00000050H	TRAP1n (n = 0 to FH)
00000060H	ILGOP
00000080H	INTOV0/INTP04/INTP05
00000090H	INTOV1/INTP14
000000A0H	INTCC00/INTP00
000000B0H	INTCC01/INTP01
000000C0H	INTCC02/INTP02
000000D0H	INTCC03/INTP03
000000E0H	INTC10
000000F0H	INTC11
00000100H	INTCP12
00000110H	INTCP13
00000120H	INTCM10
00000130H	INTCM11
00000140H	INTCM20/INTP20
00000150H	INTCM21/INTP21
00000160H	INTCM22/INTP22
00000170H	INTCM23/INTP23
00000180H	INTCM24/INTP24
00000190H	INTCC3/INTP30
000001A0H	INTCSI0
000001B0H	INTCSI1
000001C0H	INTCSI2
000001D0H	INTCSI3
000001E0H	INIIC
000001F0H	INTSER
00000200H	INTSR
00000210H	INTST
00000220H	INTAD
00000230H	INTP50
00000240H	INTP51
00000250H	INTP52
00000260H	INTP53

Caution The internal ROM area becomes the external memory area in ROM-less mode or in the μ PD703006. For normal operation after reset, keep the destination address for the reset routine in external memory address 0.

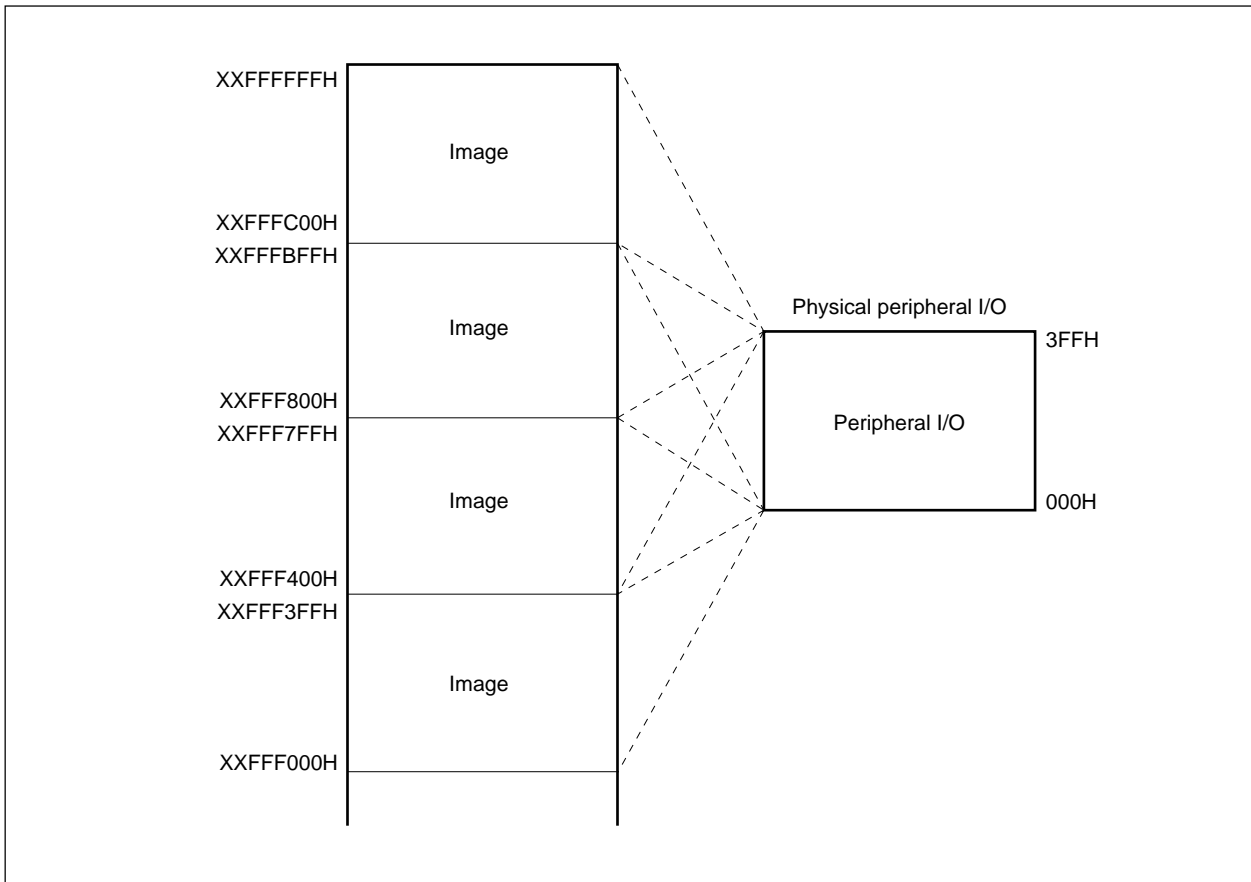
(2) Internal RAM area

The V854 is provided with 4 Kbytes of addresses FFE000H to FFEFFFH as a physical internal RAM area.



(3) Peripheral I/O area

A 4-Kbyte area of addresses FFF000H to FFFFFFFH is reserved as a peripheral I/O area. The V854 is provided with a 1-Kbyte area of addresses FFF000H to FFF3FFH as a physical peripheral I/O area, and the image of FFF000H to FFF3FFH can be seen on the rest of the area (FFF400H to FFFFFFFH).



Peripheral I/O registers associated with the operation mode specification and the state monitoring for the on-chip peripherals are all memory-mapped to the peripheral I/O area. Program fetches are not allowed in this area.

- Cautions**
1. The least significant bit of an address is not decoded since all registers reside on an even address. If an odd address ($2n + 1$) in the peripheral I/O area is referenced, the register at the next lowest even address ($2n$) will be accessed.
 2. If a register that can be accessed in byte units is accessed in half-word units, the higher 8 bits become undefined, if the access is a read operation. If a write access is made, only the data in the lower 8 bits is written to the register.
 3. If a register with n address that can be accessed only in halfword units is accessed with a word operation, the operation is replaced with two halfword operations. The first operation (lower 16 bits) accesses to the register with n address and the second operation (higher 16 bits) accesses to the register with $n + 2$ address.
 4. If a register with n address that can be accessed in word units is accessed with a word operation, the operation is replaced with two halfword operations. The first operation (lower 16 bits) accesses to the register with n address and the second operation (higher 16 bits) accesses to the register with $n + 2$ address.
 5. Addresses that are not defined as registers are reserved for future expansion. If these addresses are accessed, the operation is undefined and not guaranteed.

(4) External memory area

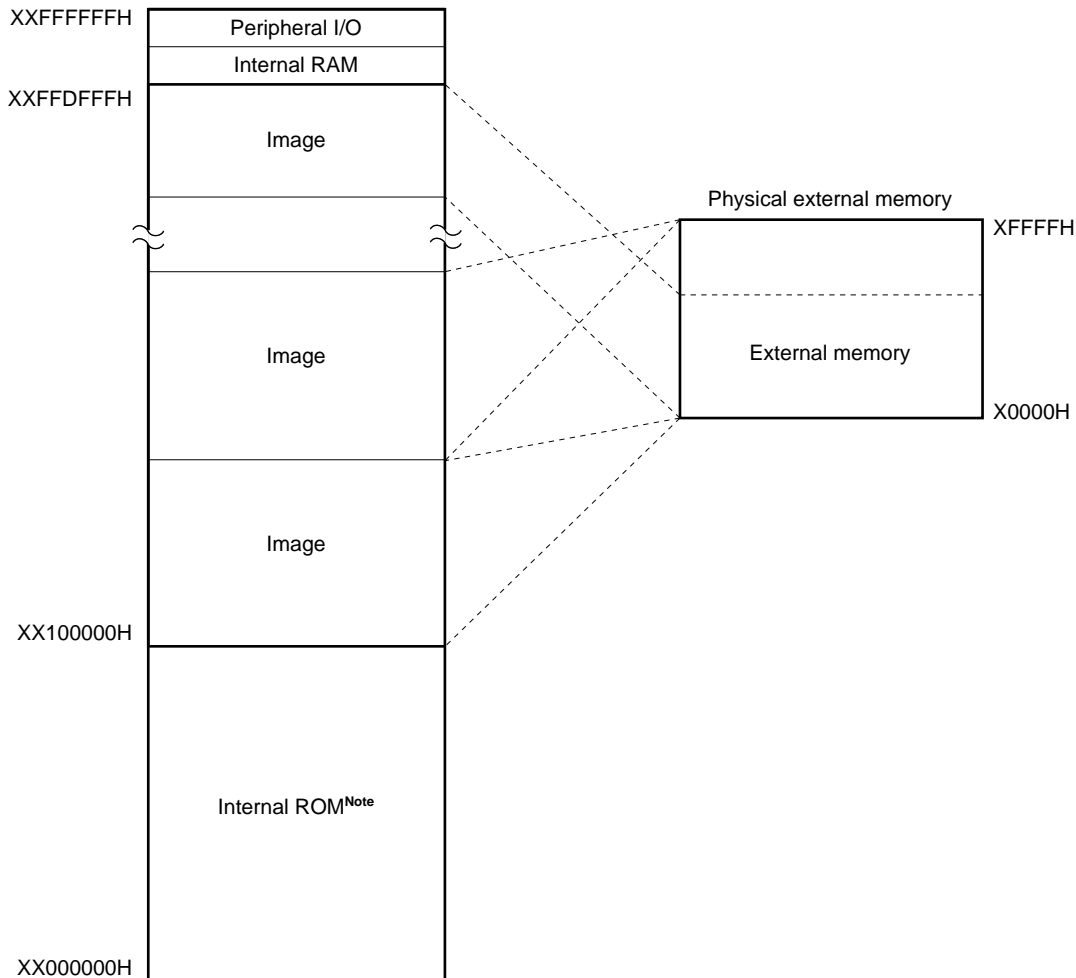
★ The μ PD703008, 70F3008, 703008Y, and 70F3008Y can use an area of up to xx100000H to xxFFDFFFH as an external memory area in the single-chip mode.

The μ PD703006, 703008, 70F3008, 703008Y, and 70F3008Y can use an area of up to xx000000H to xxFFDFFFH as an external memory area in the ROM-less mode.

In the external memory area, 64 K, 256 K, 1 M, 4 M, or 16 Mbytes of physical external memory can be allocated when the external expansion mode is specified. The same image as that of the physical external memory can be seen continuously on the external memory area, as shown in Figure 3-6, when the memory is not fully expanded (to 16 Mbytes).

The internal RAM area, peripheral I/O area, and internal ROM area in single-chip mode are not subject to external memory access.

Figure 3-6. External Memory Area (when expanded to 64 K, 256 K, or 1 Mbytes)



★ **Note** The image of the physical external memory can be seen continuously in the ROM-less mode or with the μ PD703006.

Figure 3-7. External Memory Area (when expanded to 4 Mbytes)

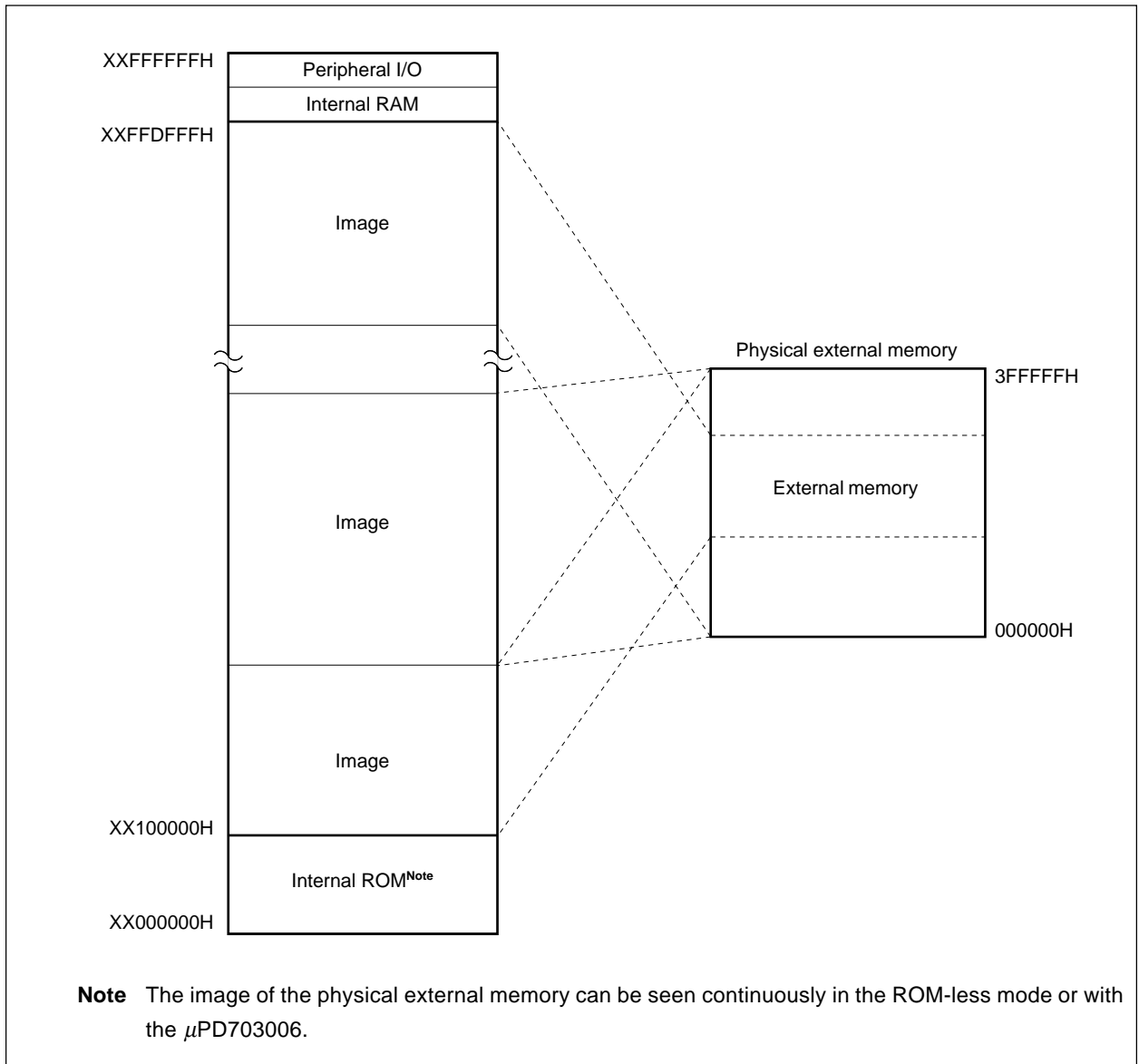
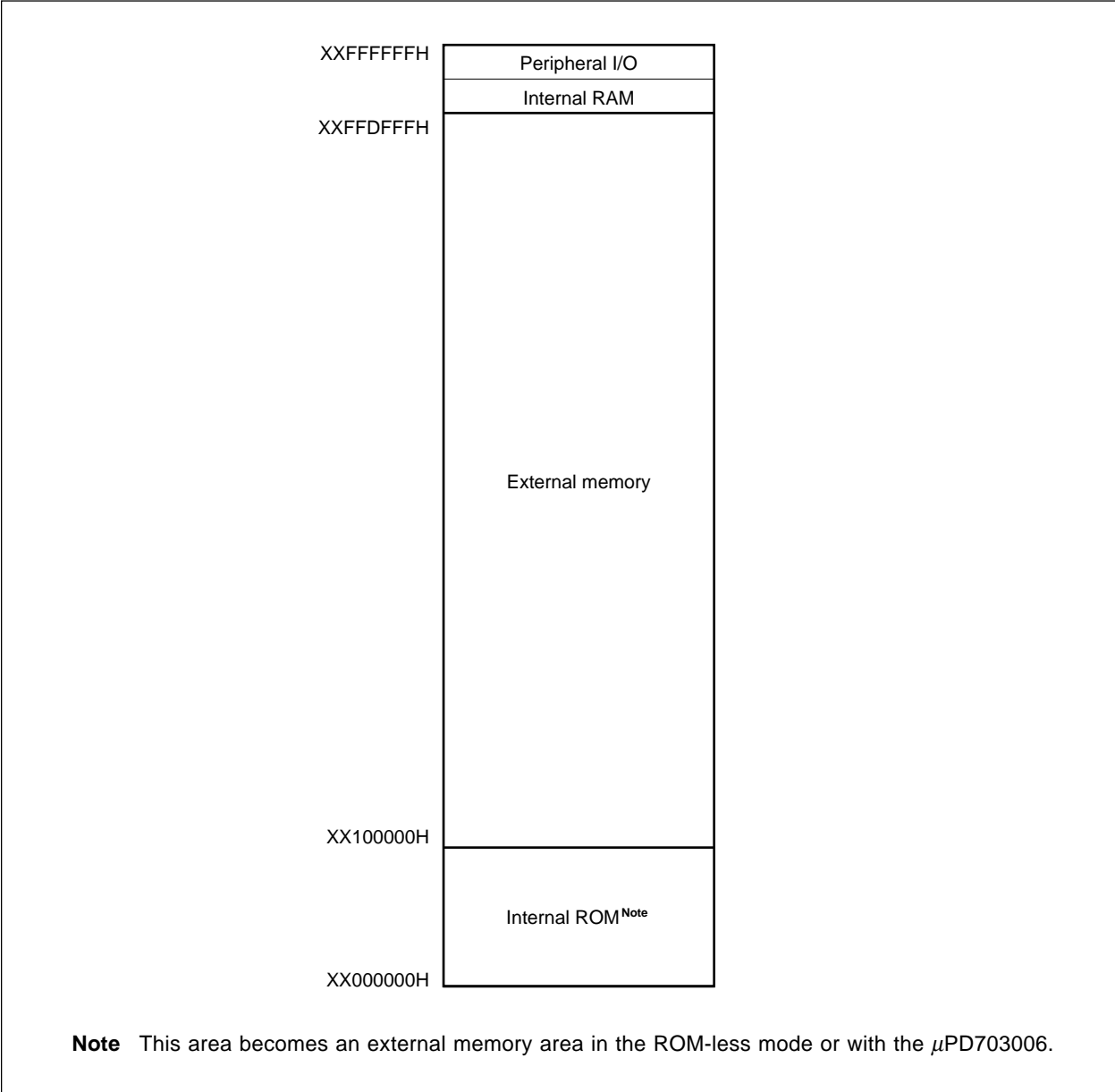


Figure 3-8. External Memory Area (when fully expanded)



3.4.6 External expansion mode

The V854 allows external devices to be connected to the external memory space by using the pins of ports 4, 5, 6, and 9. To connect an external device, the port pins must be set in the external expansion mode by using the MODEn pins and memory expansion mode register (MM). The MODEn pins specify the operation mode of the V854.

For specifying, refer to **3.3.2 Specifying operation mode**.

In ROM-less mode, the pins of port 4 to port 6 and P90 to P94 become the control mode during reset, thereby the external memory can be used.

In single-chip mode, the port/control mode alternate pins become the port mode, thereby the external memory cannot be used. When the external memory is used (external expansion mode), specify the MM register by the program (the memory area is set by the MM register).

Remark n = 0 to 2

(1) Memory expansion mode register (MM)

This register sets the mode of each pin of ports 4, 5, 6, and 9. In the external expansion mode, an external device can be connected to the external memory area of up to 16 Mbytes. However, the external device cannot be connected to the internal RAM area, peripheral I/O area, and internal ROM area in the single-chip mode (access is restricted to external locations 100000H through FFE00H).

The MM register can be read/written in 8- or 1-bit units. However, bits 4 to 7 are fixed to 0.

	7	6	5	4	3	2	1	0		
MM	0	0	0	0	MM3	MM2	MM1	MM0	Address FFFFFF04CH	After reset 07H (in ROM-less mode) 00H (in single-chip mode)

Bit Position	Bit Name	Function																																																
3	MM3	<p>Memory Expansion Mode</p> <p>Specifies operation mode of P95 and P96 of port 9.</p> <table><tr><td>MM3</td><td>Operation Mode</td><td>P95</td><td>P96</td></tr><tr><td>0</td><td>Port mode</td><td colspan="2">Port</td></tr><tr><td>1</td><td>External expansion mode</td><td>H$\overline{\text{LDAK}}$</td><td>H$\overline{\text{LDRQ}}$</td></tr></table>	MM3	Operation Mode	P95	P96	0	Port mode	Port		1	External expansion mode	H $\overline{\text{LDAK}}$	H $\overline{\text{LDRQ}}$																																				
MM3	Operation Mode	P95	P96																																															
0	Port mode	Port																																																
1	External expansion mode	H $\overline{\text{LDAK}}$	H $\overline{\text{LDRQ}}$																																															
2 to 0	MM2 to MM0	<p>Memory Expansion Mode</p> <p>Specifies operation mode of ports 4, 5, 6, and 9 (P90 to P94).</p> <table><tr><td>MM2</td><td>MM1</td><td>MM0</td><td>Address Space</td><td>Port 4</td><td>Port 5</td><td>Port 6</td><td>Port 9 (P90 to P94)</td></tr><tr><td>0</td><td>0</td><td>0</td><td>—</td><td colspan="4">Port mode</td></tr><tr><td>0</td><td>1</td><td>1</td><td>64-KB expansion</td><td rowspan="5">AD0 to AD7</td><td rowspan="6">AD8 to AD15</td><td rowspan="6"><div><div>A16</div><div>A17</div><div>A18</div><div>A19</div><div>A20</div><div>A21</div><div>A22</div><div>A23</div></div></td><td rowspan="6"><div>$\overline{\text{LBEN}}$, $\overline{\text{UBEN}}$, R/$\overline{\text{W}}$, $\overline{\text{DSTB}}$, ASTB, WRL, $\overline{\text{WRH}}$, RD</div></td></tr><tr><td>1</td><td>0</td><td>0</td><td>256-KB expansion</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1-MB expansion</td></tr><tr><td>1</td><td>1</td><td>0</td><td>4-MB expansion</td></tr><tr><td>1</td><td>1</td><td>1</td><td>16-MB expansion</td></tr><tr><td colspan="4">Others</td><td colspan="4">RFU (reserved)</td></tr></table>	MM2	MM1	MM0	Address Space	Port 4	Port 5	Port 6	Port 9 (P90 to P94)	0	0	0	—	Port mode				0	1	1	64-KB expansion	AD0 to AD7	AD8 to AD15	<div><div>A16</div><div>A17</div><div>A18</div><div>A19</div><div>A20</div><div>A21</div><div>A22</div><div>A23</div></div>	<div>$\overline{\text{LBEN}}$, $\overline{\text{UBEN}}$, R/$\overline{\text{W}}$, $\overline{\text{DSTB}}$, ASTB, WRL, $\overline{\text{WRH}}$, RD</div>	1	0	0	256-KB expansion	1	0	1	1-MB expansion	1	1	0	4-MB expansion	1	1	1	16-MB expansion	Others				RFU (reserved)			
MM2	MM1	MM0	Address Space	Port 4	Port 5	Port 6	Port 9 (P90 to P94)																																											
0	0	0	—	Port mode																																														
0	1	1	64-KB expansion	AD0 to AD7	AD8 to AD15	<div><div>A16</div><div>A17</div><div>A18</div><div>A19</div><div>A20</div><div>A21</div><div>A22</div><div>A23</div></div>	<div>$\overline{\text{LBEN}}$, $\overline{\text{UBEN}}$, R/$\overline{\text{W}}$, $\overline{\text{DSTB}}$, ASTB, WRL, $\overline{\text{WRH}}$, RD</div>																																											
1	0	0	256-KB expansion																																															
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1	1	0	4-MB expansion																																															
1	1	1	16-MB expansion																																															
Others				RFU (reserved)																																														

Remark For the details of the operation of each port pin, refer to 2.3 Pin Function.

3.4.7 Recommended use of address space

The architecture of the V854 requires that a register that serves as a pointer be secured for address generation in operand data accessing for data space. The address in this pointer register ± 32 Kbytes can be accessed directly from instruction. However, general register used as a pointer register is limited. Therefore, by minimizing the deterioration of address calculation performance when changing the pointer value, the number of usable general registers for handling variables is maximized, and the program size can be saved because instructions for calculating pointer addresses are not required.

To enhance the efficiency of using the pointer in connection with the memory map of the V854, the following points are recommended:

(1) Program space

Of the 32 bits of the PC (program counter), the higher 8 bits are fixed to "0", and only the lower 24 bits are valid. Therefore, a contiguous 16-Mbyte space, starting from address 00000000H, unconditionally corresponds to the memory map of the program space.

(2) Data space

For the efficient use of resources to be performed through the wrap-around feature of the data space, the continuous 8-Mbyte address spaces 00000000H to 007FFFFFFH and FF800000H to FFFFFFFFH of the 4-Gbyte CPU are used as the data space. With the V854, 16-Mbyte physical address space is seen as 256 images in the 4-Gbyte CPU address space. The highest bit (bit 23) of this 24-bit address is assigned as address sign-extended to 32 bits.

Application of wrap-around

For example, when R = r0 (zero register) is specified for the LD/ST disp 16 [R] instruction, an addressing range of $00000000H \pm 32$ Kbytes can be referenced with the sign-extended, 16-bit displacement value. By mapping the external memory in the 24-Kbyte area in the figure, all resources including on-chip hardware can be accessed with one pointer.

The zero register (r0) is a register set to 0 by the hardware, and eliminates the need for additional registers for the pointer.

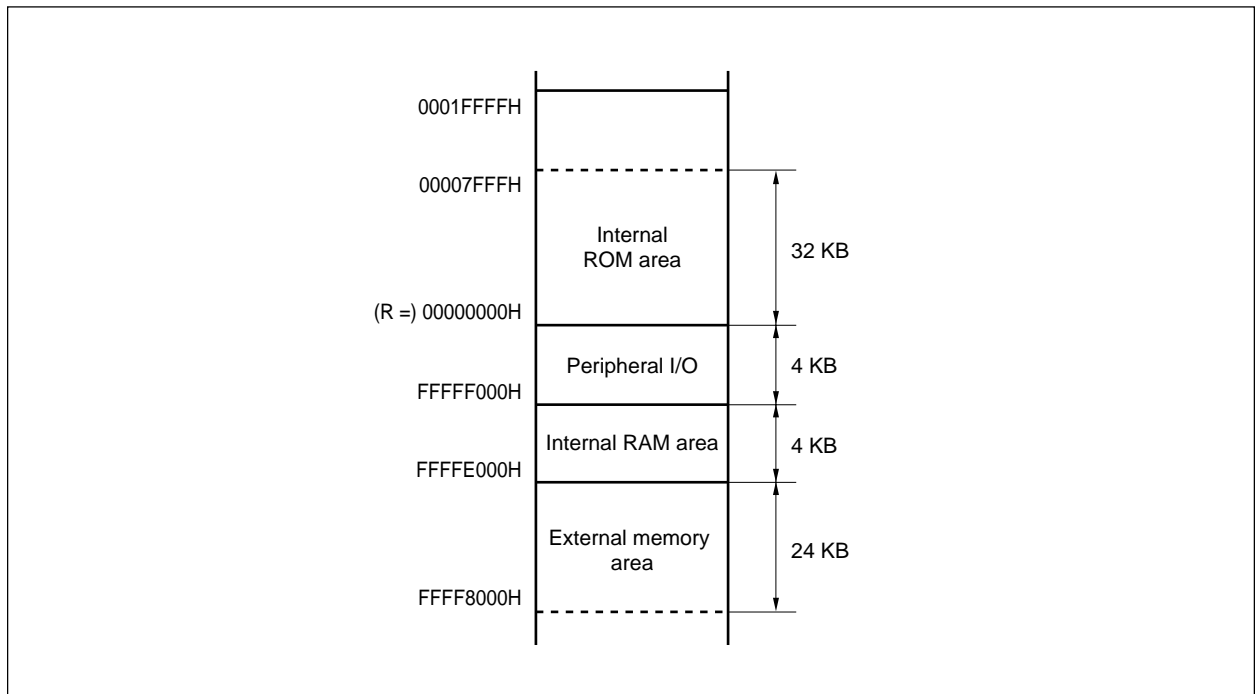
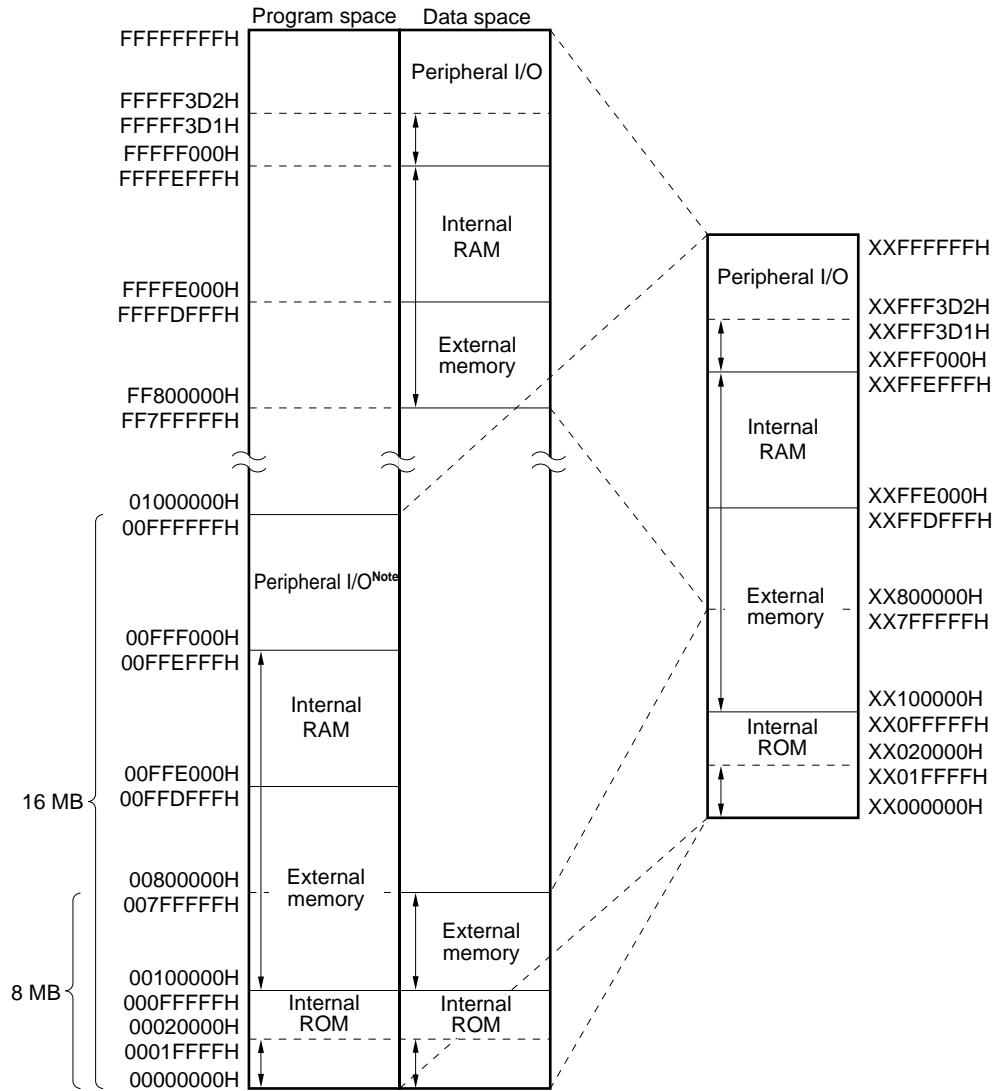


Figure 3-9. Recommended Memory Map



Note This area cannot be used as a program area.

- Remarks**
1. The vertical arrows (\updownarrow) indicate the recommended area.
 2. In this figure, the μ PD703008 is set in the single-chip mode and the recommended memory map when the external expanded memory mode being used is shown.

3.4.8 Peripheral I/O registers

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation				After Reset
				1 bit	8 bits	16 bits	32bits	
FFFFF000H	Port 0	P0	R/W	○	○			Undefined
FFFFF002H	Port 1	P1		○	○			
FFFFF004H	Port 2	P2		○	○			
FFFFF006H	Port 3	P3		○	○			
FFFFF008H	Port 4	P4		○	○			
FFFFF00AH	Port 5	P5		○	○			
FFFFF00CH	Port 6	P6		○	○			
FFFFF00EH	Port 7	P7	R	○	○			
FFFFF010H	Port 8	P8	R/W	○	○			
FFFFF012H	Port 9	P9		○	○			
FFFFF014H	Port 10	P10		○	○			
FFFFF016H	Port 11	P11		○	○			
FFFFF018H	Port 12	P12		○	○			
FFFFF01AH	Port 13	P13		○	○			
FFFFF01CH	Port 14	P14		○	○			
FFFFF020H	Port 0 mode register	PM0	R/W	○	○			FFH
FFFFF022H	Port 1 mode register	PM1		○	○			
FFFFF024H	Port 2 mode register	PM2		○	○			
FFFFF026H	Port 3 mode register	PM3		○	○			
FFFFF028H	Port 4 mode register	PM4		○	○			
FFFFF02AH	Port 5 mode register	PM5		○	○			
FFFFF02CH	Port 6 mode register	PM6		○	○			
FFFFF032H	Port 9 mode register	PM9		○	○			
FFFFF034H	Port 10 mode register	PM10		○	○			
FFFFF036H	Port 11 mode register	PM11		○	○			
FFFFF038H	Port 12 mode register	PM12		○	○			
FFFFF03AH	Port 13 mode register	PM13		○	○			
FFFFF03CH	Port 14 mode register	PM14		○	○			
FFFFF040H	Port 0 mode control register	PMC0	R/W	○	○			00H
FFFFF042H	Port 1 mode control register	PMC1		○	○			
FFFFF044H	Port 2 mode control register	PMC2		○	○			01H
FFFFF046H	Port 3 mode control register	PMC3		○	○			00H
FFFFF04CH	Memory expansion mode register	MM		○	○			00H/07H
FFFFF054H	Port 10 mode control register	PMC10		○	○			00H
FFFFF056H	Port 11 mode control register	PMC11		○	○			
FFFFF058H	Port 12 mode control register	PMC12		○	○			

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation				After Reset
				1 bit	8 bits	16 bits	32bits	
FFFFF05AH	Port 13 mode control register	PMC13	R/W	○	○			00H
FFFFF060H	Data wait control register	DWC				○		FFFFH
FFFFF062H	Bus cycle control register	BCC				○		AAAAH
FFFFF064H	System control register	SYC		○	○			00H/1H
FFFFF070H	Power save control register	PSC		○	○			00H/C0H
FFFFF072H	Clock control register	CKC		○	○			00H
FFFFF078H	System status register	SYS		○	○			0000000XB
FFFFF084H	Baud rate generator compare register 0	BRGC0		○	○			Undefined
FFFFF086H	Baud rate generator prescaler mode register 0	BPRM0		○	○			00H
FFFFF088H	Clocked serial interface mode register 0	CSIM0		○	○			
FFFFF08AH	Serial I/O shift register 0	SIO0		○	○			Undefined
FFFFF094H	Baud rate generator compare register 1	BRGC1		○	○			
FFFFF096H	Baud rate generator prescaler mode register 1	BPRM1		○	○			00H
FFFFF098H	Clocked serial interface mode register 1	CSIM1		○	○			
FFFFF09AH	Serial I/O shift register 1	SIO1		○	○			Undefined
FFFFF0A4H	Baud rate generator compare register 2	BRGC2		○	○			
FFFFF0A6H	Baud rate generator prescaler mode register 2	BPRM2		○	○			00H
FFFFF0A8H	Clocked serial interface mode register 2	CSIM2		○	○			
FFFFF0AAH	Serial I/O shift register 2	SIO2		○	○			Undefined
FFFFF0B4H	Baud rate generator register 3	BRGC3		○	○			
FFFFF0B6H	Baud rate generator prescaler mode register	BPRM3		○	○			00H
FFFFF0B8H	Clocked serial interface mode register 3	CSIM3		○	○			
FFFFF0BAH	Serial I/O shift register 3	SIO3		○	○			Undefined
FFFFF0C0H	Asynchronous serial interface mode register 0	ASIM0		○	○			80H
FFFFF0C2H	Asynchronous serial interface mode register 1	ASIM1		○	○			00H
FFFFF0C4H	Asynchronous serial interface status register	ASIS	R	○	○			
FFFFF0C8H	Receive buffer (9 bits)	RXB				○		Undefined
FFFFF0CAH	Receive buffer L (lower 8 bits)	RXBL	W	○	○			
FFFFF0CCH	Transmit shift register (9 bits)	TXS				○		00H
FFFFF0CEH	Transmit shift register L (lower 8 bits)	TXSL	R/W		○			
FFFFF0E0H	IIC control register	IICC		○	○			00H
FFFFF0E2H	IIC status register	IICS		○	○			
FFFFF0E4H	IIC clock selection register	IICCL		○	○			
FFFFF0E6H	IIC shift register	IIC		○	○			
FFFFF0E8H	Slave address register	SVA		○	○			47H
FFFFF100H	Interrupt control register	OVIC0		○	○			
FFFFF102H	Interrupt control register	OVIC1		○	○			
FFFFF104H	Interrupt control register	CC0IC0		○	○			

Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation				After Reset
				1 bit	8 bits	16 bits	32bits	
FFFFF106H	Interrupt control register	CC0IC1	R/W	○	○			47H
FFFFF108H	Interrupt control register	CC0IC2		○	○			
FFFFF10AH	Interrupt control register	CC0IC3		○	○			
FFFFF10CH	Interrupt control register	P1IC0		○	○			
FFFFF10EH	Interrupt control register	P1IC1		○	○			
FFFFF110H	Interrupt control register	P1IC2		○	○			
FFFFF112H	Interrupt control register	P1IC3		○	○			
FFFFF114H	Interrupt control register	CM1IC0		○	○			
FFFFF116H	Interrupt control register	CM1IC1		○	○			
FFFFF118H	Interrupt control register	CM2IC0		○	○			
FFFFF11AH	Interrupt control register	CM2IC1		○	○			
FFFFF11CH	Interrupt control register	CM2IC2		○	○			
FFFFF11EH	Interrupt control register	CM2IC3		○	○			
FFFFF120H	Interrupt control register	CM2IC4		○	○			
FFFFF122H	Interrupt control register	CM3IC0		○	○			
FFFFF124H	Interrupt control register	CSIC0		○	○			
FFFFF126H	Interrupt control register	CSIC1		○	○			
FFFFF128H	Interrupt control register	CSIC2		○	○			
FFFFF12AH	Interrupt control register	CSIC3		○	○			
FFFFF12CH	Interrupt control register	IIIC0		○	○			
FFFFF12EH	Interrupt control register	SEIC0		○	○			
FFFFF130H	Interrupt control register	SRIC0		○	○			
FFFFF132H	Interrupt control register	STIC0		○	○			
FFFFF134H	Interrupt control register	ADIC0		○	○			
FFFFF136H	Interrupt control register	P51C0		○	○			
FFFFF138H	Interrupt control register	P51C1		○	○			
FFFFF13AH	Interrupt control register	P51C2		○	○			
FFFFF13CH	Interrupt control register	P51C3		○	○			
FFFFF166H	In-service priority register	ISPR	R	○	○			00H
FFFFF170H	Command register	PRCMD	W		○			Undefined
FFFFF180H	External interrupt mode register 0	INTM0	R/W	○	○			00H
FFFFF182H	External interrupt mode register 1	INTM1		○	○			
FFFFF184H	External interrupt mode register 2	INTM2		○	○			
FFFFF18AH	External interrupt mode register 5	INTM5		○	○			
FFFFF18CH	External interrupt mode register 6	INTM6		○	○			
FFFFF18EH	External interrupt mode register 7	INTM7		○	○			
FFFFF1B0H	Event divide control register 0	EDVC0		○	○			01H
FFFFF1B2H	Event divide control register 1	EDVC1		○	○			

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation				After Reset
				1 bit	8 bits	16 bits	32bits	
FFFFF1B4H	Event divide control register 2	EDVC2	R/W	○	○			01H
FFFFF1B6H	Event divide counter 0	EDV0	R	○	○			00H
FFFFF1B8H	Event divide counter 1	EDV1		○	○			
FFFFF1BAH	Event divide counter 2	EDV2		○	○			
FFFFF1C0H	Event selection register	EVS	R/W	○	○			01H
FFFFF230H	Timer overflow status register	TOVS		○	○			
FFFFF232H	Timer output control register 0	TOC0		○	○			
FFFFF234H	Timer output control register 1	TOC1		○	○			
FFFFF240H	Timer control register 00	TMC00		○	○			
FFFFF242H	Timer control register 01	TMC01		○	○			
FFFFF244H	Timer control register 02	TMC02		○	○			
FFFFF250H	Timer 0	TM0	R				○	00000000H
FFFFF254H	Capture/compare register 00	CC00	R/W				○	Undefined
FFFFF258H	Capture/compare register 01	CC01					○	
FFFFF25CH	Capture/compare register 02	CC02					○	
FFFFF260H	Capture/compare register 03	CC03					○	
FFFFF264H	Timer 0L	TM0L	R			○		0000H
FFFFF266H	Capture/compare register 00L	CC00L	R/W			○		Undefined
FFFFF268H	Capture/compare register 01L	CC01L				○		
FFFFF26AH	Capture/compare register 02L	CC02L				○		
FFFFF26CH	Capture/compare register 03L	CC03L				○		
FFFFF270H	Timer control register 1	TMC1		○	○			01H
FFFFF274H	Timer 1	TM1	R				○	00000000H
FFFFF278H	Compare register 10	CM10	R/W				○	Undefined
FFFFF27CH	Compare register 11	CM11					○	
FFFFF280H	Capture register 10	CP10	R				○	0000H
FFFFF284H	Capture register 11	CP11					○	
FFFFF288H	Capture register 12	CP12					○	
FFFFF28CH	Capture register 13	CP13					○	
FFFFF290H	Timer 1L	TM1L				○		
FFFFF292H	Compare register 10L	CM10L	R/W			○		Undefined
FFFFF294H	Compare register 11L	CM11L				○		
FFFFF296H	Capture register 10L	CP10L	R			○		0000H
FFFFF298H	Capture register 11L	CP11L				○		
FFFFF29AH	Capture register 12L	CP12L				○		
FFFFF29CH	Capture register 13L	CP13L				○		
FFFFF2A0H	Timer control register 20	TMC20	R/W	○	○			01H
FFFFF2B0H	Timer 20	TM20	R			○		0000H

Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation				After Reset
				1 bit	8 bits	16 bits	32bits	
FFFFF2B2H	Compare register 20	CM20	R/W			○		Undefined
FFFFF2C0H	Timer control register 21	TMC21		○	○			01H
FFFFF2D0H	Timer 21	TM21	R			○		0000H
FFFFF2D2H	Compare register 21	CM21	R/W			○		Undefined
FFFFF2E0H	Timer control register 22	TMC22		○	○			01H
FFFFF2F0H	Timer 22	TM22	R			○		0000H
FFFFF2F2H	Compare register 22	CM22	R/W			○		Undefined
FFFFF300H	Timer control register 23	TMC23		○	○			01H
FFFFF310H	Timer 23	TM23	R			○		0000H
FFFFF312H	Compare register 23	CM23	R/W			○		Undefined
FFFFF320H	Timer control register 24	TMC24		○	○			01H
FFFFF330H	Timer 24	TM24	R			○		0000H
FFFFF332H	Compare register 24	CM24	R/W			○		Undefined
FFFFF340H	Timer control register 3	TMC3		○	○			01H
FFFFF350H	Timer 3	TM3	R			○		0000H
FFFFF352H	Capture/compare register 3	CC3	R/W			○		Undefined
FFFFF354H	Capture register 3	CP3	R			○		
FFFFF360H	PWM control register 3	PWMC0	R/W	○	○			05H
FFFFF362H	PWM modulo register 0	PWM0				○		Undefined
FFFFF364H	PWM prescaler register 0	PWPR0		○	○			00H
FFFFF368H	PWM control register 1	PWMC1		○	○			05H
FFFFF36AH	PWM modulo register 1	PWM1				○		Undefined
FFFFF36CH	PWM prescaler register 1	PWPR1		○	○			00H
FFFFF370H	PWM control register 2	PWMC2		○	○			05H
FFFFF372H	PWM modulo register 2	PWM2				○		Undefined
FFFFF374H	PWM prescaler register 2	PWPR2		○	○			00H
FFFFF378H	PWM control register 3	PWMC3		○	○			05H
FFFFF37AH	PWM modulo register 3	PWM3				○		Undefined
FFFFF37CH	PWM prescaler register 3	PWPR3		○	○			00H
FFFFF380H	A/D converter mode register 0	ADM0		○	○			
FFFFF382H	A/D converter mode register 1	ADM1		○	○			07H
FFFFF390H	A/D conversion result register 0	ADCR0	R	○	○			Undefined
FFFFF392H	A/D conversion result register 1	ADCR1		○	○			
FFFFF394H	A/D conversion result register 2	ADCR2		○	○			
FFFFF396H	A/D conversion result register 3	ADCR3		○	○			
FFFFF398H	A/D conversion result register 4	ADCR4		○	○			
FFFFF39AH	A/D conversion result register 5	ADCR5		○	○			
FFFFF39CH	A/D conversion result register 6	ADCR6		○	○			

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Address	Function Register Name	Symbol	R/W	Bit Units for Manipulation				After Reset
				1 bit	8 bits	16 bits	32bits	
FFFFF39EH	A/D conversion result register 7	ADCR7	R	○	○			Undefined
FFFFF3C0H	Port 13 buffer register	PB	R/W	○	○			
FFFFF3C2H	Output latch	RTP		○	○			
FFFFF3D0H	Clock output mode register	CL0M		○	○			00H

3.4.9 Specific registers

Specific registers are registers that are protected from being written with illegal data due to program runaway, etc. The write access of these specific registers is executed in a specific sequence, and if abnormal store operations occur, this is notified by the system status register (SYS). The V854 has two specific registers, the clock control register (CKC) and power save control register (PSC). For details of the CKC register, refer to **6.3.3**, and for details of the PSC register, refer to **6.5.2**.

The following sequence shows the data setting of the specific registers.

- (1) Set the PSW NP bit to 1 (interrupt disabled).
- (2) Write arbitrary 8-bit data in the command register (PRCMD).
- (3) Write the set data in the specific registers (by the following instructions).
 - Store instruction (ST/SST instruction)
 - Bit manipulation instruction (SET1/CLR1/NOT1 instruction)
- (4) Return the PSW NP bit to 0 (interrupt disable canceled).
- (5) To shift to the software STOP mode or IDLE mode, insert the NOP instructions (2 or 5 instructions).

No special sequence is required when reading the specific registers.

Cautions 1. If an interrupt request is accepted between the time PRCMD is issued (2) and the specific register write operation (3) that follows immediately after, the write operation to the specific register is not performed and a protection error (PRERR bit of SYS register is “1”) may occur. Therefore, set the NP bit of PSW to 1 (1) to disable the acceptance of INT/NMI. The above also applies when a bit manipulation instruction is used to set a specific register. Moreover, to ensure that the execution routine following release of the software STOP/IDLE mode is performed correctly, insert the NOP instruction as a dummy instruction (5). If the value of the ID bit of PSW does not change as the result of execution of the instruction to return the NP bit to 0 (4), insert two NOP instructions, and if the value of the ID bit of PSW changes, insert five NOP instructions. A description example is given below.

[Description example] : In case of PSC register

```
LDSR rX,5          ; NP bit = 1
ST.B  r0,PRCMD [r0] ; Write to PRCMD
ST.B  rD,PSC [r0]   ; PSC register setting
LDSR rY,5          ; NP bit = 0
NOP                ; Dummy instruction (2 or 5 instructions)
:
:
NOP
(next instruction) ; Execution routine following cancellation of software STOP/IDLE mode
:
:
```

rX: Value to be written to PSW

rY: Value to be written back to PSW

rD: Value to be set to PSC

When saving the value of PSW, the value of PSW prior to setting the NP bit must be transferred to the rY register.

2. The instructions ((4) interrupt disable cancel, (5) NOP instruction) following the store instruction for the specific register for setting the software STOP mode and IDLE mode are executed before a power save mode is entered.

(1) Command Register (PRCMD)

The command register (PRCMD) is a register used when write-accessing the special register to prevent incorrect writing to the special registers due to the erroneous program execution.

This register can be read/written in 8-bit units. It becomes undefined values in a read cycle.

Occurrence of illegal store operations can be checked by the PRERR bit of the SYS register.

	7	6	5	4	3	2	1	0		
PRCMD	REG7	REG6	REG5	REG4	REG3	REG2	REG1	REG0	Address FFFFFF170H	After reset Undefined

Bit Position	Bit Name	Function
7 to 0	REG7 to REG0	Registration Code
		Specific Register
		Registration Code
		CKC
		Arbitrary 8-bit data
		PSC
		Arbitrary 8-bit data

(2) System status register (SYS)

This register is allocated with status flags showing the operating state of the entire system. This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
SYS	0	0	0	PRERR	0	0	0	UNLOCK	Address FFFFFF078H	After reset 0000000XB

Bit Position	Bit Name	Function
4	PRERR	Protection Error Flag Indicates that writing to a special register has not be executed in the correct sequence, and protection error occurred. Accumulate flag 0 : Protection error does not occur. 1 : Protection error occurs.
0	UNLOCK	Unlock Status Flag Read-only flag. Indicates the PLL unlock state. (For details, refer to 6.4 PLL Stabilization .) 0 : Locked 1 : Unlocked

Operation conditions of PRERR Flag

- Set conditions:
(PRERR = "1")
 - (1) If the store instruction most recently executed to peripheral I/O does not write data to the PRCMD register, but to the specific register.
 - (2) If the first store instruction executed after the write operation to the PRCMD register is to a peripheral I/O register other than the specific registers.
- Reset conditions:
(PRERR = "0")
 - (1) When "0" is written to the PRERR flag of the SYS register.
 - (2) At system reset.

[MEMO]

CHAPTER 4 BUS CONTROL FUNCTION

The V854 is provided with an external bus interface function by which external memories such as ROM and RAM, and I/O can be connected.

4.1 Features

- 16-bit data bus
- Can be connected to external devices with pins having alternate function as port
- Wait function
 - Programmable wait function of up to 3 states per 2 blocks
 - External wait function through $\overline{\text{WAIT}}$ pin
- Idle state insertion function
- Bus mastership arbitration function
- Bus hold function

4.2 Bus Control Pins and Control Register

4.2.1 Bus control pins

The following pins are used for interfacing to external devices:

External Bus Interface Function	Corresponding Port (pins)
Address/data bus (AD0 to AD7)	Port 4 (P40 to P47)
Address/data bus (AD8 to AD15)	Port 5 (P50 to P57)
Address bus (A16 to A23)	Port 6 (P60 to P67)
Read/write control ($\overline{\text{LBEN}}$, $\overline{\text{UBEN}}$, R/W , $\overline{\text{DSTB}}$, $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, $\overline{\text{RD}}$)	Port 9 (P90 to P93)
Address strobe (ASTB)	Port 9 (P94)
Bus hold control ($\overline{\text{HLDRQ}}$, $\overline{\text{HLDK}}$)	Port 9 (P95, P96)
External wait control ($\overline{\text{WAIT}}$)	$\overline{\text{WAIT}}$

The bus interface function of each pin is enabled by the memory expansion mode register (MM). In ROM-less mode, the bus interface function of each pin is unconditionally enabled by the MODE input (n = 0 to 2). For the details of specifying an operation mode of the external bus interface, refer to **3.4.6 (1) Memory expansion mode register (MM)**.

4.2.2 Control register

(1) System control register (SYC)

This register switches control signals for bus interface.

The system control register can be read/written in 8- or 1-bit units.

SYC	7	6	5	4	3	2	1	0	Address	After reset
	0	0	0	0	0	0	0	BIC		
									FFFFF064H	00H (in single-chip mode 1, 2 and ROM-less mode 1) 01H (in ROM-less mode 2)

Bit Position	Bit Name	Function
1	BIC	Bus Interface Control Changes bus interface control signal 0 : $\overline{\text{DSTB}}$, R/W , $\overline{\text{UBEN}}$, $\overline{\text{LBEN}}$ signal outputs 1 : $\overline{\text{RD}}$, $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, $\overline{\text{UBEN}}$ signal outputs

$\overline{\text{RD}}$, $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, and $\overline{\text{UBEN}}$ signals are output immediately after reset in ROM-less mode 2.

4.3 Bus Access

4.3.1 Number of access clocks

The number of basic clocks necessary for accessing each resource is as follows:

Bus Cycle Type	Resource (bus width)			
	Internal ROM (32 bits)	Internal RAM (32 bits)	Internal Peripheral I/O (16 bits)	External Memory (16 bits)
Instruction fetch	1	3	Disabled	3 + n
Operand data access	3	1	3 + n	3 + n

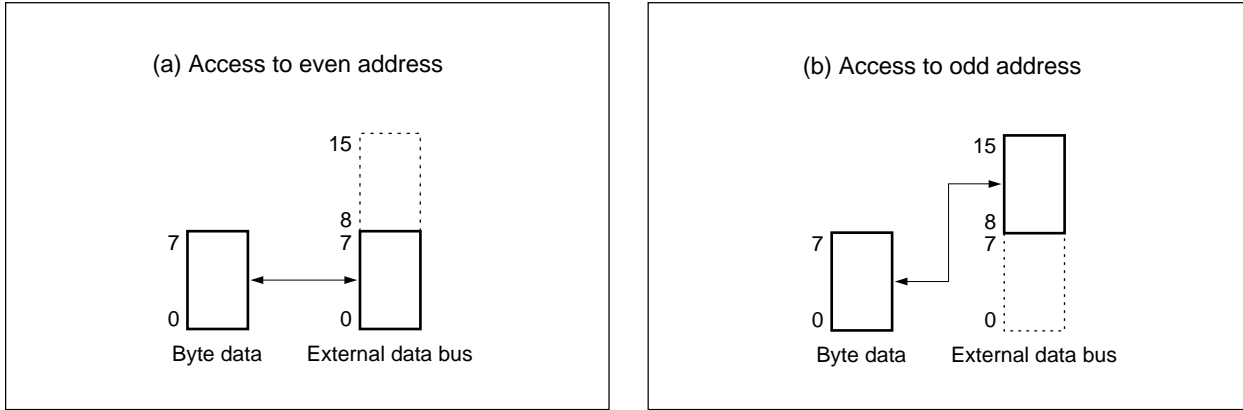
- Remarks**
1. Unit : clock/access
 2. n : number of wait insertions

4.3.2 Bus width

The V854 carries out peripheral I/O access and external memory access in 8-, 16-, or 32-bit. The following shows the operation for each access.

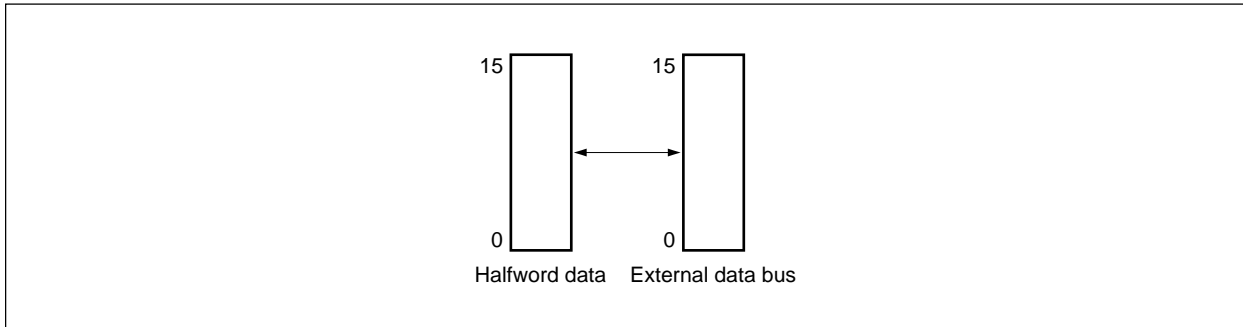
(1) Byte access (8 bits)

Byte access is divided into two types, the access to even address and the access to odd address.



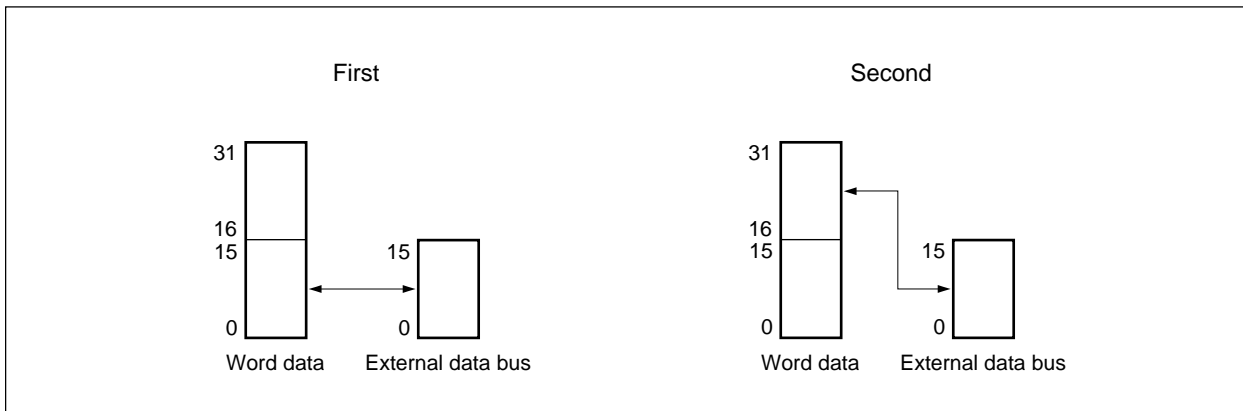
(2) Halfword access (16 bits)

In halfword access to external memory, data is dealt with as it is because the data bus is fixed to 16 bits.



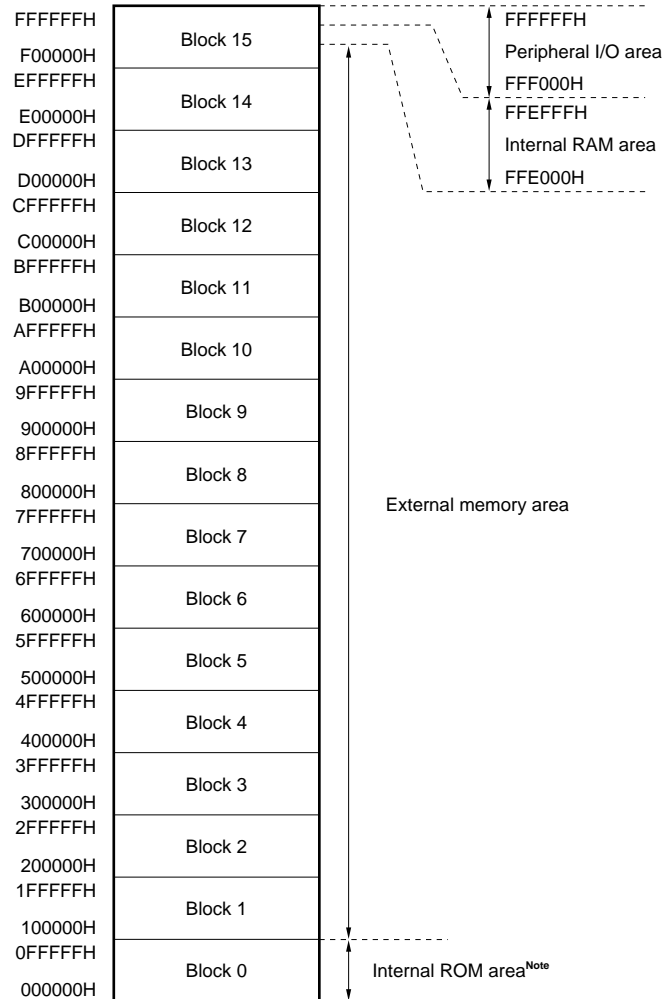
(3) Word access (32 bits)

In word access to external memory, lower halfword is accessed first and then the upper halfword is accessed.



4.4 Memory Block Function

The 16-Mbyte memory space is divided into memory blocks of 1-Mbyte units. The programmable wait function and bus cycle operation mode can be independently controlled for every two memory blocks.



Note In the ROM-less modes or for the μ PD703006, this area becomes the external memory area.

4.5 Wait Function

4.5.1 Programmable wait function

To facilitate interfacing with low-speed memories and I/O devices, up to 3 data wait states can be inserted in a bus cycle for two memory blocks. The number of wait states can be programmed by using data wait control register (DWC). Immediately after the system has been reset, three data wait states are automatically programmed for all memory blocks.

(1) Data wait control register (DWC)

This register can be read/written in 16-bit units.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
DWC	DW71	DW70	DW61	DW60	DW51	DW50	DW41	DW40	DW31	DW30	DW21	DW20	DW11	DW10	DW01	DW00	Address FFFFFF060H	After reset FFFFH

Bit Position	Bit Name	Function																		
15 to 0	DWn1 DWn0 (n = 0 to 7)	Data Wait Specifies number of wait states to be inserted																		
		<table><tr><th>DWn1</th><th>DWn0</th><th>Number of wait states to be inserted</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>2</td></tr><tr><td>1</td><td>1</td><td>3</td></tr></table>	DWn1	DWn0	Number of wait states to be inserted	0	0	0	0	1	1	1	0	2	1	1	3			
		DWn1	DWn0	Number of wait states to be inserted																
		0	0	0																
		0	1	1																
		1	0	2																
		1	1	3																
		<table><tr><th>n</th><th>Blocks into which wait states are inserted</th></tr><tr><td>0</td><td>Blocks 0/1</td></tr><tr><td>1</td><td>Blocks 2/3</td></tr><tr><td>2</td><td>Blocks 4/5</td></tr><tr><td>3</td><td>Blocks 6/7</td></tr><tr><td>4</td><td>Blocks 8/9</td></tr><tr><td>5</td><td>Blocks 10/11</td></tr><tr><td>6</td><td>Blocks 12/13</td></tr><tr><td>7</td><td>Blocks 14/15</td></tr></table>	n	Blocks into which wait states are inserted	0	Blocks 0/1	1	Blocks 2/3	2	Blocks 4/5	3	Blocks 6/7	4	Blocks 8/9	5	Blocks 10/11	6	Blocks 12/13	7	Blocks 14/15
		n	Blocks into which wait states are inserted																	
		0	Blocks 0/1																	
1	Blocks 2/3																			
2	Blocks 4/5																			
3	Blocks 6/7																			
4	Blocks 8/9																			
5	Blocks 10/11																			
6	Blocks 12/13																			
7	Blocks 14/15																			

- Cautions**
1. Block 0 is reserved for the internal ROM area in the single-chip mode. It is not subject to programmable wait control, regardless of the setting of DWC, and is always accessed without wait states.
 2. The internal RAM area of block 15 is not subject to programmable wait control and is always accessed without wait states. The peripheral I/O area of this block is not subject to programmable wait control, either. The only wait control is dependent upon the execution of each peripheral function.

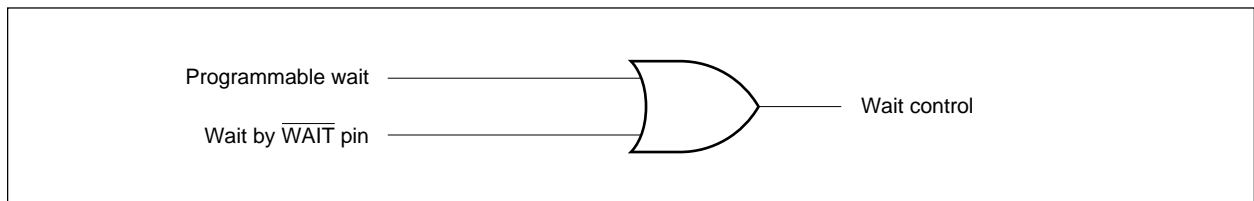
4.5.2 External wait function

When an extremely slow device, I/O, or asynchronous system is connected, any number of wait states can be inserted in a bus cycle by sampling the external wait pin ($\overline{\text{WAIT}}$) to synchronize with the external device.

The external $\overline{\text{WAIT}}$ signal does not affect the access times of the internal ROM, internal RAM, and peripheral I/O areas. Input of the external $\overline{\text{WAIT}}$ signal can be done asynchronously to CLKOUT and is sampled at the falling edge of the clock in the T2 and TW states of a bus cycle. If the set up and hold time of the $\overline{\text{WAIT}}$ input are not satisfied, the wait state may or may not be inserted in the next state.

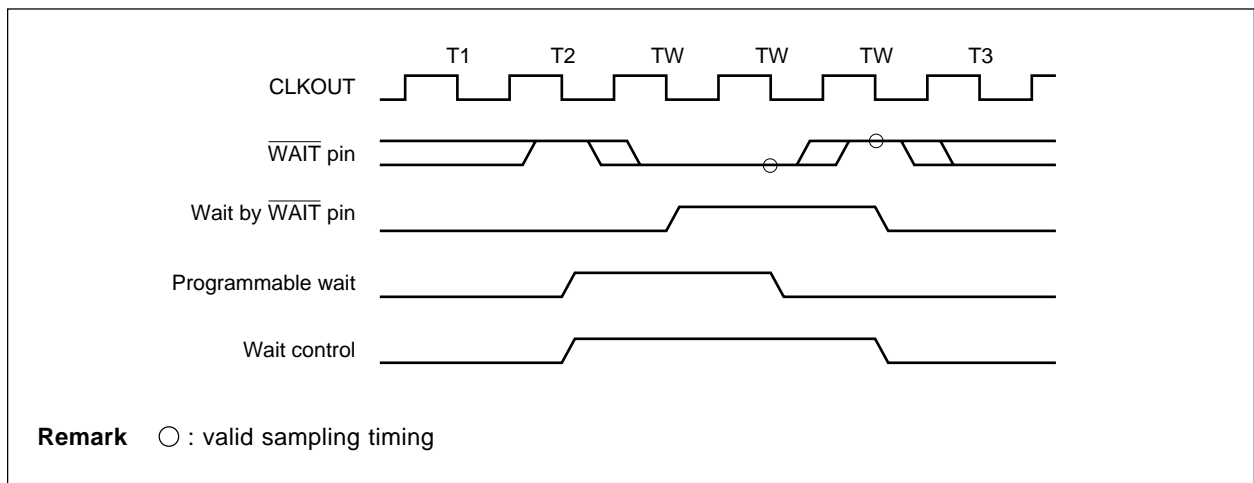
4.5.3 Relations between programmable wait and external wait

A wait cycle is inserted as a result of an OR operation between the wait cycle specified by the set value of programmable wait and the wait cycle controlled by the $\overline{\text{WAIT}}$ pin. In other words, the number of wait cycles is determined by the programmable wait value or the length of evaluation at the $\overline{\text{WAIT}}$ input pin.



For example, if the number of programmable wait states is 2 and the timing of the $\overline{\text{WAIT}}$ pin input signal is as illustrated below, three wait states will be inserted in the bus cycle.

Figure 4-1. Example of Inserting Wait States



4.6 Idle State Insertion Function

To facilitate interfacing with low-speed memory devices and meeting the data output float delay time (t_{DF}) on memory read accesses, one idle state (TI) can be inserted into the current bus cycle after the T3 state. The bus cycle following continuous bus cycles starts after one idle state.

Specifying insertion of the idle state is programmable by using the bus cycle control register (BCC).

Immediately after the system has been reset, idle state insertion is automatically programmed for all memory blocks.

(1) Bus cycle control register (BCC)

This register can be read/written in 16-bit units.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
BCC	BC71	0	BC61	0	BC51	0	BC41	0	BC31	0	BC21	0	BC11	0	BC01	0	
	Address FFFF062H																After reset AAAAH

Bit Position	Bit Name	Function																		
15, 13, 11, 9, 7, 5, 3, 1	BCn1 (n = 0 to 7)	<p>Bus Cycle</p> <p>Specifies insertion of idle state.</p> <p>0: Not inserted</p> <p>1: Inserted</p> <table><tr><th>n</th><th>Blocks into Which Idle State Is Inserted</th></tr><tr><td>0</td><td>Blocks 0/1</td></tr><tr><td>1</td><td>Blocks 2/3</td></tr><tr><td>2</td><td>Blocks 4/5</td></tr><tr><td>3</td><td>Blocks 6/7</td></tr><tr><td>4</td><td>Blocks 8/9</td></tr><tr><td>5</td><td>Blocks 10/11</td></tr><tr><td>6</td><td>Blocks 12/13</td></tr><tr><td>7</td><td>Blocks 14/15</td></tr></table>	n	Blocks into Which Idle State Is Inserted	0	Blocks 0/1	1	Blocks 2/3	2	Blocks 4/5	3	Blocks 6/7	4	Blocks 8/9	5	Blocks 10/11	6	Blocks 12/13	7	Blocks 14/15
n	Blocks into Which Idle State Is Inserted																			
0	Blocks 0/1																			
1	Blocks 2/3																			
2	Blocks 4/5																			
3	Blocks 6/7																			
4	Blocks 8/9																			
5	Blocks 10/11																			
6	Blocks 12/13																			
7	Blocks 14/15																			

- Cautions**
- Block 0 is reserved for the internal ROM area in the single-chip mode; therefore, no insertion of the idle state can be specified for block 0 regardless of the BCC settings.
 - The internal RAM area and peripheral I/O area of block 15 are not subject to insertion of the idle state.
 - Be sure to set bits 0, 2, 4, 6, 8, 10, 12, and 14 to 0. If these bits are set to 1, the operation is not guaranteed.

4.7 Bus Hold Function

4.7.1 Outline of function

When P95 and P96 of port 9 are programmed to be in the control mode, the functions of the $\overline{\text{HLDRQ}}$ and $\overline{\text{HLDK}}$ pins become valid.

When the $\overline{\text{HLDRQ}}$ pin becomes active (low) indicating that another bus master is requesting acquisition of the bus, the external address/data bus and strobe pins go into a high-impedance state, and the bus is released (bus hold status). When the $\overline{\text{HLDRQ}}$ pin becomes inactive (high) indicating that the request for the bus is cleared, these pins are driven again.

During bus hold period, the V854 continues internal operation until the next external memory access.

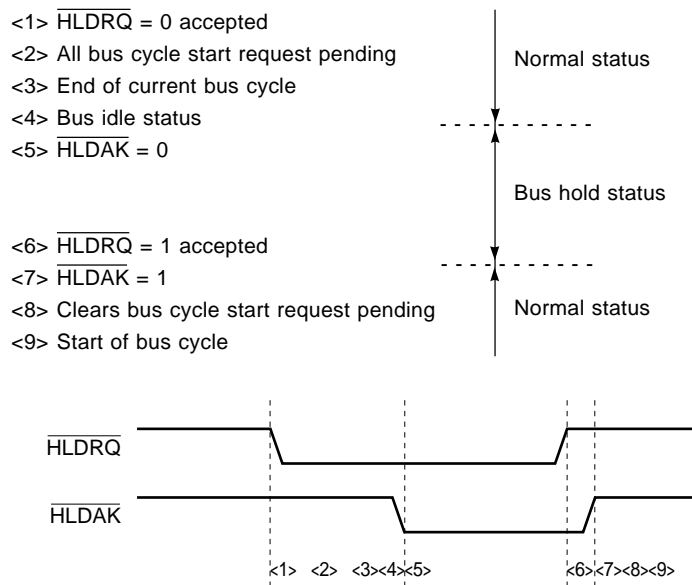
In the bus hold status, the $\overline{\text{HLDK}}$ pin becomes active (low).

This feature can be used to design a system where two or more bus masters exist, such as when multi-processor configuration is used and when a DMA controller is connected.

Bus hold request is not acknowledged between the first and the second word access. Bus hold request is also acknowledged between read access and write access in read modify write access of bit manipulation instruction.

4.7.2 Bus hold procedure

The procedure of the bus hold function is illustrated below.



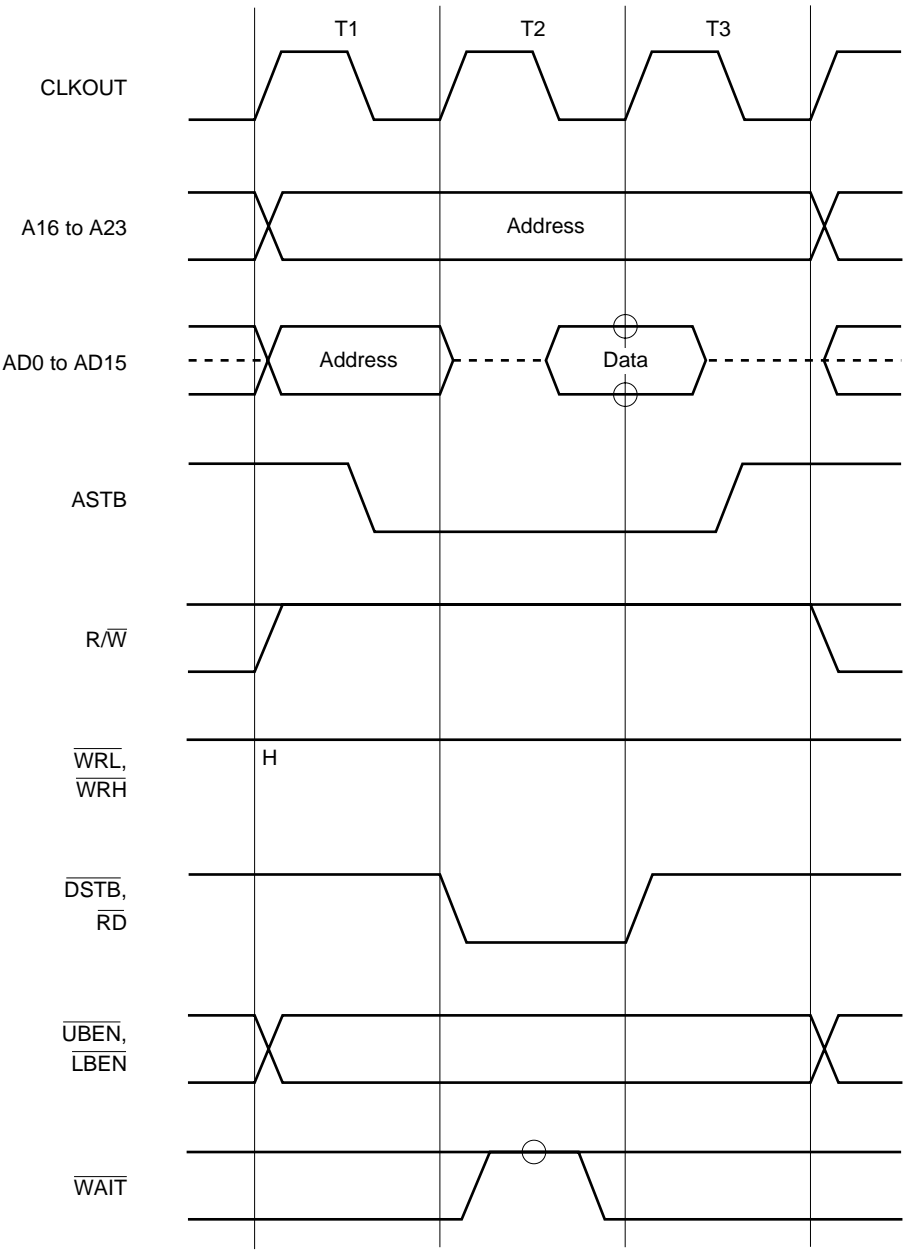
4.7.3 Operation in power save mode

In the STOP or IDLE mode, the system clock is stopped. Consequently, the bus hold status is not set even if the $\overline{\text{HLDRQ}}$ pin becomes active.

In the HALT mode, the $\overline{\text{HLDK}}$ pin immediately becomes active when the $\overline{\text{HLDRQ}}$ pin becomes active, and the bus hold status is set. When the $\overline{\text{HLDRQ}}$ pin becomes inactive, the $\overline{\text{HLDK}}$ pin becomes inactive. As a result, the bus hold status is cleared, and the HALT mode is set again.

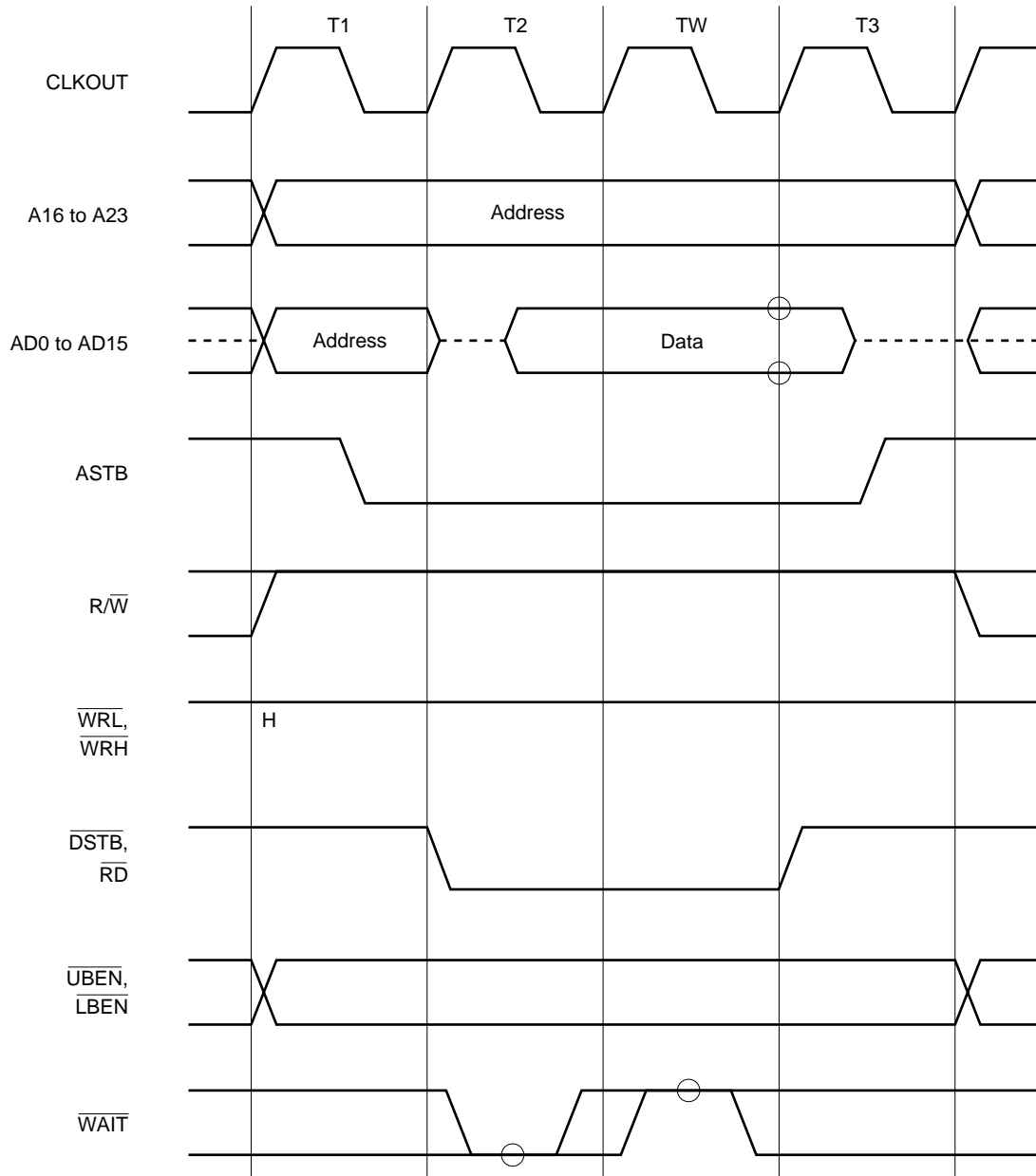
4.8 Bus Timing

(1) Memory read (0 wait)



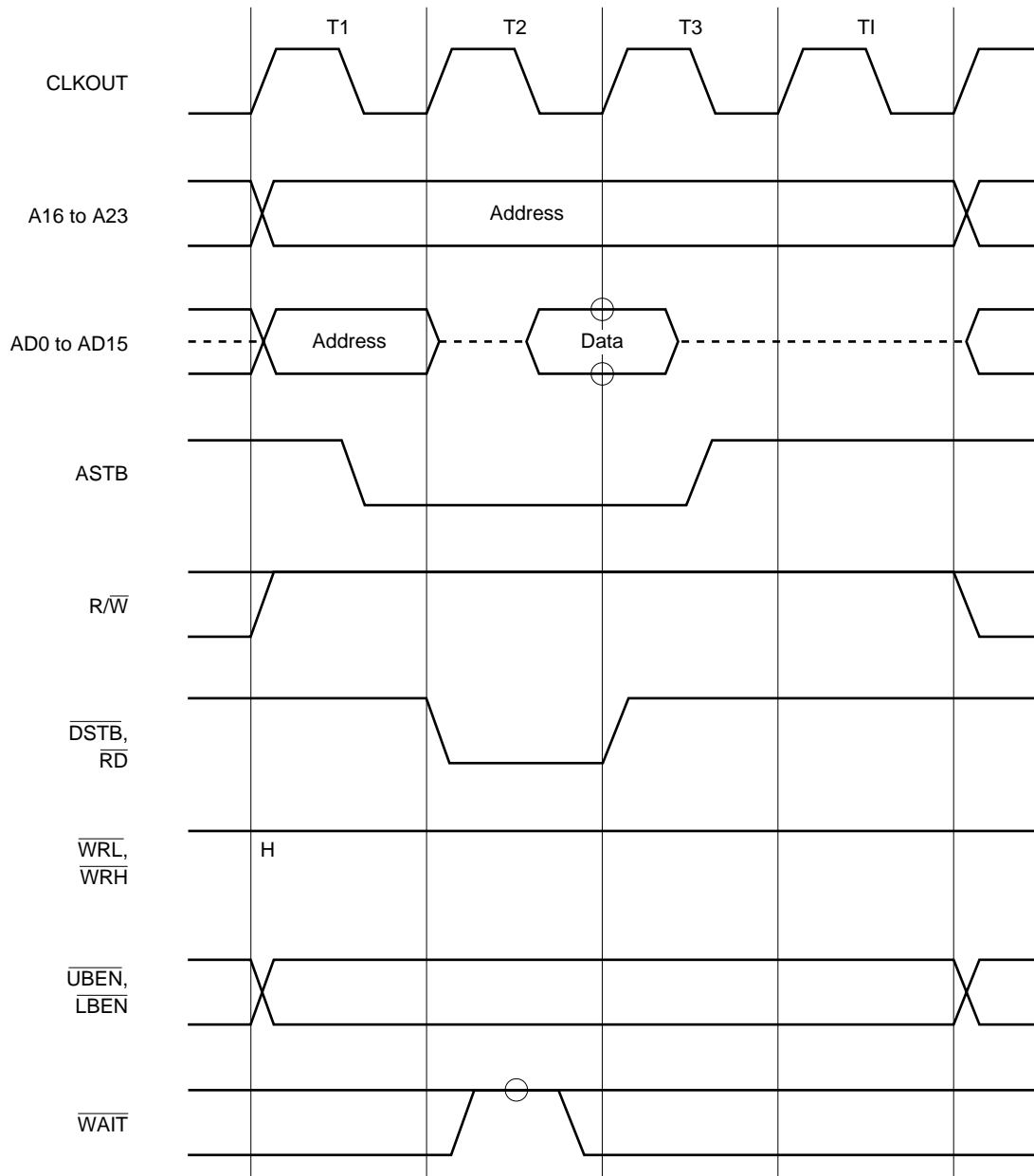
- Remarks**
- 1. ○ indicates the sampling timing when the number of programmable waits is set to 0.
 - 2. The dotted line indicates the high-impedance state.

(2) Memory read (1 wait)



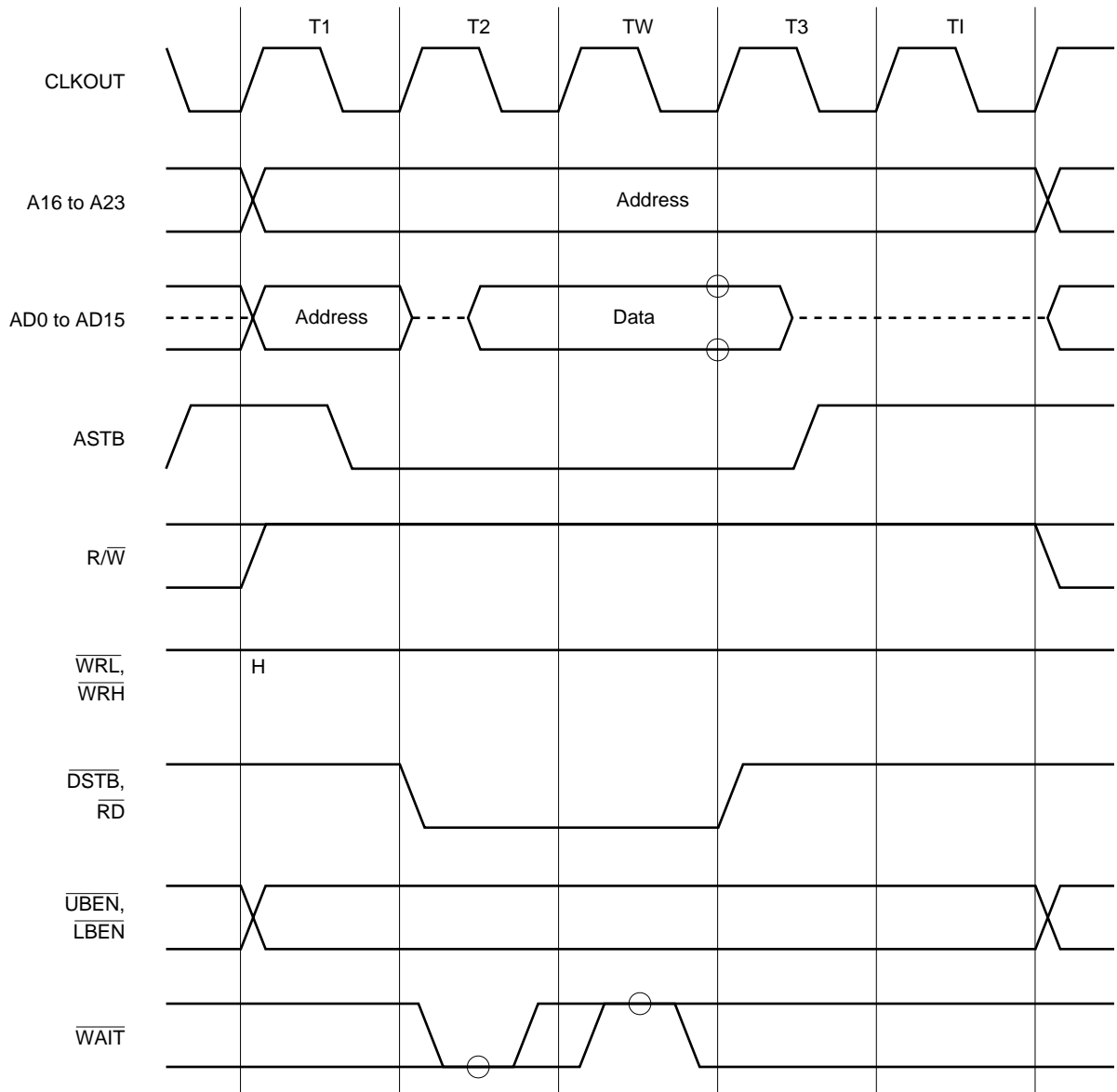
- Remarks**
- indicates the sampling timing when the number of programmable waits is set to 0.
 - The dotted line indicates the high-impedance state.

(3) Memory read (0 wait, idle state)



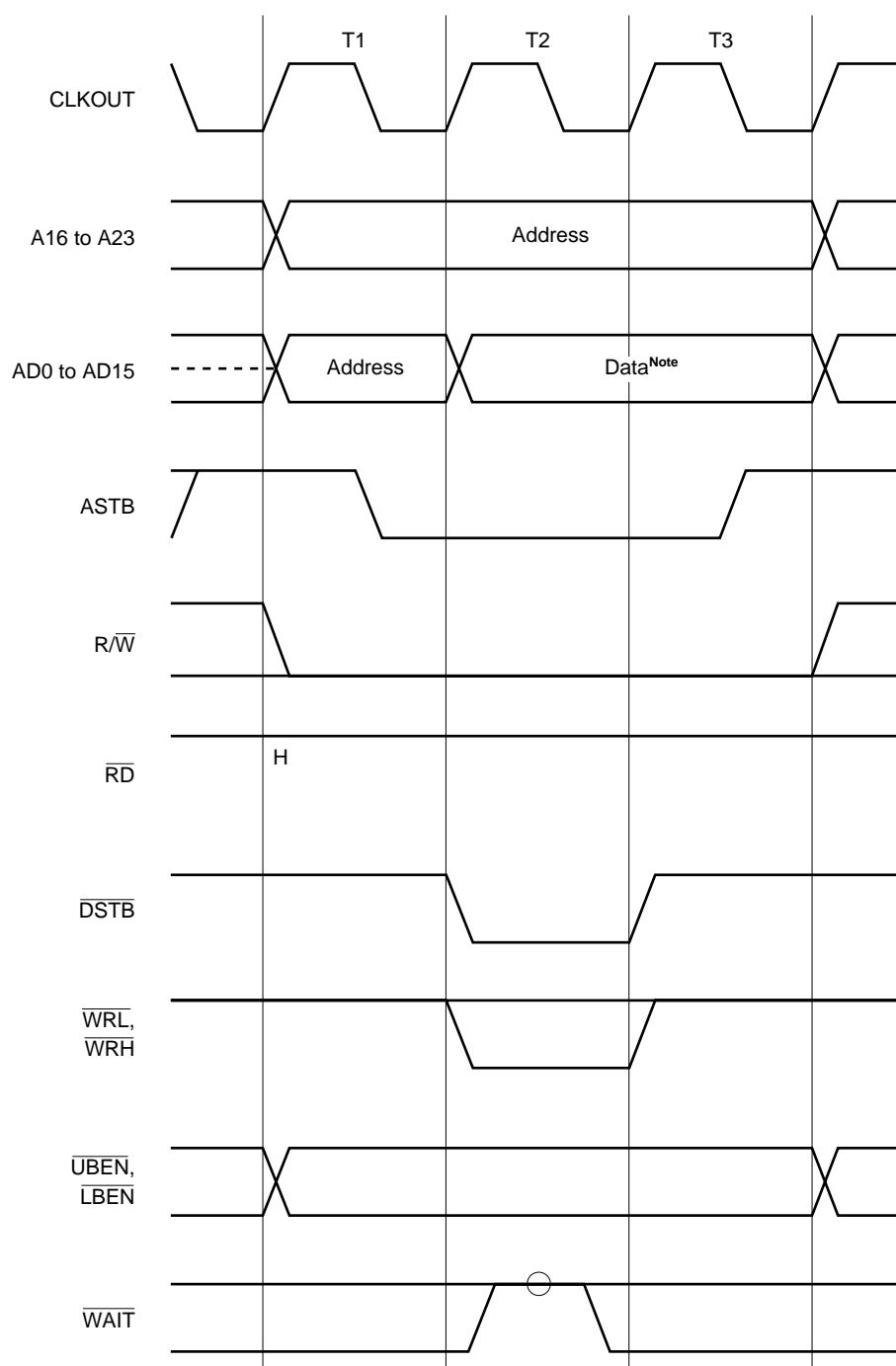
- Remarks**
1. ○ indicates the sampling timing when the number of programmable waits is set to 0.
 2. The dotted line indicates the high-impedance state.

(4) Memory read (1 wait, idle state)



- Remarks**
- indicates the sampling timing when the number of programmable waits is set to 0.
 - The dotted line indicates the high-impedance state.

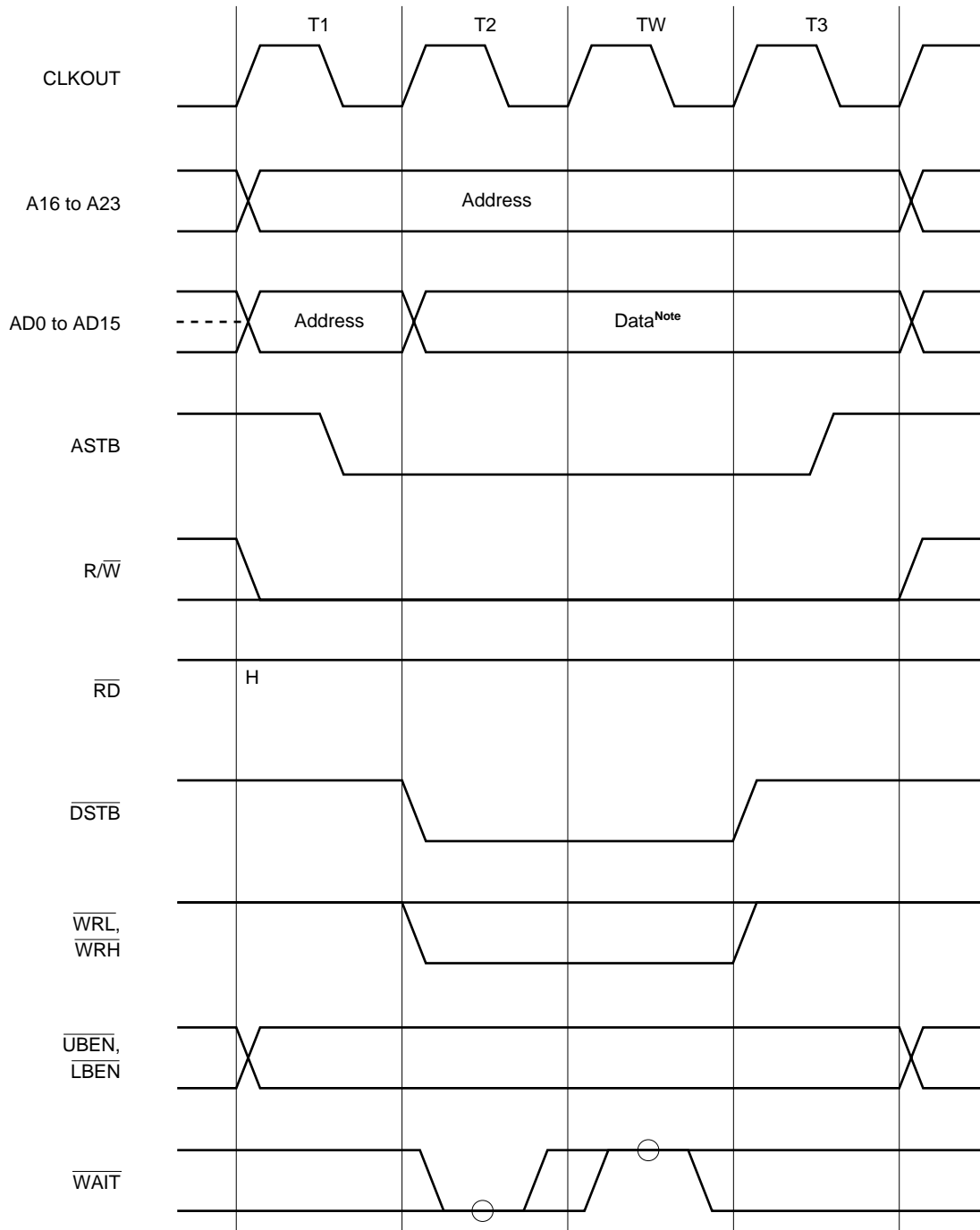
(5) Memory write (0 wait)



Note AD0 to AD7 output invalid data when odd address byte data is accessed.
AD8 to AD15 output invalid data when even address byte data is accessed.

Remarks 1. ○ indicates the sampling timing when the number of programmable waits is set to 0.
2. The dotted line indicates the high-impedance state.

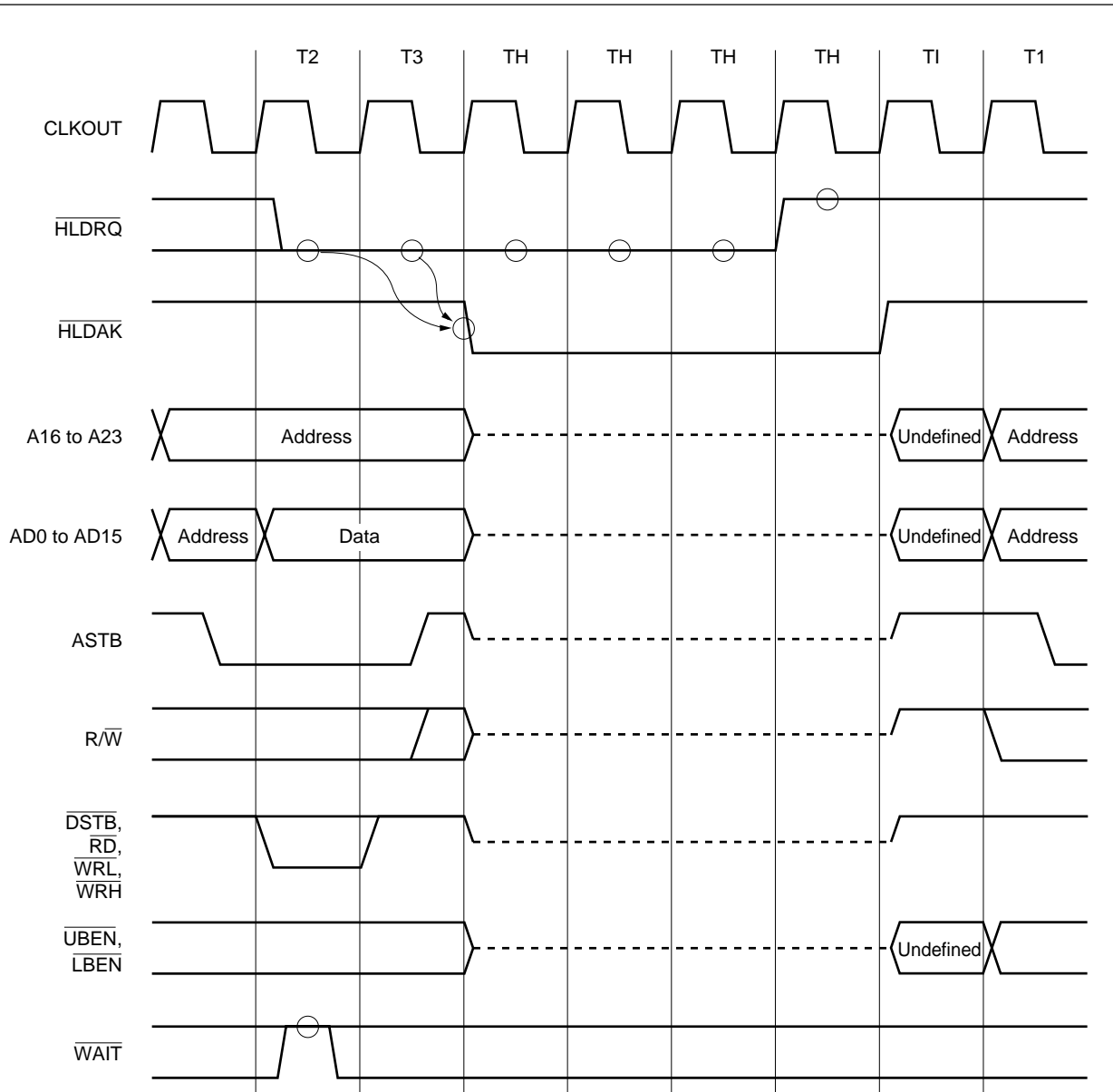
(6) Memory write (1 wait)



Note AD0 to AD7 output invalid data when odd address byte data is accessed.
AD8 to AD15 output invalid data when even address byte data is accessed.

Remarks 1. ○ indicates the sampling timing when the number of programmable waits is set to 0.
2. The dotted line indicates the high-impedance state.

(7) Bus hold timing



- Remarks**
1. ○ indicates the sampling timing.
 2. The dotted line indicates the high-impedance state.

Caution When the bus hold state is entered after the write cycle, a high-level signal may be briefly output from the $\overline{R/W}$ pin immediately before the $\overline{HLD A K}$ signal changes from the high level to the low level.

4.9 Bus Priority

There are four external bus cycles: bus hold, operand data access, instruction fetch (branch), and instruction fetch (continuous). The bus hold cycle is given the highest priority, followed by operand data access, instruction fetch (branch), and instruction fetch (continuous) in that order.

The instruction fetch cycle may be inserted in between the read access and write access of read-modify-write access.

No instruction fetch cycle and bus hold are inserted between the lower half-word access and higher half-word access of word operations.

Table 4-1. Bus Priority

External Bus Cycle	Priority
Bus hold	1
Operand data access	2
Instruction fetch (branch)	3
Instruction fetch (continuous)	4

4.10 Memory Boundary Operation Condition

4.10.1 Program space

- (1) Do not execute branch to the peripheral I/O area or continuous fetch from the internal RAM area to peripheral I/O area. Of course, it is impossible to fetch from external memory. If branch or instruction fetch is executed nevertheless, the NOP instruction code is continuously fetched.
- (2) A prefetch operation straddling over the peripheral I/O area (invalid fetch) does not take place if a branch instruction exists at the upper-limit address of the internal RAM area.

4.10.2 Data space

Only the address aligned at the half-word (when the least significant bit of the address is "0")/word (when the lowest 2 bits of the address are "0") boundary is accessed for data half-word (16 bits)/word (32 bits) long.

Therefore, access that straddles over the memory or memory block boundary does not take place.

For the details, refer to **V850 Family Architecture User's Manual**.

4.11 Internal Peripheral I/O Interface

Access to the internal peripheral I/O area is not output to the external bus. Therefore, the internal peripheral I/O area can be accessed in parallel with instruction fetch access.

Accesses to the internal peripheral I/O area takes, in most cases, three clock cycles. However, when accessing to certain timer/counter registers, wait may take place from 3 to 4 cycles.

Peripheral I/O Register	Access	Number of Waits	Number of Cycles
CC00 to CC03	Read	2	8
	Write	0/2	6/8
CC00L to CC03L, CC3	Read	1	4
	Write	0/1	3/4
CP10 to CP13, CM10 CM11, TM0, TM1	Read	2	8
	Write	0	6
CP10L, CP13L, CM10L, CM11L, TM0L, TM1L, CP3, TM3	Read	1	4
	Write	0	3
CM20 to CM24	Read	0/1	6/8
	Write	0/1	6/8
TM20 to TM24	Read	0/1	6/8
	Write	0	6
Others	Read	0	3
	Write	0	3

Remark In 32-bit access, two 16-bit accesses are executed. Therefore, the numbers of waits and cycles are twice those in 16-bit access.

CHAPTER 5 INTERRUPT/EXCEPTION PROCESSING FUNCTION

The V854 is provided with a dedicated interrupt controller (INTC) for interrupt processing and can process a total of 32 interrupt requests.

An interrupt is an event that occurs independently of program execution, and an exception is an event that occurs dependently on program execution. Generally, an exception takes precedence over an interrupt.

The V854 can process interrupt requests from the internal peripheral hardware and external sources. Moreover, exception processing can be started by the TRAP instruction (software exception) or by generation of an exception event (fetching of an illegal op code).

5.1 Features

- Interrupt
 - Non-maskable interrupt: 1 source
 - Maskable interrupt: 31 sources
 - 8 levels programmable priorities control
 - Multiple interrupt control according to priority
 - Mask specification for each maskable interrupt request
 - Noise elimination, edge detection, and valid edge of external interrupt request signal can be specified.
- Exception
 - Software exception: 32 sources
 - Exception trap: 1 source (illegal op code exception)

Interrupt/exception sources are listed in Table 5-1.

Table 5-1. Interrupt List (1/2)

Type	Classification	Interrupt/Exception Source				Default Priority	Exception Code	Vector Address	Restored PC
		Name	Control Register	Generating Source	Generating Unit				
Reset	Interrupt	RESET	—	Reset input	—	—	0000H	00000000H	Undefined
Non-maskable	Interrupt	NMI	—	NMI input	—	—	0010H	00000010H	nextPC
Software exception	Exception	TRAP0n ^{Note}	—	TRAP instruction	—	—	004n ^{Note} H	00000040H	nextPC
	Exception	TRAP1n ^{Note}	—	TRAP instruction	—	—	005n ^{Note} H	00000050H	nextPC
Exception trap	Exception	ILGOP	—	Illegal op code	—	—	0060H	00000060H	nextPC
Maskable	Interrupt	INTOV0/ INTP04/ INTP05	OVI0	Timer 0 overflow/ INTP04, INTP05 input	Pin/RPU	0	0080H	00000080H	nextPC
	Interrupt	INTOV1/ INTP14	OVI1	Timer 1 overflow/ INTP14 input	Pin/RPU	1	0090H	00000090H	nextPC
	Interrupt	INTP00/ INTCC00	CC0IC0	INTP00/CC00 coincidence	Pin/RPU	2	00A0H	000000A0H	nextPC
	Interrupt	INTP01/ INTCC01	CC0IC1	INTP01/CC01 coincidence	Pin/RPU	3	00B0H	000000B0H	nextPC
	Interrupt	INTP02/ INTCC02	CC0IC2	INTP02/CC02 coincidence	Pin/RPU	4	00C0H	000000C0H	nextPC
	Interrupt	INTP03/ INTCC03	CC0IC3	INTP03/CC03 coincidence	Pin/RPU	5	00D0H	000000D0H	nextPC
	Interrupt	INTCP10	P1IC0	INTP10 input	Pin	6	00E0H	000000E0H	nextPC
	Interrupt	INTCP11	P1IC1	INTP11 input	Pin	7	00F0H	000000F0H	nextPC
	Interrupt	INTCP12	P1IC2	INTP12 input	Pin	8	0100H	00000100H	nextPC
	Interrupt	INTCP13	P1IC3	INTP12/INTP13 input	Pin	9	0110H	00000110H	nextPC
	Interrupt	INTCM10	CM1IC0	CM10 coincidence	RPU	10	0120H	00000120H	nextPC
	Interrupt	INTCM11	CM1IC1	CM11 coincidence	RPU	11	0130H	00000130H	nextPC
	Interrupt	INTP20/ INTCM20	CM2IC0	INTP20/CM20 coincidence	Pin/RPU	12	0140H	00000140H	nextPC
	Interrupt	INTP21/ INTCM21	CM2IC1	INTP21/CM21 coincidence	Pin/RPU	13	0150H	00000150H	nextPC
	Interrupt	INTP22/ INTCM22	CM2IC2	INTP22/CM22 coincidence	Pin/RPU	14	0160H	00000160H	nextPC
	Interrupt	INTP23/ INTCM23	CM2IC3	INTP23/CM23 coincidence	Pin/RPU	15	0170H	00000170H	nextPC
	Interrupt	INTP24/ INTCM24	CM2IC4	INTP24/CM24 coincidence	Pin/RPU	16	0180H	00000180H	nextPC

Note n: value of 0 to FH

Remarks 1. Default Priority : Priority that takes precedence when two or more maskable interrupt requests occur at the same time. The highest priority is 0.

Restored PC : The value of the PC saved to EIPC or FEPC when interrupt/exception processing is started. However, the value of the PC saved when an interrupt is granted during the DIVH (division) instruction execution is the value of the PC of the current instruction (DIVH).

2. The execution address of the illegal instruction when an illegal op code exception occurs is calculated with (Restored PC – 4).

Table 5-1. Interrupt List (2/2)

Type	Classification	Interrupt/Exception Source				Default Priority	Exception Code	Vector Address	Restored PC
		Name	Control Register	Generating Source	Generating Unit				
Maskable	Interrupt	INTP30/ INTCC3	CC3IC0	INTP30/CC3 coincidence	Pin/RPU	17	0190H	00000190H	nextPC
	Interrupt	INTCSI0	CSIC0	CSI0 transmission/ reception completion	CSI	18	01A0H	000001A0H	nextPC
	Interrupt	INTCSI1	CSIC1	CSI1 transmission/ reception completion	CSI	19	01B0H	000001B0H	nextPC
	Interrupt	INTCSI2	CSIC2	CSI2 transmission/ reception completion	CSI	20	01C0H	000001C0H	nextPC
	Interrupt	INTCSI3	CSIC3	CSI3 transmission/ reception completion	CSI	21	01D0H	000001D0H	nextPC
	Interrupt	INTIIC	IIC0	I ² C interrupt	I ² C	22	01E0H	000001E0H	nextPC
	Interrupt	INTSER	SEIC0	UART reception error	UART	23	01F0H	000001F0H	nextPC
	Interrupt	INTSR	SRIC0	UART reception completion	UART	24	0200H	00000200H	nextPC
	Interrupt	INTST	STIC0	UART transmission completion	UART	25	0210H	00000210H	nextPC
	Interrupt	INTAD	ADIC0	A/D conversion end	ADC	26	0220H	00000220H	nextPC
	Interrupt	INTP50	P5IC0	INTP50 input	Pin	27	0230H	00000230H	nextPC
	Interrupt	INTP51	P5IC1	INTP51 input	Pin	28	0240H	00000240H	nextPC
	Interrupt	INTP52	P5IC2	INTP52 input	Pin	29	0250H	00000250H	nextPC
	Interrupt	INTP53	P5IC3	INTP53 input	Pin	30	0260H	00000260H	nextPC

Remarks 1. Default Priority : Priority that takes precedence when two or more maskable interrupt requests occur at the same time. The highest priority is 0.

Restored PC : The value of the PC saved to EIPC or FEPC when interrupt/exception processing is started. However, the value of the PC saved when an interrupt is granted during the DIVH (division) instruction execution is the value of the PC of the current instruction (DIVH).

2. The execution address of the illegal instruction when an illegal op code exception occurs is calculated with (Restored PC – 4).

5.2 Non-Maskable Interrupt

The non-maskable interrupt is accepted unconditionally, even when interrupts are disabled (DI states) in the interrupt disabled (DI) status. The NMI is not subject to priority control and takes precedence over all the other interrupts.

The non-maskable interrupt request is input from the NMI pin. When the valid edge specified by bit 0 (ESN0) of the external interrupt mode register 0 (INTM0) is detected on the NMI pin, the interrupt occurs.

While the service routine of the non-maskable interrupt is being executed (PSW.NP = 1), the acceptance of another non-maskable interrupt request is kept pending. The pending NMI is accepted after the original service routine of the non-maskable interrupt under execution has been terminated (by the RETI instruction), or when PSW.NP is cleared to 0 by the LDSR instruction. Note that if two or more NMI requests are input during the execution of the service routine for an NMI, the number of NMIs that will be acknowledged after PSW.NP goes to "0", is only one.

The operation at the execution of pending non-maskable interrupt request differs depending on the V854 operation mode.

(1) In single-chip mode

The operation is returned to the main routine once and at least one instruction in the main routine is executed between the end of the first non-maskable interrupt processing and the start of the pending non-maskable interrupt processing.

(2) In ROM-less mode

The pending non-maskable interrupt processing starts following the end of the first non-maskable interrupt processing. The operation is not returned to the main routine.

5.2.1 Operation

If the non-maskable interrupt is generated by NMI input, the CPU performs the following processing, and transfers control to the handler routine:

- (1) Saves the restored PC to FEPC.
- (2) Saves the current PSW to FEPSW.
- (3) Writes exception code 0010H to the higher half-word (FECC) of ECR.
- (4) Sets the NP and ID bits of PSW and clears the EP bit.
- (5) Loads the handler address (00000010H) of the non-maskable interrupt routine to the PC, and transfers control.

Figure 5-1 illustrates how the non-maskable interrupt is processed.

Figure 5-1. Non-Maskable Interrupt Processing

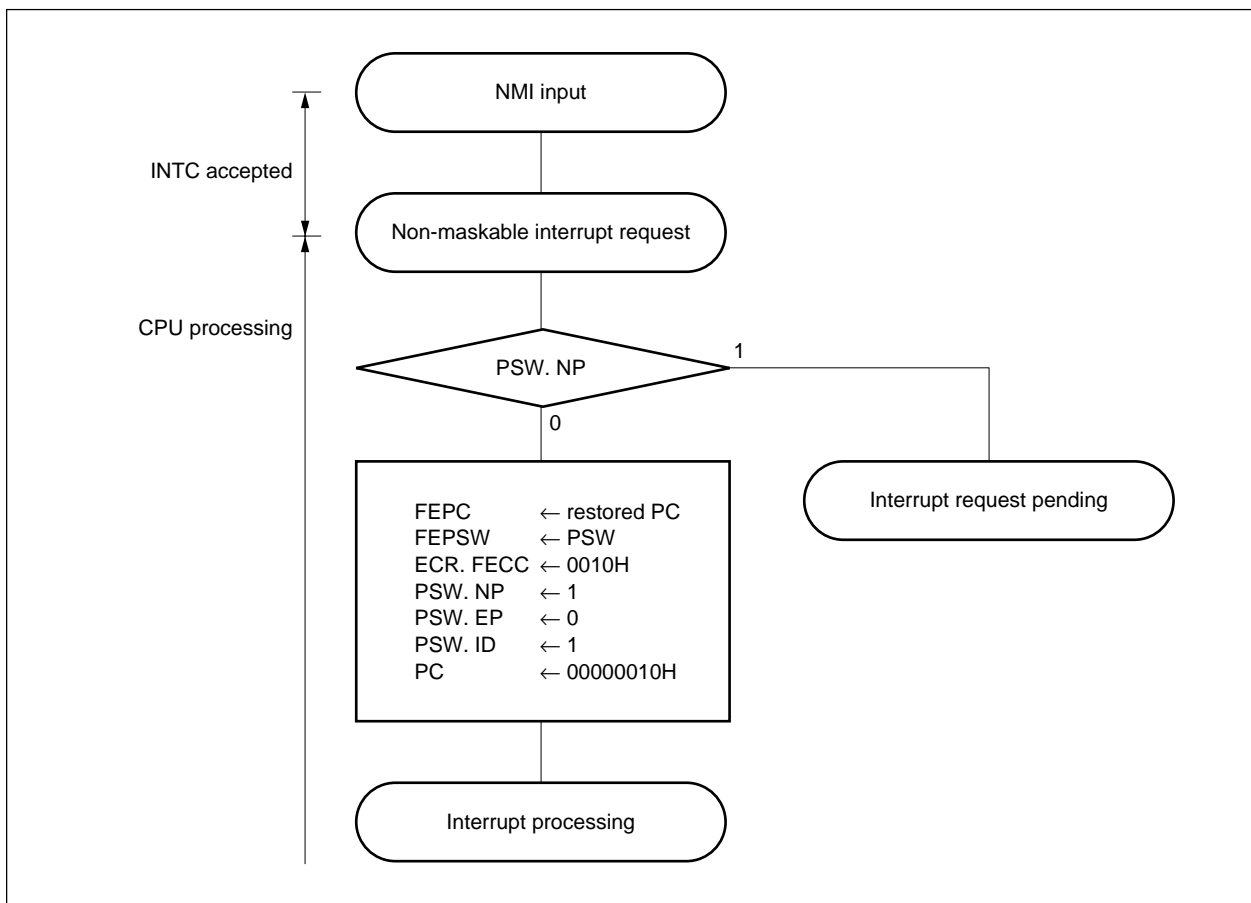
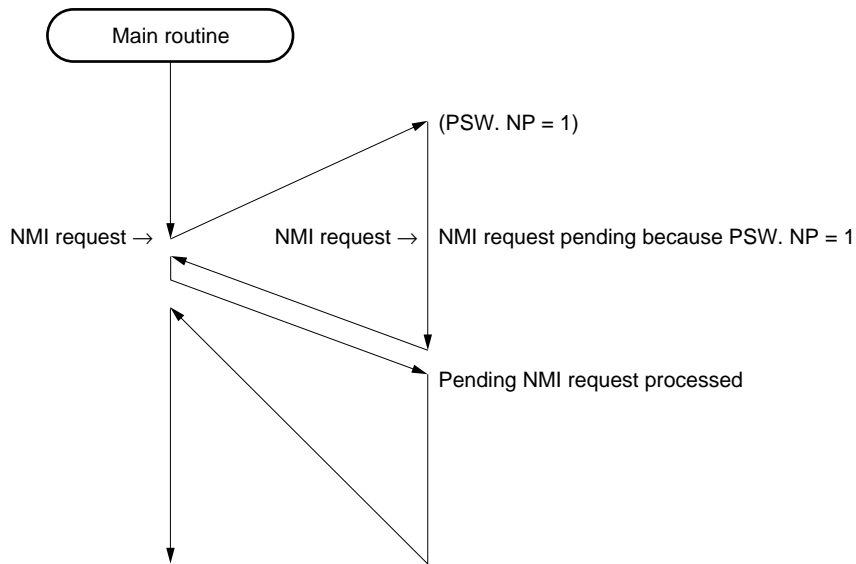
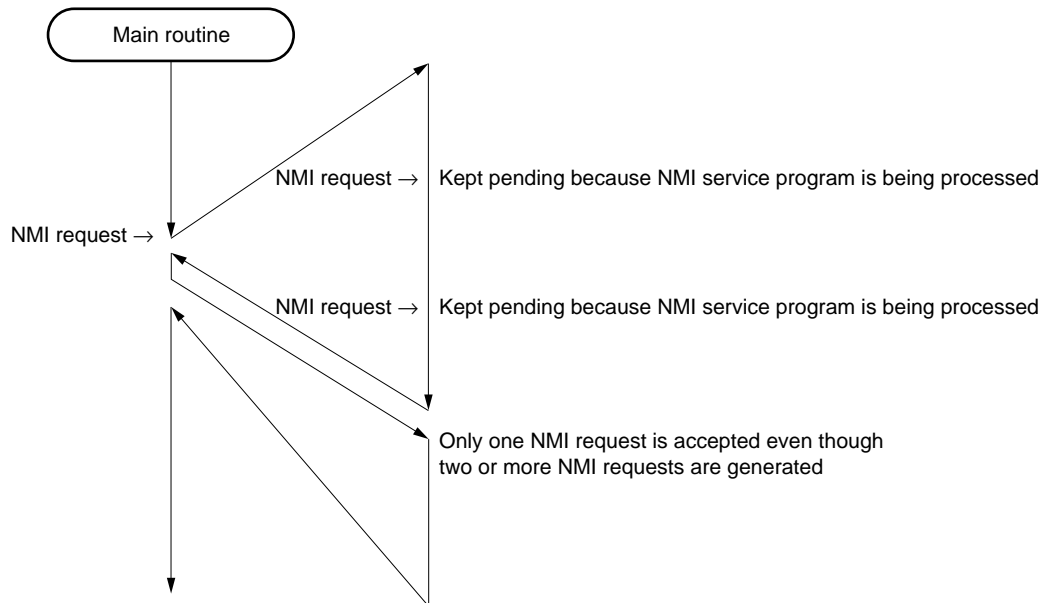


Figure 5-2. Accepting Non-Maskable Interrupt Request

(a) If a new NMI request is generated while an NMI service routine is executing:



(b) If a new NMI request is generated twice while an NMI service routine is executing:



5.2.2 Restore

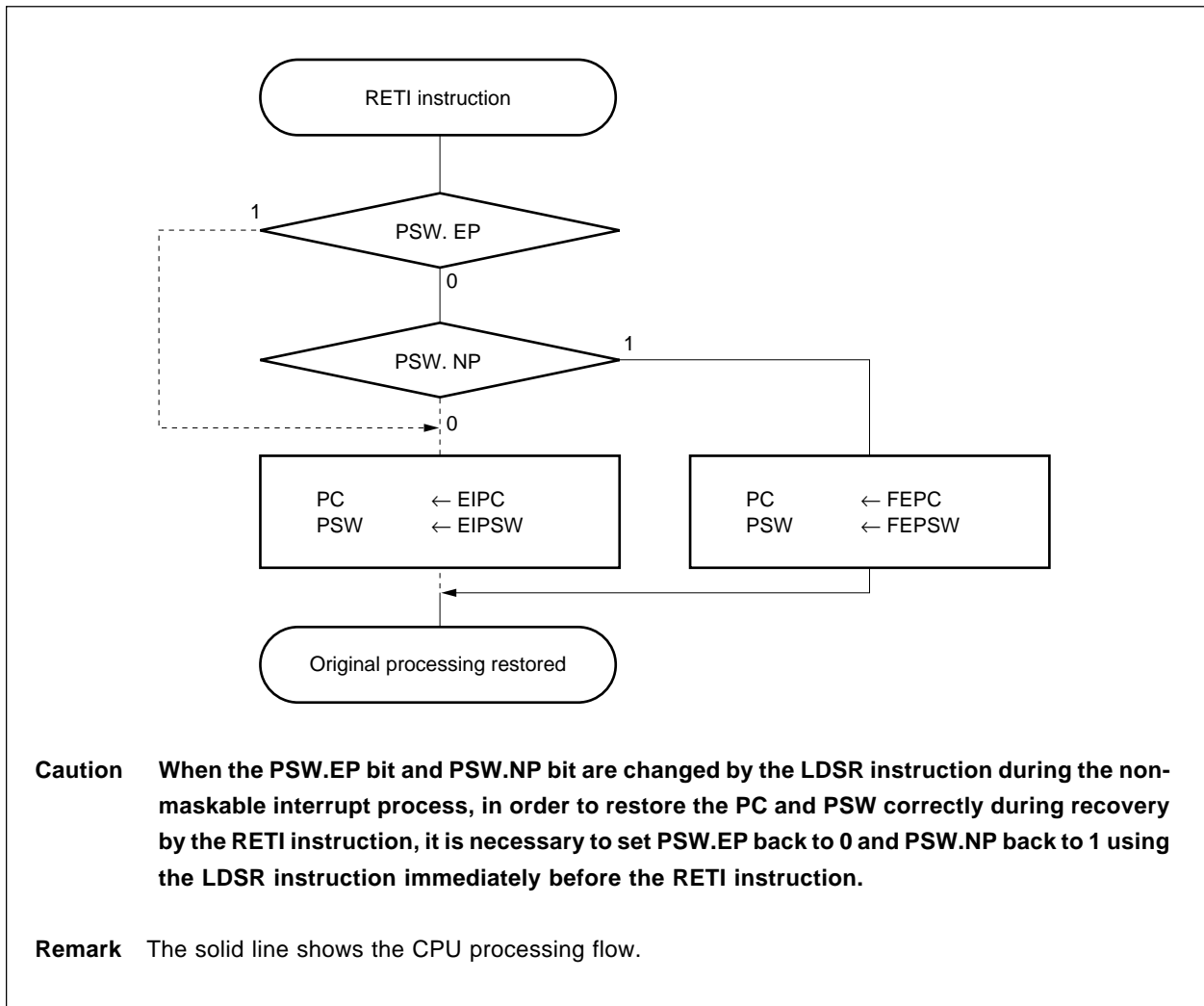
Execution is restored from the non-maskable interrupt processing by the RETI instruction.

When the RETI instruction is executed, the CPU performs the following processing, and transfers control to the address of the restored PC.

- (1) Restores the values of PC and PSW from FEPC and FEPSW, respectively, because the EP bit of PSW is 0 and the NP bit of PSW is 1.
- (2) Transfers control back to the restored PC address and PSW status.

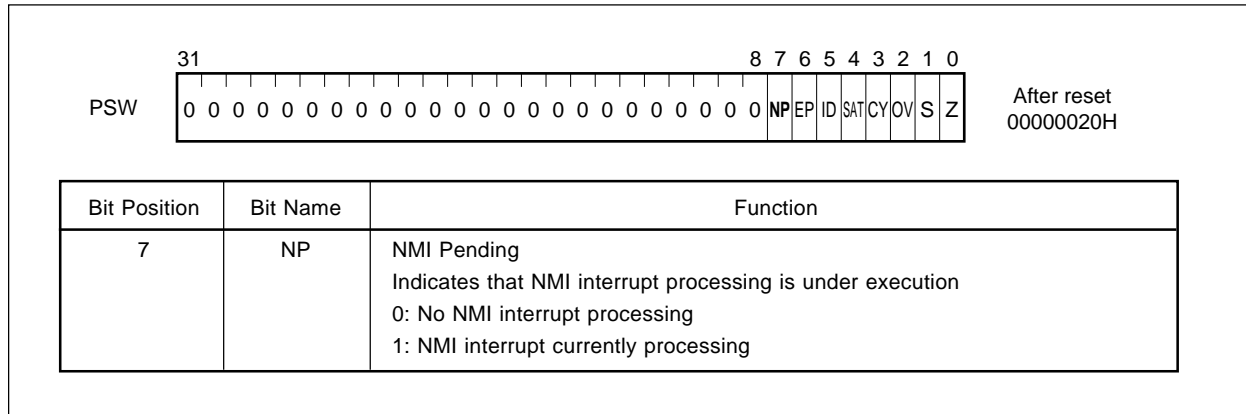
Figure 5-3 illustrates how the RETI instruction is processed.

Figure 5-3. RETI Instruction Processing



5.2.3 Non-maskable interrupt status flag (NP)

The NP flag is a status flag that indicates that non-maskable interrupt (NMI) processing is under execution. This flag is set when all the interrupts and requests have been accepted, and masks all interrupt requests and exceptions to prohibit multiple interrupts from being acknowledged.



5.2.4 Noise elimination circuit of NMI pin

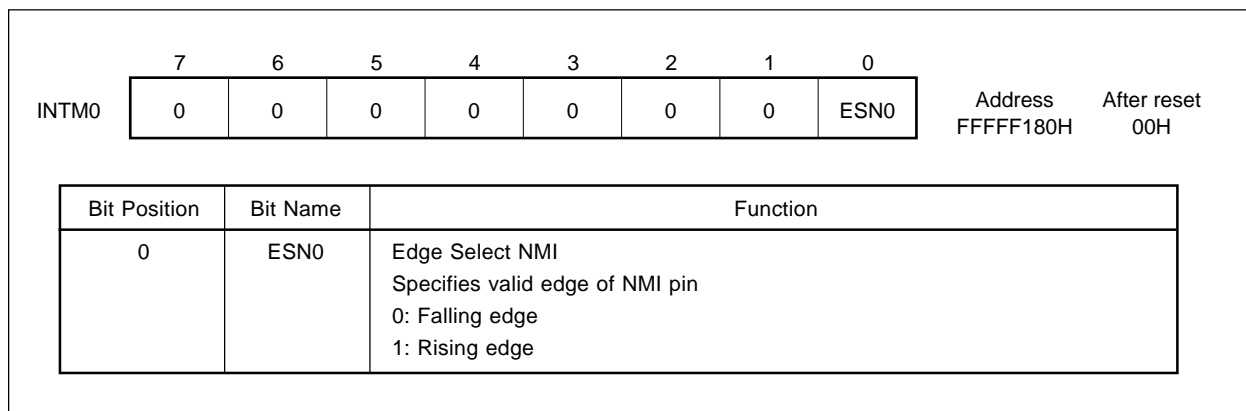
NMI pin noise is eliminated with analog delay. The delay time is 60 to 220 ns. The signal input that changes in less than this time period is not internally acknowledged.

NMI pin is used for canceling the software stop mode. In the software stop mode, noise elimination does not use system clock for noise elimination because the internal system clock is stopped.

5.2.5 Edge detection function of NMI pin

INTM0 is a register that specifies the valid edge of the non-maskable interrupt (NMI). The valid edge of NMI can be specified as the rising or falling edge by the ESN0 bit of this register.

This register can be read or written in 8- or 1-bit units.



5.3 Maskable Interrupts

Maskable interrupt requests can be masked by interrupt control registers. The V854 has 31 maskable interrupt sources.

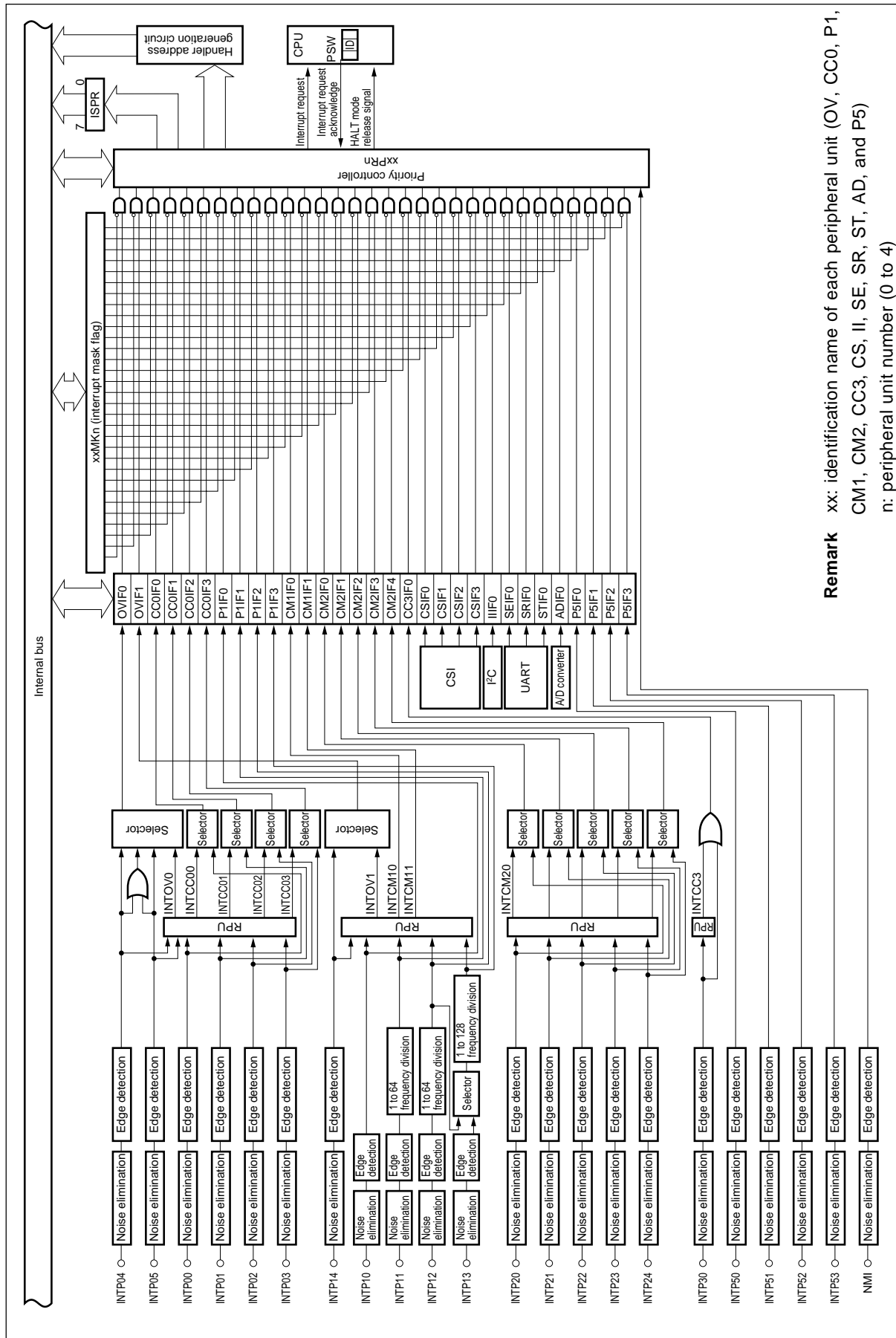
If two or more maskable interrupt requests are generated at the same time, they are accepted according to the default priority. In addition to the default priority, eight levels of priorities can be specified by using the interrupt control registers, allowing programmable priority control.

When an interrupt request has been acknowledged, the acceptance of other maskable interrupts is disabled and the interrupt disabled (DI) status is set.

When the EI instruction is executed in an interrupt processing routine, the interrupt enabled (EI) status is set which enables interrupts having a higher priority to immediately interrupt the current service routine in progress. Note that only interrupts with a higher priority will have this capability; interrupts with the same priority level cannot be nested.

To use multiple interrupts, it is necessary to save EIPC and EIPSW to memory or a register before executing the EI instruction, and restore EIPC and EIPSW to the original values by executing the DI instruction before the RETI instruction.

Figure 5-4. Block Diagram of Maskable Interrupt



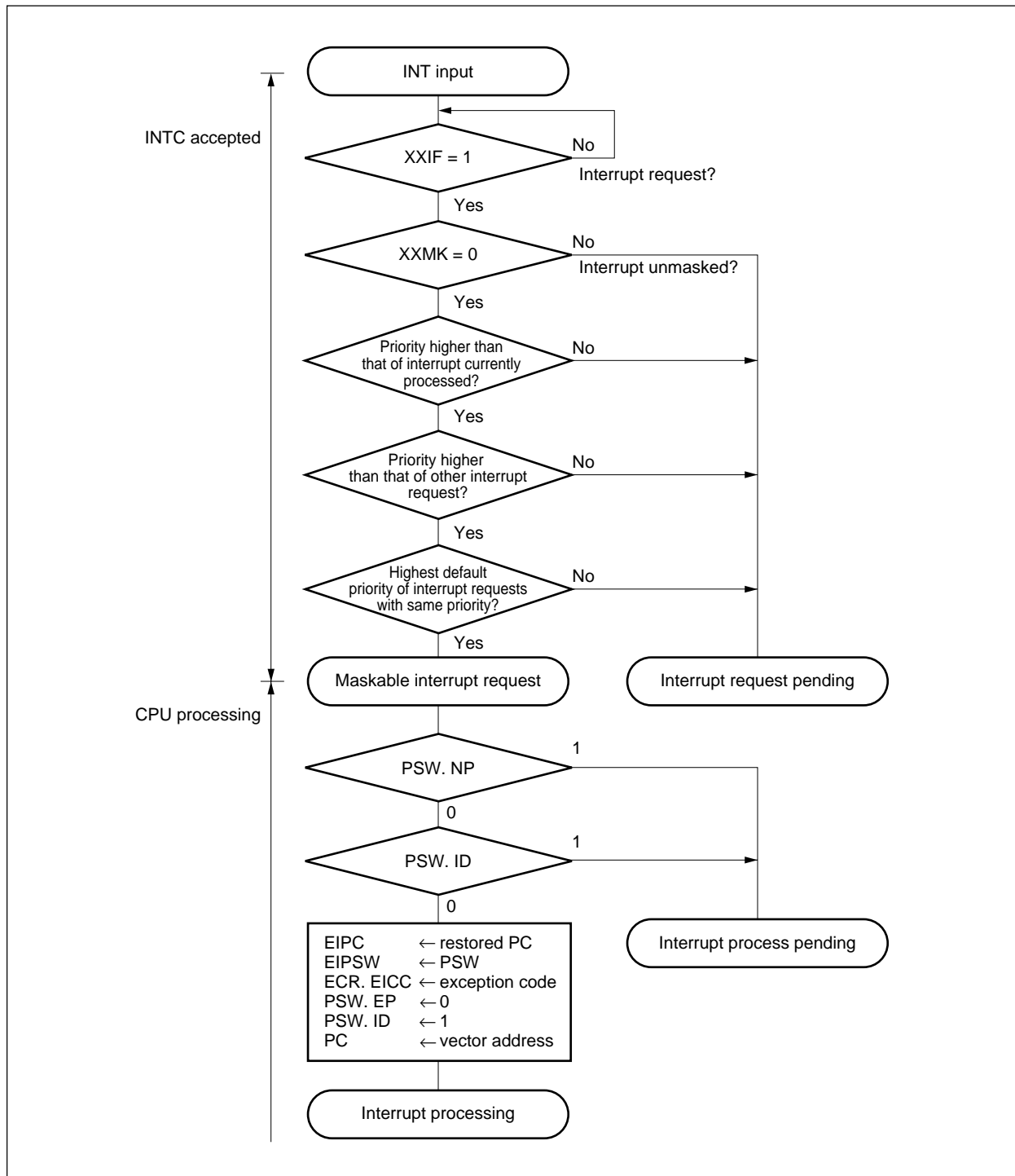
5.3.1 Operation

If a maskable interrupt occurs, the CPU performs the following processing, and transfers control to a handler routine:

- (1) Saves the restored PC to EIPC.
- (2) Saves the current PSW to EIPSW.
- (3) Writes an exception code to the lower half-word of ECR (EICC).
- (4) Sets the ID bit of PSW and clears the EP bit.
- (5) Loads the corresponding handler address to the PC, and transfers control.

Figure 5-5 illustrates how the maskable interrupts are processed.

Figure 5-5. Maskable Interrupt Processing



The INT input masked by the interrupt controllers and the INT input that occurs while the other interrupt is being processed (when PSW.NP = 1 or PSW.ID = 1) are internally pending by the interrupt controller. When the interrupts are unmasked, or when PSW.NP = 0 and PSW.ID = 0 by using the RETI and LDSR instructions, the pending INT input starts the new maskable interrupt processing.

5.3.2 Restore

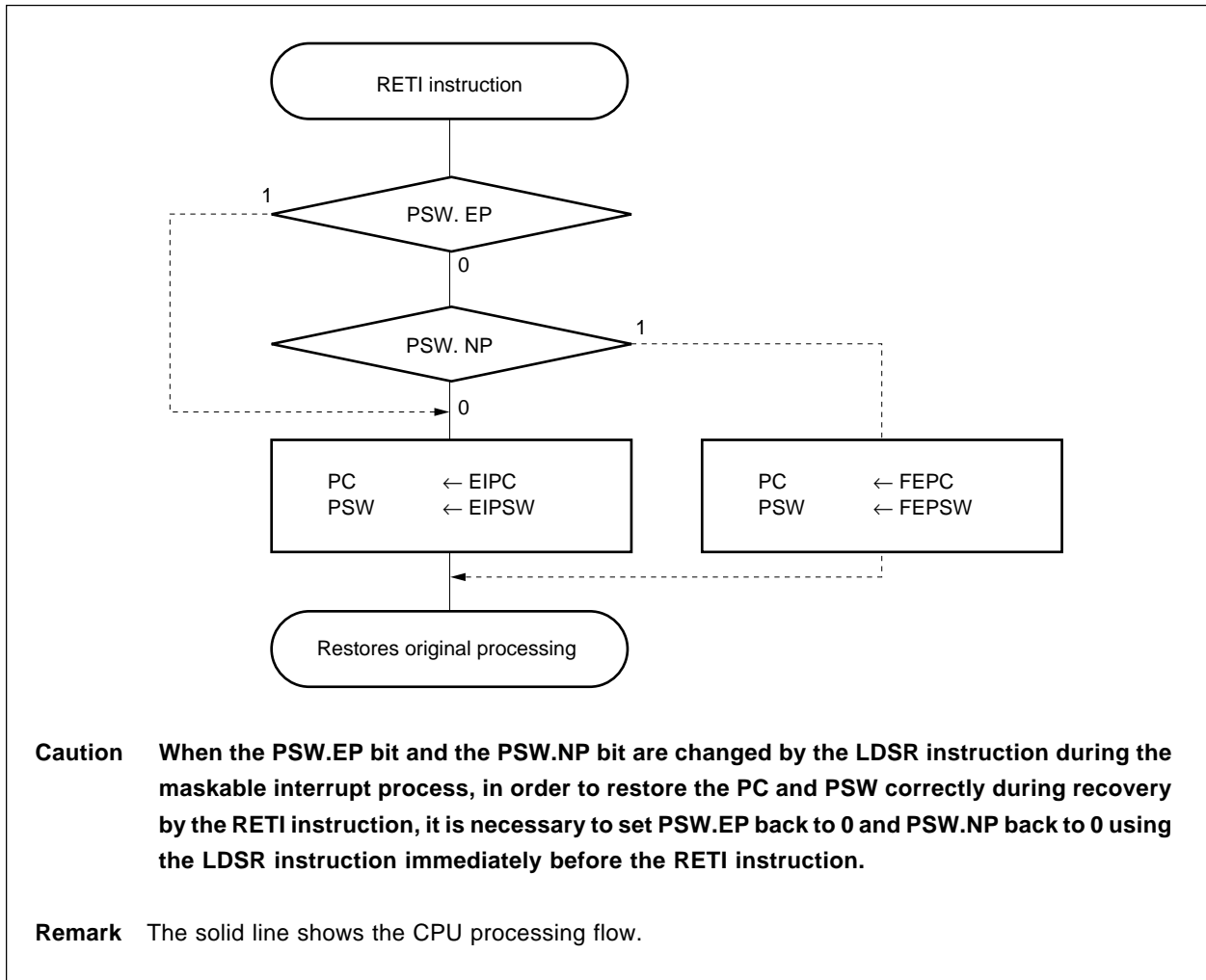
To restore execution from the maskable interrupt processing, the RETI instruction is used.

When the RETI instruction is executed, the CPU performs the following steps, and transfers control to the address of the restored PC.

- (1) Restores the values of PC and PSW from EIPC and EIPSW because the EP bit of PSW is 0 and the NP bit of PSW is 0.
- (2) Transfers control to the restored PC address and PSW status.

Figure 5-6 illustrates the processing of the RETI instruction.

Figure 5-6. RETI Instruction Processing



5.3.3 Priorities of maskable interrupts

The V854 provides multiple interrupt service that accepts an interrupt while servicing another interrupt. Multiple interrupts can be controlled by priority levels.

There are two types of priority level control: control based on the default priority levels, and control based on the programmable priority levels that are specified by the interrupt priority level specification bits (xxPRn0 to xxPRn2) of the interrupt control register (xxICn). When two or more interrupts having the same priority level specified by the xxPRn0 to xxPRn2 are generated at the same time, the control based on default priority levels services them in the order of the priority level allocated to each interrupt request type (default priority level) beforehand. For more information refer to **Table 5-1**. The programmable priority control customizes interrupt requests into eight levels by setting the priority level specification flag.

The relation between the programmable priority levels and default priority levels is as follows.

Programmable priority levels > Default priority levels

Note that when an interrupt is acknowledged, the ID flag of PSW is automatically set to “1”. Therefore, when multiple interrupts are to be used, clear the ID flag to “0” beforehand (for example, by placing the EI instruction into the interrupt service program) to set the interrupt enable mode.

Remarks xx : Each peripheral unit identifier (OV, CC0, P1, CM1, CM2, CC3, CS, II, SE, SR, ST, AD, P5)
n : Peripheral unit number (0 to 4)

Figure 5-7. Example of Interrupt Nesting Process (1/2)

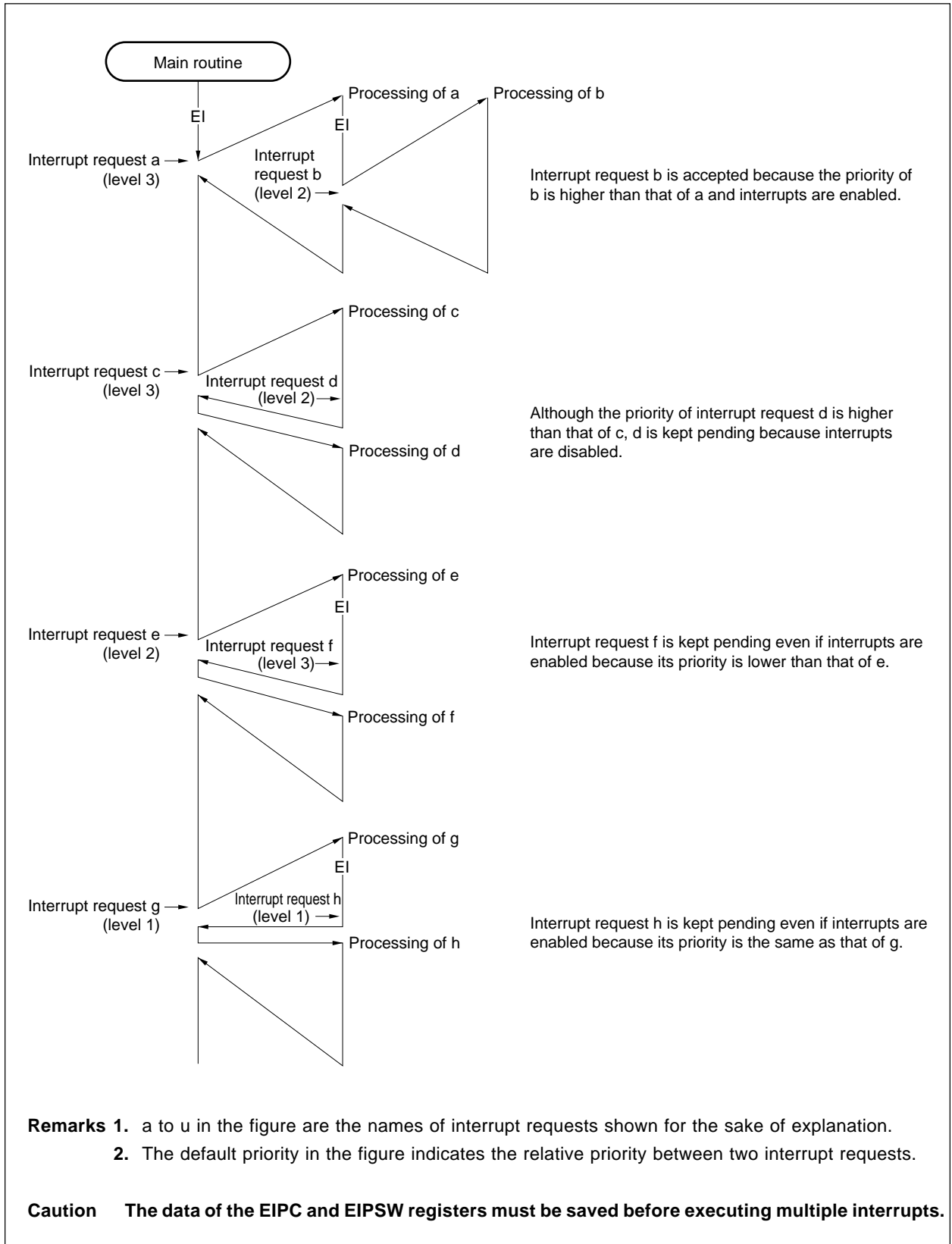


Figure 5-7. Example of Interrupt Nesting Process (2/2)

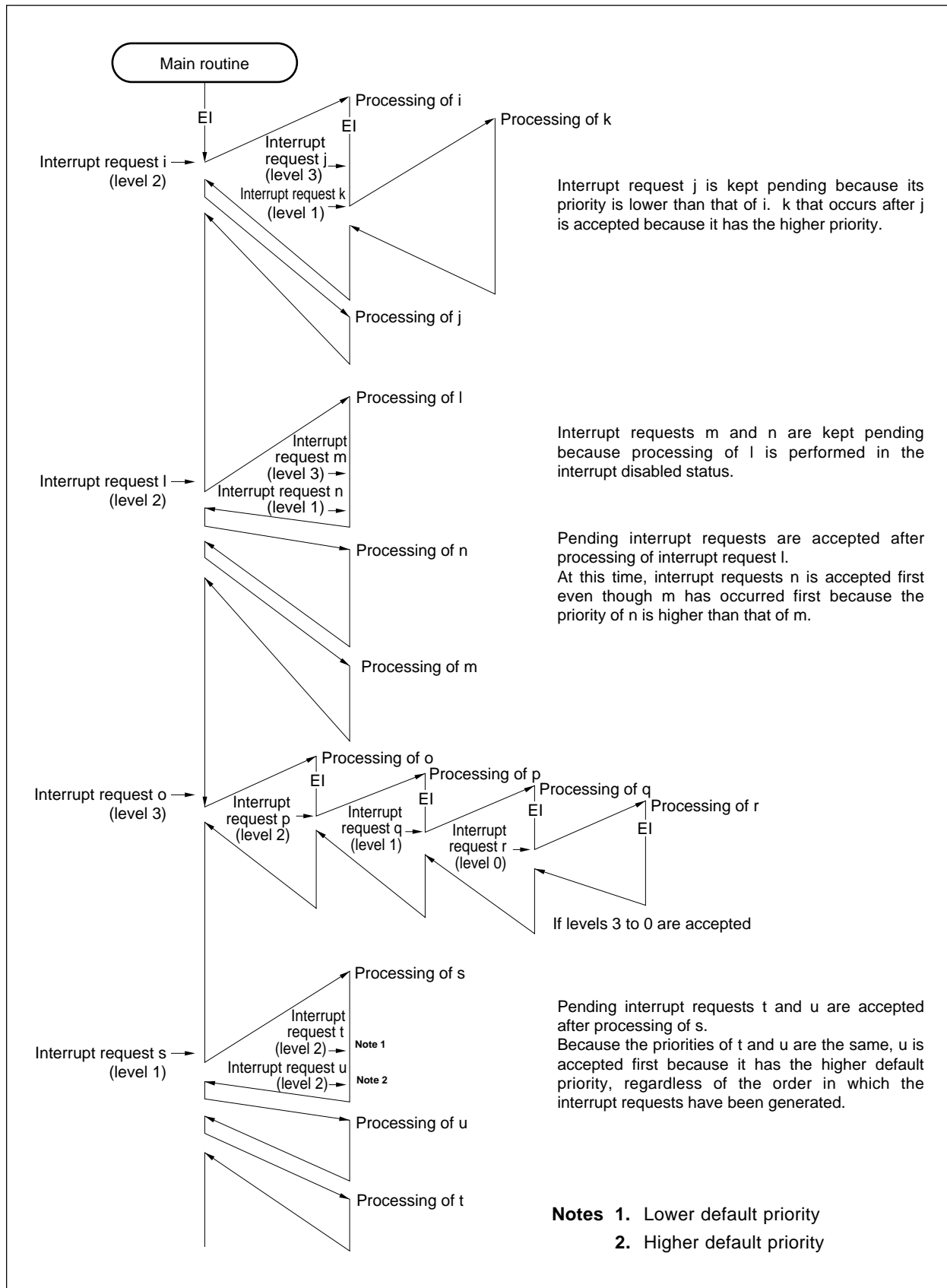
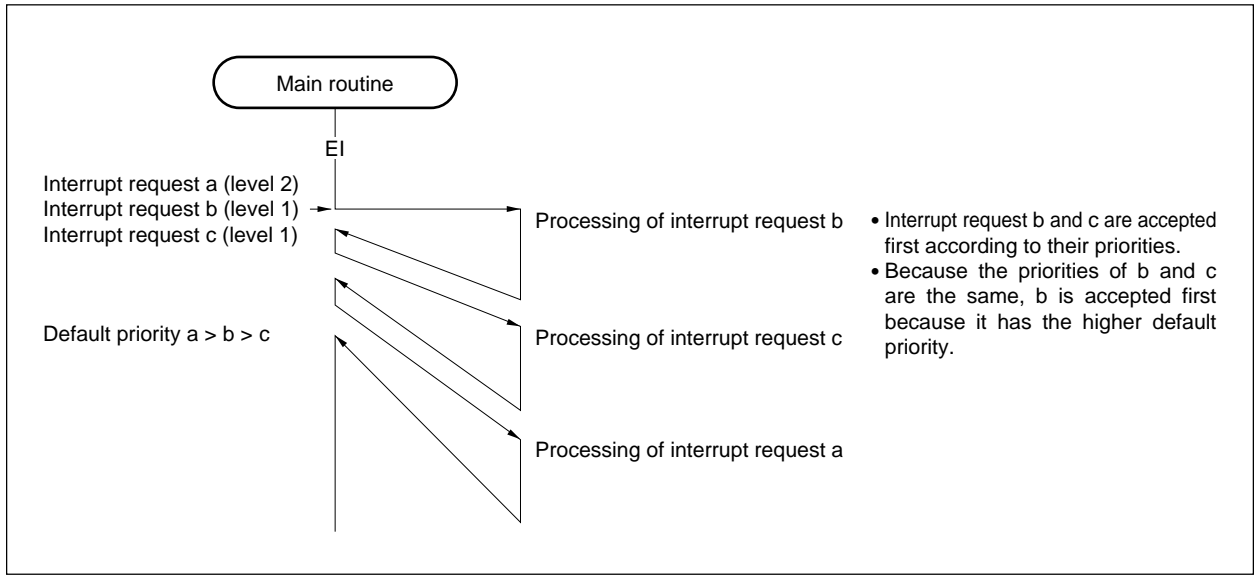
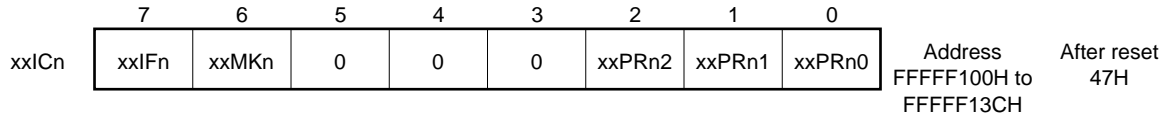


Figure 5-8. Example of Processing Interrupt Requests Simultaneously Generated

5.3.4 Interrupt control register (xxICn)

An interrupt control register is assigned to each maskable interrupt and sets the control conditions for each maskable interrupt request.

The interrupt control register can be read/written in 8- or 1-bit units.



Bit Position	Bit Name	Function																																				
7	xxIFn	Interrupt Request Flag Interrupt request flag 0: Interrupt request not issued 1: Interrupt request issued xxIFn flag is automatically reset by hardware when interrupt request is accepted.																																				
6	xxMKn	Mask Flag Interrupt mask flag 0: Enables interrupt processing 1: Disables interrupt processing (pending)																																				
2 to 0	xxPRn2 to xxPRn0	Priority Specifies eight levels of priorities for each interrupt <table border="1"><thead><tr><th>xxPRn2</th><th>xxPRn1</th><th>xxPRn0</th><th>Interrupt priority specification bit</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>Specifies level 0 (highest)</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Specifies level 1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Specifies level 2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Specifies level 3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Specifies level 4</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Specifies level 5</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Specifies level 6</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Specifies level 7 (lowest)</td></tr></tbody></table>	xxPRn2	xxPRn1	xxPRn0	Interrupt priority specification bit	0	0	0	Specifies level 0 (highest)	0	0	1	Specifies level 1	0	1	0	Specifies level 2	0	1	1	Specifies level 3	1	0	0	Specifies level 4	1	0	1	Specifies level 5	1	1	0	Specifies level 6	1	1	1	Specifies level 7 (lowest)
xxPRn2	xxPRn1	xxPRn0	Interrupt priority specification bit																																			
0	0	0	Specifies level 0 (highest)																																			
0	0	1	Specifies level 1																																			
0	1	0	Specifies level 2																																			
0	1	1	Specifies level 3																																			
1	0	0	Specifies level 4																																			
1	0	1	Specifies level 5																																			
1	1	0	Specifies level 6																																			
1	1	1	Specifies level 7 (lowest)																																			

Remark xx : identification name of each peripheral unit (OV, CC0, P1, CM1, CM2, CC3, CS, II, SE, SR, ST, AD, P5)

n : peripheral unit number (0 to 4)

Address and bit of each interrupt control register is as follows:

Address	Register	Bit							
		7	6	5	4	3	2	1	0
FFFFF100H	OVIC0	OVIF0	OVMK0	0	0	0	OVPR02	OVPR01	OVPR00
FFFFF102H	OVIC1	OVIF1	OVMK1	0	0	0	OVPR12	OVPR11	OVPR10
FFFFF104H	CC0IC0	CC0IF0	CC0MK0	0	0	0	CC0PR02	CC0PR01	CC0PR00
FFFFF106H	CC0IC1	CC0IF1	CC0MK1	0	0	0	CC0PR12	CC0PR11	CC0PR10
FFFFF108H	CC0IC2	CC0IF2	CC0MK2	0	0	0	CC0PR22	CC0PR21	CC0PR20
FFFFF10AH	CC0IC3	CC0IF3	CC0MK3	0	0	0	CC0PR32	CC0PR31	CC0PR30
FFFFF10CH	P1IC0	P1IF0	P1MK0	0	0	0	P1PR02	P1PR01	P1PR00
FFFFF10EH	P1IC1	P1IF1	P1MK1	0	0	0	P1PR12	P1PR11	P1PR10
FFFFF110H	P1IC2	P1IF2	P1MK2	0	0	0	P1PR22	P1PR21	P1PR20
FFFFF112H	P1IC3	P1IF3	P1MK3	0	0	0	P1PR32	P1PR31	P1PR30
FFFFF114H	CM1IC0	CM1IF0	CM1MK0	0	0	0	CM1PR02	CM1PR01	CM1PR00
FFFFF116H	CM1IC1	CM1IF1	CM1MK1	0	0	0	CM1PR12	CM1PR11	CM1PR10
FFFFF118H	CM2IC0	CM2IF0	CM2MK0	0	0	0	CM2PR02	CM2PR01	CM2PR00
FFFFF11AH	CM2IC1	CM2IF1	CM2MK1	0	0	0	CM2PR12	CM2PR11	CM2PR10
FFFFF11CH	CM2IC2	CM2IF2	CM2MK2	0	0	0	CM2PR22	CM2PR21	CM2PR20
FFFFF11EH	CM2IC3	CM2IF3	CM2MK3	0	0	0	CM2PR32	CM2PR31	CM2PR30
FFFFF120H	CM2IC4	CM2IF4	CM2MK4	0	0	0	CM2PR42	CM2PR41	CM2PR40
FFFFF122H	CC3IC0	CC3IF0	CC3MK0	0	0	0	CC3PR02	CC3PR01	CC3PR00
FFFFF124H	CSIC0	CSIF0	CSMK0	0	0	0	CSPR02	CSPR01	CSPR00
FFFFF126H	CSIC1	CSIF1	CSMK1	0	0	0	CSPR12	CSPR11	CSPR10
FFFFF128H	CSIC2	CSIF2	CSMK2	0	0	0	CSPR22	CSPR21	CSPR20
FFFFF12AH	CSIC3	CSIF3	CSMK3	0	0	0	CSPR32	CSPR31	CSPR30
FFFFF12CH	IIC0	IIF0	IIMK0	0	0	0	IIPR02	IIPR01	IIPR00
FFFFF12EH	SEIC0	SEIF0	SEMK0	0	0	0	SEPR02	SEPR01	SEPR00
FFFFF130H	SRIC0	SRIF0	SRMK0	0	0	0	SRPR02	SRPR01	SRPR00
FFFFF132H	STIC0	STIF0	STMK0	0	0	0	STPR02	STPR01	STPR00
FFFFF134H	ADIC0	ADIF0	ADMK0	0	0	0	ADPR02	ADPR01	ADPR00
FFFFF136H	P5IC0	P5IF0	P5MK0	0	0	0	P5PR02	P5PR01	P5PR00
FFFFF138H	P5IC1	P5IF1	P5MK1	0	0	0	P5PR12	P5PR11	P5PR10
FFFFF13AH	P5IC2	P5IF2	P5MK2	0	0	0	P5PR22	P5PR21	P5PR20
FFFFF13CH	P5IC3	P5IF3	P5MK3	0	0	0	P5PR32	P5PR31	P5PR30

5.3.7 Noise elimination

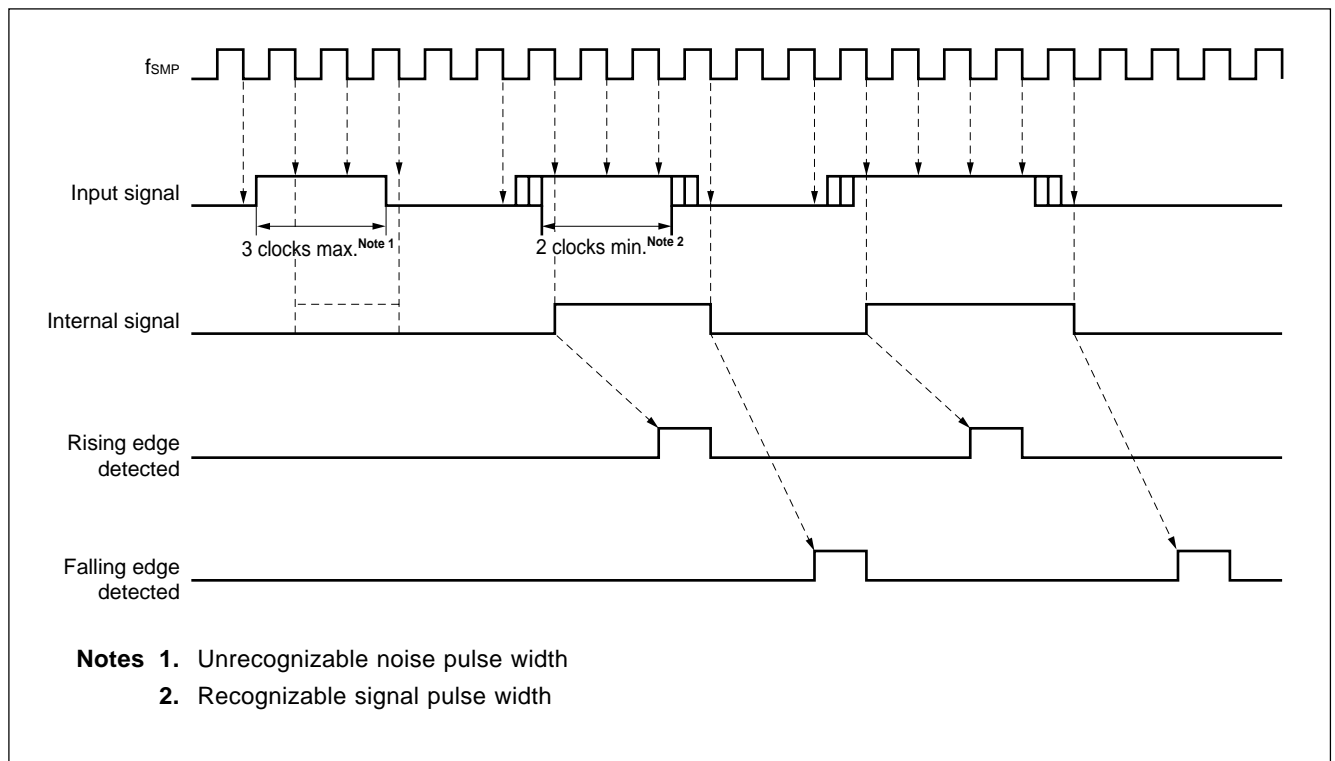
INTP, TI, TCLR, and ADTRG pins are attached with respective digital noise elimination circuit. Thereby, the input levels of these pins are sampled at each sampling clock (f_{SMP}). As a result, if the same level cannot be detected three times consecutively, the input pulse is eliminated as a noise.

The noise elimination time for each pin is shown below. The sampling clock of INTP30 pin can be selected from ϕ , $\phi/64$, $\phi/128$, or $\phi/256$. For the settings, write values to INTM7 register (refer to 5.3.8 (2) (a) External interrupt request register 7 (INTM7)).

Pin	f_{SMP}	Noise Elimination Time
INTP00 to INTP03	ϕ	2 to 3 system clocks
TCLR0/INTP04	ϕ	
TI0/INTP05	ϕ	
INTP10 to INTP13	ϕ	
TI1/INTP14	ϕ	
TI20/INTP20 to TI24/INTP24	ϕ	
ADTRG	ϕ	2 to 3 system clocks
INTP30	ϕ	
	$\phi/64$	
	$\phi/128$	
	$\phi/256$	

Remark f_{SMP} : Sampling clock
 ϕ : Internal system clock

Figure 5-9. Example of Noise Elimination Timing



- Cautions**
1. In the case that the input pulse width is two to three sampling clocks, it is indefinite whether the input pulse is detected as a valid edge or eliminated as a noise.
 2. To securely detect the level as a pulse, input the same level at least three sampling clocks.
 3. When noise is generated in synchronization with sampling, its may recognized as noise. In such cases, attach a filter to the input pin to eliminate the noise.

5.3.8 Edge detection function

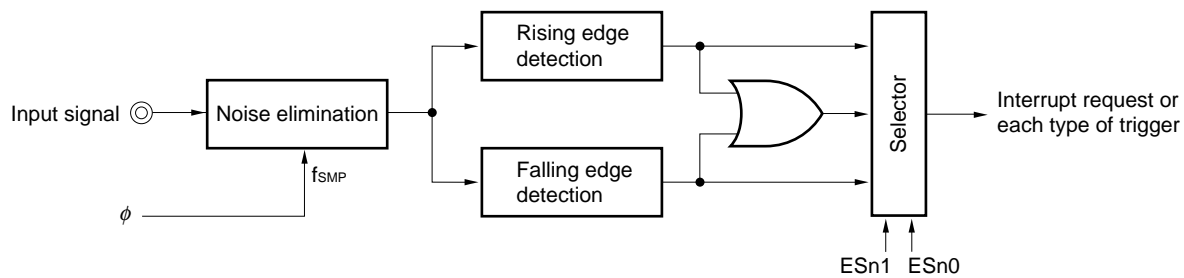
(1) Edge detection of INTP pin (except INTP30 pin), TI pin, TCLR pin, ADTRG pin

These pins can be programmably selected. The valid edge can be selected from the followings:

- Rising edge
- Falling edge
- Both rising and falling edges

The detected INTP signal becomes an interrupt source or capture trigger.

The block diagram of the edge detection of these pins is shown below.

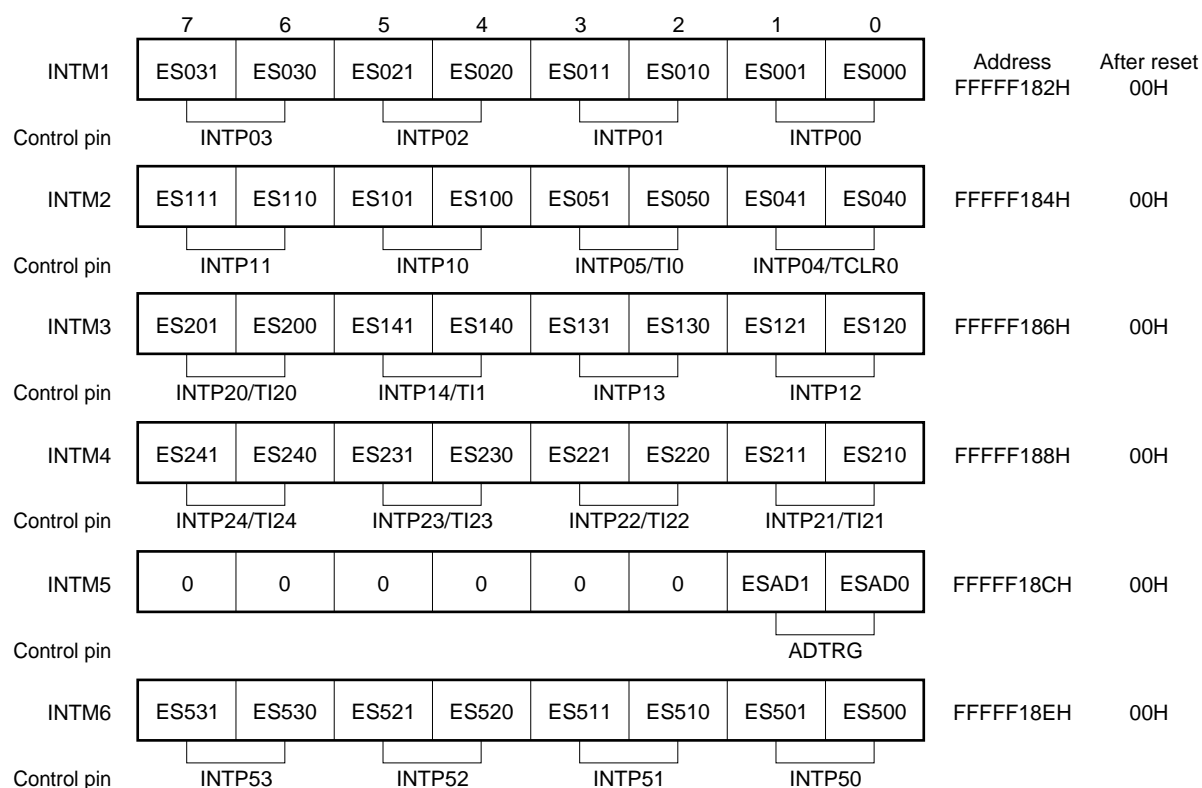


Remark n = 00 to 05, 10 to 14, 20 to 24, 50 to 53, AD

(2) External interrupt mode registers 1 to 6 (INTM1 to INTM6)

These registers specify the valid edges of external interrupt requests or each type of trigger that are input from external pins.

The valid edge of each pin can be specified to be the rising, falling, and both rising and falling edges. Both the registers can be read/written in 8- or 1-bit units.



Bit Position	Bit Name	Function															
7, 5, 3, 1 6, 4, 2, 0	ESn1, ESn0 (n = 00 to 05, 10 to 14, 20 to 24, 50 to 53, AD)	Edge Select Specifies valid edges of INTPm pin and ADTRG pin (m = 00 to 05, 10 to 14, 20 to 24, 50 to 53) <table border="1"> <thead> <tr> <th>ESn1</th><th>ESn0</th><th>Operation</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>Falling edge</td></tr> <tr> <td>0</td><td>1</td><td>Rising edge</td></tr> <tr> <td>1</td><td>0</td><td>RFU (reserved)</td></tr> <tr> <td>1</td><td>1</td><td>Both rising and falling edges</td></tr> </tbody> </table>	ESn1	ESn0	Operation	0	0	Falling edge	0	1	Rising edge	1	0	RFU (reserved)	1	1	Both rising and falling edges
ESn1	ESn0	Operation															
0	0	Falling edge															
0	1	Rising edge															
1	0	RFU (reserved)															
1	1	Both rising and falling edges															

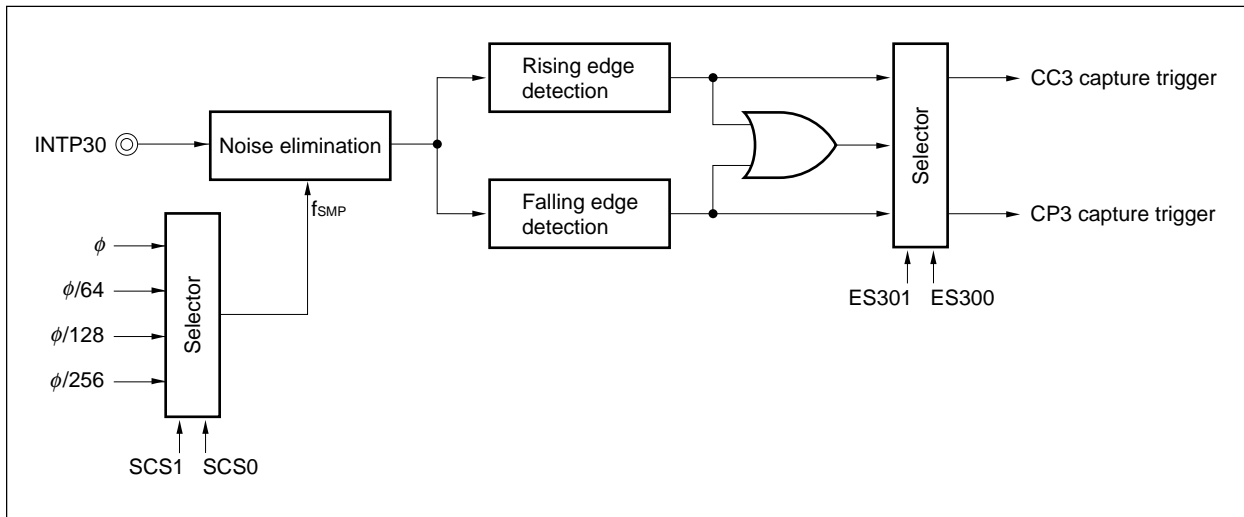
(3) Edge detection of INTP30 pin

To set the valid edge of INTP30 pin, write values to INTM7 register. The valid edge can be selected from the followings.

- Rising edge
- Falling edge
- Both rising and falling edges

The edge detected INTP30 signal becomes the capture trigger of CC3 register and CP3 register of timer function. The triggers of CC3 register and CP3 register have reverse edges. However, when both edges are specified, either one trigger is valid.

The block diagram of the edge detection of INTP30 pin is shown below.



(a) External interrupt mode register 7 (INTM7)

This register specifies the sampling clock (f_{SMP}) and the valid edge of digital noise elimination by INTP30 pins.

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
INTM7	ES301	ES300	0	0	0	0	SCS1	SCS0	Address FFFFFF18EH	After reset 00H

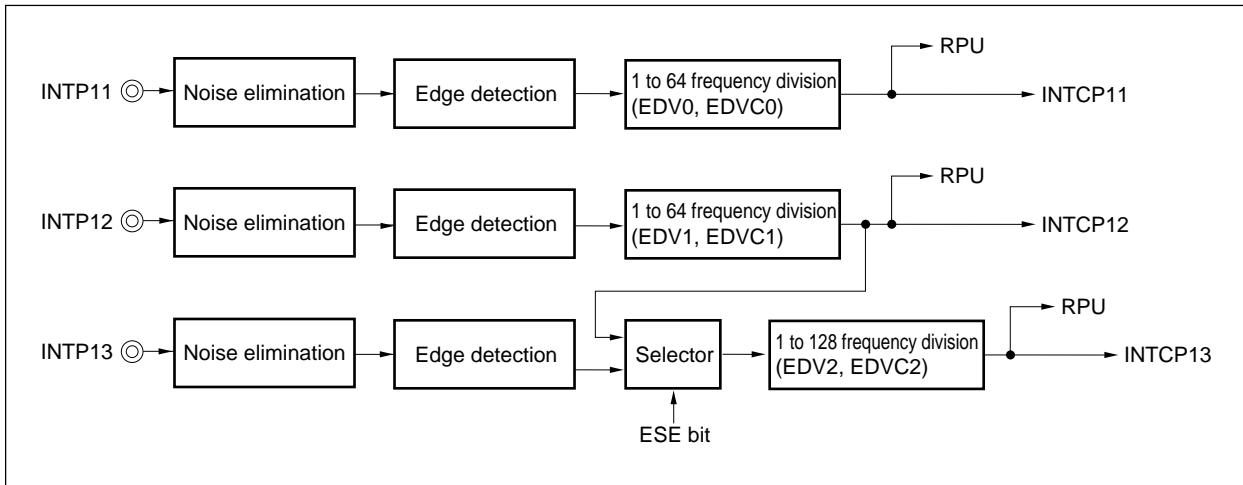
Bit Position	Bit Name	Function																									
7, 6	ES301, ES300	Edge Select Specifies valid edge of INTP30 pin																									
		<table><tr><th>ES301</th><th>ES300</th><th>INTP30, CC3 Capture Trigger</th><th>CP3 Capture Trigger</th></tr><tr><td>0</td><td>0</td><td>Falling edge</td><td>Rising edge</td></tr><tr><td>0</td><td>1</td><td>Rising edge</td><td>Falling edge</td></tr><tr><td>1</td><td>0</td><td>Without selection edge</td><td>Both rising and falling edges</td></tr><tr><td>1</td><td>1</td><td>Both rising and falling edges</td><td>Not captured</td></tr></table>	ES301	ES300	INTP30, CC3 Capture Trigger	CP3 Capture Trigger	0	0	Falling edge	Rising edge	0	1	Rising edge	Falling edge	1	0	Without selection edge	Both rising and falling edges	1	1	Both rising and falling edges	Not captured					
		ES301	ES300	INTP30, CC3 Capture Trigger	CP3 Capture Trigger																						
		0	0	Falling edge	Rising edge																						
		0	1	Rising edge	Falling edge																						
		1	0	Without selection edge	Both rising and falling edges																						
		1	1	Both rising and falling edges	Not captured																						
Remark ϕ : internal system clock																											
1, 0	SCS1, SCS0	Sampling Clock Select Specifies sampling clock																									
		<table><tr><th>SCS1</th><th>SCS0</th><th>Sampling Clock (f_{SMP})</th><th>Pulse Width Eliminated as Noise</th><th>Minimum Pulse Width Recognized as Signal</th></tr><tr><td>0</td><td>0</td><td>ϕ</td><td>$2/\phi$</td><td>$3/\phi$</td></tr><tr><td>0</td><td>1</td><td>$\phi/64$</td><td>$128/\phi$</td><td>$192/\phi$</td></tr><tr><td>1</td><td>0</td><td>$\phi/128$</td><td>$256/\phi$</td><td>$384/\phi$</td></tr><tr><td>1</td><td>1</td><td>$\phi/256$</td><td>$512/\phi$</td><td>$768/\phi$</td></tr></table>	SCS1	SCS0	Sampling Clock (f _{SMP})	Pulse Width Eliminated as Noise	Minimum Pulse Width Recognized as Signal	0	0	ϕ	$2/\phi$	$3/\phi$	0	1	$\phi/64$	$128/\phi$	$192/\phi$	1	0	$\phi/128$	$256/\phi$	$384/\phi$	1	1	$\phi/256$	$512/\phi$	$768/\phi$
		SCS1	SCS0	Sampling Clock (f _{SMP})	Pulse Width Eliminated as Noise	Minimum Pulse Width Recognized as Signal																					
		0	0	ϕ	$2/\phi$	$3/\phi$																					
		0	1	$\phi/64$	$128/\phi$	$192/\phi$																					
		1	0	$\phi/128$	$256/\phi$	$384/\phi$																					
		1	1	$\phi/256$	$512/\phi$	$768/\phi$																					
Remark ϕ : internal system clock																											

5.3.9 Frequency divider

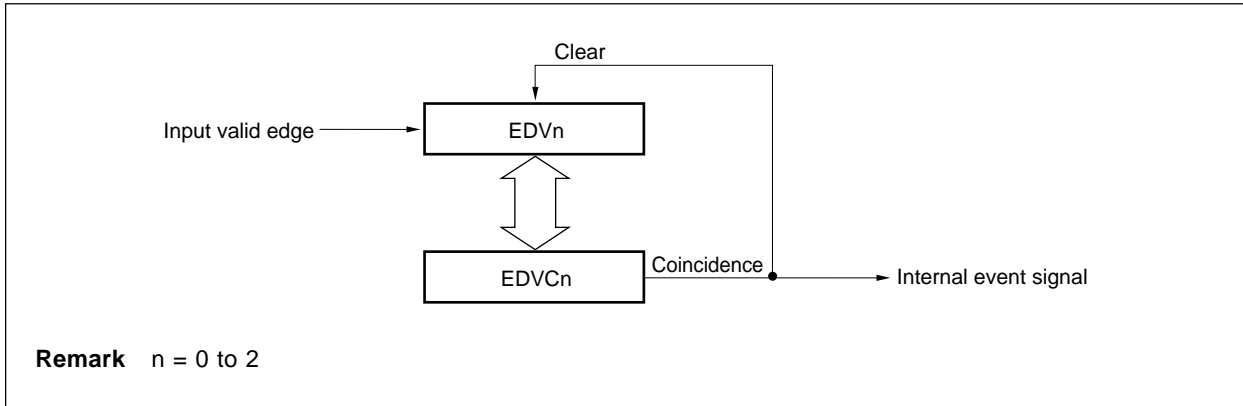
The V854 can internally divide the frequency of the signals input to P11 to P13 (INTP11 to INTP13) pins. The divided result becomes external interrupt request signal or timer capture trigger.

Frequency division ratio is set to event divide control register (EDVC) and comparing it with the value in event divide counter (EDV), and if they coincide, the value becomes the internal event signal, so that the frequency of the INTP signal is divided. 1 to 64 frequency division is possible for INTP11 and INTP12 signal. If INTP12 signal is divided 1 to 64, it can be further divided 1 to 128. However, INTP13 signal cannot be used when this function is used.

The block diagram of the INTP11 to INTP13 input is shown below.



The block diagram of the frequency divider is shown below.



(1) Event divide counter 0 to 2 (EDV0 to EDV2)

This register counts the valid edge of the INTP_n input signal (n = 11 to 13). The EDV0 and EDV1 registers are configured with a 6-bit counter, and EDV2 register is configured with a 7-bit counter.

These registers are cleared at the following timings:

- Coincidence of the value in the event divide control register (EDVC_n) and the count value
- Write to EDVC_n register

Remark n = 0 to 2

These registers can be only read in 8/1-bit units. Edge inputs may not be counted when changing the specification of the valid edge of the INTM_n register (n = 1 to 6).

	7	6	5	4	3	2	1	0		
EDV0	0	0	EDV05	EDV04	EDV03	EDV02	EDV01	EDV00	Address FFFFF1B6H	After reset 00H
EDV1	0	0	EDV15	EDV14	EDV13	EDV12	EDV11	EDV10	FFFFF1B8H	00H
EDV2	0	EDV26	EDV25	EDV24	EDV23	EDV22	EDV21	EDV20	FFFFF1BAH	00H

(2) Event divide control register 0 to 2 (EDVC0 to EDVC2)

These registers set the frequency division ratio of the valid edge of INTP_n input signal (n = 11 to 13). The set value as it is becomes the frequency division ratio. However, when 0 is set, the frequency division ratio is the maximum, that is, the frequency division of EDVC0 and EDVC1 is 64 and that of EDVC2 is 128.

Bits 7 and 6 of EDVC0 and bit 7 of EDVC2 are fixed to 0, and if 1 is written, it will be ignored.

These registers can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
EDVC0	0	0	EDVC05	EDVC04	EDVC03	EDVC02	EDVC01	EDVC00	Address FFFFF1B0H	After reset 01H
EDVC1	0	0	EDVC15	EDVC14	EDVC13	EDVC12	EDVC11	EDVC10	FFFFF1B2H	01H
EDVC2	0	EDVC26	EDVC25	EDVC24	EDVC23	EDVC22	EDVC21	EDVC20	FFFFF1B4H	01H

(3) Event select register (EVS)

This register selects the signal to be input to EDV2 register.

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
EVS	0	0	0	0	0	0	0	ESE	Address FFFFF1C0H	After reset 00H

Bit Position	Bit Name	Function
0	ESE	Event Select Selects input signal to EDV2 register 0: INTP13 signal 1: INTP12 signal frequency division result by EDVC1 register

5.4 Software Exception

A software exception is generated when the CPU executes the TRAP instruction, and can be always accepted.

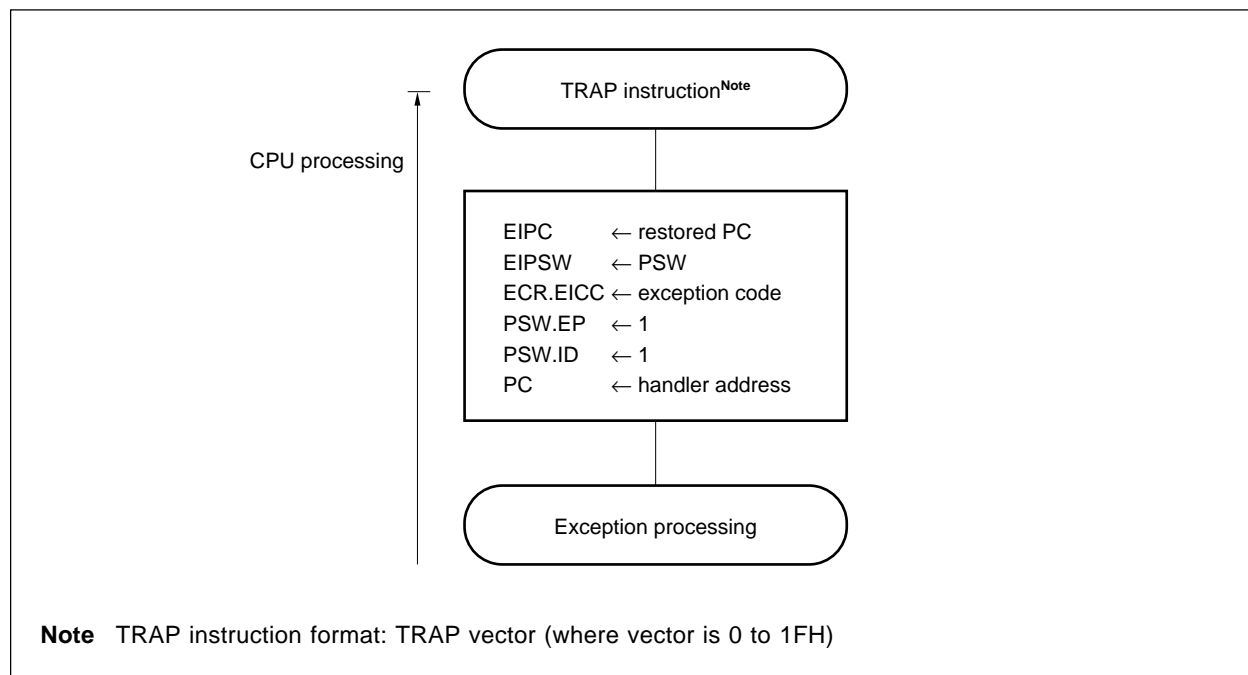
5.4.1 Operation

If a software exception occurs, the CPU performs the following processing, and transfers control to the handler routine:

- (1) Saves the restored PC to EIPC.
- (2) Saves the current PSW to EIPSW.
- (3) Writes an exception code to the lower 16 bits (EICC) of ECR (interrupt source).
- (4) Sets the EP and ID bits of PSW.
- (5) Loads the handler address (00000040H or 00000050H) of the software exception routine in the PC, and transfers control.

Figure 5-10 illustrates how a software exception is processed.

Figure 5-10. Software Exception Processing



The handler address is determined by the operand of the TRAP instruction (vector). If the vector is 0 to 0FH, the handler address is 00000040H; if the operand is 10H to 1FH, it is 00000050H.

5.4.2 Restore

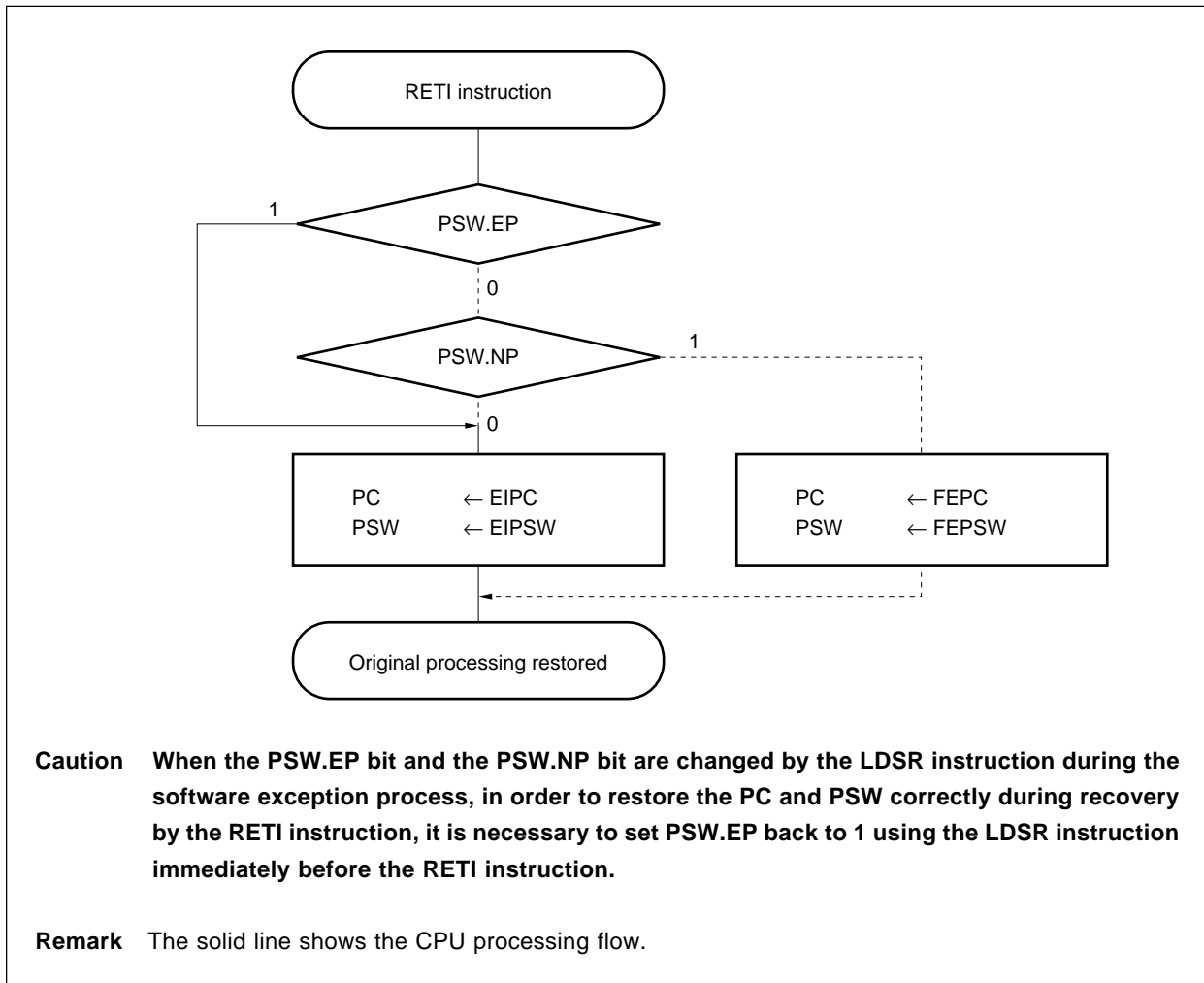
To restore or return execution from the software exception service routine, the RETI instruction is used.

When the RETI instruction is executed, the CPU performs the following steps, and transfers control to the address of the restored PC.

- (1) Restores the restored PC and PSW from EIPC and EIPSW because the EP bit of PSW is 1.
- (2) Transfers control to the restored PC address and PSW status.

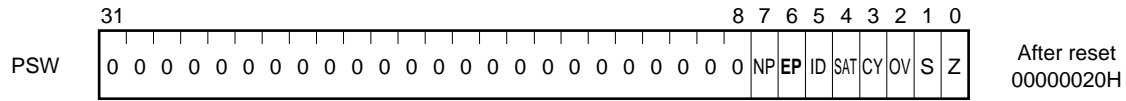
Figure 5-11 illustrates the processing of the RETI instruction.

Figure 5-11. RETI Instruction Processing



5.4.3 Exception status flag (EP)

The EP flag in PSW is a status flag used to indicate that trap processing is in progress. It is set when a trap occurs.



Bit Position	Bit Name	Function
6	EP	Exception Pending Indicates that trap processing is in progress 0: Trap processing not in progress 1: Trap processing in progress

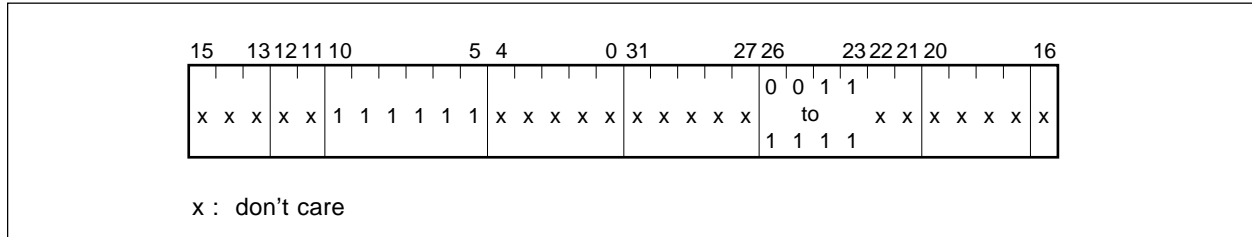
5.5 Exception Trap

The exception trap is an interrupt that is requested when illegal execution of an instruction takes place. In the V854, an illegal op code exception (ILGOP: ILeGal OPcode trap) is considered as an exception trap.

An illegal op code exception occurs if the subop code field of an instruction to be executed next is not a valid op code.

5.5.1 Illegal op code definition

An illegal op code is defined to be a 32-bit word with bits 5 to 10 being 11111B and bits 23 to 26 being 0011B to 1111B.



Caution It is recommended that the illegal op code not be defined since an instruction may newly be assigned later.

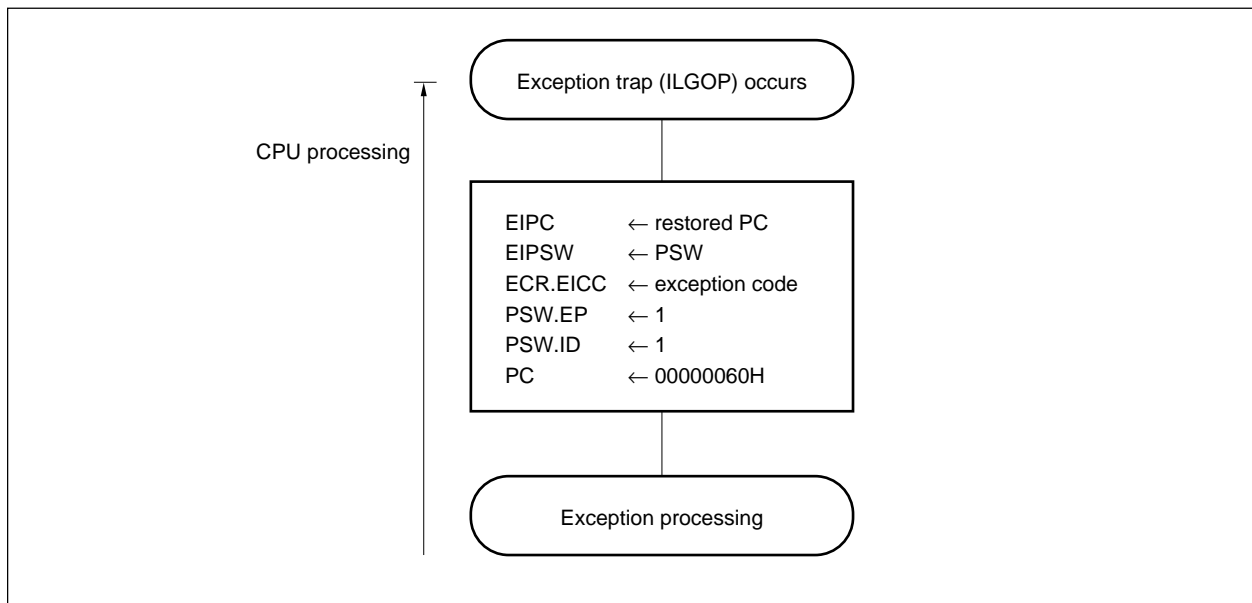
5.5.2 Operation

If an exception trap occurs, the CPU performs the following processing, and transfers control to the handler routine:

- (1) Saves the restored PC to EIPC.
- (2) Saves the current PSW to EIPSW.
- (3) Writes an exception code (0060H) to the lower 16 bits (EICC) of ECR.
- (4) Sets the EP and ID bits of PSW.
- (5) Loads the handler address (00000060H) for the exception trap routine to the PC, and transfers control.

Figure 5-12 illustrates how the exception trap is processed.

Figure 5-12. Exception Trap Processing



5.5.3 Restore

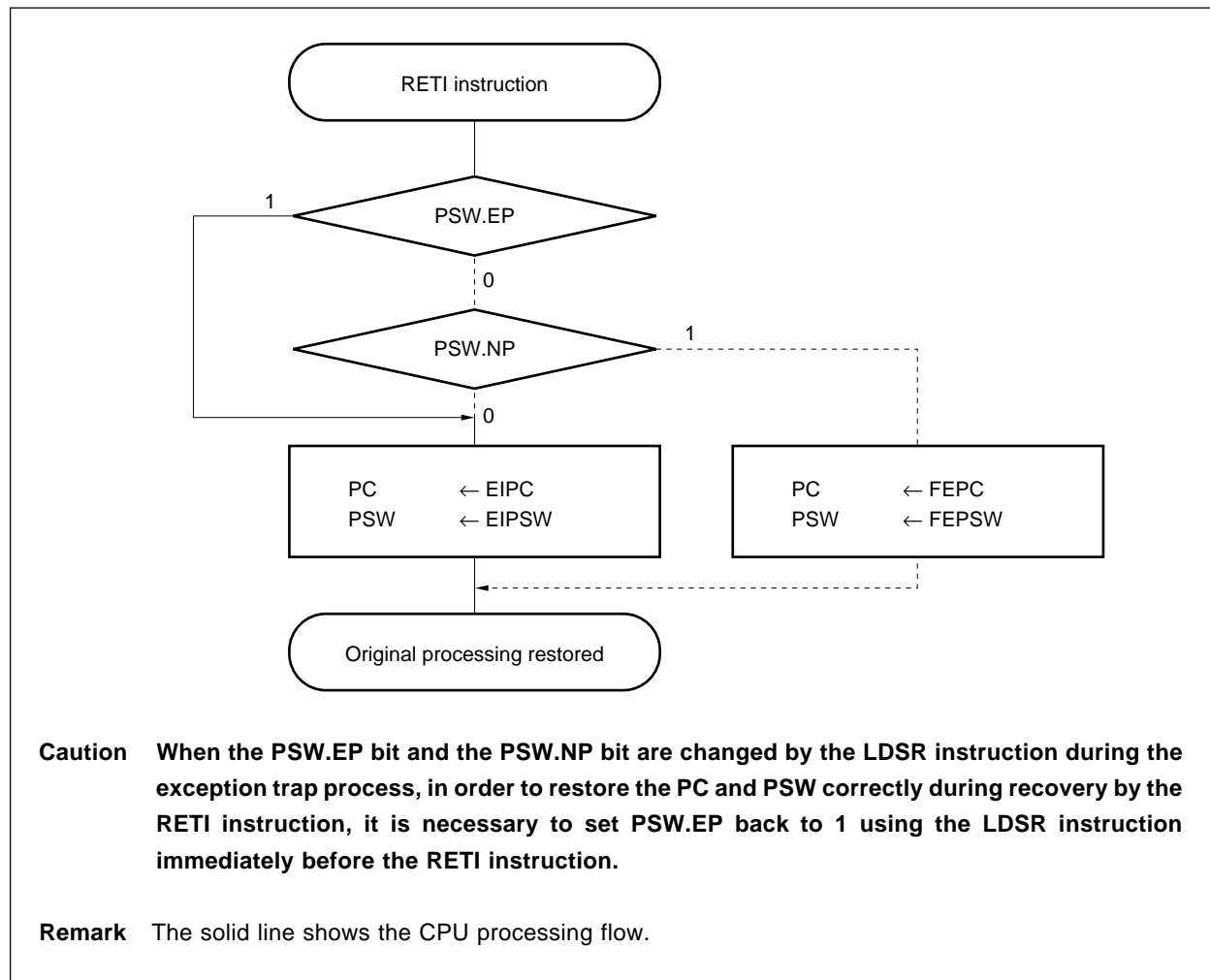
To restore or return execution from the exception TRAP, the RETI instruction is used.

When the RETI instruction is executed, the CPU performs the following processing, and transfers control to the address of the restored PC.

- (1) Restores the restored PC and PSW from EIPC and EIPSW because the EP bit of PSW is 1.
- (2) Transfers control to the restored PC address and PSW status.

Figure 5-13 illustrates the processing of the RETI instruction.

Figure 5-13. RETI Instruction Processing



5.6 Multiple interrupt processing

Multiple interrupt processing is a function that allows the nesting of interrupts. If a higher priority interrupt is generated and accepted, it will be allowed to stop a current interrupt service routine in progress. Execution of the original routine will resume once the higher priority interrupt routine is completed.

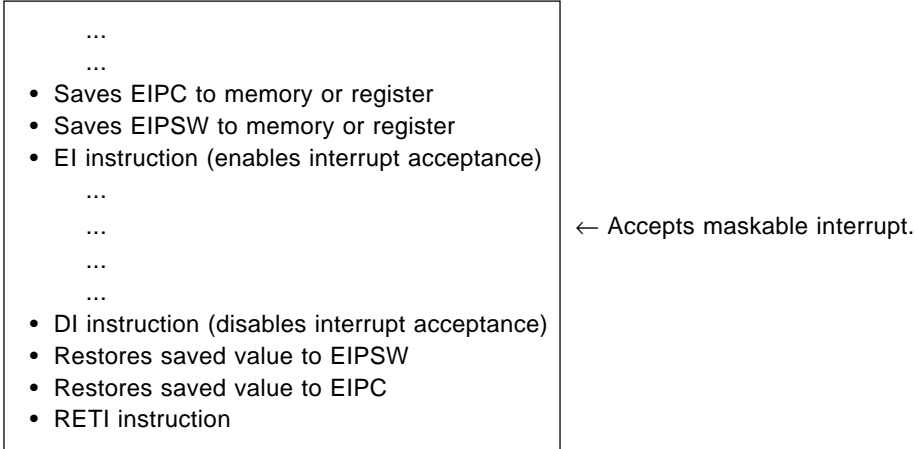
If an interrupt with a lower or equal priority is generated and a service routine is currently in progress, the later interrupt will be pended.

Multiple processing control of maskable interrupts is performed when in the state of interrupt acceptance (ID = 0). To perform maskable interrupt even in an interrupt processing routine, this control must be set in the state of acceptance (ID = 0). If a maskable interrupt acceptance or exception is generated during a service program of maskable interrupt or exception, EIPC and EIPSW must be saved.

The following example shows the procedure of interrupt nesting.

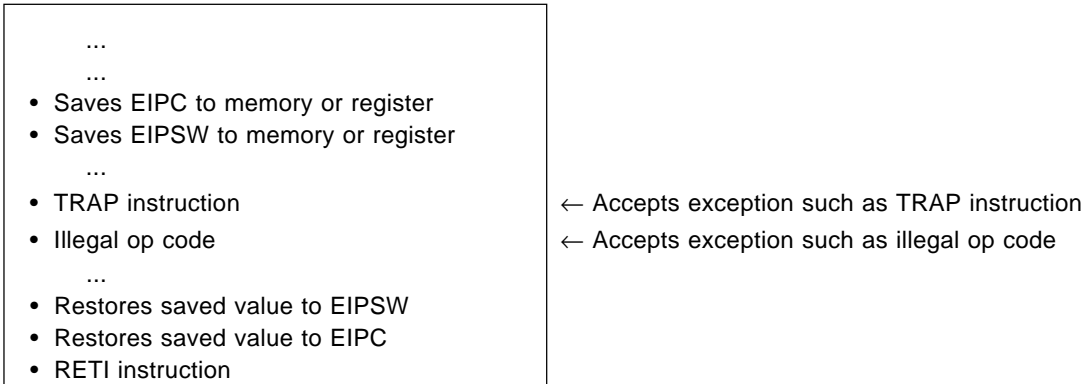
(1) To accept maskable interrupts in service routine

Service routine of maskable interrupt or exception



(2) To generate exception in service program

Service program of maskable interrupt or exception



Priorities 0 to 7 (0 is the highest priority) can be programmed for each maskable interrupt request for multiple interrupt processing control. To set a priority level, write values to the xxPRn0 to xxPRn2 bits of the interrupt request control register (xxICn) corresponding to each maskable interrupt request. At system reset, the interrupt request is masked by the xxMKn bit, and the priority level is set to 7 by the xxPRn0 to xxPRn2 bits.

The priorities of maskable interrupts are as follows:

(High) Level 0 > Level 1 > Level 2 > Level 3 > Level 4 > Level 5 > Level 6 > Level 7 (Low)

Interrupt processing that has been suspended as a result of multiple interrupt processing is resumed after the interrupt processing of the higher priority has been completed and the RETI instruction has been executed. A pending interrupt request is accepted after the current interrupt processing has been completed and the RETI instruction has been executed.

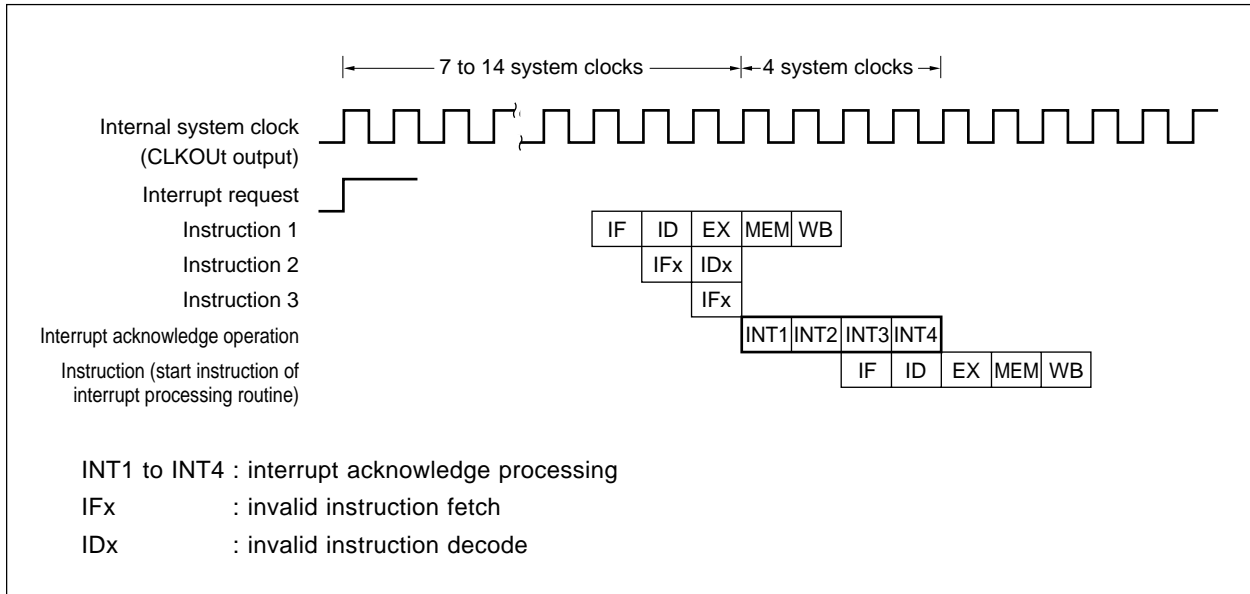
Caution In the non-maskable interrupt processing routine (time until the RETI instruction is executed), maskable interrupts are not accepted but are suspended.

Remarks xx: Each peripheral unit identifier (OV, CC0, P1, CM1, CM2, CC3, CS, II, SE, SR, ST, AD, P5)
 n: Peripheral unit number (0 to 4)

5.7 Interrupt Response Time

Interrupt Response Time from the interrupt request generation to the interrupt processing activation is as follows:

Figure 5-14. Pipeline Operation at Interrupt Request Acknowledge (General Description)



Interrupt Response Time (internal system clock)			Condition
	Internal interrupt	External interrupt	
Minimum	11	13	Except the condition below: <ul style="list-style-type: none"> • In IDLE/software STOP mode • External bus is accessed • Two or more interrupt request non-sample instructions are executed in succession • Access to interrupt control register
Maximum	18	20	

5.8 Periods Where Interrupt is Not Acknowledged

An interrupt request is acknowledged while an instruction is being executed. However, no interrupt request will be acknowledged between an interrupt request non-sample instruction and the next instruction.

- EI instruction
- DI instruction
- LDSR reg2, 0x5 instruction (vs. PSW)

In the following conditions, an interrupt may not be acknowledged.

- (1) Immediately after the RETI instruction execution
- (2) Immediately after the data write to the following registers.
 - Interrupt control register (xxICn)
 - Command register (PRCMD)
 - In-service priority register (ISPR)

[MEMO]

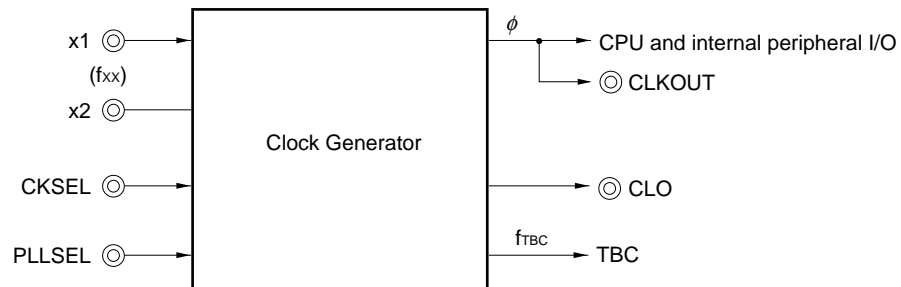
CHAPTER 6 CLOCK GENERATOR FUNCTION

The clock generator (CG) produces and controls the internal system clock (ϕ) which is supplied to all the internal hardware units including the CPU.

6.1 Features

- Multiplication function by PLL (Phase Locked Loop) synthesizer
- Clock source
 - Oscillation through oscillator connection: $f_{xx} = \phi, \phi/5$
 - External clock input: $f_{xx} = \phi, 2 \times \phi, \phi/5$
- Power save control
 - HALT mode
 - IDLE mode
 - Software STOP mode
 - Clock output inhibit function
- Internal system clock output function

6.2 Configuration



Remark ϕ : Internal system clock
 f_{TBC} : Time base counter (TBC) input clock (= $f_{xx}/2$)

6.3 Selecting Input Clock

The clock generator consists of an oscillator and a PLL synthesizer. It generates, for example, a 32.768 (Max. 33)-MHz internal system clock (ϕ) when a 6.5536-MHz crystal resonator or ceramic resonator is connected across the X1 and X2 pins at 5-x multiplication.

An external clock can be directly connected to the oscillator circuit. In this case, input the clock signal to the X1 pin, and leave the X2 pin open.

The clock generator is provided with two basic operation modes: PLL mode and direct mode. The operation modes are selected by the CKSEL pin. The CKSEL pin is latched at reset.

CKSEL	Operation Mode
0	PLL mode
1	Direct mode

Caution Use CKSEL pin with a fixed input level. Changing the level during operations of this pin may cause erroneous operation.

6.3.1 Direct mode

In the direct mode, external clock with frequency twice higher than that of the internal system clock is input. Because the oscillator circuit and PLL synthesizer do not run, power consumption is significantly reduced. This mode is mainly used for application systems that operate the V854 in a relatively low frequency. Considering EMI measures, the PLL mode is recommended when the external clock frequency (f_{xx}) is 32 MHz (internal system clock (ϕ) = 16 MHz) or more.

6.3.2 PLL mode

In the PLL mode, an external clock is input by connecting an external oscillator, which is multiplied by the PLL synthesizer to generate the internal system clock (ϕ).

The PLL multiplication number that can be selected is either one or five. The PLL multiplication number can be selected by the PLLSEL pin (refer to **2.3.16 PLLSEL**).

PLLSEL	Multiplication
0	1-x multiplication
1	5-x multiplication

- Cautions**
1. Fix the PLLSEL pin so that the input level does not change (changing the input level of this pin during operation may cause erroneous operation). When this pin is set in the direct mode (CKSEL = 1), the PLLSEL pin has no function. Treat it as an unused pin.
 2. When using an external by a resonator, use this mode with f_{xx} = 16 MHz max.

At reset, with reference to the input clock frequency (f_{xx}), an internal system clock (ϕ) that is either equivalent to the base clock (1 x f_{xx}) or five times the base clock (5 x f_{xx}) is generated depending on whether 1-x or 5-x multiplication is selected.

In the PLL mode, when the clock supply from the external oscillator or external clock source is stopped, the internal system clock (ϕ) based on the freerunning frequency of the voltage-controlled oscillator circuit (VCO) in the clock generator continues operating. In this case, ϕ is approximately 1 MHz (target). Do not use this mode expecting to obtain the freerunning frequency.

Examples of the clock used in the PLL mode

Multiplication	Internal System Clock Frequency (ϕ) [MHz]	External Oscillator/External Clock Frequency (f _{xx}) [MHz]
1-x multiplication	33.000	33.000 ^{Note}
	25.000	25.000 ^{Note}
	20.000	20.000 ^{Note}
	16.000	16.000
5-x multiplication	33.000	6.6000
	25.000	5.0000
	20.000	4.0000
	16.000	3.2000

Note Cannot be oscillated by a resonator. Oscillate not higher than 16 MHz.

6.3.3 Clock control register (CKC)

This is an 8-bit register which controls the internal system clock frequency. It can be written only by a specific combination of instruction sequences so that its contents are not written by mistake due to erroneous program execution.

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
CKC	0	0	0	0	0	0	CKDIV1	CKDIV0	Address FFFFF072H	After reset 00H

Bit Position	Bit Name	Function																																																																				
1, 0	CKDIV1, CKDIV0	Clock Divide Sets the internal system clock frequency in the PLL mode.																																																																				
		<table><tr><th rowspan="2">Operation Mode</th><th colspan="2">Pins</th><th colspan="2">CKC</th><th rowspan="2">Internal System Clock (ϕ)</th></tr><tr><th>CKSEL</th><th>PLLSEL</th><th>CKDIV1</th><th>CKDIV0</th></tr><tr><td rowspan="3">Direct mode</td><td>H</td><td>Note</td><td>0</td><td>0</td><td>$f_{xx}/2$</td></tr><tr><td>H</td><td>Note</td><td>Any values</td><td>1</td><td>Setting prohibited</td></tr><tr><td>H</td><td>Note</td><td>1</td><td>Any values</td><td>Setting prohibited</td></tr><tr><td rowspan="4">PLL mode (1-x multiplication)</td><td>L</td><td>L</td><td>0</td><td>0</td><td>$f_{xx}/2$</td></tr><tr><td>L</td><td>L</td><td>0</td><td>1</td><td>Setting prohibited</td></tr><tr><td>L</td><td>L</td><td>1</td><td>0</td><td>$f_{xx}/5$</td></tr><tr><td>L</td><td>L</td><td>1</td><td>1</td><td>$f_{xx}/10$</td></tr><tr><td rowspan="4">PLL mode (5-x multiplication)</td><td>L</td><td>H</td><td>0</td><td>0</td><td>$f_{xx}/5$</td></tr><tr><td>L</td><td>H</td><td>0</td><td>1</td><td>Setting prohibited</td></tr><tr><td>L</td><td>H</td><td>1</td><td>0</td><td>f_{xx}</td></tr><tr><td>L</td><td>H</td><td>1</td><td>1</td><td>$f_{xx}/2$</td></tr></table>	Operation Mode	Pins		CKC		Internal System Clock (ϕ)	CKSEL	PLLSEL	CKDIV1	CKDIV0	Direct mode	H	Note	0	0	$f_{xx}/2$	H	Note	Any values	1	Setting prohibited	H	Note	1	Any values	Setting prohibited	PLL mode (1-x multiplication)	L	L	0	0	$f_{xx}/2$	L	L	0	1	Setting prohibited	L	L	1	0	$f_{xx}/5$	L	L	1	1	$f_{xx}/10$	PLL mode (5-x multiplication)	L	H	0	0	$f_{xx}/5$	L	H	0	1	Setting prohibited	L	H	1	0	f_{xx}	L	H	1	1	$f_{xx}/2$
		Operation Mode		Pins		CKC			Internal System Clock (ϕ)																																																													
			CKSEL	PLLSEL	CKDIV1	CKDIV0																																																																
		Direct mode	H	Note	0	0	$f_{xx}/2$																																																															
			H	Note	Any values	1	Setting prohibited																																																															
			H	Note	1	Any values	Setting prohibited																																																															
		PLL mode (1-x multiplication)	L	L	0	0	$f_{xx}/2$																																																															
			L	L	0	1	Setting prohibited																																																															
			L	L	1	0	$f_{xx}/5$																																																															
			L	L	1	1	$f_{xx}/10$																																																															
		PLL mode (5-x multiplication)	L	H	0	0	$f_{xx}/5$																																																															
			L	H	0	1	Setting prohibited																																																															
			L	H	1	0	f_{xx}																																																															
			L	H	1	1	$f_{xx}/2$																																																															
Note Connect V _{DD} or V _{SS} directly (refer to 2.4 Pin I/O Circuit Type and Connection of Unused Pins).																																																																						
Remark H : High level input L : Low level input f _{xx} : Input clock																																																																						

The sequence of setting data in this register is the same as the power save control register (PSC). However, the limitation items listed in **Cautions 2** for the **3.4.9 Specific registers** do not apply. For details, refer to **6.5.2 Control register**.

(1) Example of settings

The example of settings is as below.

Operation Mode	Pins		CKC Register		Input Clock (f _{xx})	Internal System Clock (φ)
	CKSEL	PLLSEL	CKDIV1	CKDIV0		
Direct mode	H	Note	0	0	16 MHz	8 MHz
PLL mode (1-x multiplication)	L	L	0	0	33 MHz	33 MHz
	L	L	1	0	33 MHz	6.6 MHz
	L	L	1	1	33 MHz	3.3 MHz
PLL mode (5-x multiplication)	L	H	0	0	6.6 MHz	33 MHz
	L	H	1	0	6.6 MHz	6.6 MHz
	L	H	1	1	6.6 MHz	3.3 MHz
Other than the above					Setting prohibited	

Note Connect directly to V_{DD} or V_{SS}.

Remark H : High level input
L : Low level input

6.4 PLL Lock-up

Following the power-on reset or when exiting the software STOP mode is released, a certain length of time will be required for the PLL to stabilize. This required time is called PLL lock-up time. The status in which the frequency is not stable is called unlock status and the status in which it has been stabilized is called lock status.

Two system status registers are available to check the stabilization of the PLL frequency: UNLOCK flag that indicates the stabilization status of the PLL frequency, and PRERR flag that indicates occurrence of a protection error (for the details of the PRERR flag, refer to **3.4.9 (2) System status register (SYS)**).

The SYS register, which contains these UNLOCK and PRERR flags, can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
SYS	0	0	0	PRERR	0	0	0	UNLOCK	Address FFFFF078H	After reset 0000000xB

Bit Position	Bit Name	Function
0	UNLOCK	Unlock Status Flag This is a read-only flag and indicates unlock status of PLL. It holds "0" as long as lock up status is maintained, and is not changed even if system is reset. 0 : Indicates lock status 1 : Indicates unlock status

Remark For the description of the PRERR flag, refer to **3.4.9 (2) System status register (SYS)**.

If the unlock status condition should arise, due to a power or clock source failure, the UNLOCK flag should be checked to verify that the PLL has stabilized before performing any execution speed dependent operations, such as real-time processing.

Static processing such as setting of the on-chip hardware units and initialization of the register data and memory data, however, can be executed before the UNLOCK flag is reset.

The following is the relation between the oscillation stabilization time (the time from the oscillator starts oscillating until the input wave form stabilizes) and the PLL lockup time (the time until the frequency stabilizes) when using an oscillator:

Oscillation stabilization time < PLL lockup time

6.5 Power Save Control

6.5.1 General

The V854 is provided with the following power save or standby modes to reduce power consumption when CPU operation is not required.

(1) HALT mode

In this mode, the clock generator (oscillator and PLL synthesizer) continues operation but the operating clock of the CPU stops. The internal peripherals continue to function in reference to the internal system clock. Total power consumption of the system can be reduced through intermittent operation between normal operation and HALT modes.

A dedicated instruction (HALT instruction) transfers to the V854 to the HALT mode.

(2) IDLE mode

In this mode, both the CPU clock and the internal system clock are stopped to further reduce power consumption. However, since the clock generator continues to run, normal operation can resume without having to wait for the oscillator and PLL circuits to stabilize.

Setting the PSC register, which is a specific register, transfers the V854 to the IDLE mode.

The IDLE mode is somewhere between the STOP and HALT modes in terms of clock stabilization time and power consumption, and is used in applications where the clock oscillation time should be eliminated but low power consumption is required.

★ **Caution** When inputting external clocks, continue the supply of clocks.

(3) Software STOP mode

In this mode, the CPU clock, the internal system clock, and the clock generator are stopped, reducing power consumption to just the leakage current. In this state, power consumption is minimized.

Setting the PSC register, which is a specific register, transfers the V854 to the software STOP mode.

★ (a) PLL mode

Setting the register by software transfers the V854 to the software STOP mode. As soon as the oscillator circuit stops, the clock output of the PLL synthesizer is stopped. After the software STOP mode has been released, it is necessary to allow for stabilization time of the oscillator and system clock. Moreover, the lock up or stabilization time of the PLL may also be necessary, depending on the application.

★ (b) Direct mode

The software STOP mode cannot be used in direct mode.

(4) Clock output inhibit

Output of the system clock from the CLKOUT pin is prohibited.

The operations of the clock generator in the normal, HALT, IDLE, and software STOP modes are shown in Table 6-1.

By combining and selecting the mode best suited for a specific application, the power consumption of the system can be effectively reduced.

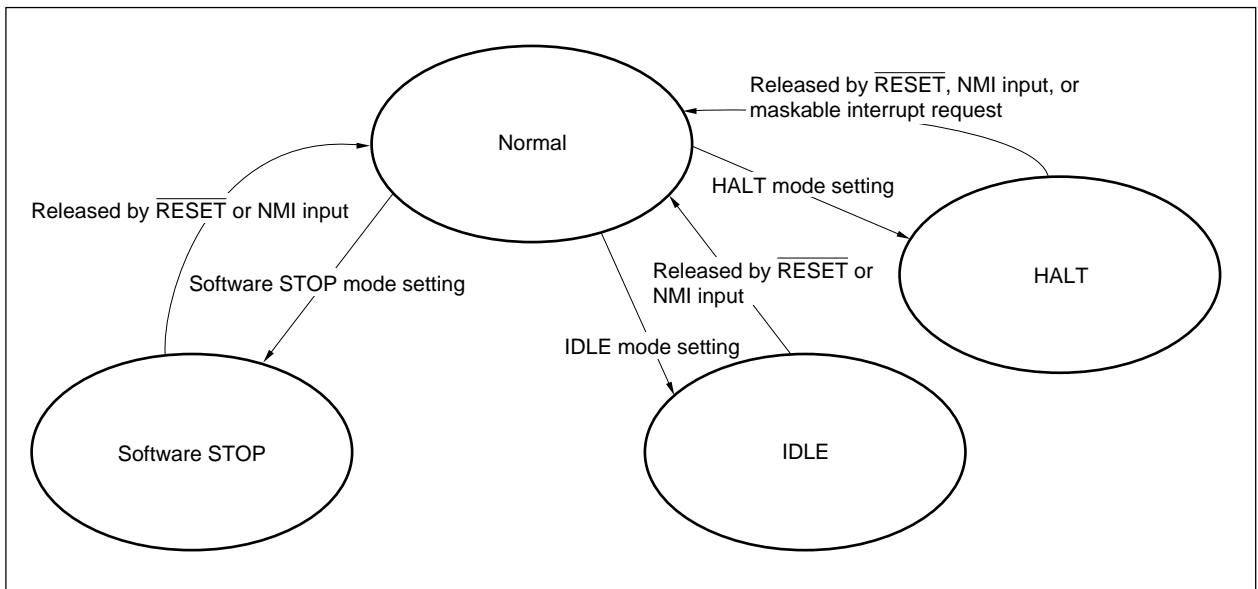
Table 6-1. Operation of Clock Generator by Power Save Control

Clock Source		Standby Mode	Oscillator Circuit (OSC)	PLL Synthesizer	Clock Supply to Peripheral I/O	Clock Supply to CPU
PLL mode	Oscillation by crystal oscillator	Normal	○	○	○	○
		HALT	○	○	○	x
		IDLE	○	○	x	x
		STOP	x	x	x	x
	External clock	Normal	x	○	○	○
		HALT	x	○	○	x
		IDLE	x	○	x	x
		STOP	x	x	x	x
Direct mode		Normal	x	x	○	○
		HALT	x	x	○	x
		IDLE	x	x	x	x
		STOP	x	x	x	x

○ : Operates

x : Stops

Status Transition Diagram



6.5.2 Control registers

(1) Power save control register (PSC)

This is an 8-bit register that controls the power save mode. This is a specific register, and only the access by the specific sequence is valid during write cycles. For details, refer to **3.4.9 Specific registers**.

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
PSC	DCLK1	DCLK0	TBCS	CESEL	0	IDLE	STP	0	Address FFFFFF070H	After reset Note

Bit Position	Bit Name	Function															
7, 6	DCLKn (n = 1, 0)	Disable CLKOUT Specifies operation mode of CLKOUT pin <table border="1"> <tr> <th>DCLK1</th><th>DCLK0</th><th>Mode</th></tr> <tr> <td>0</td><td>0</td><td>Normal output mode</td></tr> <tr> <td>0</td><td>1</td><td>RFU (reserved)</td></tr> <tr> <td>1</td><td>0</td><td>RFU (reserved)</td></tr> <tr> <td>1</td><td>1</td><td>Clock output inhibit mode</td></tr> </table>	DCLK1	DCLK0	Mode	0	0	Normal output mode	0	1	RFU (reserved)	1	0	RFU (reserved)	1	1	Clock output inhibit mode
DCLK1	DCLK0	Mode															
0	0	Normal output mode															
0	1	RFU (reserved)															
1	0	RFU (reserved)															
1	1	Clock output inhibit mode															
5	TBCS	Time Base Count Select Selects a number of dividing of time base counter, and specifies oscillation stabilization time. 0: $2^{15}/f_{TBC}$ (s) 1: $2^{16}/f_{TBC}$ (s) For details, refer to explanation of “ Time base counter (TBC) ” in section 6.6 “ Specifying Oscillation Stabilization Time ”.															
4	CESEL	Crystal/External Select Specifies functions of X1 and X2 pins 0: Oscillator connected to X1 and X2 pins 1: External clock connected to X1 pin When CESEL = 1, the software STOP mode cannot be used.															
2	IDLE	IDLE Mode Specifies IDLE mode. When “1” is written to this bit, IDLE mode is entered. When IDLE mode is released, this bit is automatically reset to “0”.															
1	STP	STOP Mode Specifies software STOP mode. When “1” is written to this bit, STOP mode is entered. When STOP mode is released, this bit is automatically reset to “0”.															

Note 00H (in ROM-less mode 1 and 2, in single-chip mode 2)
C0H (in single-chip mode 1 and the PROM mode)

6.5.3 HALT mode

(1) Entering and operation status

In the HALT mode, the clock generator (oscillator circuit and PLL synthesizer) operates, while the operating clock of the CPU stops. The internal peripherals continue to function in reference to the internal system clock. The total lower consumption of the system can be reduced by entering the HALT mode during the idle time of the CPU.

This mode is entered by the HALT instruction.

In the HALT mode, program execution is stopped, but the contents of the registers and internal RAM immediately before entering the HALT mode are retained. The on-chip peripheral functions that are not dependent on the instruction processing of the CPU continue to operate.

Table 6-2 shows the status of each hardware unit in the HALT mode.

Table 6-2. Operating Status in HALT Mode

Function		Operating Status	
Clock Generator		Operates	
Internal System Clock		Operates	
CPU		Stops	
I/O Port		Retained	
Peripheral Function		Operates	
Internal Data		Status of internal data before setting of HALT mode, such as CPU registers, status, data, and internal RAM contents, are retained.	
External Expansion Mode	AD0 to AD15	High impedance ^{Note}	
	A16 to A23	Retained ^{Note}	High-impedance when $\overline{\text{HLD\!A\!K}} = 0$
	$\overline{\text{LBEN}}, \overline{\text{UBEN}}$		
	$\text{R}/\overline{\text{W}}$	High level output ^{Note}	
	$\overline{\text{DSTB}}, \overline{\text{WRL}}, \overline{\text{WRH}}, \overline{\text{RD}}$		
	ASTB		
	$\overline{\text{HLD\!A\!K}}$	Operates	
CLKOUT		Clock output (when clock output is not disabled)	
CLO		Retained (CLE bit of the CLOM register = 0) Clock output (CLE bit of the CLOM register = 1)	

Note The instruction fetch operation continues even after the HALT instruction has been executed, until the internal instruction prefetch queue becomes full. After the queue has become full, the operation is stopped in the status indicated in the above Table 6-2.

(2) Releasing HALT mode

The HALT mode can be released by the non-maskable interrupt request, an unmasked maskable interrupt request, or a $\overline{\text{RESET}}$ signal input.

(a) Releasing by interrupt request

The HALT mode is unconditionally released by the NMI request or an unmasked maskable interrupt request, regardless of the priority. However, if the HALT mode is set in an interrupt processing routine, the operation will differ as follows:

- (i) If an interrupt request with a priority lower than that of the interrupt request under execution is generated, the HALT mode is released, but the newly generated interrupt request is not accepted. The new interrupt request will be kept pending.
- (ii) If an interrupt request with a priority higher (including NMI request) than the interrupt request under execution is generated, the HALT mode is released, and the interrupt request is also accepted.

Operation after HALT mode has been released by interrupt request

Releasing Source	Interrupt Enable (EI) Status	Interrupt disable (DI) Status
NMI request	Branches to handler address	
Maskable interrupt request	Branches to handler address or executes next instruction	Executes next instruction

(b) Releasing by $\overline{\text{RESET}}$ signal input

The same operation as the normal reset operation is performed.

6.5.4 IDLE mode

(1) Entering and operation status

In this mode, both the CPU clock and the internal system clock are stopped to further reduce power consumption. However, since the clock generator continues to run, normal operation can resume without having to wait for the oscillator and PLL circuit to stabilize.

The IDLE mode is entered when the PSC register is programmed by the store (ST/SST) instruction or bit manipulation (SET1/CLR1/NOT1) instruction.

Execution of the program is stopped in the IDLE mode, but the contents of the registers and internal RAM immediately before entering the IDLE mode are retained. The on-chip peripheral functions are stopped in this mode. External bus hold request ($\overline{\text{HLDRQ}}$) is not accepted.

Table 6-3 shows the hardware status in the IDLE mode.

Table 6-3. Operating Status in IDLE Mode

Function		Operating Status
Clock Generator		Operates
Internal System Clock		Stops
CPU		Stops
I/O Port		Retained
Peripheral Function		Stops
Internal Data		Status of all internal data immediately before IDLE mode is entered, such as CPU registers, status, data, and internal RAM contents, are retained.
External Expansion Mode	AD0 to AD15	High-impedance
	A16 to A23	
	$\overline{\text{LBEN}}$, $\overline{\text{UBEN}}$	
	$\text{R}/\overline{\text{W}}$	
	$\overline{\text{DSTB}}$, $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, $\overline{\text{RD}}$	
	ASTB	
	$\overline{\text{HLDK}}$	
CLKOUT		Low level output
CLO		Retained ^{Note}

Note Set the CLE bit of the CLOM register to 0 before switching over to the IDLE mode.

(2) Releasing IDLE mode

The IDLE mode is released by the NMI signal input or $\overline{\text{RESET}}$ signal input.

(a) Releasing by NMI signal input

The NMI request is accepted and serviced as soon as the IDLE mode has been released.

If the IDLE mode is entered in the NMI processing routine, however, only the IDLE mode is released, and the interrupt will not be accepted. The interrupt request will be retained and kept pending.

The interrupt processing that is started by the NMI signal input when the IDLE mode is released is treated in the same manner as a normal NMI interrupt that is processed (because there is only one vector address of the NMI interrupt). Therefore, if it is necessary to distinguish between the two types of NMI interrupts, a software flag should be defined in advance, and the flag must be set before setting the IDLE flag by the store/bit manipulation instruction. By checking this flag during the NMI interrupt processing, the NMI used to released the IDLE mode can be distinguished from the normal NMI.

(b) Releasing by $\overline{\text{RESET}}$ signal input

The same operation as the normal reset operation is performed.

6.5.5 Software STOP mode

(1) Entering and operation status

In this mode, the CPU clock, the internal system clock, and the clock generator are stopped, reducing power consumption to only leakage current. In this state, power consumption is minimized.

The software STOP mode is entered by programming the PSC register (Specific register) using the store (ST/SST) or bit manipulation (SET1/CLR1/NOT1) instruction (refer to **3.4.9 Specific register**).

It is necessary to ensure the oscillation stabilization time of the oscillator circuit after the software STOP mode has been released, when the oscillator connection mode (CESEL bit = "0") are set.

In the software STOP mode, program execution is stopped, but all the contents of the registers and internal RAM immediately before entering the STOP mode are retained. The on-chip peripheral function also stops operation.

Table 6-4 shows the hardware status in the software STOP mode.

Table 6-4. Operating Status in Software STOP Mode

Function		Operating Status
Clock Generator		Stops
Internal System Clock		Stops
CPU		Stops
I/O Port ^{Note 1}		Retained
Peripheral Function		Stops
Internal Data ^{Note 1}		Status of all internal data immediately before software STOP mode is set, such as CPU registers, status, data, and internal RAM contents, are retained.
External Expansion Mode	AD0 to AD15	High-impedance
	A16 to A23	
	LBEN, UBEN	
	R/W	
	DSTB, WRL, WRH, RD	
	ASTB	
	HLD $\overline{\text{AK}}$	
CLKOUT		Low level output
CLO		Retained ^{Note 2}

- Notes**
1. When the value of V_{DD} is within the operating range.
Even if V_{DD} drops below the minimum operating voltage, the contents of the internal RAM can be retained if the data retention voltage V_{DDDR} is maintained.
 2. Set the CLE bit of the CLOM register to 0 before switching over to the software STOP mode.

(2) Releasing software STOP mode

The STOP mode is released by the NMI signal input or $\overline{\text{RESET}}$ signal input.

It is necessary to ensure the oscillation stabilization time when releasing from the STOP mode in the PLL mode (CKSEL bit = "0") and oscillator connection mode (CESEL bit = "0").

Moreover, the lock up time of the PLL may also be necessary, depending on the application. For details, refer to section **6.4 PLL Lock-up**.

(a) Releasing by NMI signal input

When the STOP mode is released by the NMI signal, the NMI request is also accepted.

If the STOP mode is set in an NMI processing routine, however, only the STOP mode is released, and the interrupt is not accepted. The interrupt request is retained and kept pending.

NMI interrupt processing on releasing STOP mode

The interrupt processing that is started by the NMI signal input when the STOP mode is released is treated in the same manner as a normal NMI interrupt that is processed (because there is only one handler address of the NMI interrupt). Therefore, if it is necessary to distinguish between the two types of NMI interrupts, a software flag should be defined in advance, and the flag must be set before setting the STOP flag by the store/bit manipulation instruction. By checking this flag during the NMI interrupt processing, the NMI used to released the STOP mode can be distinguished from the normal NMI.

(b) Releasing by $\overline{\text{RESET}}$ signal input

The operation same as the normal reset operation is performed.

6.6 Specifying Oscillation Stabilization Time

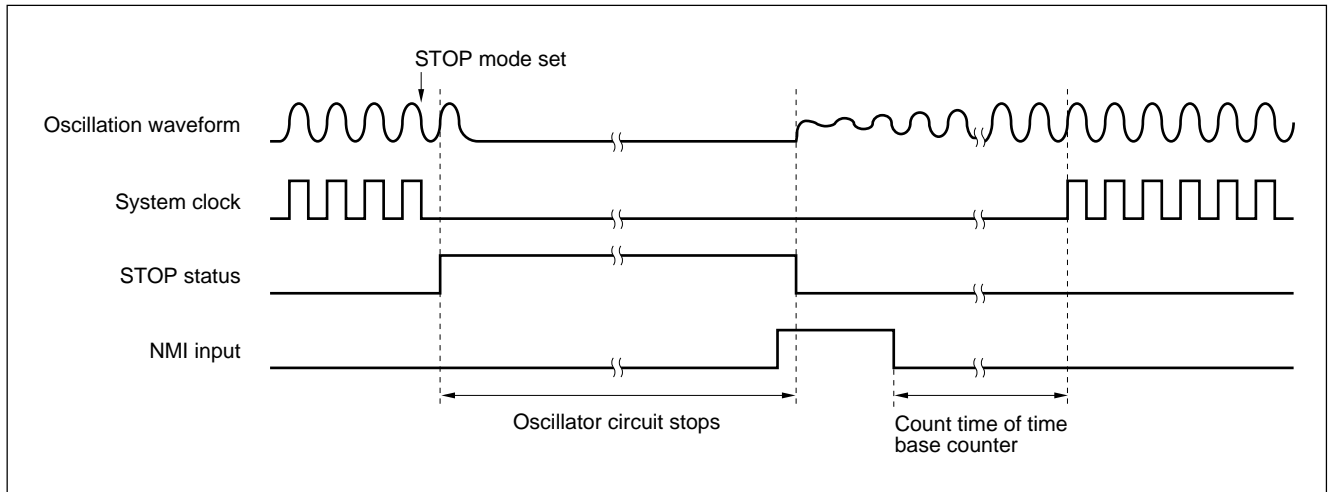
The time required for the oscillator circuit to become stabilized after the STOP mode has been released can be specified in the following two ways:

★ (1) Securing time using internal time base counter (NMI pin input)

When the valid edge is input to the NMI pin, the STOP mode is released. When the inactive edge is input to the pin, the time base counter (TBC) starts counting, and the time required for the clock output from the oscillator circuit to become stabilized is specified by that count time.

Oscillation stabilization time \simeq (Active level width after valid edge of NMI input has been detected) + (Count time of TBC)

After a specific time has elapsed, the system clock output is started, and execution branches to the handler address of the NMI interrupt.



During inactivity, the NMI pin should be kept at the inactive level (e.g. when the valid edge is specified to be the falling edge).

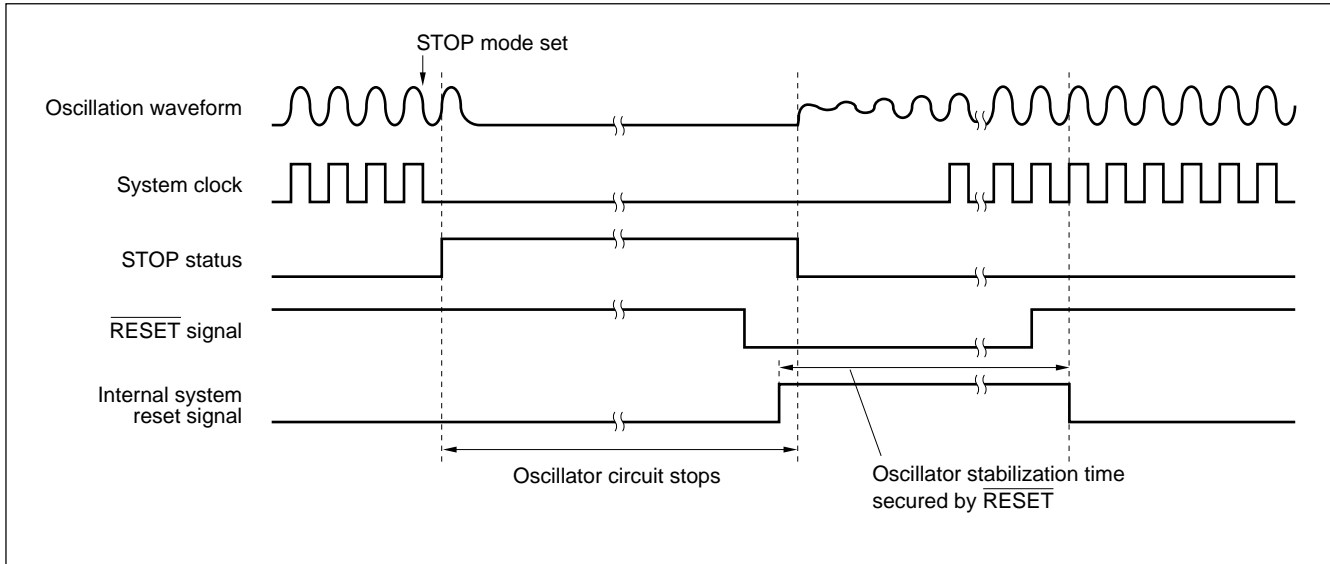
If an operation to enter the STOP mode is performed while a valid edge has been input to the NMI pin before the CPU accepts the interrupt, the STOP mode will immediately be released. If the clock generator is driven by a PLL (CKSEL = 0) and an oscillator (CESEL = 0), program execution is started after the oscillation stabilization time specified in the time base counter has elapsed.

(2) Securing time by signal level width ($\overline{\text{RESET}}$ pin input)

The STOP mode is released when the falling edge is input to the $\overline{\text{RESET}}$ pin.

The time required for the clock output from the oscillator circuit to become stabilized is specified by the low-level width of the signal input to the $\overline{\text{RESET}}$ pin.

After the rising edge has been input to the $\overline{\text{RESET}}$ pin, operation of the internal system clock begins, and execution branches to the vector address that is used when the system is reset.



★ **Time base counter (TBC)**

The time base counter (TBC) is used to secure the oscillation stabilization time of the oscillator circuit when the software STOP mode is released.

- In oscillator connecting mode (CESEL = 0)

TBC counts the oscillation stabilization time after the STOP mode is released, and the execution of a program is started after the counting is completed.

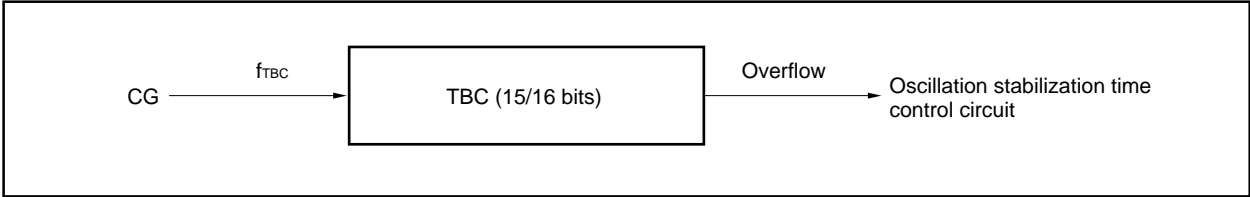
- ★ In both the PLL mode (CKSEL = 0) and oscillator connecting mode (CESEL = 0), the count clock of TBC is selected by the TBCS bit of the PSC register and the following count time can be set.

Table 6-5. Example of Count Time

TBCS	Frequency Division	Count Time			
		$f_{XX} = 5.0 \text{ MHz}$	$f_{XX} = 6.6 \text{ MHz}$	$f_{XX} = 25.0 \text{ MHz}$	$f_{XX} = 33.0 \text{ MHz}$
0	$2^{15}/f_{TBC}$	13.1 ms	9.8 ms	2.6 ms	2.0 ms
1	$2^{16}/f_{TBC}$	26.2 ms	19.6 ms	5.2 ms	4.0 ms

f_{TBC} : $f_{XX}/2$

Figure 6-1. Block Configuration



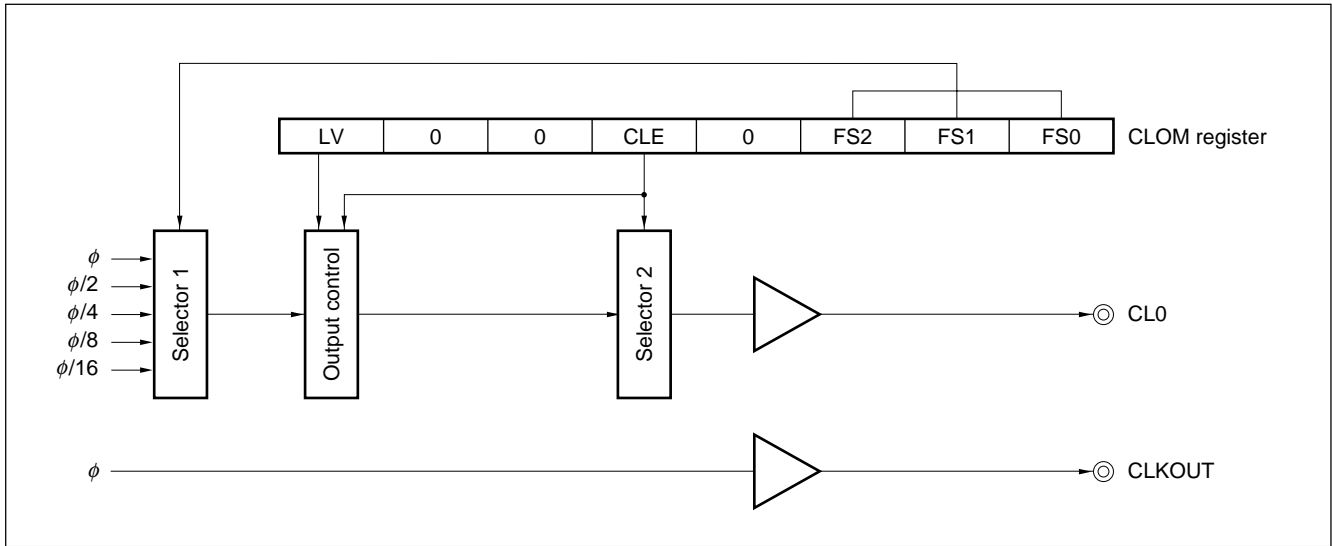
6.7 Clock Output Control

The V854 can output CLKOUT signal which has the same frequency as that of the system clock and CLO signal which is the frequency division of the system clock.

- CLKOUT signal = ϕ (system clock)
- CLO signal = ϕ , $\phi/2$, $\phi/4$, $\phi/8$, $\phi/16$

The V854 can also be used as a 1-bit output port.

6.7.1 Configuration



6.7.2 CLKOUT signal output control

The operation mode of the CLKOUT pin can be selected by the DCLK0 and DCLK1 bits of the PSC register.

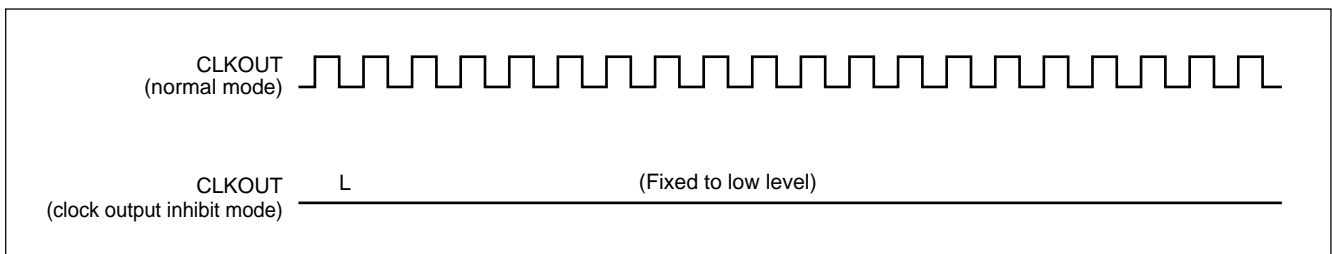
By using this operation mode in combination with the HALT, IDLE, or software STOP mode, the power dissipation can be effectively reduced (for how to write these bits, refer to **6.5.2 Control registers**).

Clock output inhibit mode

The clock output from the CLKOUT pin is inhibited.

This mode is ideal for single-chip mode systems or systems that fetch instructions to external expansion devices or asynchronously accesses data.

Because the operation of CLKOUT is completely stopped in this mode, the power dissipation can be minimized and radiation noise from the CLKOUT pin can be suppressed.



The PSC register reset value is 00H in ROMless mode 1 and 2 and single-chip mode 2 and C0H in single-chip mode 1 and PROM mode. Therefore, the CLKOUT signal is output during the reset period in ROMless mode 1 and 2 and single-chip mode 2. In single-chip mode 1, the CLKOUT signal is not output until the DCLK1 and DCLK0 bits of the PSC register are set to “11” after reset is released (low level output).

In the PROM mode, the CLKOUT signal is not output (low level output).

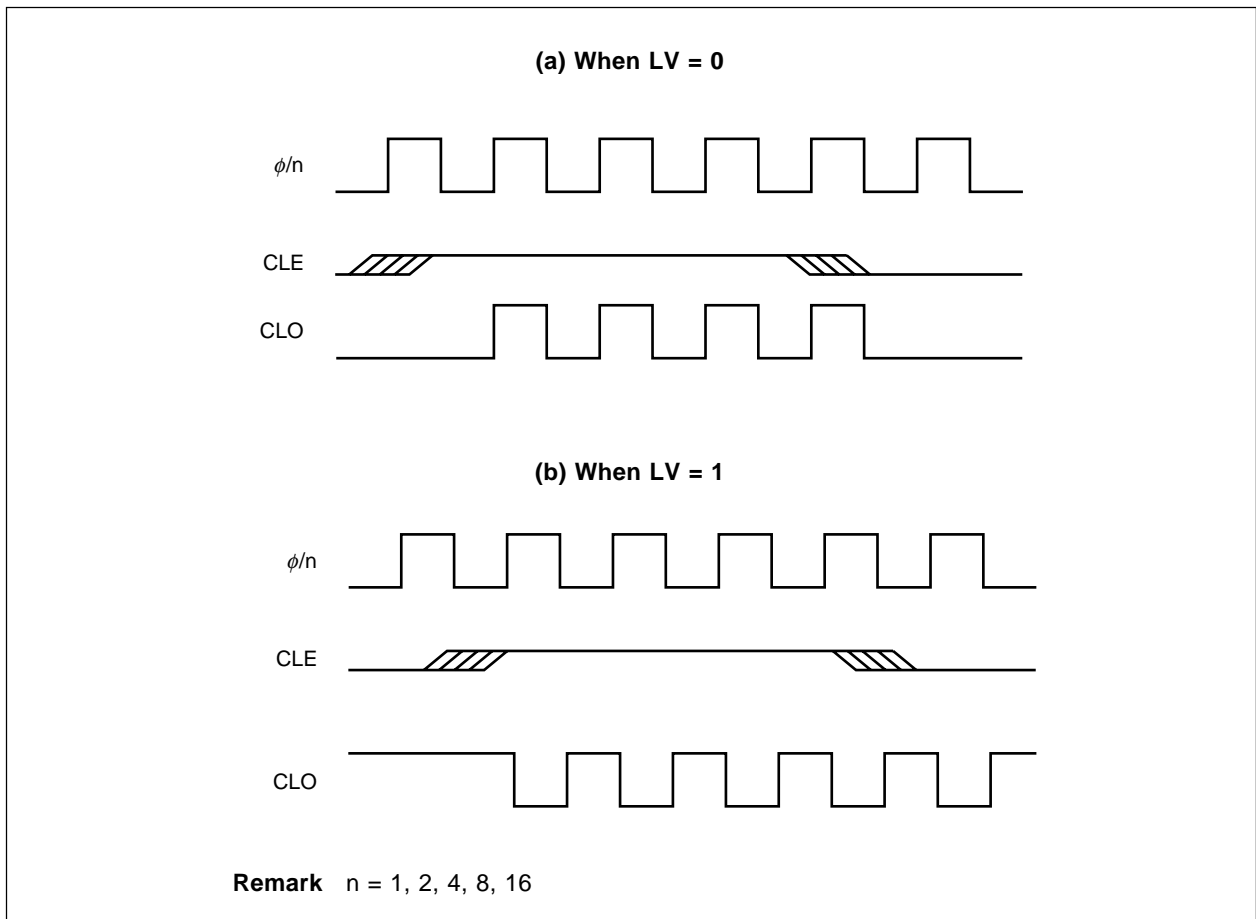
6.7.3 CLO signal output control

The clock to be output to CLO pin can be selected by the FS bit of the CLOM register.

CLO pin outputs a signal which has the same level as that of the LV bit when the CLE bit is 0. Signal is output synchronized with the clock (the frequency selected by the FS bit) immediately after the CLE bit is set to 1.

Then, if the CLE bit is set to 0, the same level as that of the LV bit is output, and the output operation thereafter is stopped.

Figure 6-2. CLO Signal Output Timing



(1) Clock output mode register (CLOM)

This register controls clock output function. This register can be read/written in 8- or 1-bit units.

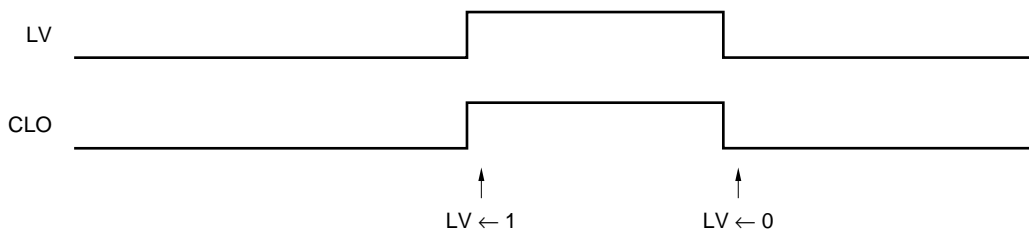
	7	6	5	4	3	2	1	0		
CLOM	LV	0	0	CLE	0	FS2	FS1	FS0	Address FFFFFF3D0H	After reset 00H

Bit Position	Bit Name	Function																												
7	LV	Level Selects output level of CLO signal 0 : Low-level output 1 : High-level output																												
4	CLE	Clock Enable Controls clock output of CLO signal 0 : Outputs the contents of LV bit 1 : Outputs the clock selected by FS2 to FS0 bits																												
2 to 0	FS2 to FS0	Frequency Select Selects the frequency of CLO signal <table border="1"><thead><tr><th>FS2</th><th>FS1</th><th>FS0</th><th>Selection of Frequency</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>ϕ</td></tr><tr><td>0</td><td>0</td><td>1</td><td>$\phi/2$</td></tr><tr><td>0</td><td>1</td><td>0</td><td>$\phi/4$</td></tr><tr><td>0</td><td>1</td><td>1</td><td>$\phi/8$</td></tr><tr><td>1</td><td>0</td><td>0</td><td>$\phi/16$</td></tr><tr><td colspan="3">Others</td><td>Setting prohibited</td></tr></tbody></table> Remark ϕ : Internal system clock	FS2	FS1	FS0	Selection of Frequency	0	0	0	ϕ	0	0	1	$\phi/2$	0	1	0	$\phi/4$	0	1	1	$\phi/8$	1	0	0	$\phi/16$	Others			Setting prohibited
FS2	FS1	FS0	Selection of Frequency																											
0	0	0	ϕ																											
0	0	1	$\phi/2$																											
0	1	0	$\phi/4$																											
0	1	1	$\phi/8$																											
1	0	0	$\phi/16$																											
Others			Setting prohibited																											

Caution Do not change the values of the other bits (LV, FS2 to FS0) during setting of the CLE bit (1).
Do not change the values of other bits (LV, FS2 to FS0) simultaneously with changing the value of the CLE bit.

(2) 1-bit output port

When the CLE bit is 0, CLO pin outputs the signals of the same level as that of the LV bit. When the contents of the LV bit is changed, CLO signal changes immediately.



(3) Operations in standby mode**(a) HALT mode**

The status before setting HALT mode is maintained. Clock continues to be output while clock is being output. When clock output is disabled, the signal of the same level that of the LV bit before HALT mode is set is output.

(b) Software STOP mode/IDLE mode

Disables clock output before setting these modes (the CLE bit is cleared by software). The signal of the same level as that of the LV bit before these modes are set is output from the CLO pin.

[MEMO]

CHAPTER 7 TIMER/COUNTER FUNCTION (REAL-TIME PULSE UNIT)

7.1 Features

- Timer 0: 24-bit timer/event counter (1 channel)
 - Capture/compare registers: 4
 - Can be used as a trigger of A/D converter (CC03 coincidence)
 - Set/reset outputs: 2
 - Clearing and starting timer
 - External input pulse measurement
 - Overflow interrupt request and overflow flag
 - Applications: measurement of pulse interval and frequency, output of pulses with various waveforms
- Timer 1: 24-bit timer/event counter (1 channel)
 - Capture registers: 4
 - Compare registers: 2
 - INTP edge detection circuit with 1 to 64/1 to 128 frequency divider
 - Can be used as a trigger of real time output port (CM10 coincidence)
 - Overflow interrupt request and overflow flag
 - Clearing and starting timer
 - Applications: measurement of pulse interval and frequency of software servo, etc.
- Timer 2: 16-bit interval timer counter (5 channels)
 - Compare registers: 1
 - Toggle output: 1
 - External input pulse measurement
 - Clearing and starting timer
 - Applications: interval timer, pulse counter, and pulse output of constant period for software
- Timer 3: 16-bit interval timer (1 channel)
 - Dedicated capture register: 1
 - Capture/compare register: 1
 - INTP edge detection circuit with digital noise elimination
 - Clearing and starting timer
 - Applications: measurement of pulse interval and frequencies such as pulse width measurement of remote controllers

7.2 Basic Configuration

Table 7-1. List of Real-Time Pulse Unit (RPU) Configuration

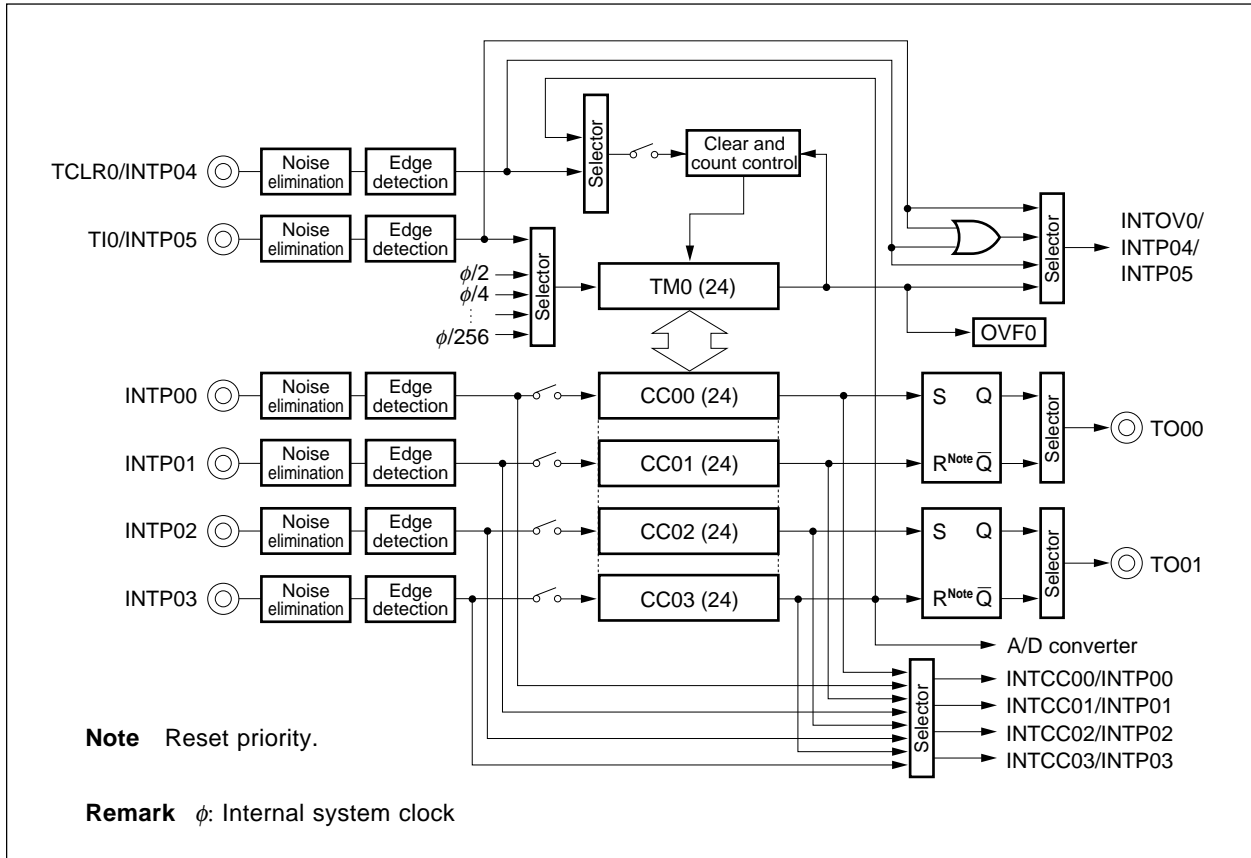
Timer	Bit Width	Count Clock	Register	Read/Write (R/W)	Clear Condition	Generated Interrupt Signal	Capture Trigger	Compare Match Trigger
Timer 0	24	$\phi/2$, $\phi/4$, $\phi/8$, $\phi/16$, $\phi/32$, $\phi/64$, $\phi/128$, $\phi/256$, T10 pin input	TM0	R	• INTOV0 input	INTOV0	—	—
			CC00	R/W	• TCLR0 input	INTCC00	INTP00	TO00 (S)
			CC01		• INTCC03 input	INTCC01	INTP01	TO00 (R)
			CC02			INTCC02	INTP02	TO01 (S)
			CC03			INTCC03	INTP03	TO01 (R), A/D converter
Timer 1	24	ϕ , $\phi/2$, $\phi/4$, $\phi/8$, $\phi/16$, $\phi/32$, $\phi/64$, $\phi/128$, $\phi/256$, T11 pin input	TM1	R	• INTOV1 input	INTOV1	—	—
			CP10		• Software clear	INTCP10	INTP10	—
			CP11			INTCP11	Frequency division of INTP11	—
			CP12			INTCP12	Frequency division of INTP12	—
			CP13			INTCP13	Frequency division of INTP12/INTP13	—
			CM10	R/W		INTCM10	—	Real time output port
			CM11			INTCM11	—	—
Timer 2	16	$\phi/2$, $\phi/4$, $\phi/8$, $\phi/16$, $\phi/32$, $\phi/64$, $\phi/128$, $\phi/256$, T12n pin input (n = 0 to 4)	TM20	R	• INTCM2n input	—	—	—
			CM20	R/W	• Software clear	INTCM20	—	TO20 (T)
			TM21	R		—	—	—
			CM21	R/W		INTCM21	—	TO21 (T)
			TM22	R		—	—	—
			CM22	R/W		INTCM22	—	TO22 (T)
			TM23	R		—	—	—
			CM23	R/W		INTCM23	—	TO23 (T)
			TM24	R		—	—	—
Timer 3	16	$\phi/2$, $\phi/4$, $\phi/8$, $\phi/16$, $\phi/32$, $\phi/64$, $\phi/128$, $\phi/256$	TM3	R	• INTCC3 input	—	—	—
			CC3	R/W	• Capture trigger of CC3	INTCC3	INTP30	—
			CP3	R	• Software clear	—	—	—

Remark ϕ : Internal system clock

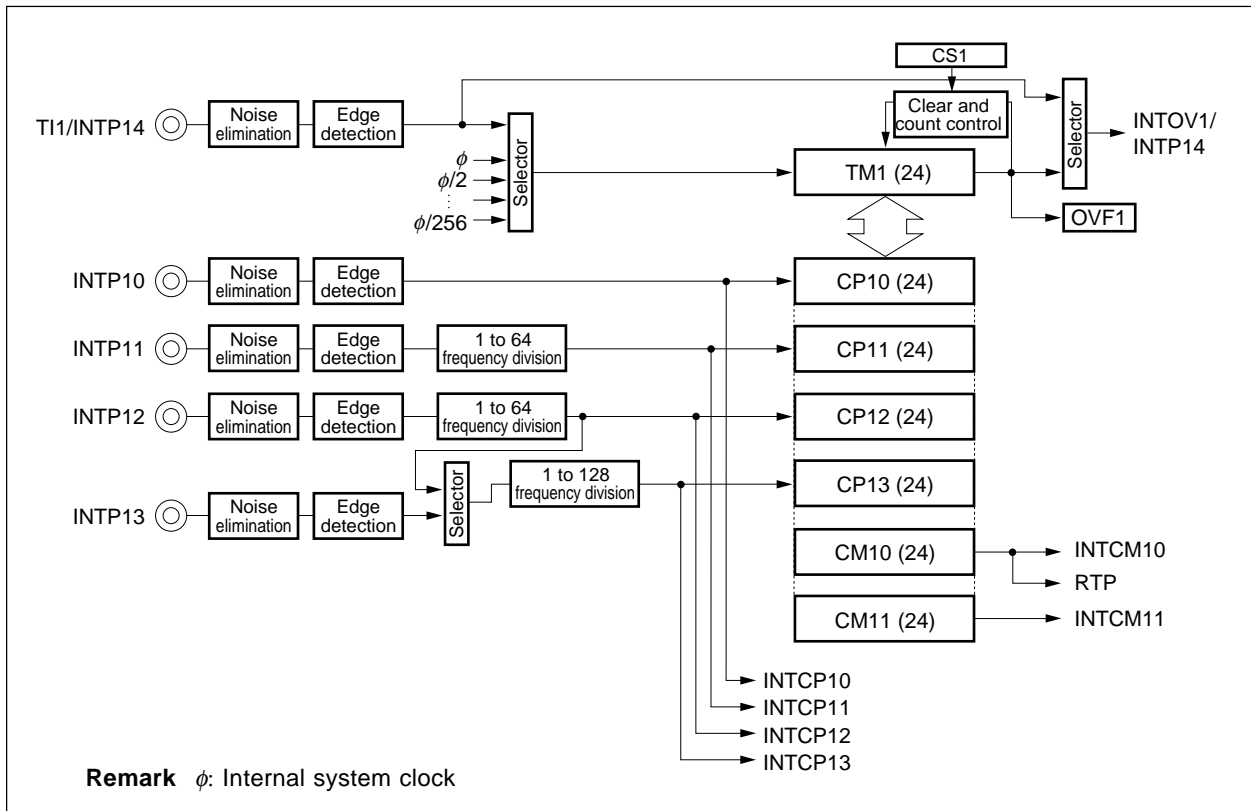
S/R: Set/reset

T : Toggle output

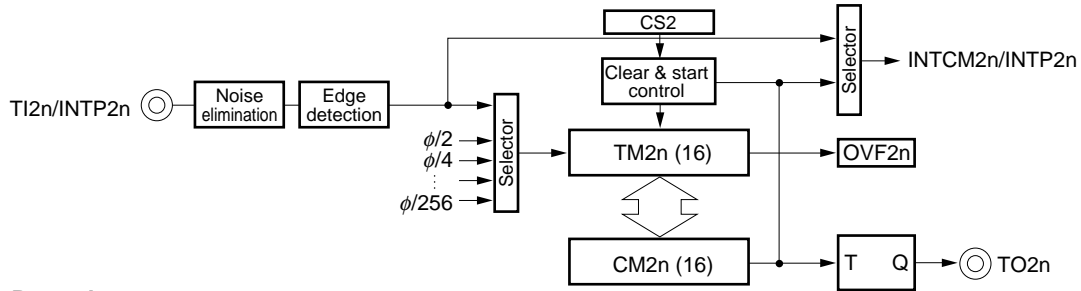
(1) Timer 0 (24-bit timer/event counter)



(2) Timer 1 (24-bit timer/event counter)

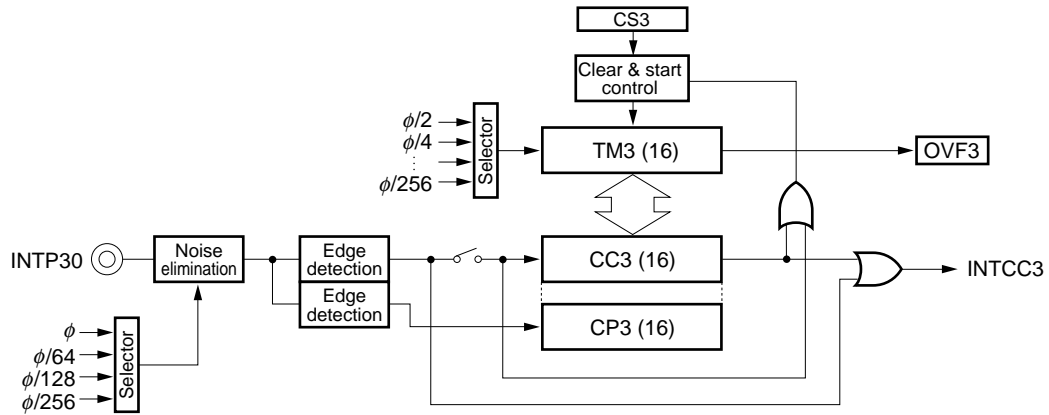


(3) Timer 2 (16-bit interval timer counter)



Remark $n : 0 \text{ to } 4$
 ϕ : Internal system clock

(4) Timer 3 (16-bit interval timer)

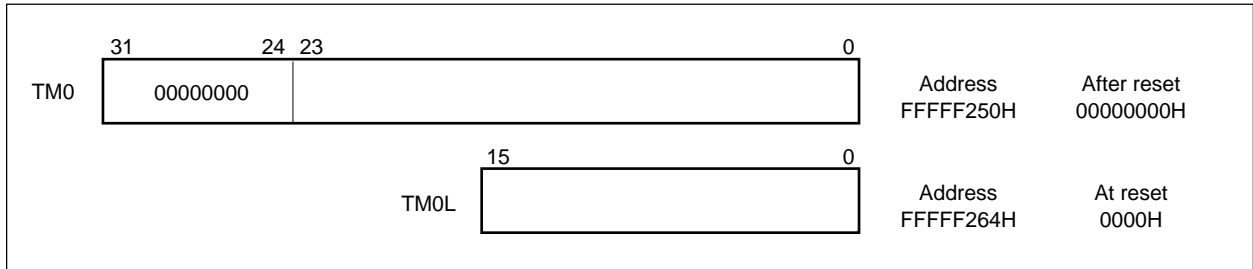


Remark ϕ : Internal system clock

7.2.1 Timer 0

(1) Timers 0, 0L (TM0, TM0L)

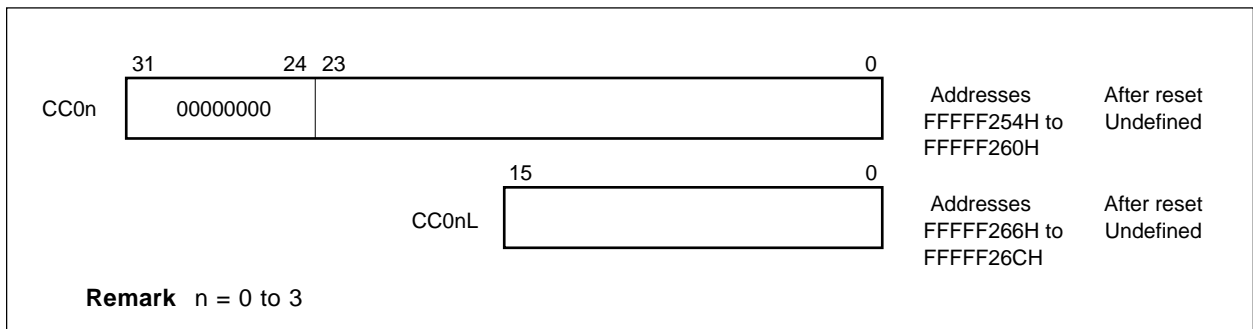
- ★ TM0 functions as a 24-bit interval timer, free-running timer or event counter for external signals. It is used to measure cycles and frequency, and also for pulse generation.
- Only 32-bit read access is enabled for TM0 (however, the high-order 8 bits are fixed to 0), and only 16-bit read access is enabled for TM0L.
- To read the low-order 24 bits of timer 0, specify TM0 with word access, and to read the low-order 16 bits only, specify TM0 with half-word access.



TM0 counts up the internal count clock or external count clock. The timer is started or stopped by the CEO bit of timer control register 00 (TMC00).

(2) Capture/compare registers 00 to 03 (CC00 to CC03, CC00L to CC03L)

- The capture/compare registers are 24-bit registers connected to TM0. They can be used as capture registers or compare registers depending on the specification of timer control register 01 (TMC01).
- 32-bit read/write access is enabled for CC0n (however, the high-order 8 bits are fixed to 0, and are ignored during write operation), and 16-bit read/write access is enabled for CC0nL.
- To access the low-order 24 bits or the low-order 16 bits of these registers, specify CC0n and CC0nL, respectively.



(a) When used as a capture register

When a capture/compare register is used as a capture register, it detects the valid edge of the corresponding external interrupt INTPn (n = 10 to 13) as a capture trigger. Timer 0 latches the count value in synchronization with the capture trigger (capture operation). The latched value is held by the capture register until the next capture operation is performed.

(b) When used as a compare register

When a capture/compare register is used as a compare register, it compares its contents with the value of the timer at each clock tick.

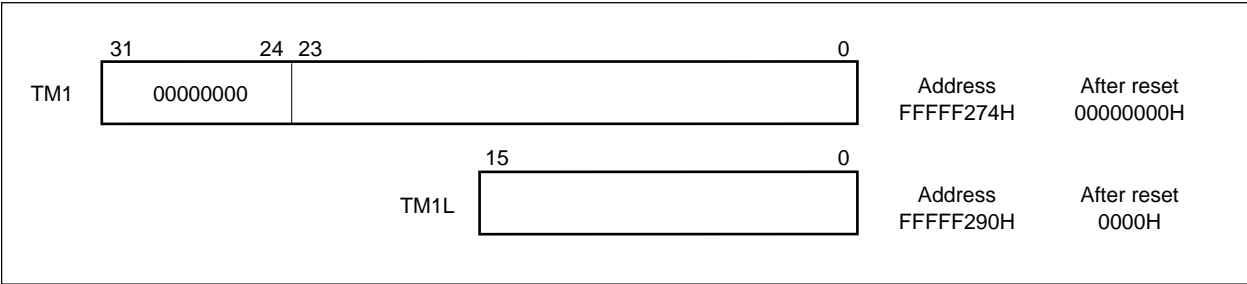
Compare registers support the set/reset output function. In other words, they set or reset the corresponding timer output synchronously with the coincidence signal generation.

7.2.2 Timer 1

(1) Timers 1, 1L (TM1, TM1L)

TM1 functions as a 24-bit free-running timer or event counter. Timers 1 to 14 are used to measure cycles and frequency, and also for programmable pulse generation.

TM1 is specified in 32-bit access, and TM1L is specified in lower 16-bit access. Only 32-bit read access is enabled for TM1, and only 16-bit read access is enabled for TM1L.

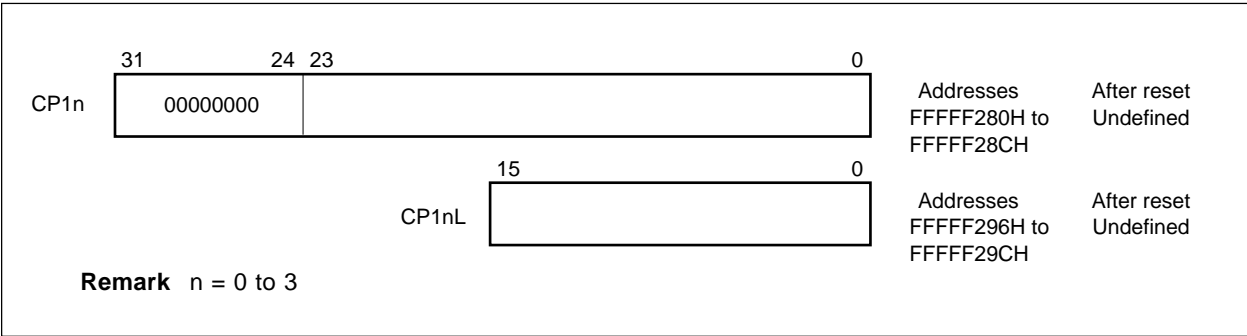


TM1 counts up the internal count clock or external count clock. The timer is started or stopped by the CE1 bit of timer control register 1 (TMC1).

(2) Capture registers 10 to 13 (CP10 to CP13, CP10L to CP13L)

The capture registers are 24-bit registers connected to TM1. These registers can be only read in 32-bit units. CP1n is specified in 32-bit access to this register. CP1nL is specified in lower 16-bit access.

Only 32-bit read access is enabled for CP1n, and only 16-bit read access is enabled for CP1nL.



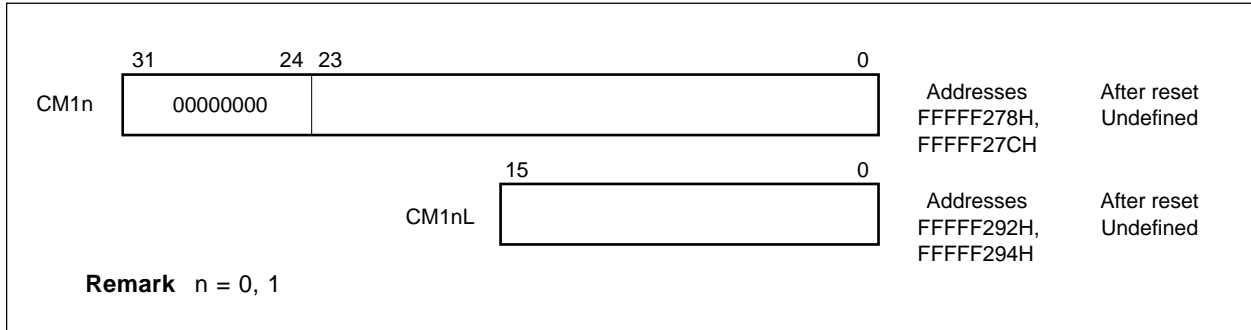
(3) Compare registers 10, 11 (CM10, CM11, CM10L, CM11L)

The compare registers are 24-bit registers connected to TM1. These registers can be read or written in 32-bit units.

CM1n is specified in 32-bit access to this register. CM1nL is specified in lower 16-bit access.

CM1n can be read or written in 32-bit units. The values written in bits 24 to 31 are ignored.

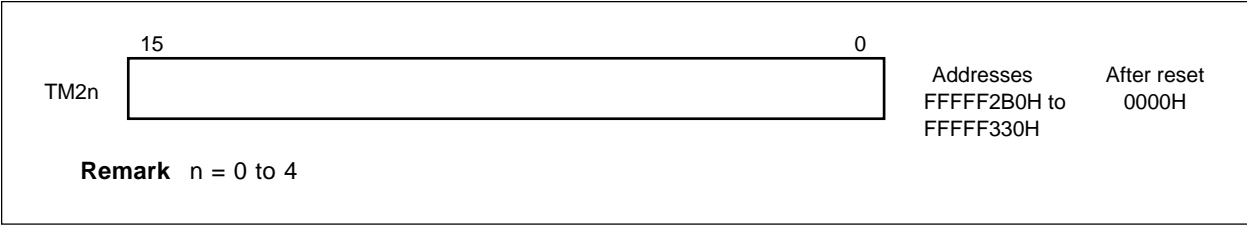
CM1nL can be read or written in 16-bit units. 00H is written in the higher bits (bits 16 to 23) in write access to CM1nL.



7.2.3 Timer 2

(1) Timers 20 to 24 (TM20 to TM24)

TM2n is a 16-bit timer and is mainly used as an interval timer for software.
TM2n can be only read in 16-bit units.

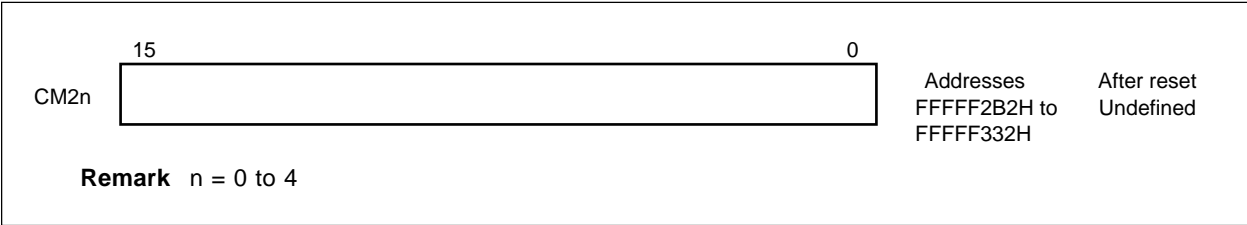


TM2n is started or stopped by the CE2n bit of timer control register 2n (TMC2n).
The count clock is selected by the TMC2n register from $\phi/2$, $\phi/4$, $\phi/8$, $\phi/16$, $\phi/32$, $\phi/64$, $\phi/128$, $\phi/256$, and TI2n input.

Caution When the value of the timer coincides with the value of the compare register (CM2n), the timer is cleared by the next clock tick. If the division ratio is large and results in a slow clock period, the timer value may not be cleared to zero yet, if the timer is read immediately after the occurrence of the coincidence signal interrupt.
The count clock cannot be changed during timer operations.

(2) Compare registers 20 to 24 (CM20 to CM24)

The compare registers are 16-bit registers connected to TM2n. These registers can be read or written in 16-bit units.

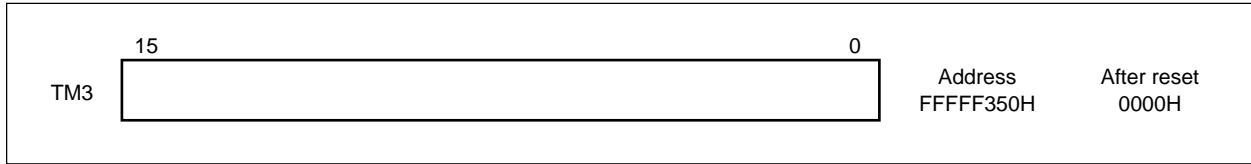


7.2.4 Timer 3

(1) Timer 3 (TM3)

TM3 is a 16-bit timer and is mainly used as an interval timer for software.

This timer can be only read in 16-bit units.



TM3 is started or stopped by the CE3 bit of timer control register 3 (TMC3).

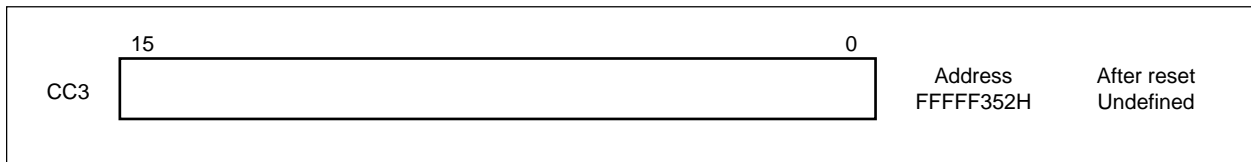
The count clock is selected by the TMC3 register from $\phi/2$, $\phi/4$, $\phi/8$, $\phi/16$, $\phi/32$, $\phi/64$, $\phi/128$, or $\phi/256$.

Caution When the value of the timer matches the value of the compare register (CM4), the timer is cleared by the next clock tick. If the division ratio is large and results in a slow clock period, the timer value may not be cleared to zero yet, if the timer is read immediately after the occurrence of the coincidence signal interrupt.

The count clock cannot be changed during timer operations.

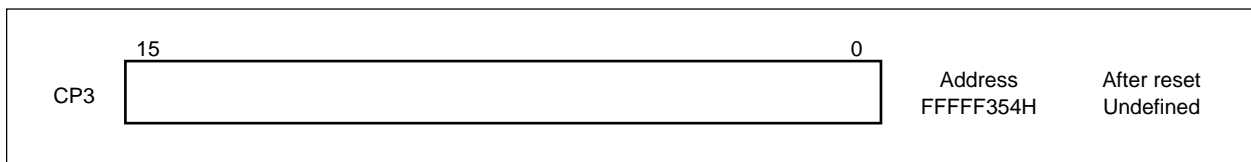
(2) Capture compare register 3 (CC3)

CC3 is a 16-bit register connected to TM3. This register can be read/written in 16-bit units.



(3) Capture register 3 (CP3)

CP3 is a 16-bit register connected to TM3. This register can be only read in 16-bit units.



7.3 Control Register

(1) Timer control register 00 (TMC00)

TMC00 specifies control of count enable/disable and the count clock of TM0.

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
TMC00	CE0	OST0	0	0	PRM03	PRM02	PRM01	PRM00	Address FFFFFF240H	After reset 01H

Bit Position	Bit Name	Function																																																							
7	CE0	<p>Count Enable</p> <p>Specifies enable/disable of timer/count.</p> <p>0 : Timer count disabled (stops at TM0 = 000000H)</p> <p>1 : Timer count enabled</p> <p>When TMC02. ECLR0 = 1, the timer does not start counting up until TCLR0 input.</p> <p>When TMC02. ECLR0 = 0, writing “1” to the CE0 bit triggers count start of the timer.</p> <p>Therefore, even ECLR0 = 0 is set after setting CE0 with ECLR0 = 1, the timer does not start.</p>																																																							
6	OST0	<p>Overflow Stop</p> <p>Specifies the operation after overflow of timer.</p> <p>0 : The timer continues counting after overflow has occurred</p> <p>1 : The timer retains 000000H and stops after overflow has occurred</p> <p>The timer resumes counting when the following operation is performed.</p> <p>When ECLR0 = 0: writing 1 to CE0 bit</p> <p>When ECLR0 = 1: trigger inputting to timer clear pin (TCLR0)</p>																																																							
3 to 0	PRM03 to PRM00	<p>Prescaler Clock Mode</p> <p>Selects the count clock frequency.</p> <table><tr><th>PRM03</th><th>PRM02</th><th>PRM01</th><th>PRM00</th><th>Count Clock</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>$\phi/2$</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>$\phi/4$</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>$\phi/8$</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>$\phi/16$</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>$\phi/32$</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>$\phi/64$</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>$\phi/128$</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>$\phi/256$</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>TIO input</td></tr><tr><td colspan="4">Others</td><td>Setting prohibited</td></tr></table> <p>Caution Do not change the count clock frequency while the timer operates.</p> <p>Remark ϕ: Internal system clock</p>	PRM03	PRM02	PRM01	PRM00	Count Clock	0	0	0	1	$\phi/2$	0	0	1	0	$\phi/4$	0	0	1	1	$\phi/8$	0	1	0	0	$\phi/16$	0	1	0	1	$\phi/32$	0	1	1	0	$\phi/64$	0	1	1	1	$\phi/128$	1	0	0	0	$\phi/256$	1	1	1	1	TIO input	Others				Setting prohibited
PRM03	PRM02	PRM01	PRM00	Count Clock																																																					
0	0	0	1	$\phi/2$																																																					
0	0	1	0	$\phi/4$																																																					
0	0	1	1	$\phi/8$																																																					
0	1	0	0	$\phi/16$																																																					
0	1	0	1	$\phi/32$																																																					
0	1	1	0	$\phi/64$																																																					
0	1	1	1	$\phi/128$																																																					
1	0	0	0	$\phi/256$																																																					
1	1	1	1	TIO input																																																					
Others				Setting prohibited																																																					

(2) Timer control register 01 (TMC01)

TMC01 selects the function of the capture/compare register and sets enable/disable of the timer clear function.

The contents of the register and the timer count operation are not affected even if the contents of TMC01 is rewritten during timer 0 operation.

This register can be read/written in 8- or 1-bit units.

TMC01

	7	6	5	4	3	2	1	0
	CMS03	CMS02	CMS01	CMS00	IMS03	IMS02	IMS01	IMS00

Address
After reset

FFFFFF242H
00H

Bit Position	Bit Name	Function															
7 to 4	CMS03 to CMS00	Capture/Compare Mode Select Selects the operation mode of the capture/compare register (CC0n). Set in combination with the IMS bit. For the contents of the setting, refer to the explanation of the IMS bit.															
3 to 0	IMS03 to IMS00	Interrupt Mode Select Selects the interrupt source. Set in combination with the CMS bit. <table border="1" style="border-collapse: collapse; margin-top: 10px; width: 100%;"> <thead> <tr> <th style="width: 15%;">CMS0n</th> <th style="width: 15%;">IMS0n</th> <th style="width: 70%;">CC0n Register Operation Mode/Interrupt Source Selection</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td>Operates as a capture register. Interrupt is generated at capture timing.</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td>Setting prohibited</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td>Operates as a compare register. Interrupt is generated by coincidence signal of compare register. Capture trigger from INTP0n is ignored.</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td>Operates as a compare register. Interrupt is generated at INTP0n signal input timing.</td> </tr> </tbody> </table>	CMS0n	IMS0n	CC0n Register Operation Mode/Interrupt Source Selection	0	0	Operates as a capture register. Interrupt is generated at capture timing.	0	1	Setting prohibited	1	0	Operates as a compare register. Interrupt is generated by coincidence signal of compare register. Capture trigger from INTP0n is ignored.	1	1	Operates as a compare register. Interrupt is generated at INTP0n signal input timing.
CMS0n	IMS0n	CC0n Register Operation Mode/Interrupt Source Selection															
0	0	Operates as a capture register. Interrupt is generated at capture timing.															
0	1	Setting prohibited															
1	0	Operates as a compare register. Interrupt is generated by coincidence signal of compare register. Capture trigger from INTP0n is ignored.															
1	1	Operates as a compare register. Interrupt is generated at INTP0n signal input timing.															

Remark n = 0 to 3

(3) Timer control register 02 (TMC02)

TMC02 selects the function of the capture/compare register and sets enable/disable of the timer clear function.

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
TMC02	0	0	IMS05	IMS04	0	0	ECLR0	CCLR0	Address FFFFFF244H	After reset 00H

Bit Position	Bit Name	Function															
5, 4	IMS05, IMS04	<p>Interrupt Mode Select Selects the interrupt source.</p> <table><tr><th>IMS05</th><th>IMS04</th><th>Selection of Interrupt Source</th></tr><tr><td>0</td><td>0</td><td>Overflow interrupt is generated by TM0</td></tr><tr><td>0</td><td>1</td><td>Interrupt is generated by INTP04</td></tr><tr><td>1</td><td>0</td><td>Interrupt is generated by INTP05</td></tr><tr><td>1</td><td>1</td><td>Interrupt is generated by OR of INTP04 and INTP05</td></tr></table>	IMS05	IMS04	Selection of Interrupt Source	0	0	Overflow interrupt is generated by TM0	0	1	Interrupt is generated by INTP04	1	0	Interrupt is generated by INTP05	1	1	Interrupt is generated by OR of INTP04 and INTP05
IMS05	IMS04	Selection of Interrupt Source															
0	0	Overflow interrupt is generated by TM0															
0	1	Interrupt is generated by INTP04															
1	0	Interrupt is generated by INTP05															
1	1	Interrupt is generated by OR of INTP04 and INTP05															
1	ECLR0	<p>External Input Timer Clear Controls clear and start of TM0 by external clear input (TCLR0).</p> <table><tr><th>ECLR0</th><th>Clear and Start of TM0</th></tr><tr><td>0</td><td>TM0 is not cleared</td></tr><tr><td>1</td><td>TM0 is cleared and count up starts</td></tr></table>	ECLR0	Clear and Start of TM0	0	TM0 is not cleared	1	TM0 is cleared and count up starts									
ECLR0	Clear and Start of TM0																
0	TM0 is not cleared																
1	TM0 is cleared and count up starts																
0	CCLR0	<p>Compare Input Timer Clear Controls clear and start of TM0 by CC03 match.</p> <table><tr><th>CCLR0</th><th>Clear and Start of TM0</th></tr><tr><td>0</td><td>TM0 is not cleared</td></tr><tr><td>1</td><td>TM0 is cleared and count up starts</td></tr></table>	CCLR0	Clear and Start of TM0	0	TM0 is not cleared	1	TM0 is cleared and count up starts									
CCLR0	Clear and Start of TM0																
0	TM0 is not cleared																
1	TM0 is cleared and count up starts																

(4) Timer control register 1 (TMC1)

TMC1 specifies count enable/disable and controls the count clock of TM1.

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
TMC1	CE1	OST1	CS1	IMS1	PRM13	PRM12	PRM11	PRM10	Address FFFFFF270H	After reset 01H

Bit Position	Bit Name	Function																																																							
7	CE1	Count Enable Specifies enable/disable of timer count. 0 : Timer count disabled (stops at TM1 = 000000H) 1 : Timer count enabled																																																							
6	OST1	Overflow Stop Specifies the operation after overflow of timer. 0 : The timer continues counting after overflow has occurred 1 : The timer retains 000000H and stops after overflow has occurred The timer resumes counting when the following operation is performed. Writing 1 to CE1 bit Writing 1 to CS1 bit																																																							
5	CS1	Clear & Start Controls clear/start of TM1 by software. This bit is always 0 when writing. 0 : Continues counting 1 : Clears TM1 and resumes counting																																																							
4	IMS1	Interrupt Mode Select Selects interrupt source. 0 : Interrupt occurs by overflow of TM1 1 : Interrupt occurs by INTP14 signal																																																							
3 to 0	PRM13 to PRM10	Prescaler Clock Mode Selects the count clock frequency. <table><tr><th>PRM13</th><th>PRM12</th><th>PRM11</th><th>PRM10</th><th>Count Clock</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>ϕ</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>$\phi/2$</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>$\phi/4$</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>$\phi/8$</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>$\phi/16$</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>$\phi/32$</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>$\phi/64$</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>$\phi/128$</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>$\phi/256$</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>TI1 input</td></tr></table> <div><div>Caution</div><div>Do not change the count clock frequency while the timer operates.</div></div> <div><div>Remark</div><div>ϕ: Internal system clock</div></div>	PRM13	PRM12	PRM11	PRM10	Count Clock	0	0	0	0	ϕ	0	0	0	1	$\phi/2$	0	0	1	0	$\phi/4$	0	0	1	1	$\phi/8$	0	1	0	0	$\phi/16$	0	1	0	1	$\phi/32$	0	1	1	0	$\phi/64$	0	1	1	1	$\phi/128$	1	0	0	0	$\phi/256$	1	1	1	1	TI1 input
PRM13	PRM12	PRM11	PRM10	Count Clock																																																					
0	0	0	0	ϕ																																																					
0	0	0	1	$\phi/2$																																																					
0	0	1	0	$\phi/4$																																																					
0	0	1	1	$\phi/8$																																																					
0	1	0	0	$\phi/16$																																																					
0	1	0	1	$\phi/32$																																																					
0	1	1	0	$\phi/64$																																																					
0	1	1	1	$\phi/128$																																																					
1	0	0	0	$\phi/256$																																																					
1	1	1	1	TI1 input																																																					

(5) Timer control register 20 to 24 (TMC20 to TMC24)

TMC2n specifies count enable/disable and controls the count clock of TM2n.

This register can be read/written in 8- or 1-bit units.

TMC20	7	6	5	4	3	2	1	0	Address FFFFF2A0H	After reset 01H
	CE20	IMS20	CS20	0	PRM203	PRM202	PRM201	PRM200		
TMC21	7	6	5	4	3	2	1	0	Address FFFFF2C0H	After reset 01H
	CE21	IMS21	CS21	0	PRM213	PRM212	PRM211	PRM210		
TMC22	7	6	5	4	3	2	1	0	Address FFFFF2E0H	After reset 01H
	CE22	IMS22	CS22	0	PRM223	PRM222	PRM221	PRM220		
TMC23	7	6	5	4	3	2	1	0	Address FFFFF300H	After reset 01H
	CE23	IMS23	CS23	0	PRM233	PRM232	PRM231	PRM230		
TMC24	7	6	5	4	3	2	1	0	Address FFFFF320H	After reset 01H
	CE24	IMS24	CS24	0	PRM243	PRM242	PRM241	PRM240		

Bit Position	Bit Name	Function																																																							
7	CE2n	Count Enable Specifies enable/disable of timer count. 0 : Timer count disabled (stops at TM2n = 0000H) 1 : Timer count enabled																																																							
6	IMS2n	Interrupt Mode Select Selects interrupt source. 0 : Interrupt is generated by coincidence signal of the compare register (CM2n) 1 : Interrupt is generated by INTP2n signal																																																							
5	CS2n	Clear & Start Controls clear/start of TM2n by software. This bit is set to 0 when reading. 0 : Continues counting 1 : Clears TM2n and resumes counting																																																							
3 to 0	PRM2n3 to PRM2n0	Prescaler Clock Mode Selects the count clock frequency. <table><tr><th>PRM2n3</th><th>PRM2n2</th><th>PRM2n1</th><th>PRM2n0</th><th>Count Clock</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>$\phi/2$</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>$\phi/4$</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>$\phi/8$</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>$\phi/16$</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>$\phi/32$</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>$\phi/64$</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>$\phi/128$</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>$\phi/256$</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>TI2n input</td></tr><tr><td colspan="4">Others</td><td>Setting prohibited</td></tr></table> <p>Caution Do not change the count clock frequency while the timer operates. Remark ϕ: Internal system clock</p>	PRM2n3	PRM2n2	PRM2n1	PRM2n0	Count Clock	0	0	0	1	$\phi/2$	0	0	1	0	$\phi/4$	0	0	1	1	$\phi/8$	0	1	0	0	$\phi/16$	0	1	0	1	$\phi/32$	0	1	1	0	$\phi/64$	0	1	1	1	$\phi/128$	1	0	0	0	$\phi/256$	1	1	1	1	TI2n input	Others				Setting prohibited
PRM2n3	PRM2n2	PRM2n1	PRM2n0	Count Clock																																																					
0	0	0	1	$\phi/2$																																																					
0	0	1	0	$\phi/4$																																																					
0	0	1	1	$\phi/8$																																																					
0	1	0	0	$\phi/16$																																																					
0	1	0	1	$\phi/32$																																																					
0	1	1	0	$\phi/64$																																																					
0	1	1	1	$\phi/128$																																																					
1	0	0	0	$\phi/256$																																																					
1	1	1	1	TI2n input																																																					
Others				Setting prohibited																																																					

Remark n = 0 to 4

(6) Timer control register 3 (TMC3)

TMC3 specifies count enable/disable and controls the count clock of TM3.

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
TMC3	CE3	0	CS3	CMS3	PRM33	PRM32	PRM31	PRM30	Address FFFFFF340H	After reset 01H

Bit Position	Bit Name	Function																																																		
7	CE3	Count Enable Specifies enable/disable of timer count. 0 : Timer count disabled (stops at TM3 = 0000H) 1 : Timer count enabled																																																		
5	CS3	Clear & Start Controls clear/start of TM3 by software. This bit is always 0 when reading. 0 : Continues counting 1 : Clears TM3 and resumes counting																																																		
4	CMS3	Capture/Compare Mode Select Selects capture/compare mode. 0 : Operates as a capture register 1 : Operates as a compare register																																																		
3 to 0	PRM33 to PRM30	Prescaler Clock Mode Selects the count clock frequency. <table><tr><th>PRM33</th><th>PRM32</th><th>PRM31</th><th>PRM30</th><th>Count Clock</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>$\phi/2$</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>$\phi/4$</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>$\phi/8$</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>$\phi/16$</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>$\phi/32$</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>$\phi/64$</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>$\phi/128$</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>$\phi/256$</td></tr><tr><td colspan="4">Others</td><td>Setting prohibited</td></tr></table> <div><div>Caution</div><div>Do not change the count clock frequency while the timer operates.</div></div> <div><div>Remark</div><div>ϕ: Internal system clock</div></div>	PRM33	PRM32	PRM31	PRM30	Count Clock	0	0	0	1	$\phi/2$	0	0	1	0	$\phi/4$	0	0	1	1	$\phi/8$	0	1	0	0	$\phi/16$	0	1	0	1	$\phi/32$	0	1	1	0	$\phi/64$	0	1	1	1	$\phi/128$	1	0	0	0	$\phi/256$	Others				Setting prohibited
PRM33	PRM32	PRM31	PRM30	Count Clock																																																
0	0	0	1	$\phi/2$																																																
0	0	1	0	$\phi/4$																																																
0	0	1	1	$\phi/8$																																																
0	1	0	0	$\phi/16$																																																
0	1	0	1	$\phi/32$																																																
0	1	1	0	$\phi/64$																																																
0	1	1	1	$\phi/128$																																																
1	0	0	0	$\phi/256$																																																
Others				Setting prohibited																																																

(7) Timer output control registers 0 and 1 (TOC0, TOC1)

TOC0, TOC1 control the timer outputs from the TO00, TO01, and TO20 to TO24 pins.

These registers can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
TOC0	0	0	ENTO20	ALV20	ENTO01	ALV01	ENTO00	ALV00	Address FFFFF232H	After reset 00H
TOC1	ENTO24	ALV24	ENTO23	ALV23	ENTO22	ALV22	ENTO21	ALV21	Address FFFFF234H	After reset 00H

Bit Position	Bit Name	Function
7, 5, 3, 1	ENTOn	<p>Enable TO pin Enables corresponding timer output (TO_n).</p> <p>0: Timer output is disabled. The anti-phase levels of ALV_n bit (inactive levels) are output from TO_n pins. Even if coincidence signal is generated from corresponding compare register, levels of TO_n pins do not change.</p> <p>1: Timer output function is enabled. Timer output changes when coincidence signal is generated from corresponding compare register. After the timer output has been enabled before the first coincidence signal is generated, the anti-phase levels of ALV_n bit (inactive levels) are output.</p>
6, 4, 2, 0	ALVn	<p>Active Level TO pin Specifies the active level of timer output.</p> <p>0: Active-low 1: Active-high</p>

- Remarks**
1. The flip-flops of the TO00 and TO01 outputs is a reset priority.
 2. n = 00, 01, 20 to 24

Caution The TO00, TO01 outputs are not changed by the external interrupt signals (INTP00 to INTP03). When using the TO00 and TO01 signals, specify the capture/compare registers as compare registers CMS00 to CMS03 (set CMS00 to CMS03 to “1”).

(8) Timer overflow status register (TOVS)

The overflow flags TM0 to TM3 are assigned.

This register can be read/written in 8- or 1-bit units.

By testing and resetting the TOVS register via software, occurrence of an overflow can be polled.

TOVS	7	6	5	4	3	2	1	0	Address FFFFF230H	After reset 00H
	OVF3	OVF24	OVF23	OVF22	OVF21	OVF20	OVF1	OVF0		

Bit Position	Bit Name	Function
7 to 0	OVFn	<p>Overflow Flag TMn overflow flag. 0: No overflow 1: Overflow</p> <p>From TM0 and TM1, the interrupt requests (INTOV0 and INTOV1) are generated for the interrupt controller in synchronization with the overflow. However, the interrupt operation and TOVS are independent from each other, and the overflow flags (OVF0 and OVF1) from TM0 and TM1 can be rewritten in the same manner as in other overflow flags. At this time, the interrupt request flags (OVF0 and OVF1) corresponding to INTOV0 and INTOV1 are not affected.</p> <p>No transmission is executed to the TOVS register during access from the CPU. Therefore, even if an overflow occurs when the TOVS register is being read, the overflow flag value will not be updated and this overflow condition will be reflected the next time the TOVS register is read.</p>

Remark n = 0, 1, 20 to 24, and 3

(9) External interrupt mode registers 1 to 4, 7 (INTM1 to INTM4, INTM7)

These registers set the following 3 types of valid edges:

- Sets valid edge of external interrupt request signal (INTP) when using CP10 to CP13 (timer 1), CC3, CP3 (timer 3) as capture registers.
- Sets valid edges at external count clock input (TI) of timer 0, timer 1, and timer 2.
- Sets valid edges at timer clear (TCLR0) of timer 0.

For the details, refer to **CHAPTER 5 INTERRUPT/EXCEPTION PROCESSING FUNCTION**.

(10) Event divide counter 0 to 2 (EDV0 to EDV2)

Counts valid edges detected by the INTM1 to INTM3 registers. For the details, refer to **5.3 Maskable Interrupt**.

(11) Event divide control register 0 to 2 (EDVC0 to EDVC2)

Sets the frequency division ratio of event divide counter (EDV0 to EDV2). For the details, refer to **5.3. Maskable Interrupt**.

(12) Event selection register (EVS)

Selects INTP signal to input to the EDV2 register. For the details, refer to **5.3 Maskable Interrupt**.

7.4 Timer 0 Operation

7.4.1 Count operation

Timer 0 functions as a 24-bit interval timer or event counter, as specified by timer control registers 00 to 02 (TMC00 to TMC02).

Timer 0 performs counting up by count clock. Start/stop of counting is controlled by the CE0 bit of timer control register 00 (TMC00).

(1) Start counting

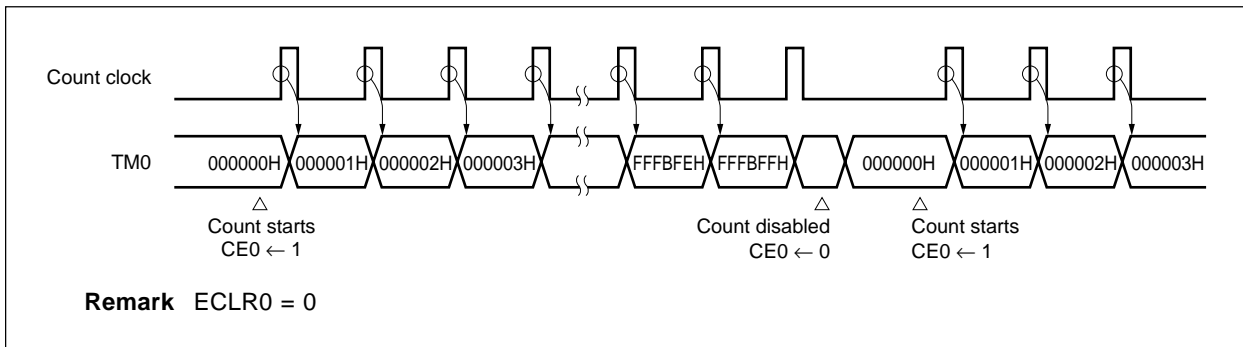
Timer 0 starts counting by setting the CE0 bit to 1 while the ECLR0 bit of the TMC02 register is 0. However, when the ECLR0 bit is 1, timer 0 does not start counting until the TCLR0 signal is input. Therefore, it does not start counting by setting ECLR = 0 after setting CE0 = 1 while ECLR0 = 1.

Writing 1 to TM0 during counting operations (CE0 = 1) does not clear the TM0 register, and timer 0 continues counting.

(2) Stop counting

Timer 0 stops counting by setting the CE0 bit to 0. If the OST bit of the TMC00 register is set to 1, timer 0 stops operation after occurrence of overflow. However, the value of the timer register can immediately be cleared by setting CE0 = 0.

Figure 7-1. Basic Operation of Timer 0



7.4.2 Count clock selection

An internal or external count clock frequency can be input to timer 0. Which count clock frequency is used is selected by the PRM00 to PRM03 bits of the TMC00 register.

Caution Do not change the count clock frequency while the timer operates.

(1) Internal count clock

An internal count clock frequency is selected by the PRM bit of the TMC00 register, from $\phi/2$, $\phi/4$, $\phi/8$, $\phi/16$, $\phi/32$, $\phi/64$, $\phi/128$, and $\phi/256$.

PRM03	PRM02	PRM01	PRM00	Internal Count Clock
0	0	0	1	$\phi/2$
0	0	1	0	$\phi/4$
0	0	1	1	$\phi/8$
0	1	0	0	$\phi/16$
0	1	0	1	$\phi/32$
0	1	1	0	$\phi/64$
0	1	1	1	$\phi/128$
1	0	0	0	$\phi/256$

(2) External count clock

The signal input to the TI0 pin is counted. At this time, timer 0 operates as an event counter. To set an external count clock see the table as follows.

PRM03	PRM02	PRM01	PRM00	External Count Clock
1	1	1	1	TI0 input

The valid edge of TI0 is specified by the ES bit of the INTM2 register.

ES051	ES050	Valid Edge
0	0	Falling edge
0	1	Rising edge
1	0	RFU (reserved)
1	1	Both rising and falling edges

7.4.3 Overflow

If the TM0 register overflows as a result of counting the count clock frequency to FFFFFFFH, a flag is set to the OVF0 flag of the TOVS registers, and an overflow interrupt (INTOV0) is generated. The value of the OVF0 flag is retained until it is changed by user application.

The operation of the TM0 register after occurrence of overflow is determined by the OST0 bit.

(1) Operation after occurrence of overflow when OST0 = 0

The TM0 register continues counting.

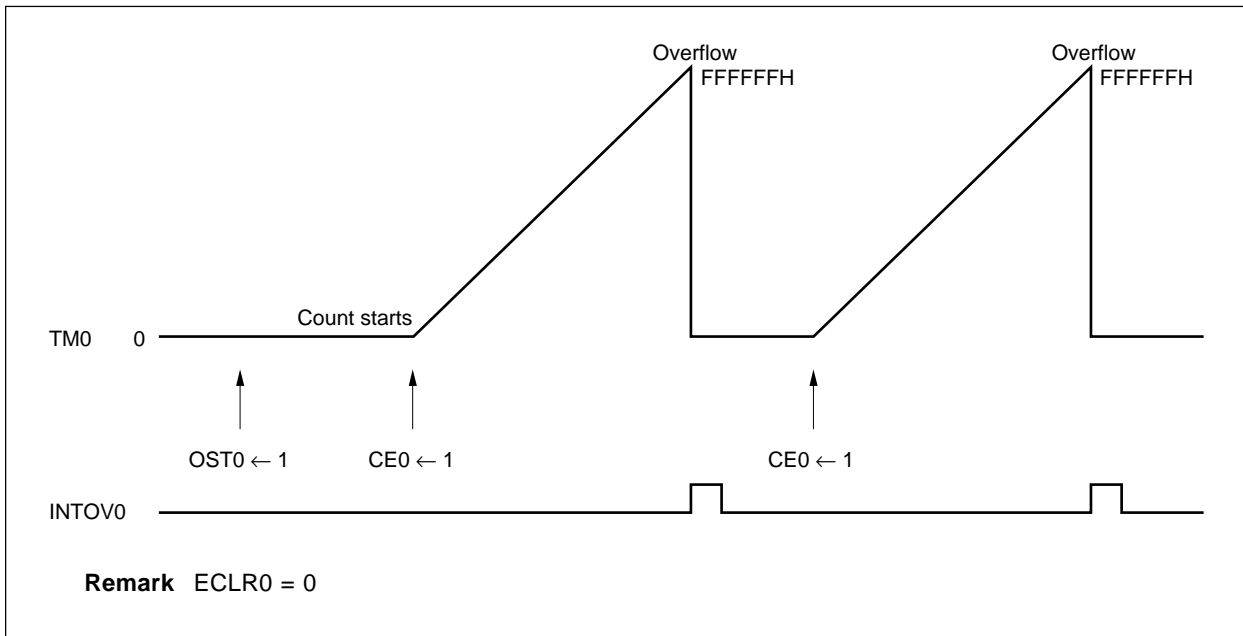
(2) Operation after occurrence of overflow when OST0 = 1

TM0 = 000000H is retained, and the TM0 register stops counting. At this time TM0 stops with CE0 = 1. Perform the following to resume counting.

- When ECLR0 = 0 : write 1 to CE0 bit
- When ECLR0 = 1 : trigger input to timer clear pin (TCLR0)

The operation is not affected even if the CE0 bit is set to 1 during count operation.

Figure 7-2. Operation after Occurrence of Overflow (when ECLR0 = 0, OST0 = 1)



7.4.4 Clearing/starting timer

There are three methods of clearing/starting timer 0: by overflow, by TCLR0 signal input, and by CC03 coincidence.

(1) Clearing/starting by overflow

For the details of the operation, refer to **7.4.3 Overflow**.

(2) Clearing/starting by TCLR0 signal input

Timer 0 usually starts the count operation when the CE0 bit of the TMC00 register is set to 1. It is also possible to clear TM0 and start the count operation by using external input TCLR0.

When the valid edge is input to TCLR0 after ECLR0 = 1, OST0 = 0, and the CE0 bit is set to 1, the count operation is started. If the valid edge is input to TCLR0 during operation, TM0 clears its value and then resume the count operation (refer to **Figure 7-3**).

When the valid edge is input to the TCLR0 signal after ECLR0 = 0, OST0 = 1, and the CE0 bit is set to 1, the count operation is started. When TM0 overflows, the count operation is stopped once and is not resumed until the valid edge is input to TCLR0. If the valid edge of TCLR0 is detected during count operation, TM0 is cleared and continues counting (refer to **Figure 7-4**). Timer 0 does not resume counting even if the CE0 bit is set to 1 after occurrence of overflow. When CE0 = 0, TCLR0 input is invalid.

Figure 7-3. Clearing/Starting Timer by TCLR0 Signal Input (when ECLR0 = 1, CCLR0 = 0, OST0 = 0)

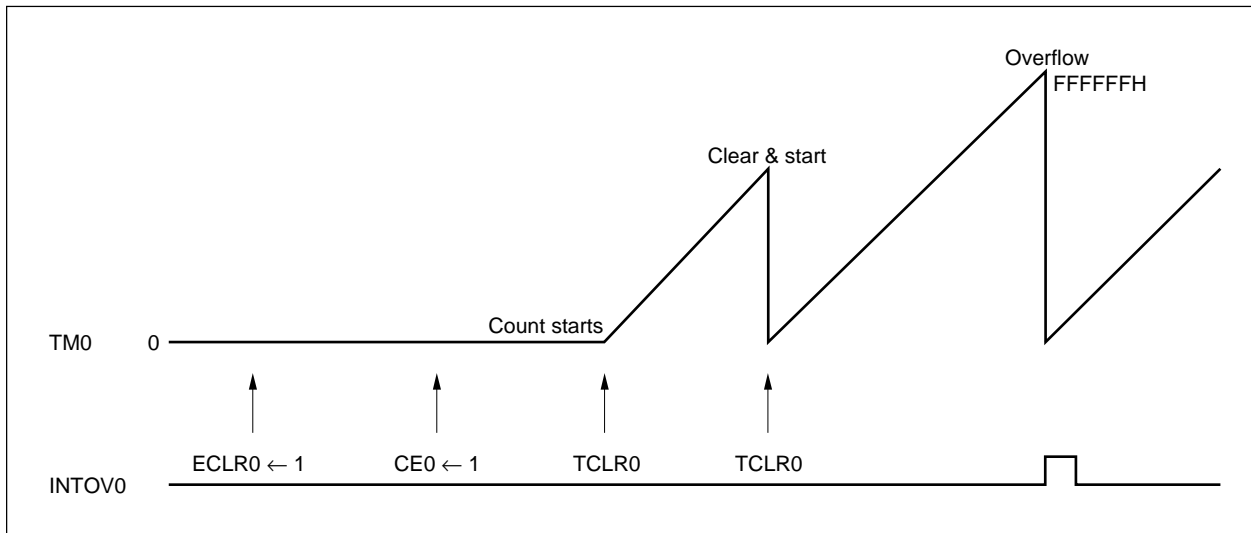
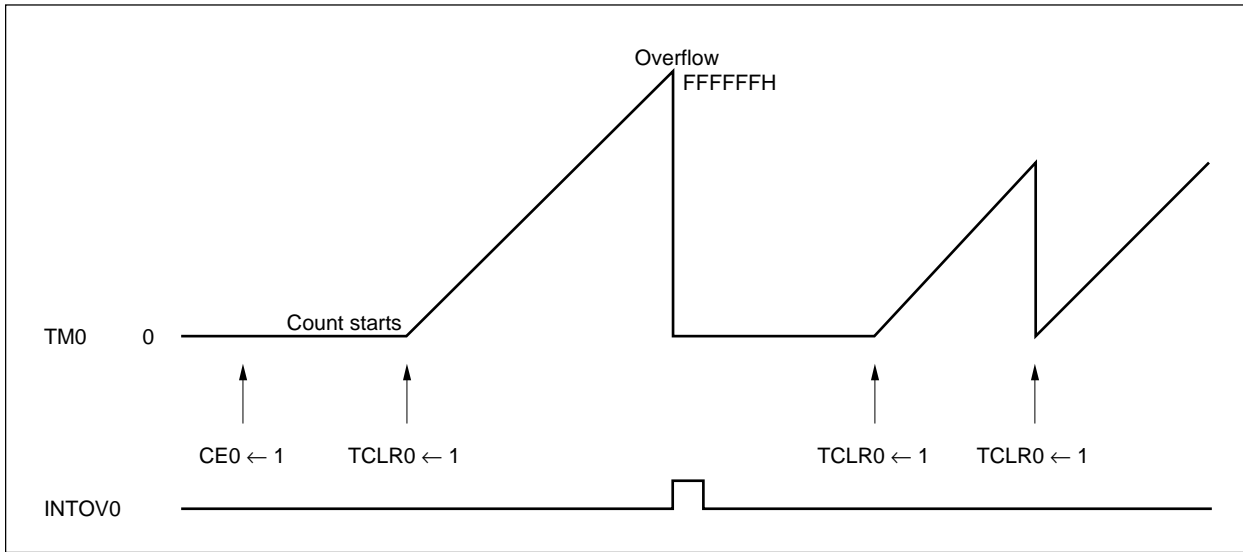


Figure 7-4. Relations between Clear/Start by TCLR0 Signal Input and Overflow (when ECLR0 = 1, OST0 = 1)



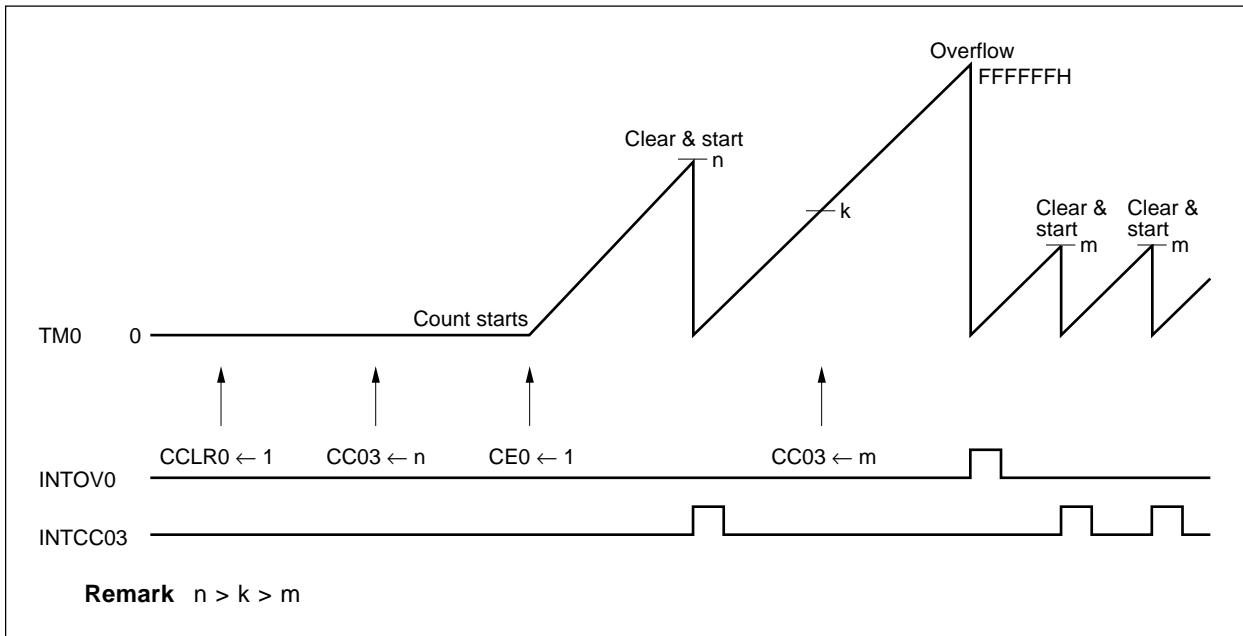
(3) Clearing/starting by CC03 match

Timer 0 usually starts the count operation when CCLR = 1, CMS03 = 1, and the CE0 bits of the TMC00 registers are set to 1. It is also possible to clear TM0 and start the count operation by generation of CC03 match (INTCC03).

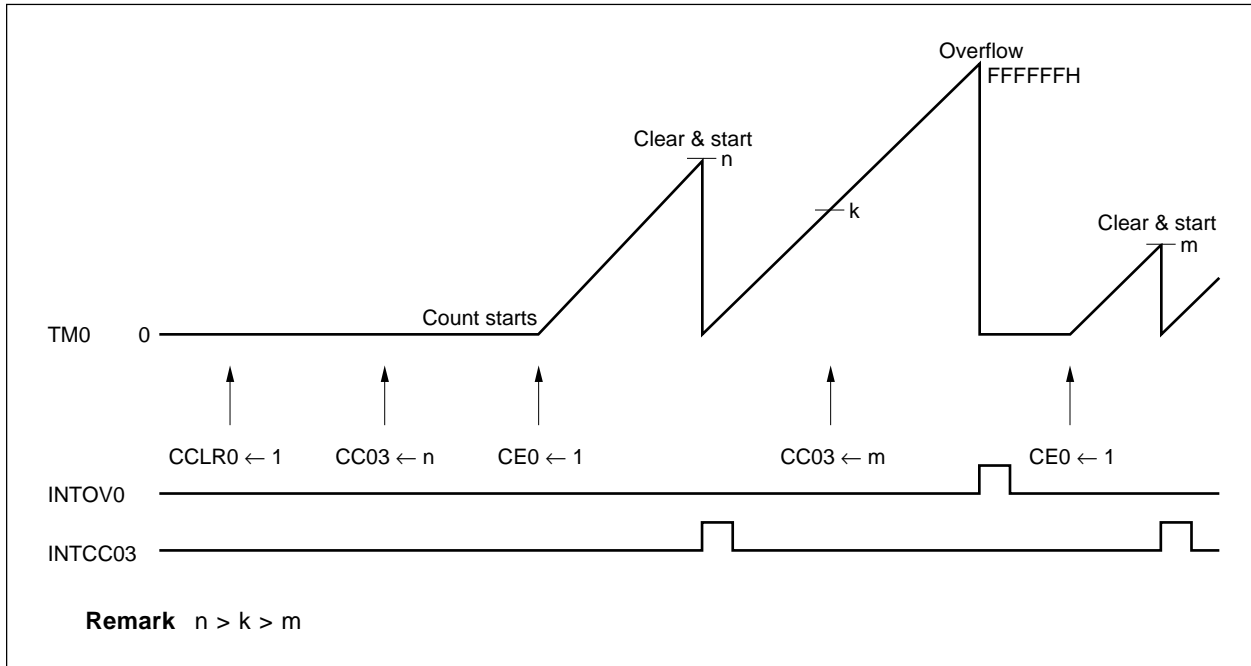
When CCLR0 = 1, CMS03 = 1, and the CE0 bit is set to 1, the count operation is started. If CC03 match is generated during operation, TM0 clears its value and then resumes the count operation (refer to **Figure 7-5**).

If a value smaller than the current count value of TM0 is set to CC03 during count operation, overflow of TM0 occurs (refer to **Figure 7-6**). For the operation after occurrence of overflow, refer to **7.4.3 Overflow**.

Figure 7-5. Clearing/Starting Timer by CC03 Match (when CCLR0 = 1, OST0 = 0)



**Figure 7-6. Relations between Clear/Start by CC03 Coincidence and Overflow Operation
(when CCLR0 = 1, OST0 = 1)**



7.4.5 Capture operation

When the TMC01 register is set to a capture register, the capture/compare registers (CC00 to CC03) perform capture operations that capture and hold the count values of TM0 and load them to a capture register in asynchronization with an external trigger. The valid edge from the external interrupt request input pin INTP0n is used as the capture trigger. In synchronization with this capture trigger signal, the count values of TM0 during counting are captured and loaded to the capture register and the interrupt request INTCC0n is simultaneously issued. The value of the capture register is retained until the next capture trigger is generated.

When the capture timing to a capture register and write operation to a register by instruction are in contention, the latter is given priority and the capture operation is ignored.

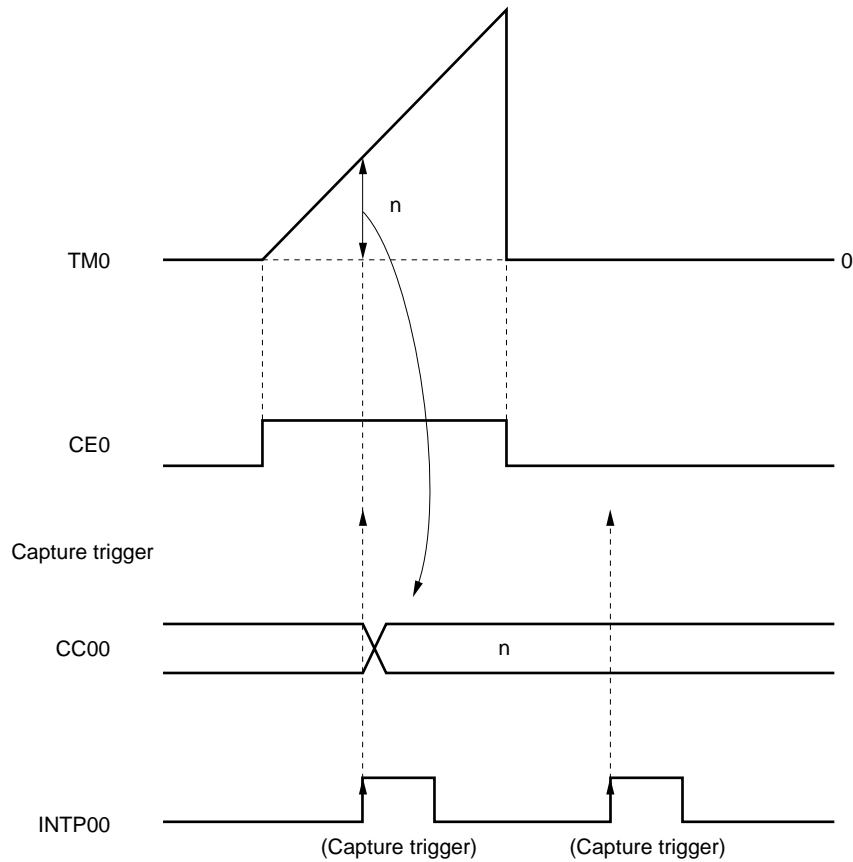
Table 7-2. Capture Trigger Signal to 24-Bit Capture Register

Capture Trigger Signal	Capture Register	Interrupt Request
INTP00	CC00/CC00L	INTCC00
INTP01	CC01/CC01L	INTCC01
INTP02	CC02/CC02L	INTCC02
INTP03	CC03/CC03L	INTCC03

The valid edge of the capture trigger is set by the external interrupt mode register (INTM1).

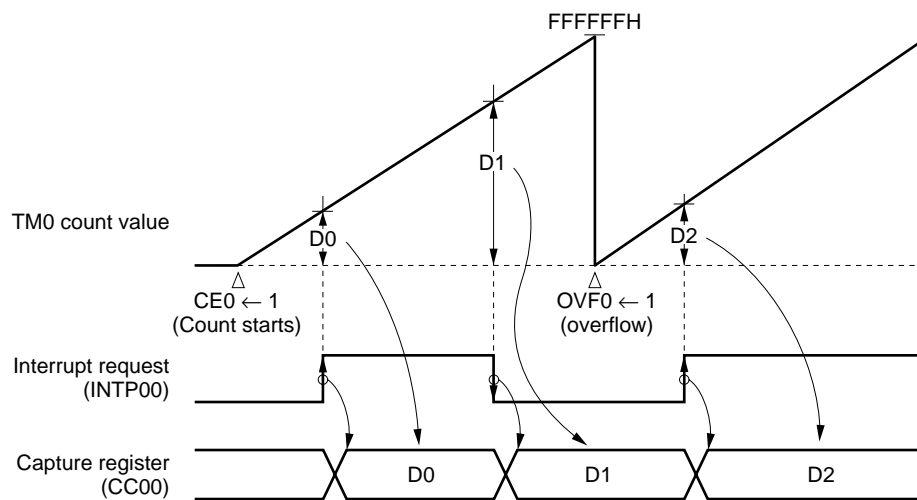
When both the rising and falling edges are specified as the capture trigger, the width of an externally input pulse can be measured. If either the rising or falling edge is specified as the capture trigger, the frequency of the input pulse can be measured.

Figure 7-7. Example of TM0 Capture Operation



Remark The capture operation is not performed even if the interrupt request (INTP00) is input when CE0 is cleared to 0.

Figure 7-8. Example of TM0 Capture Operation (when both edges are specified)



Remark D0 to D2 : count value of TM0

7.4.6 Compare operation

When the TMC01 register is set as a compare register, the capture/compare registers (CC00 to CC03) perform a comparison between the value of the compare register with the count values of TM0.

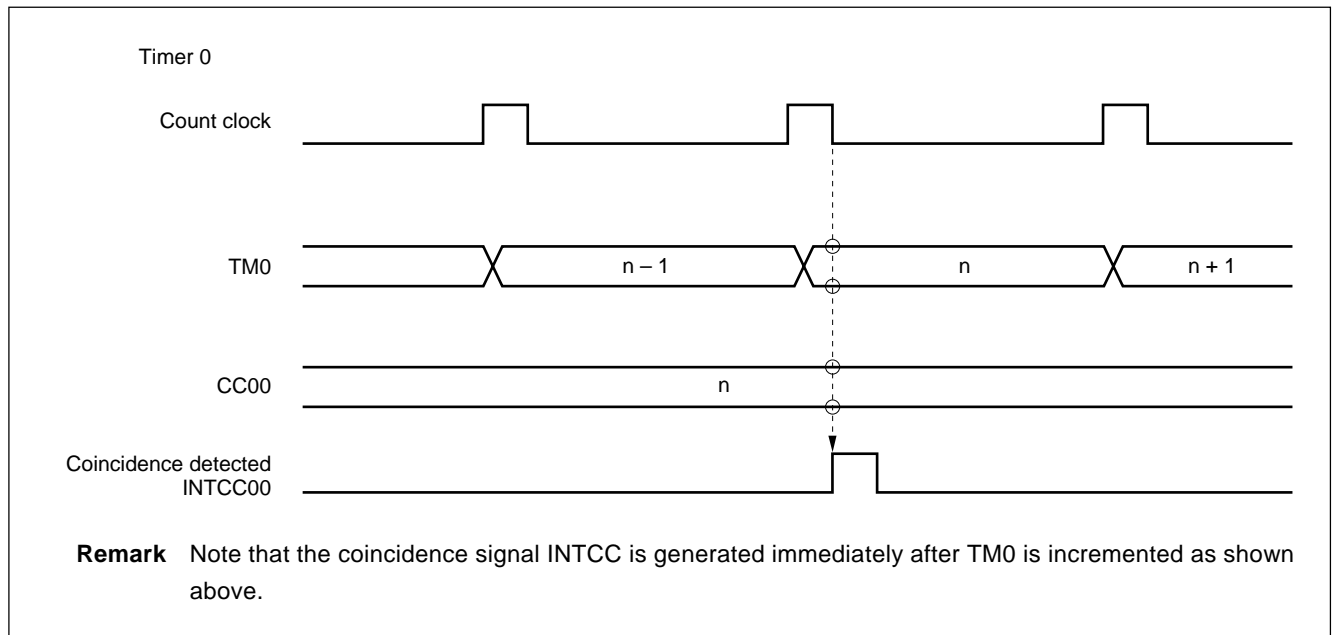
When the count values of TM0 coincide with the value of the compare register programmed in advance, a coincidence signal is sent to the output control circuit (refer to **Figure 7-9**). The levels of the timer output pins (TO) can be changed by the coincidence signal, and an interrupt request signal INTCC can be generated at the same time ($n = 00, 01$).

Table 7-3. Interrupt Request Signal from 24-Bit Compare Register

Compare Register	Interrupt Request	Compare Match Trigger
CC00/CC00L	INTCC00	TO00 (S)
CC01/CC01L	INTCC01	TO00 (R)
CC02/CC02L	INTCC02	TO01 (S)
CC03/CC03L	INTCC03	TO01 (R), A/D converter

Remark S/R: set/reset

Figure 7-9. Example of Compare Operation



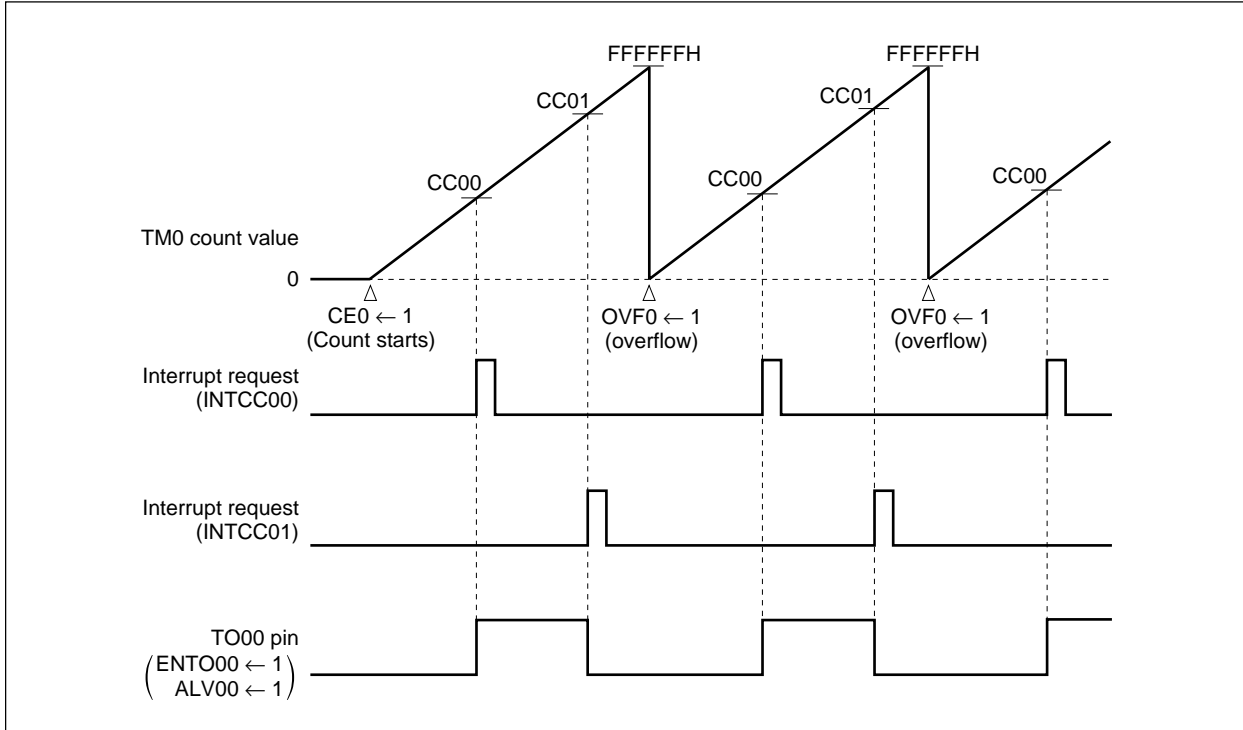
Timer 0 has two timer output pins: TO00 and TO01.

The count values of TM0 are compared with the values of CC02. When the two values coincide, the output level of the TO01 pin is set. The count values of TM0 are also compared with the values of CC03. When the two values coincide, the output levels of the TO01 pin are reset.

Similarly, the count values of TM0 are compared with the values of CC00. When the two values coincide, the output levels of the TO00 pin are set. The count values of TM0 are also compared with the values of CC01. When the two values coincide, the output levels of the TO00 pin are reset.

The output levels of the TOn pins can be specified by the TOC0 register (n = 00, 01).

Figure 7-10. Example of TM0 Compare Operation (set/reset output mode)



7.5 Timer 1 Operation

7.5.1 Count operation

Timer 1 functions as a 24-bit free-running timer or event counter, as specified by timer control register 1 (TMC1).

Timer 1 performs counting up by count clock. Start/stop of counting is controlled by the CE1 bit of timer control register 1 (TMC1).

(1) Start counting

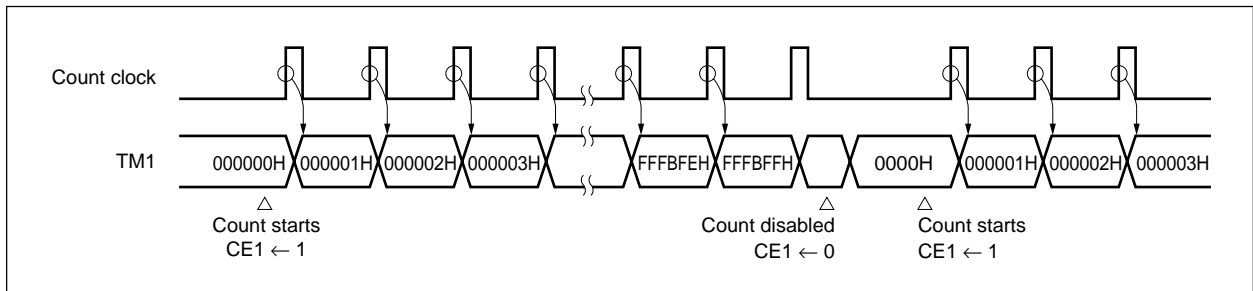
Timer 1 starts counting by setting the CE1 bit to 1.

Writing 1 to TM1 during counting operations (CE1 = 1) does not clear the TM1 register, and timer 1 continues counting.

(2) Stop counting

Timer 1 stops counting by setting the CE1 bit to 0. If the OST bit of the TMC1 register is set to 1, timer 1 stops operation after occurrence of overflow. However, the value of the timer register can immediately be cleared by setting CE1 = 0.

Figure 7-11. Basic Operation of Timer 1



7.5.2 Count clock selection

An internal or external count clock frequency can be input to timer 1. Which count clock frequency is used is selected by the PRM10 to PRM13 bits of the TMC1 register.

Caution Do not change the count clock frequency while the timer operates.

(1) Internal count clock

An internal count clock frequency is selected by the PRM bits of the TMC1 register, from ϕ , $\phi/2$, $\phi/4$, $\phi/8$, $\phi/16$, $\phi/32$, $\phi/64$, $\phi/128$, and $\phi/256$.

PRM13	PRM12	PRM11	PRM10	Internal Count Clock Frequency
0	0	0	0	ϕ
0	0	0	1	$\phi/2$
0	0	1	0	$\phi/4$
0	0	1	1	$\phi/8$
0	1	0	0	$\phi/16$
0	1	0	1	$\phi/32$
0	1	1	0	$\phi/64$
0	1	1	1	$\phi/128$
1	0	0	0	$\phi/256$

(2) External count clock

The signal input to the TI1 pins is counted. At this time, timer 1 operates as an event counter.

To set an external count clock, see the table below.

PRM13	PRM12	PRM11	PRM10	External Count Clock
1	1	1	1	TI1 input

The valid edge of TI1 is specified by the ES bits of the INTM3 register.

ES141	ES140	Valid Edge
0	0	Falling edge
0	1	Rising edge
1	0	RFU (reserved)
1	1	Both rising and falling edges

7.5.3 Overflow

If overflow occurs as a result of counting the TM1 register count clock frequency to FFFFFFFH, a flag is set to the OVF1 bits of the TOVS register, and an overflow interrupt (INTOV1) is generated.

The value of the OVF1 flag is retained until it is changed by user application.

The operation of the TM1 register after occurrence of overflow is determined by the OST1 bit.

(1) Operation after occurrence of overflow when OST1 = 0

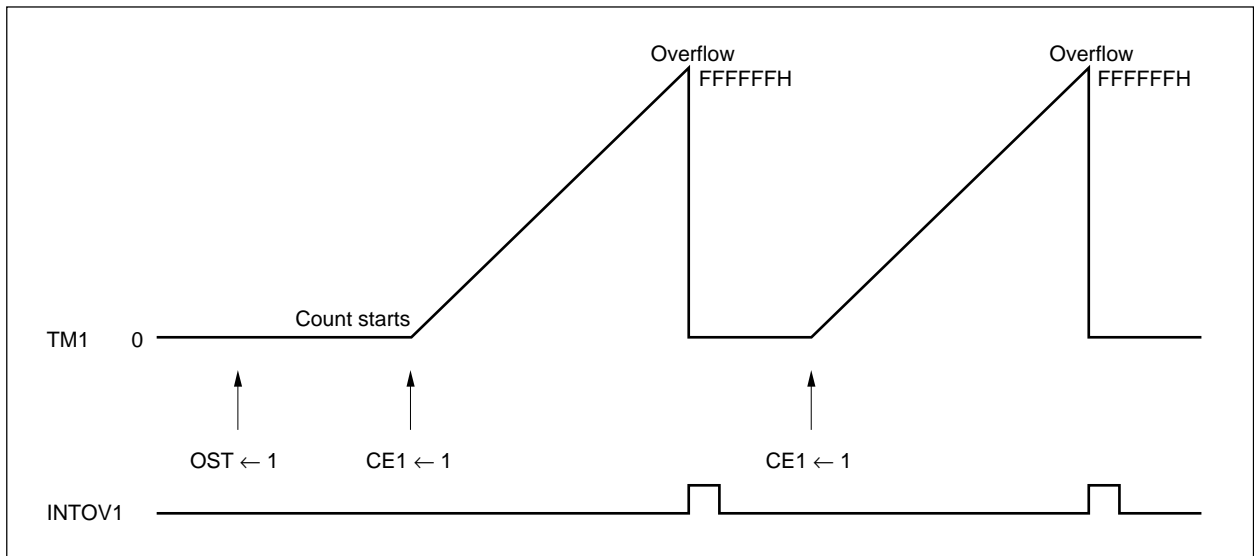
The TM1 register continues counting.

(2) Operation after occurrence of overflow when OST1 = 1

TM1 = 000000H is retained, and the TM1 register stops counting. At this time TM1 stops with CE1 = 1. Perform the following to resume counting.

- Write 1 to CE1 bit
- Write 1 to CS1 bit

The operation is not affected even if the CE1 bit is set to 1 during count operation.

Figure 7-12. Operation after Occurrence of Overflow (OST1 = 1)**7.5.4 Clearing/starting timer**

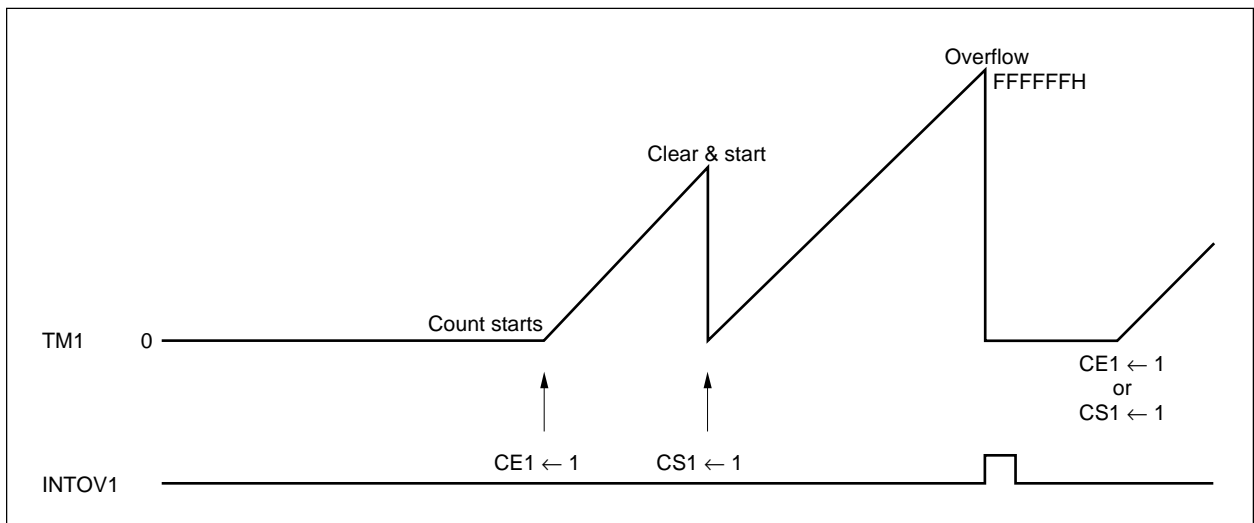
There are two methods of clearing/starting timer 1: by overflow and by software.

(1) Clearing/starting by overflow

For the details of the operation, refer to **7.5.3 Overflow**.

(2) Clearing/starting by software

When the CS1 bit is set to 1 by software, the TM1 register clears its value and starts counting from 0. However, this setting of the bit is valid only when the value of the CE1 bit is 1.

Figure 7-13. Clearing/Starting Timer by Software (when OST1 = 1)

7.5.5 Capture operation

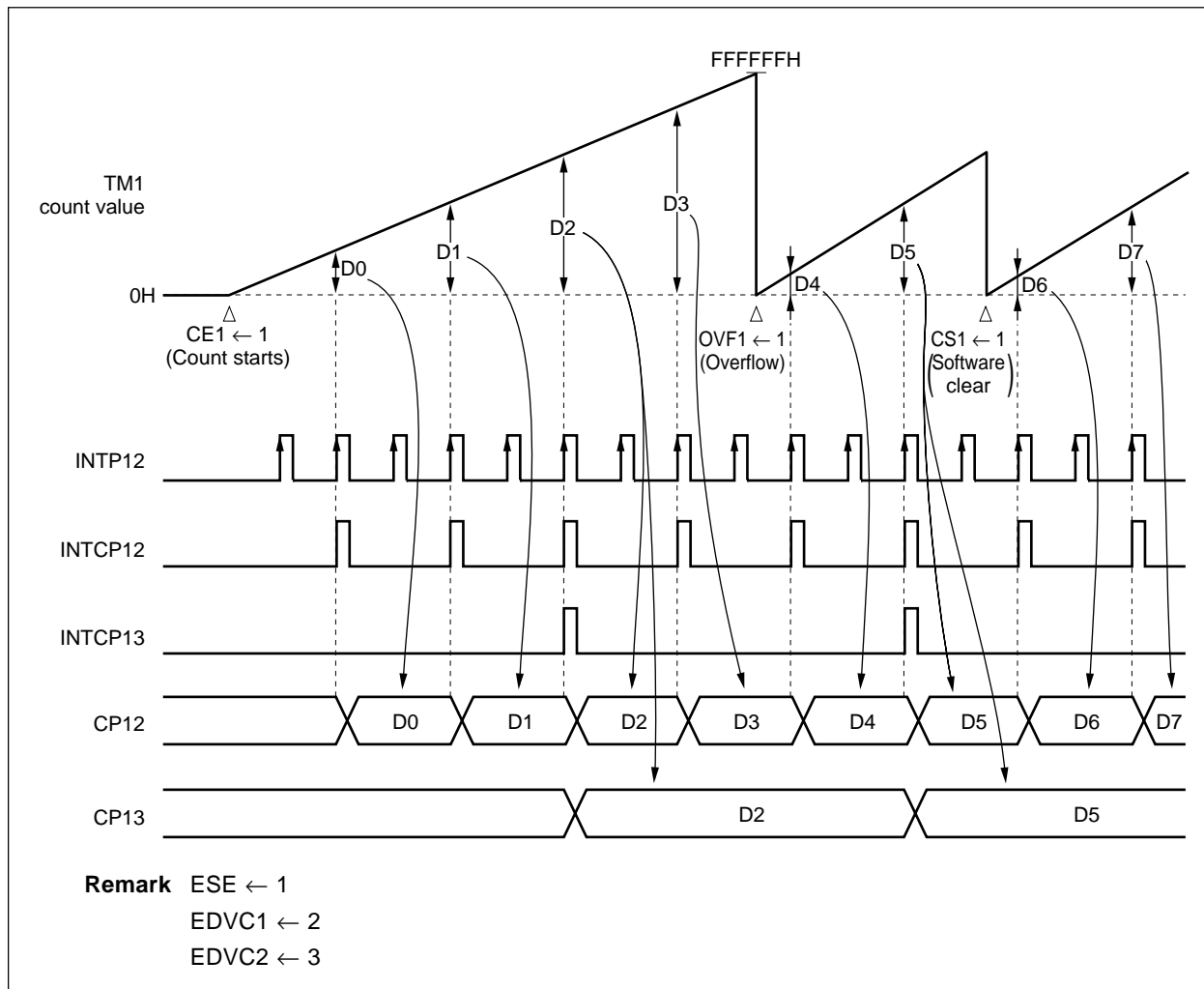
A capture operation that captures and holds the count values of TM1 and loads them to a capture register in asynchronization with an external trigger can be performed. The trigger divided by the valid edge from the external interrupt request input pin INTP1n is used as the capture trigger. In synchronization with this capture trigger signal, the count values of TM1n during counting, are captured and loaded to the capture register and the interrupt request INTCP1n is simultaneously issued. The value of the capture register is retained until the next capture trigger is generated.

Table 7-4. Capture Trigger Signal to 24-Bit Capture Register

Capture Trigger Signal	Capture Register	Interrupt Request
INTP10	CP10/CP10L	INTCP10
Divide of INTP11	CP11/CP11L	INTCP11
Divide of INTP12	CP12/CP12L	INTCP12
Divide of INTP12/INTP13	CP13/CP13L	INTCP13

The valid edge of the INTP1n input is set by the external interrupt mode registers (INTM2, INTM3). The frequency dividing ratio of the INTCP11 to INTCP13 triggers is set by the EDVCn register and the EVS register. For the details, refer to **5.3.9 Frequency divider**.

Figure 7-14. Example of TM1 Capture Operation



7.5.6 Compare operation

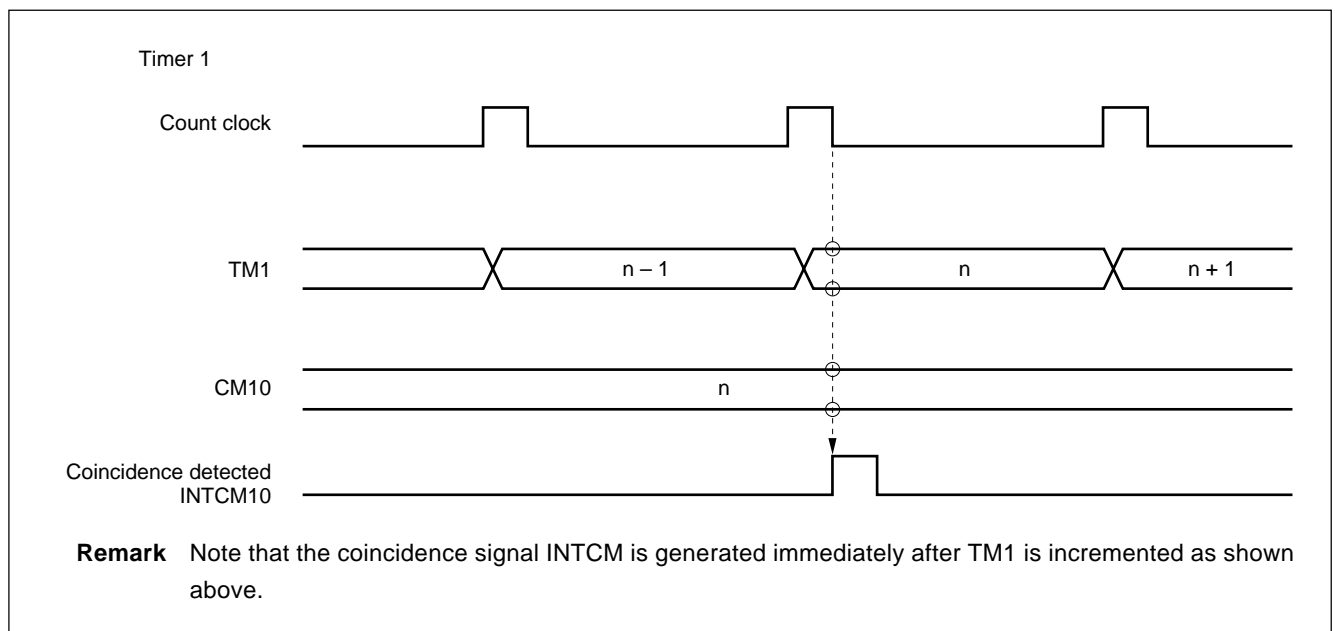
A comparison between the value in a compare register with the count values of TM1 can be performed.

When the count values of TM1 coincide with the value of the compare register programmed in advance, INTCM10 coinciding with CM10 is generated as a trigger of the real time output port. An interrupt request signal INTCM can be generated at the same time.

Table 7-5. Interrupt Request Signal from 24-Bit Compare Register

Compare Register	Interrupt Request	Compare Match Trigger
CM10/CM10L	INTCM10	Real time output port
CM11/CM11L	INTCM11	—

Figure 7-15. Example of Compare Operation



7.6 Timer 2 Operation

7.6.1 Count operation

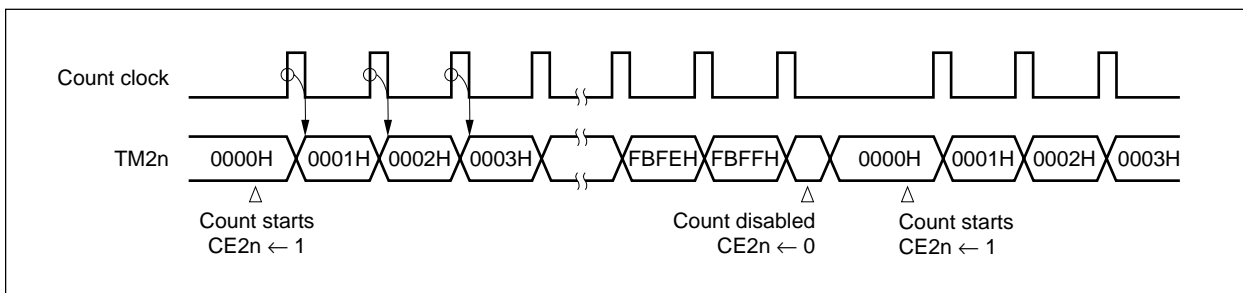
Timer 2 functions as a 16-bit interval timer. The operation is specified by the timer control registers 20 to 24 (TMC20 to TMC24).

The operation of timer 2 counts the internal count clocks ($\phi/2$ to $\phi/256$ or the external count clock (T12n)) specified by the PRM2n0 to PRM2n3 bits of the TMC2n register.

If the count value of TM2n coincides with the value of CM2n, the value TM2n is cleared while simultaneously a coincidence interrupt (INTCM2n) is generated and the TO2n signal is output in toggle.

Remark n = 0 to 4

Figure 7-16. Basic Operation of Timer 2



7.6.2 Count clock selection

An internal or external count clock frequency can be input to timer 2. Which count clock frequency is used is selected by the PRM2n0 to PRM2n3 bits of the TMC2n register (n = 0 to 4).

Caution Do not change the count clock frequency while the timer operates.

(1) Internal count clock

An internal count clock frequency is selected by the PRM bits of the TMC2n register, from $\phi/2$, $\phi/4$, $\phi/8$, $\phi/16$, $\phi/32$, $\phi/64$, $\phi/128$, and $\phi/256$.

PRM2n3	PRM2n2	PRM2n1	PRM2n0	Internal Count Clock Frequency
0	0	0	1	$\phi/2$
0	0	1	0	$\phi/4$
0	0	1	1	$\phi/8$
0	1	0	0	$\phi/16$
0	1	0	1	$\phi/32$
0	1	1	0	$\phi/64$
0	1	1	1	$\phi/128$
1	0	0	0	$\phi/256$

(2) External count clock

The signal input to the TI2n pins are counted. At this time, timer 2 operates as an event counter.

To set an external count clock see the table below.

PRM2n3	PRM2n2	PRM2n1	PRM2n0	External Count Clock
1	1	1	1	TI2n input

The valid edge of TI2n is specified by the ES bits of the INTM3 and the INTM4 registers.

ES2n1	ES2n0	Valid Edge
0	0	Falling edge
0	1	Rising edge
1	0	RFU (reserved)
1	1	Both rising and falling edges

Remark n = 0 to 4

7.6.3 Overflow

If TM2n overflows as a result of counting the internal count clock, a flag is set to the OVF2n bit of the TOVS register (n = 0 to 4).

7.6.4 Clearing/starting timer

There are two methods of clearing/starting timer 2: by coincidence with a compare register and by software.

(1) Clearing/starting by coincidence signal of a compare register

When the set value of the compare register (CM2n) and the value of TM2n coincide, TM2n clears its value at the next count clock and starts count operation (n = 0 to 4). At the same time, it generates an interrupt request signal (INTCM20 to INTCM24) and a timer output trigger.

The interval time set to a compare register can be calculated by the following expression:

$$(\text{Set value} + 1) \times \text{Count cycle}$$

For the details, refer to **7.6.5 Compare operation**.

(2) Clearing/starting by software

When the value of the CS2n bit of the TMC2n register is set to 1, TM2n clears its value at the next count clock and starts count operation (n = 0 to 4). However, the setting of this bit is valid only when the value of the CE2n bit is 1 (n = 0 to 4).

7.6.5 Compare operation

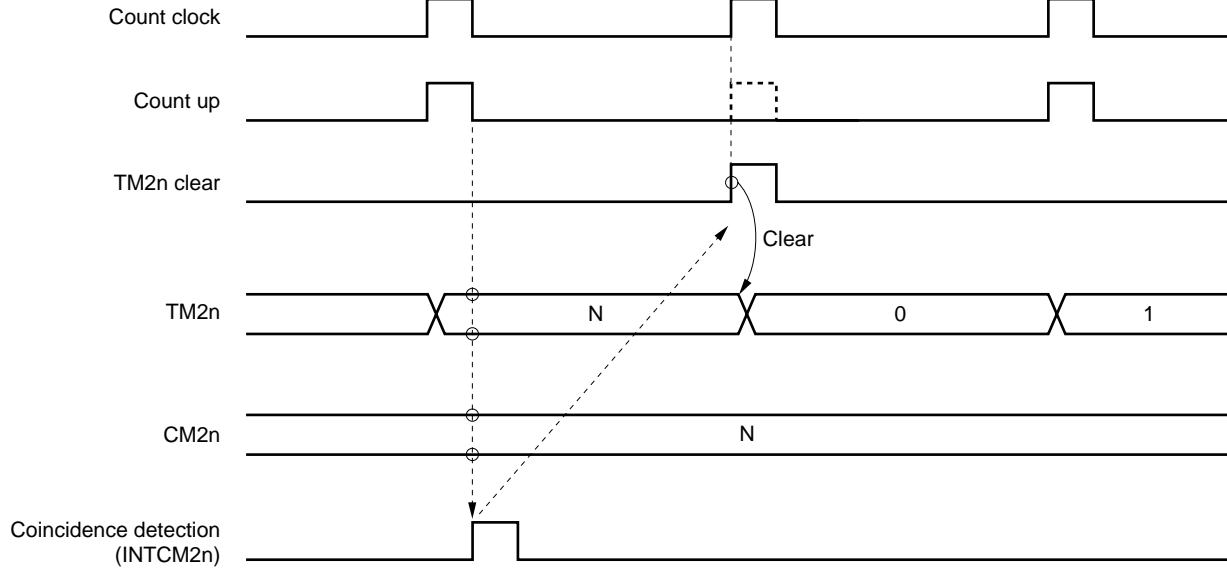
A comparison can be performed with the counter values of TM20 to TM24 and the compare registers (CM20 to CM24).

When the count value of TM2n coincides with the value of the compare register, a coincidence interrupt (INTCM2n) is generated. As a result, TM2n is cleared to 0 at the next count timing (refer to **Figure 7-17**). This function allows timer 2 to be used as an interval timer.

CM2n can be also set to 0. In this case, a coincidence is detected when TM2n overflows and is cleared to 0, and INTCM2n is generated. The value of TM2n is cleared to 0 at the next count timing, but INTCM2n is not generated when a coincidence occurs at this time (refer to **Figure 7-18**).

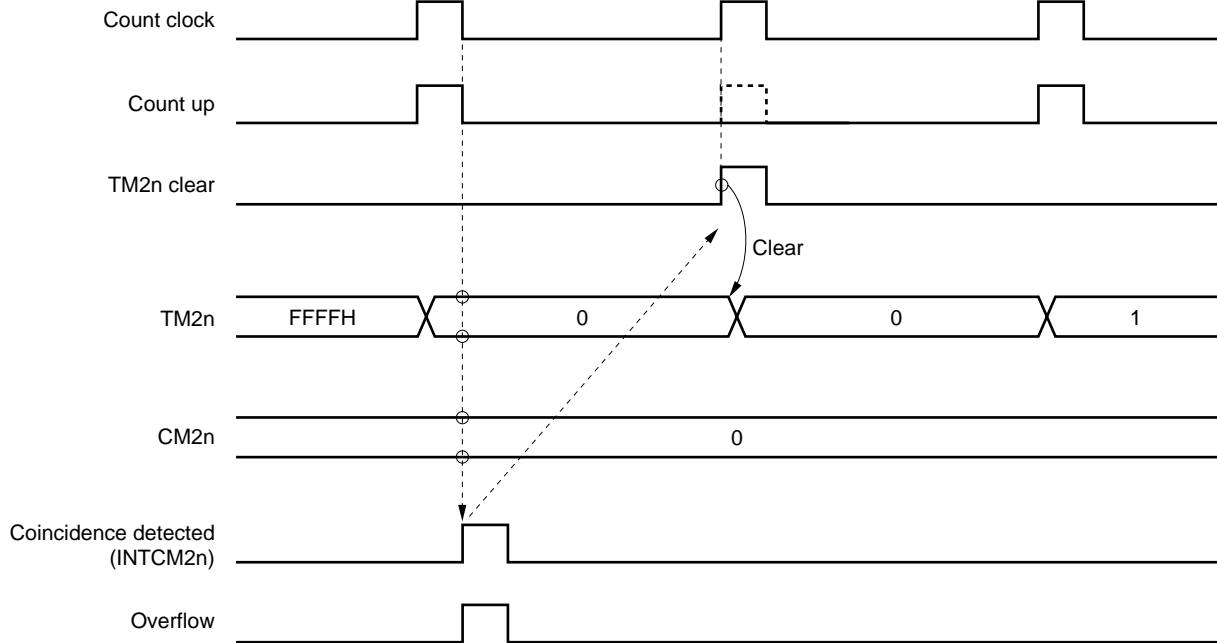
Remark n = 0 to 4

Figure 7-17. Operation with CM2n at 1 to FFFFH



Remark Interval time = $(N + 1) \times \text{count clock cycle}$
 $N = 1 \text{ to } 65535 \text{ (FFFFH)}$

Figure 7-18. When CM2n is Set to 0



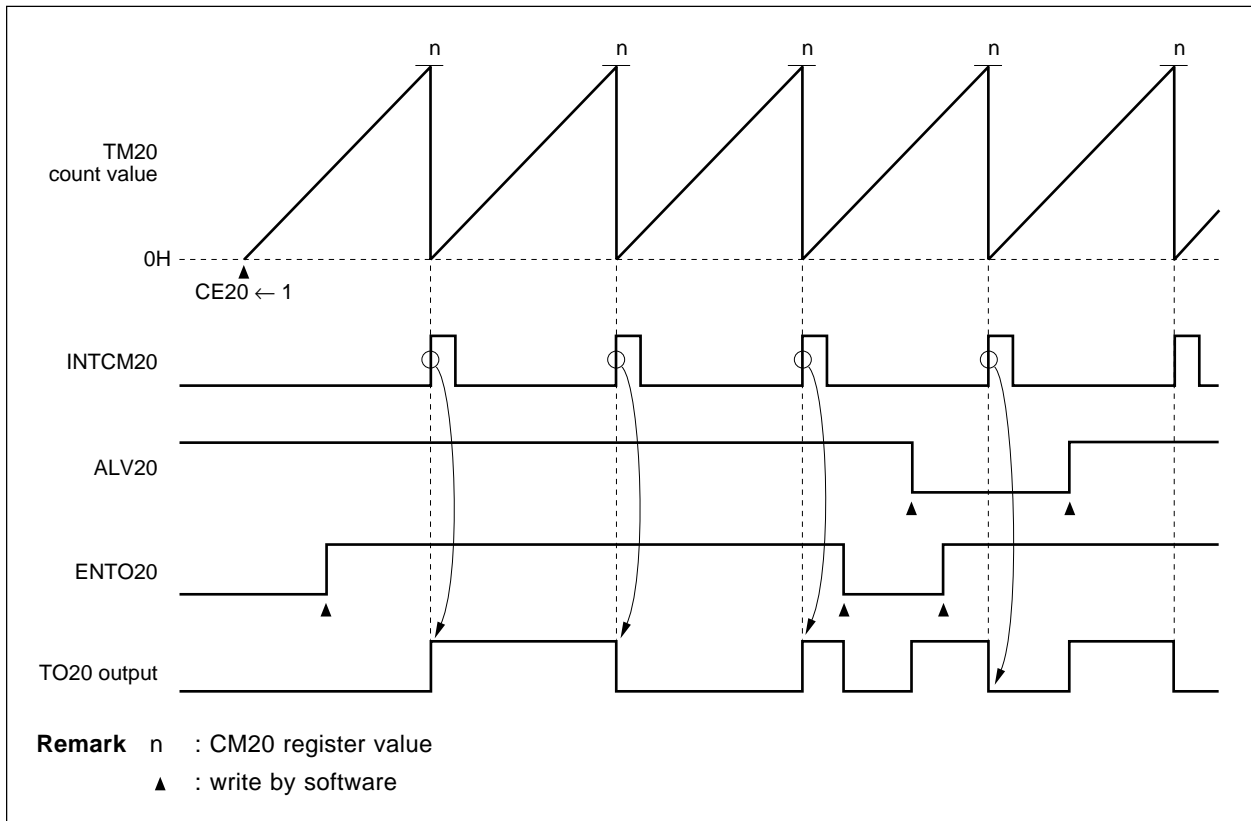
Remark Interval time = $(FFFFH + 2) \times \text{count clock cycle}$

7.6.6 Toggle output

Toggle output is an operation mode to invert output levels each time the value of the compare register (CM20 to CM24) coincides with that of CM2n ($n = 0$ to 4). The relations between timers to be compared and compare register to timer outputs are shown below.

- TM20, CM20 → TO20
- TM21, CM21 → TO21
- TM22, CM22 → TO22
- TM23, CM23 → TO23
- TM24, CM24 → TO24

Figure 7-19. Example of Toggle Output Operation



7.7 Timer 3 Operation

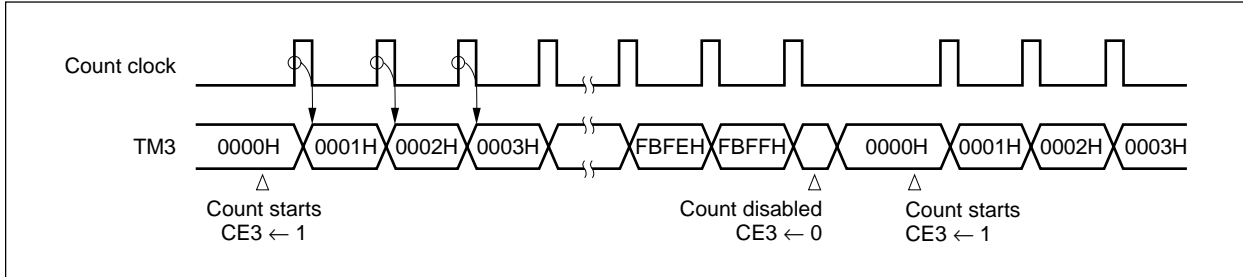
7.7.1 Count operation

Timer 3 functions as a 16-bit interval timer. The operation is specified by the timer control registers 3 (TMC3).

The operation of timer 3 counts the internal count clocks ($\phi/2$ to $\phi/256$) specified by the PRM30 to PRM33 bits of the TMC3 register.

If the count value of TM3 coincides with the value of CC3, the value TM3 is cleared while simultaneously a coincidence interrupt (INTCC3) is generated.

Figure 7-20. Basic Operation of Timer 3



7.7.2 Count clock selection

An internal count clock frequency is selected by the PRM30 to PRM33 bits of the TMC3 register, from $\phi/2$, $\phi/4$, $\phi/8$, $\phi/16$, $\phi/32$, $\phi/64$, $\phi/128$, and $\phi/256$.

Caution Do not change the count clock frequency while the timer operates.

PRM33	PRM32	PRM31	PRM30	Internal Count Clock Frequency
0	0	0	1	$\phi/2$
0	0	1	0	$\phi/4$
0	0	1	1	$\phi/8$
0	1	0	0	$\phi/16$
0	1	0	1	$\phi/32$
0	1	1	0	$\phi/64$
0	1	1	1	$\phi/128$
1	0	0	0	$\phi/256$

7.7.3 Overflow

If TM3 overflows as a result of counting the internal count clock, a flag is set to the OVF3 bit of the TOVS register.

7.7.4 Clearing/starting timer

There are three methods of clearing/starting timer 3: by coincidence of compare register, by capture trigger of CC3, and by software.

(1) Clearing/starting by compare coincidence of CC3

If CC3 is specified as a compare register by the CMS3 bit, TM3 clears its value at the next count clock and starts count operation when the set value of the compare register (CC3) and the value of TM3 coincide. At the same time, an interrupt request (INTCC30) is generated.

The interval timer set to a compare register can be calculated by the following expression:

$$(\text{Set value} + 1) \times \text{Count cycle}$$

For the details, refer to **7.7.6 Compare operation**.

(2) Clearing/staring by capture trigger of CC3

If CC3 is specified as a capture register by the CMS3 bit, when a capture trigger of CC3 is generated, the count value of TM3 is captured in CC3, TM3 is cleared, and count operation is started. At the same time, an interrupt request (INTCC3) is generated.

(3) Clearing/starting by software

When the CS3 bit of the TMC3 register is set to 1, the TM1 register clears its value and start counting from 0.

However, this setting of the bit is valid only when the value of the CE3 bit is 1.

7.7.5 Capture operation

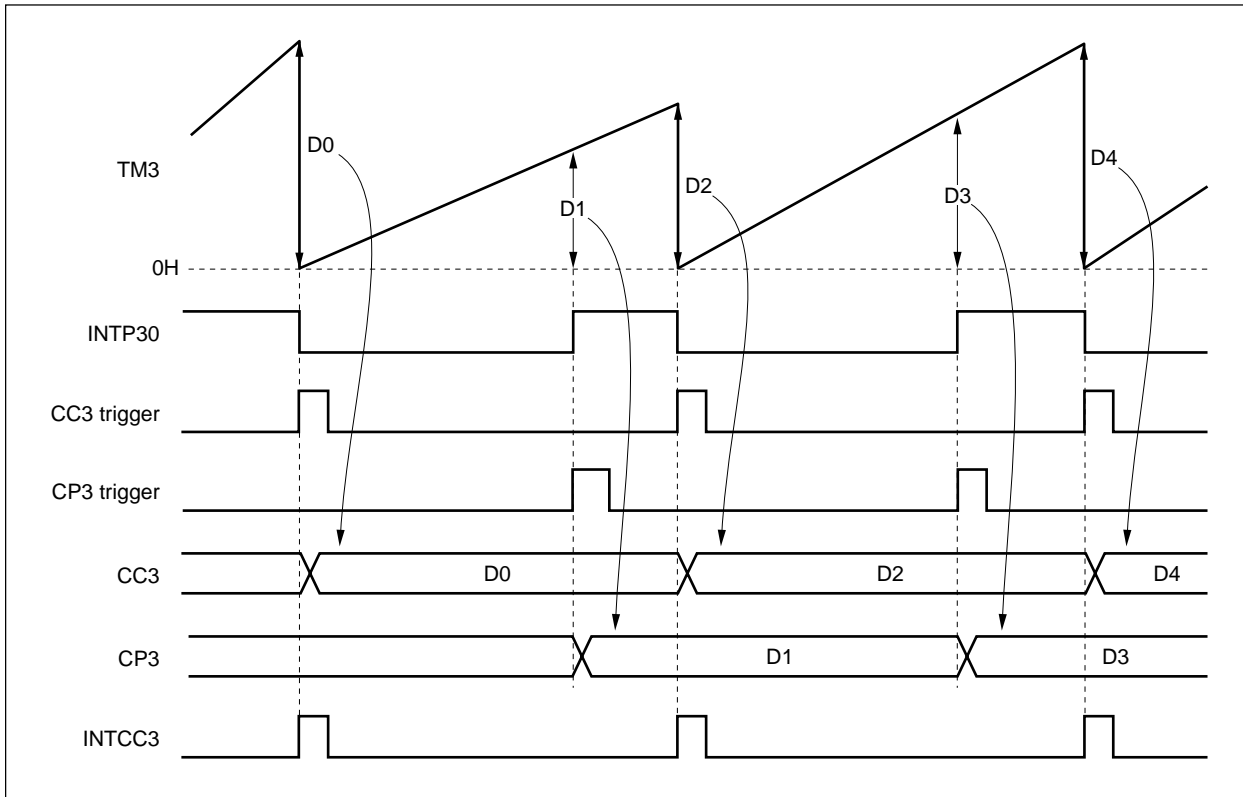
When the TMC3 register is set as a capture register, the capture/compare register (CC3) performs a capture operation that captures and holds the count value of TM3 and loads it to a capture register in synchronization with an external trigger and in asynchronization with the count clock. The valid edge from the external interrupt request input pin INTP30 is used as the capture trigger. In synchronization with this capture trigger signal the count values of TM3 during counting are captured and loaded to the capture register. The value of the capture register is retained until the next capture trigger is generated.

When the capture timing of the capture register and the write operation to the register are in contention, the latter is given priority and the capture operation is ignored.

Table 7-6. Capture Trigger Signal to 16-Bit Capture Register

Capture Source	Selection of Valid Edge				Capture Trigger	Interrupt Request
INTP30	↓	↑	—	↑↓	CC3	INTCC3
	↑	↓	↑↓	—	CP3	—

The valid edge of the capture trigger is set by the external interrupt mode register (INTM7). When the CC3 trigger is set to the falling edge and the CP3 trigger is set to the rising edge, input pulse width and input pulse cycle from external can be measured with one interrupt (INTCC3).

Figure 7-21. Example of TM3 Capture Operation (when ES301 = 0, ES300 = 0, CMS3 = 0, CE3 = 1)

7.7.6 Compare operation

When the TM3 register is set as a compare register, the capture/compare register (CC3) performs a comparison between the value in a compare register and the count value of TM3.

When the count value of TM3 coincides with the value of the compare register programmed in advance, clear and start of TM3 is performed, and interrupt request signal INTCC3 is generated at the same time.

7.8 Application Examples

(1) Operation as interval timer (timer 0, timer 2, and timer 3)

The following shows that timer 2 used as an interval timer that repeatedly generates an interrupt request at time intervals specified by the count value set in advance to compare register CM20. Figure 7-22 shows the timing. Figure 7-23 illustrates the setting procedure.

Figure 7-22. Example of Timing of Interval Timer Operation (timer 2)

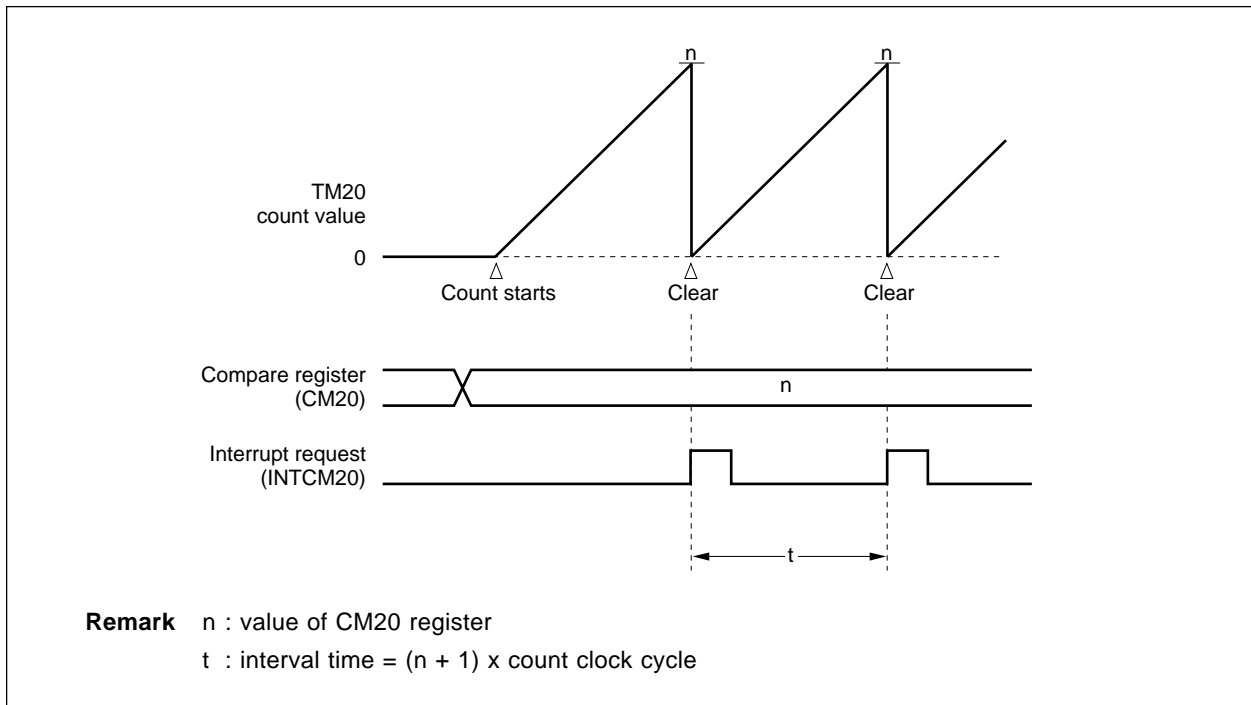
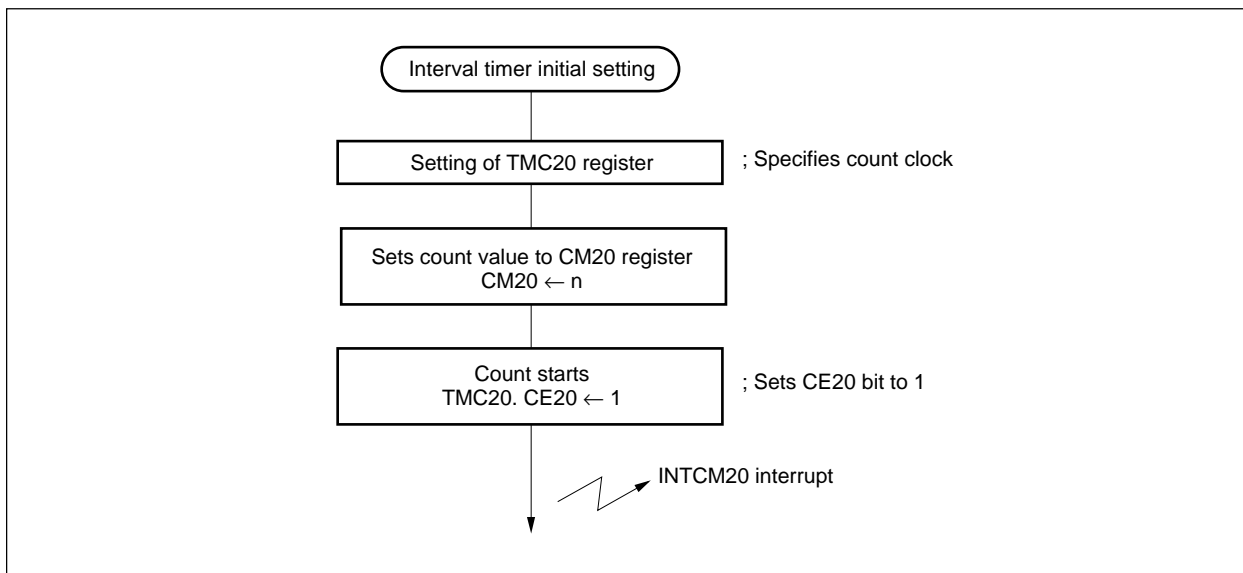


Figure 7-23. Setting Procedure of Interval Timer Operation (timer 2)



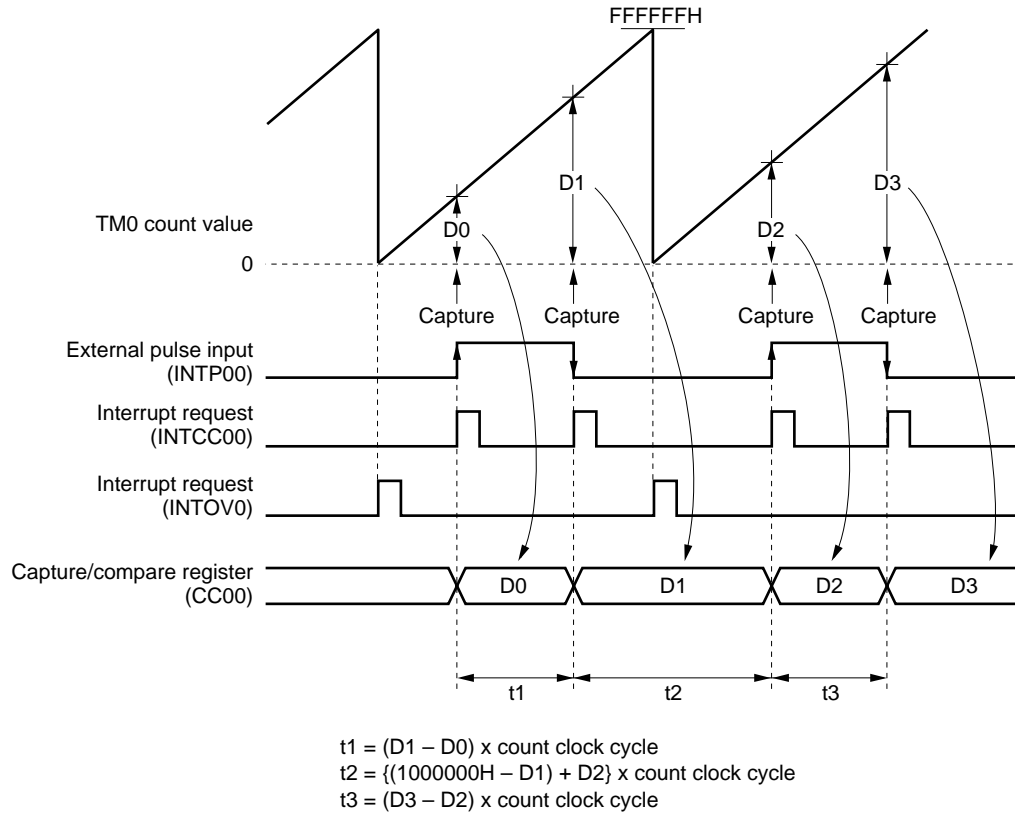
(2) Pulse width measurement (timer 0, timer 1, and timer 3)

An example of pulse width measurement is shown below.

In this example, the width of the high or low level of an external pulse input to the INTP00 pin is measured. The value of timer 1 (TM0) is captured to a capture/compare register (CC00) in synchronization with the valid edge of the INTP00 pin (both the rising and falling edges) and is pended, as shown in Figure 7-24.

To calculate the pulse width, the difference between the count value of TM0 captured to the CC00 register on detection of the nth valid edge (Dn), and the count value on detection of the (n – 1)th valid edge (Dn – 1) is calculated. This difference is multiplied by the count clock.

Figure 7-24. Pulse Width Measurement Timing (timer 0)



Remark D0 to D3: count value of TM0

Figure 7-25. Setting Procedure for Pulse Width Measurement (timer 0)

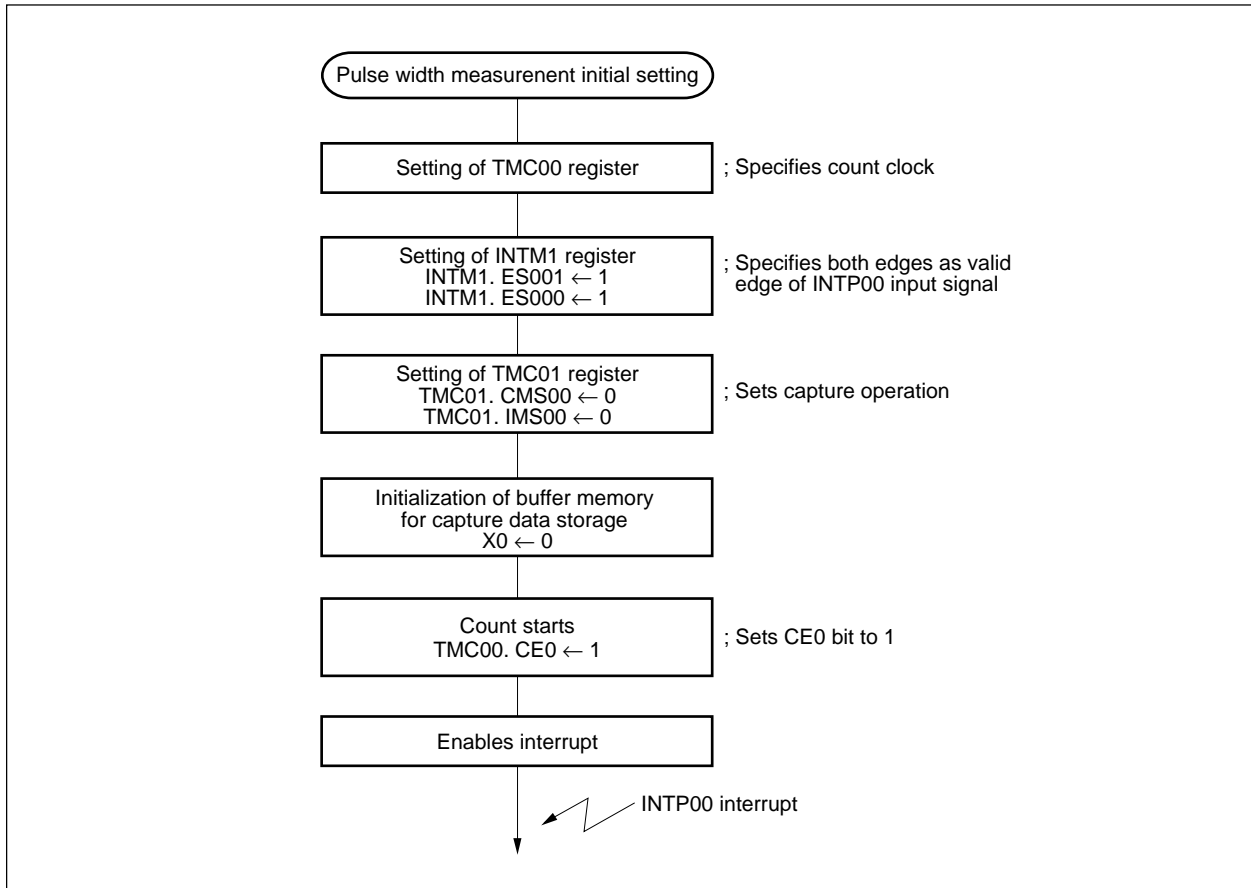
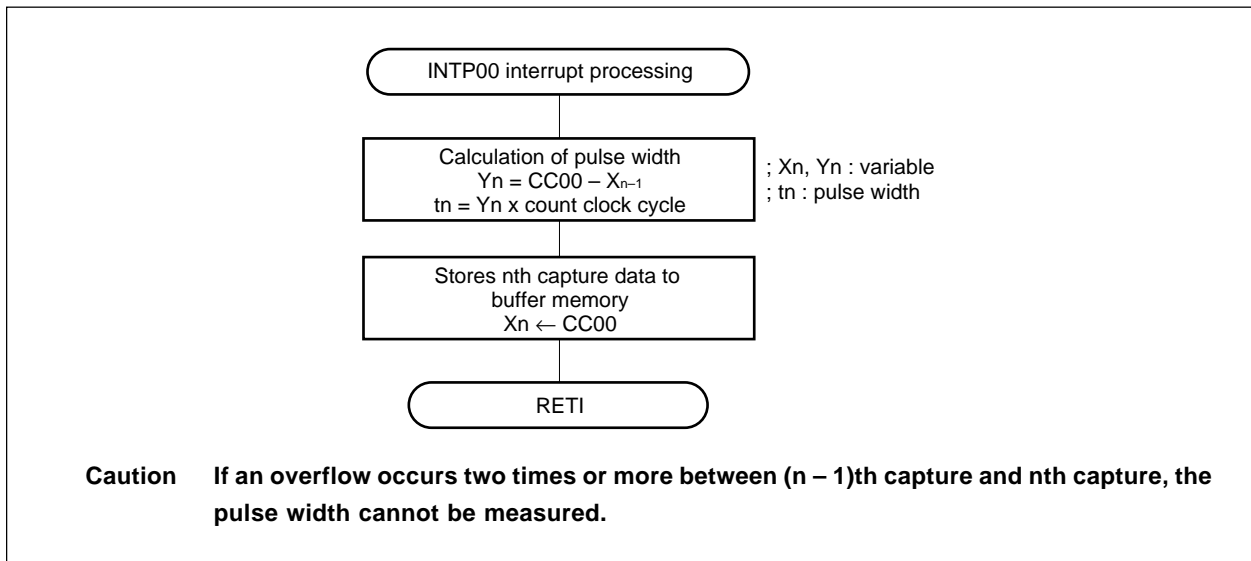


Figure 7-26. Interrupt Request Processing Routine Calculating Pulse Width (timer 0)



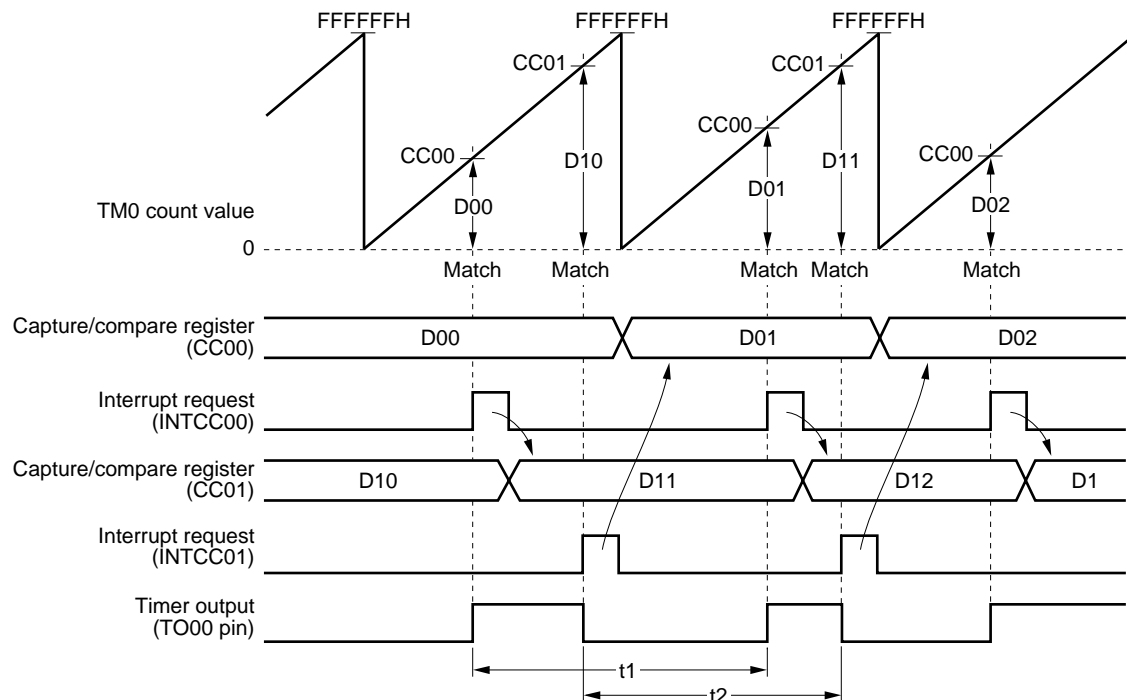
(3) PWM output (timer 0)

Any square wave can be output to timer output pin (TOn) by combining the use of timer 0 and the timer output function and can be used as a PWM output.

Shown below is an example of PWM output using two capture/compare registers, CC00 and CC01. In this case, a PWM signal with an accuracy of 24 bits can be output from the TO00 pin. Figure 7-27 shows the timing. When timer 0 is used as a 24-bit timer, the rising timing of the PWM output is determined by the value set to capture/compare register CC00, and the falling timing is determined by the value set to capture/compare register CC01.

The interval frequency of timer output can be changed freely by using compare coincidence of CC03 and by clearing and starting TM0.

Figure 7-27. Example of PWM Output Timing



Remark D00 to D02, D10 to D13 : set value of compare register

$$t1 = \{(1000000H - D00) + D01\} \times \text{count clock cycle}$$

$$t2 = \{(1000000H - D10) + D11\} \times \text{count clock cycle}$$

Figure 7-28. Example of PWM Output Programming Procedure

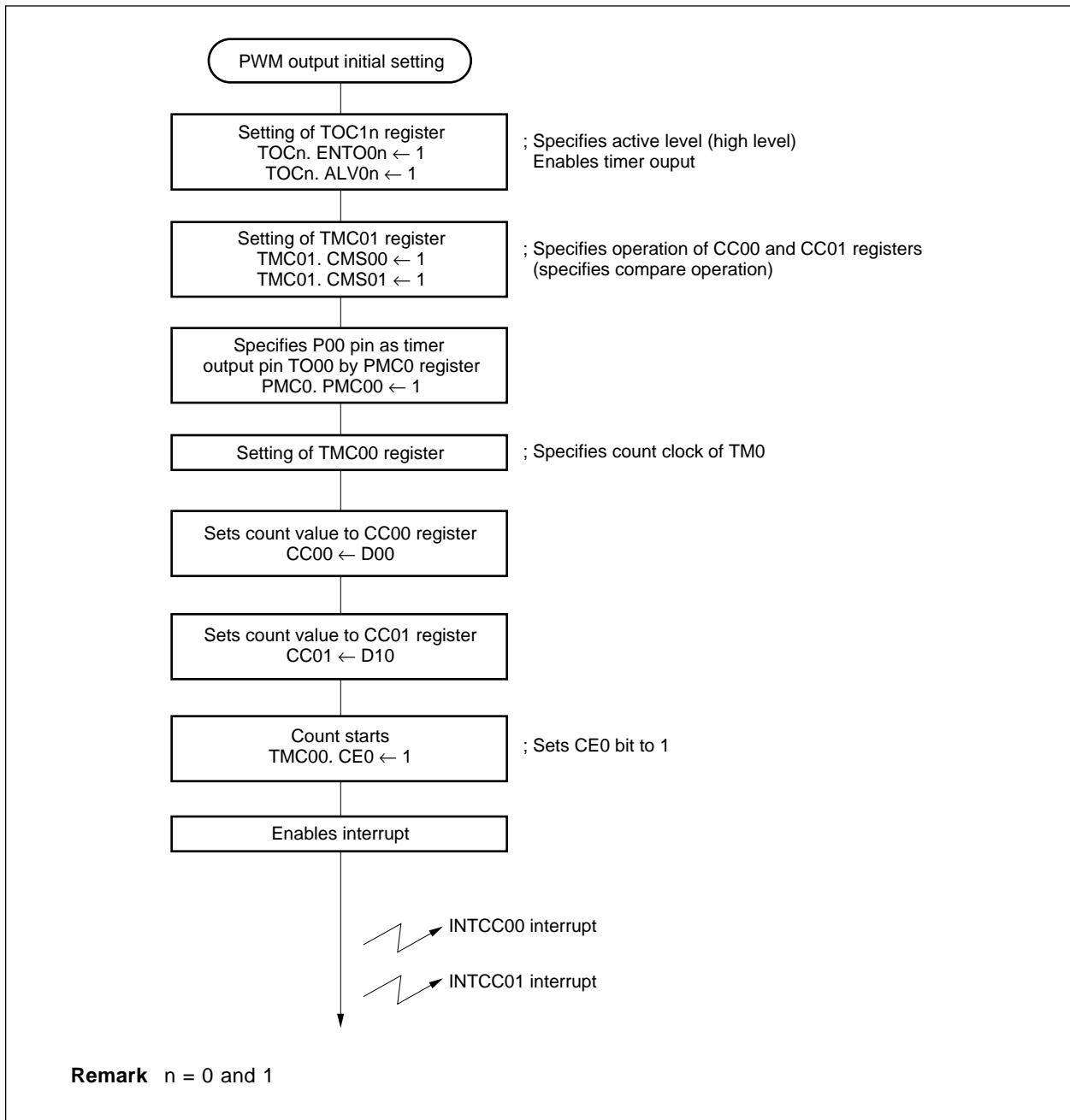
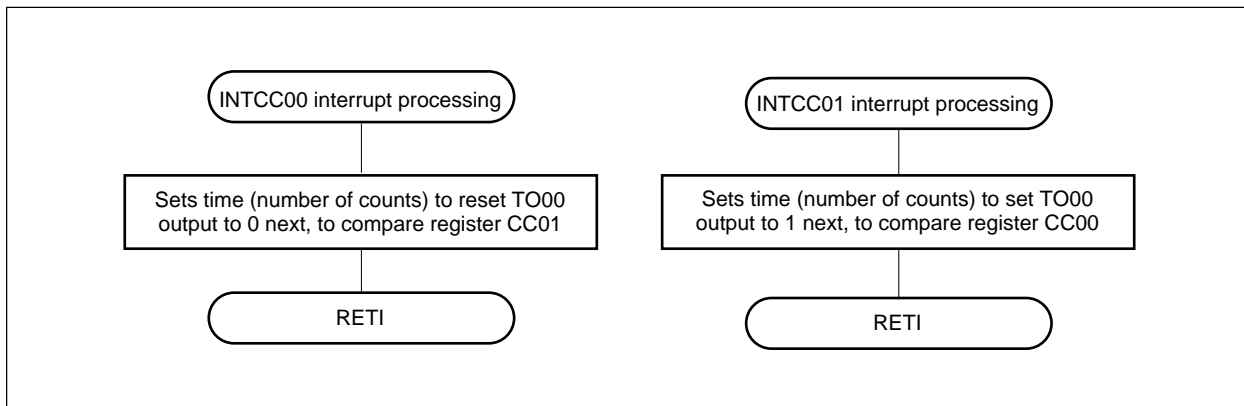


Figure 7-29. Example of Interrupt Request Processing Routine, Modifying Compare Value

(4) Frequency measurement (timer 0, timer 1, and timer 3)

Timer 0, timer 1, and timer 3 can be used to measure the cycle or frequency of an external pulse input to the INTP pin.

Shown below is an example where the frequency of the external pulse input to the INTP00 pin is measured with an accuracy of 24 bits, by combining the use of timer 0 and the capture/compare register CC00.

The valid edge of the INTP00 input signal is specified by the INTM1 register to be the rising edge.

To calculate the frequency, the difference between the count value of TM0 captured to the CC00 register at the n th rising edge (D_n), and the count value captured at the $(n - 1)$ th rising edge ($D_{n - 1}$), is calculated, and the value multiplied by the count clock frequency.

The frequency measurement exceeding the maximum count value of TM0 is performed by counting the number of overflow with the INTOV0 overflow interrupt request.

Figure 7-30. Example of Frequency Measurement Timing

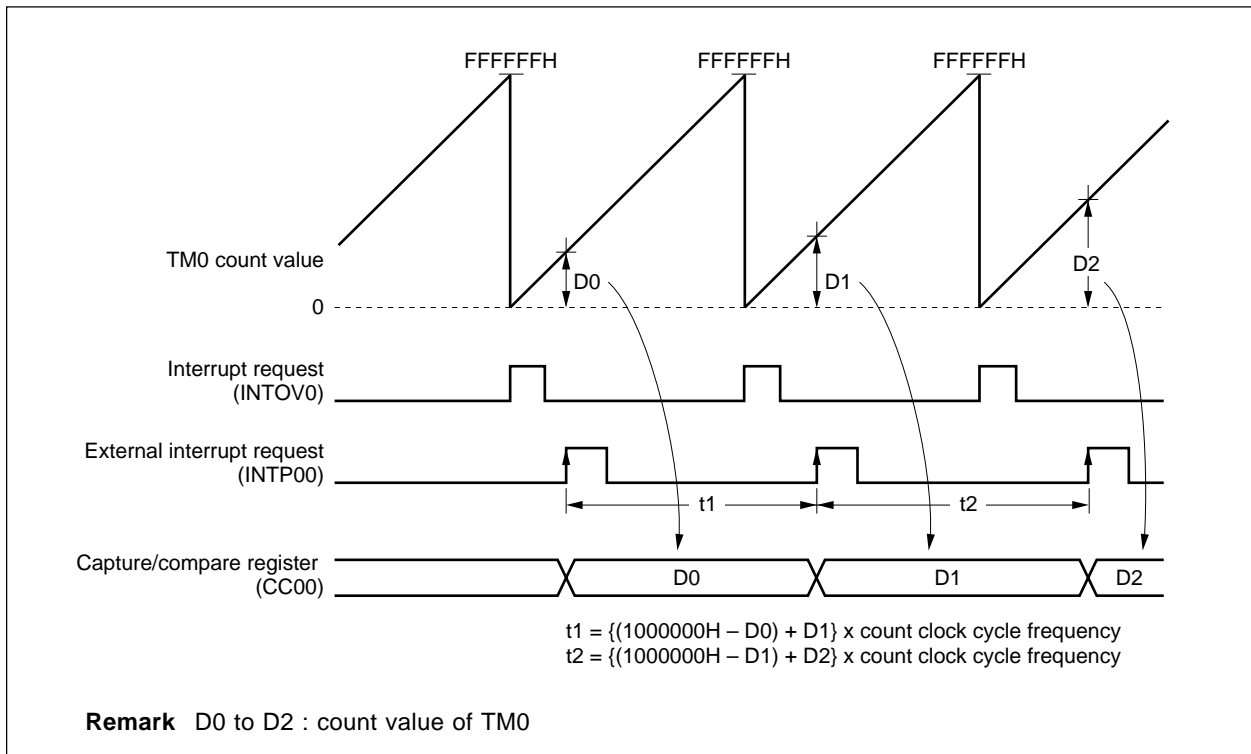


Figure 7-31. Example of Set-up Procedure for Frequency Measurement

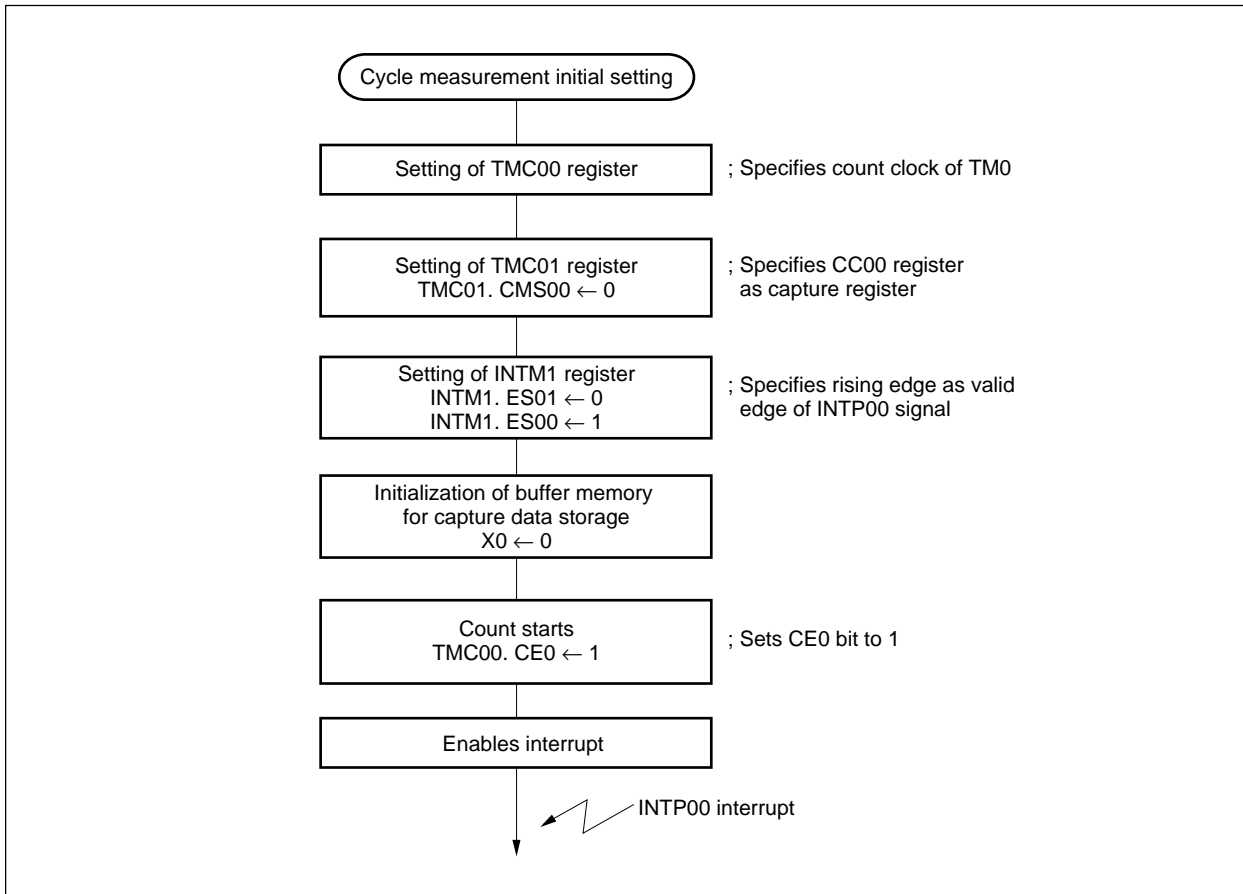
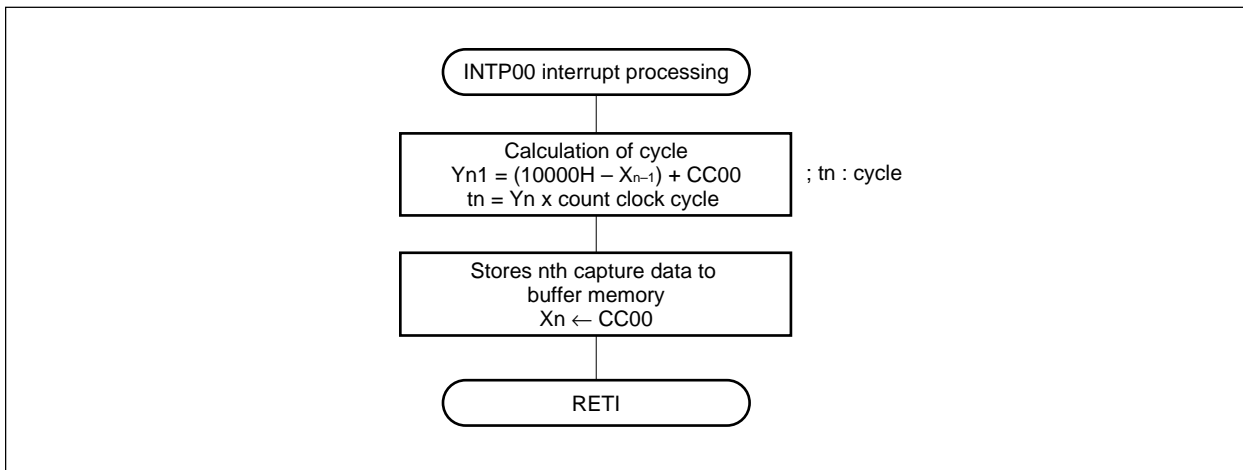


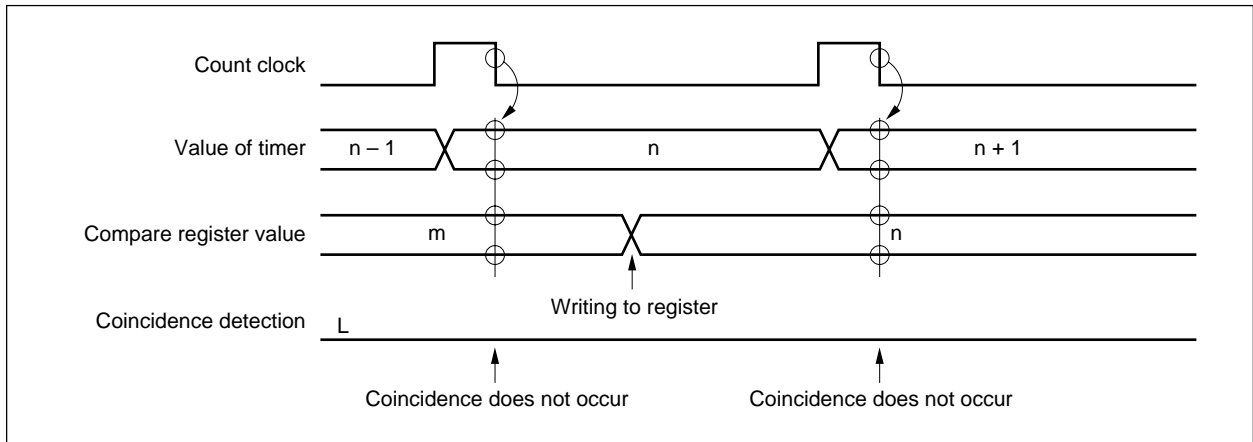
Figure 7-32. Example of Interrupt Request Processing Routine Calculating Cycle



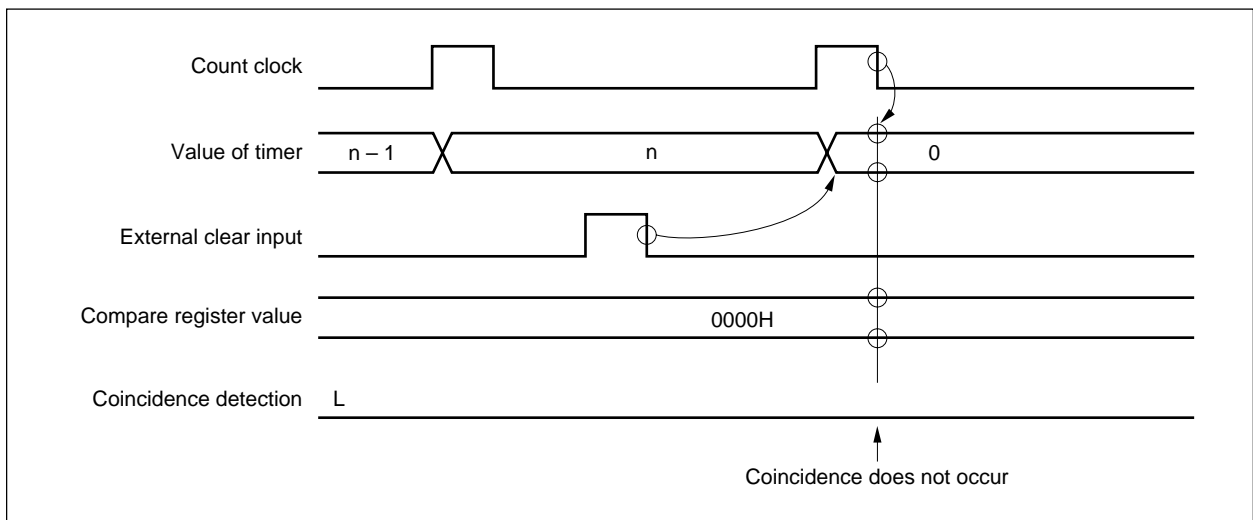
7.9 Note

Coincidence is detected by the compare register immediately after the timer value matches the compare register value, and does not take place in the following cases:

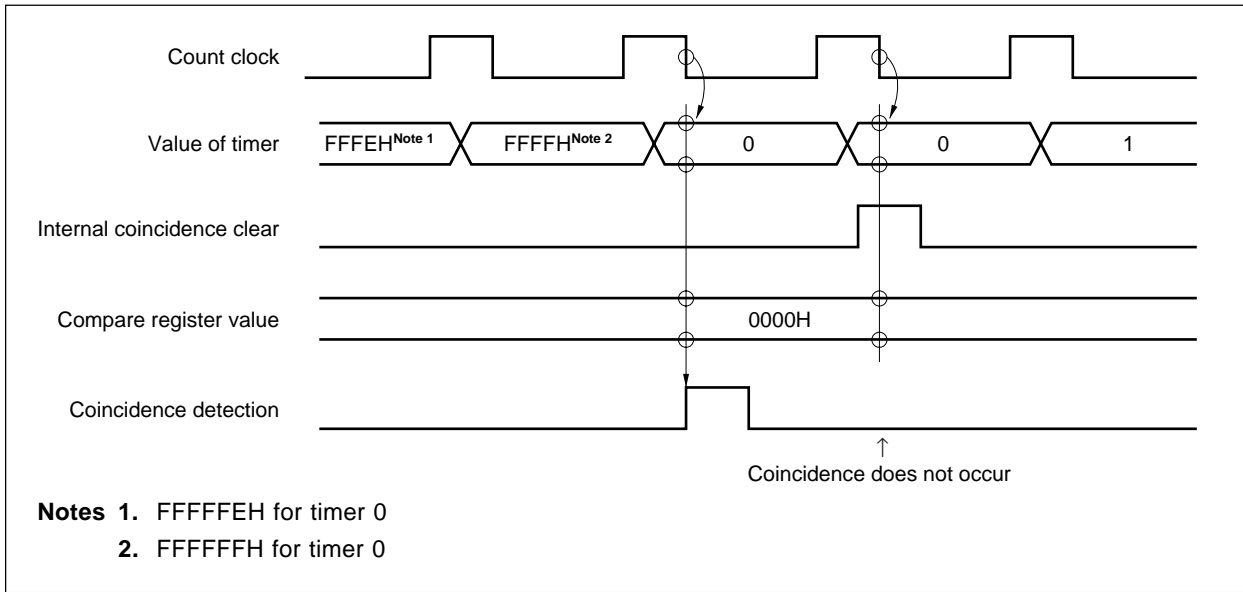
(1) When compare register is rewritten (timer 0 to timer 3)



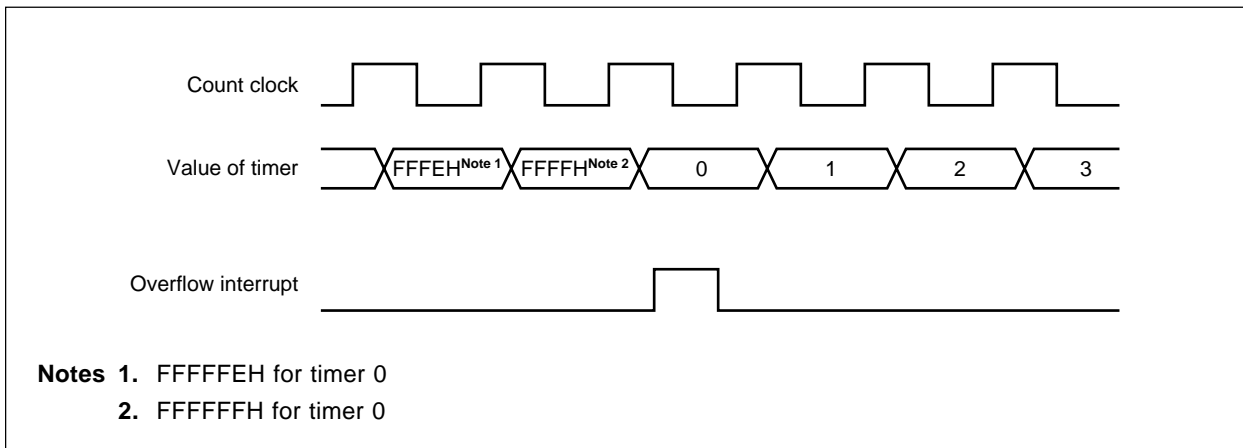
(2) When timer is cleared by external input (timer 0)



(3) When timer is cleared (timer 0, timer 2, and timer 3)



Remark When timer 0 or timer 1 is operated as a free running timer, the timer value is cleared to 0 when the timer overflows.



CHAPTER 8 SERIAL INTERFACE FUNCTION

8.1 Features

The V854 is provided with three types of serial interfaces which operate as 6-channel transmission/reception channels. Four channels can be used simultaneously.

There are the following three types of interfaces.

- (1) Asynchronous serial interface (UART) : 1 channel
- (2) Clocked serial interface (CSI) : 4 channels
- (3) I²C bus interface (I²C) : 1 channel (μ PD703008Y and 70F3008Y only)

The UART transmits/receives 1-byte serial data following a start bit and can perform full-duplex communication.

The CSI uses three signal lines to high-speed synchronous data transfers data (3-wire serial I/O): serial clock ($\overline{\text{SCKn}}$), serial input (SIn), and serial output (SOn) lines.

The I²C uses two signal lines, which are serial clock (SCL) and serial data bus (SDA), to transfer data (μ PD703008Y and 70F3008Y only).

Caution UART and CSI0, and CSI1 and I²C share the same pin respectively. Either one of these is selected according to ASIM0 and ASIM1.

8.2 Asynchronous Serial Interface (UART)

8.2.1 Features

- Transfer rate: 150 bps to 153600 bps (Baud rate generator used, @ ϕ = 33-MHz operation)
- 110 bps to 614400 bps (Baud rate generator used, @ ϕ = 19.660-MHz operation)
- ★ 110 bps to 38400 bps (Baud rate generator used, @ ϕ = 16-MHz operation)
- Max. 1031 kbps ($\phi/2$ use, @ ϕ = 33-MHz operation)
- Full-duplex communication: internal receive buffer (RXB)
- Two-pin configuration: TXD: transmit data output pin
RXD: receive data input pin
- Receive error detection function
 - Parity error
 - Framing error
 - Overrun error
- Interrupt sources: 3
 - Receive error interrupt (INTSER)
 - Reception completion interrupt (INTSR)
 - Transmission completion interrupt (INTST)
- Character length of transmit/receive data is specified by ASIMn registers.
- Character length: 7, 8 bits
9 bits (when extended)
- Parity function: odd, even, 0, none
- Transmit stop bit: 1, 2 bits
- Dedicated internal baud rate generator

Remark ϕ : Internal system clock

8.2.2 Configuration of asynchronous serial interface

The asynchronous serial interface is controlled by the asynchronous serial interface mode register (ASIMn) and the asynchronous serial interface status register (ASIS). The receive data is stored in the receive buffer (RXB), and the transmit data is written to the transmit shift register (TXS).

Figure 8-1 shows the configuration of the asynchronous serial interface.

(1) Asynchronous serial interface mode registers (ASIM0, ASIM1)

ASIMn are 8-bit registers that specify the operation of the asynchronous serial interface.

(2) Asynchronous serial interface status registers (ASIS)

ASIS are registers containing flags that indicate receive errors, if any, and a transmit status flag. Each receive error flag is set to 1 when a receive error occurs, and is reset to 0 when data is read from the receive buffer (RXB), or when new data is received (if the next data contains an error, the corresponding error flag is set). The transmit status flag is set to 1 when transmission is started, and reset to 0 when transmission ends.

(3) Reception control parity check

The reception operation is controlled according to the contents programmed in the ASIMn registers. During the receive operation, errors such as parity error are also checked. If an error is found, the appropriate value is set to the ASIS registers.

(4) Receive shift register

This shift register converts the serial data received on the RXD pin into parallel data. When it receives 1 byte of data, it transfers the receive data to the receive buffer.

This register cannot be directly operated.

(5) Receive buffers (RXB, RXBL)

RXB are 9-bit buffer registers that hold receive data. If data of 7 or 8 bits/character is received, 0 is stored to the most significant bit position of these registers.

If these registers are accessed in 16-bit units, RXB are specified. To access in lower 8-bit units, RXBL are specified.

While reception is enabled, the receive data is transferred from the receive shift register to the receive buffer in synchronization with shift-in processing of 1 frame.

When the data is transferred to the receive buffer, a reception completion interrupt request (INTSR) occurs.

(6) Transmit shift registers (TXS, TXSL)

TXS are 9-bit shift registers used for transmit operation. When data is written to these registers, the transmission operation is started.

A transmission complete interrupt request (INTST) is generated after each complete data frame is transmitted. When these registers are accessed in 16-bit units, TXS are specified. To access in lower 8-bit units, TXSL are specified.

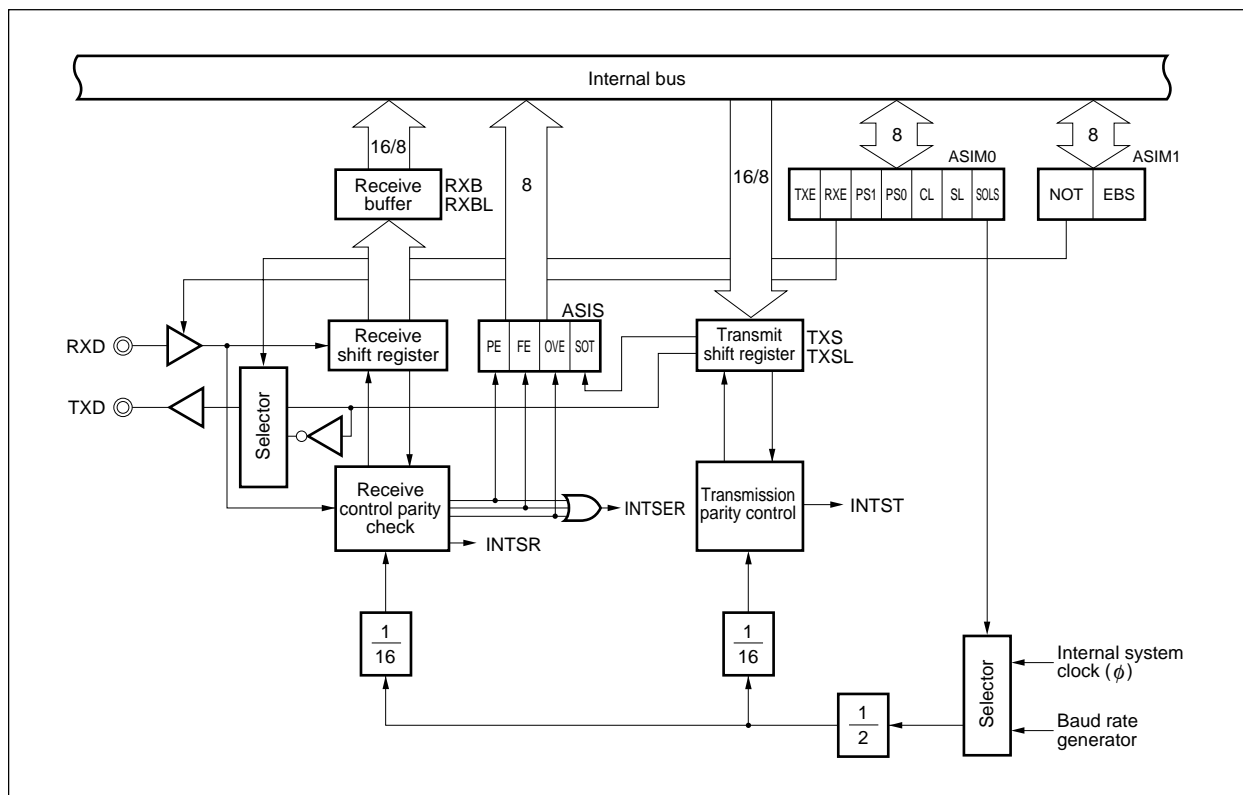
(7) Transmission parity control

A start bit, parity bit, and stop bit are appended to the data written to the TXS registers, according to the contents programmed in the ASIMn registers, to control the transmission operation.

(8) Selector

Selects the source of the serial clock.

Figure 8-1. Block Diagram of Asynchronous Serial Interface



8.2.3 Control registers

(1) Asynchronous serial interface mode registers 0, 1 (ASIM0, ASIM1)

These registers specify the transfer mode of the UART.

They can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
ASIM0	TXE	RXE	PS1	PS0	CL	SL	0	SCLS	Address FFFFFF0C0H	After reset 80H

Bit Position	Bit Name	Function
7	TXE	Transmit Enable Enable/disable transmission. 0 : Disable transmission 1 : Enable transmission
6	RXE	Receive Enable Enable/disable reception. 0 : Disable reception 1 : Enable reception When reception is disabled, the receive shift register does not detect the start bit. Data is not shifted into the receive shift register and neither is any transfer to the receive buffer performed. Therefore, the previous contents of the receive buffer are retained. When reception is enabled, the data is shifted into the receive shift register and transferred to the receive buffer when one complete frame has been received. A reception completion interrupt (INTSRn) is generated in synchronization with the transfer to the receive buffer. If this bit is set to receive disabled status during receive operation, the data being received is relinquished and the data before the receive operation is started is read out.

Bit Position	Bit Name	Function															
5, 4	PS1, PS0	<p>Parity Select Specifies parity bit.</p> <table border="1"> <thead> <tr> <th>PS1</th><th>PS0</th><th>Operation</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>No parity. Extended bit operation</td></tr> <tr> <td>0</td><td>1</td><td>0 parity Transmission side → Transmits with parity bit 0 Reception side → Does not generate parity error on reception</td></tr> <tr> <td>1</td><td>0</td><td>Odd parity</td></tr> <tr> <td>1</td><td>1</td><td>Even parity</td></tr> </tbody> </table> <ul style="list-style-type: none"> Even parity Parity bit is set to "1" when number of bits equal to one in received data is odd. If number of bits that are one is even, parity bit is cleared to 0. In this way, number of bits that are "1" in transmit data and parity bit is controlled to become even. During reception, number of bits that are "1" in receive data and parity bit are counted. If it is odd, parity error occurs. Odd parity In contrast to even parity, number of bits included in transmit data and parity bit that are "1" is controlled to become odd. Since no parity bit check is performed during reception, no parity error occurs. 0 parity Parity bit is cleared to "0" during transmission, regardless of transmit data. Since no parity bit check is performed during reception, no parity error occurs. No parity No parity bit is appended to the transmit data. Reception is performed on assumption that there is no parity bit. Because no parity bit is used, parity error does not occur. Extended bit operation can be specified by EBS bit of ASIM1 register. 	PS1	PS0	Operation	0	0	No parity. Extended bit operation	0	1	0 parity Transmission side → Transmits with parity bit 0 Reception side → Does not generate parity error on reception	1	0	Odd parity	1	1	Even parity
PS1	PS0	Operation															
0	0	No parity. Extended bit operation															
0	1	0 parity Transmission side → Transmits with parity bit 0 Reception side → Does not generate parity error on reception															
1	0	Odd parity															
1	1	Even parity															
3	CL	<p>Character Length Specifies character length of one frame.</p> <p>0 : 7 bits 1 : 8 bits</p>															
2	SL	<p>Stop Bit Length Specifies stop bit length.</p> <p>0 : 1 bit 1 : 2 bits</p>															

Bit Position	Bit Name	Function																		
0	SCLS	<p>Serial Clock Source</p> <p>Specifies serial clock.</p> <p>0 : Specified by BRGC0 and BPRM0</p> <p>1 : $\phi/2$</p> <ul style="list-style-type: none">When SCLS = 1 <p>$\phi/2$ is selected as serial clock source. In asynchronous mode, baud rate is expressed as follows because sampling rate of x16 is used:</p> <p>Baud rate = $\frac{\phi/2}{16}$ bps</p> <p>Value of baud rate when typical clock is used based on above expression is as follows:</p> <table><tr><td>ϕ</td><td>33 MHz</td><td>25 MHz</td><td>20 MHz</td><td>16 MHz</td><td>12.5 MHz</td><td>10 MHz</td><td>8 MHz</td><td>5 MHz</td></tr><tr><td>Baud rate</td><td>1031 K</td><td>781 K</td><td>625 K</td><td>500 K</td><td>390 K</td><td>312 K</td><td>250 K</td><td>156 K</td></tr></table> <ul style="list-style-type: none">When SCLS = 0 <p>Baud rate generator output is selected as serial clock source. For details of baud rate generator, refer to 8.5 Baud Rate Generator 0 to 3 (BRG0 to BRG3).</p>	ϕ	33 MHz	25 MHz	20 MHz	16 MHz	12.5 MHz	10 MHz	8 MHz	5 MHz	Baud rate	1031 K	781 K	625 K	500 K	390 K	312 K	250 K	156 K
ϕ	33 MHz	25 MHz	20 MHz	16 MHz	12.5 MHz	10 MHz	8 MHz	5 MHz												
Baud rate	1031 K	781 K	625 K	500 K	390 K	312 K	250 K	156 K												

Caution The operation of UART is not guaranteed if these registers are changed while UART is transmitting/receiving data.

Remark ϕ : Internal system clock

	7	6	5	4	3	2	1	0		
ASIM1	0	0	0	0	0	0	NOT	EBS	Address FFFFFF0C2H	After reset 00H

Bit Position	Bit Name	Function
1	NOT	<p>Not Inverts the output level from TXD pin. 0 : Does not invert the output level 1 : Inverts output level Use this function to connect an external circuit having inverted level to TXD pin.</p>
0	EBS	<p>Extended Bit Select Specifies extended bit operation of transmit/receive data when no parity is specified (PS0 = 0, PS1 = 0). 0 : Disables extended bit operation 1 : Enables extended bit operation When extended bit operation is enabled, 1 data bit is appended as most significant bit to 8-bit transmit/receive data, and therefore 9-bit data is communicated. Extended bit operation is valid only when no parity is specified by ASIM0 register. If zero, even, or odd parity is specified, specification by EBS bit is invalid, and extended bit is not appended.</p>

(2) Asynchronous serial interface status register (ASIS)

This register contains three error flags that indicate the receive error status for each character received and the status of the transmit shift register.

The error flags always indicate the status of an error that has occurred most recently. If two or more errors occur before the current received data, only the status of the error that has occurred last is retained.

If a receive error occurs, read the data of the receive buffer RXB/RXBL after reading the ASIS register, and then clear the error flag.

This register can only be read in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
ASIS	SOT	0	0	0	0	PE	FE	OVE	Address FFFFF0C4H	After reset 00H

Bit Position	Bit Name	Function
7	SOT	<p>Status of Transmission</p> <p>Status flag that indicates transmission operation status.</p> <p>Set (1) : Beginning of transmission of a data frame (writing to TXS register)</p> <p>Clear (0) : End of transmission of a data frame (occurrence of INTST)</p> <p>When serial data transfer begins, this flag will indicate if the transmit shift register is ready to be written or not.</p>
2	PE	<p>Parity Error</p> <p>Status flag that indicates parity error.</p> <p>Set (1) : Transmit parity and receive parity do not match</p> <p>Clear (0) : No error; this flag is automatically cleared to 0 when the data is read from the receive buffer.</p>
1	FE	<p>Framing Error</p> <p>Status flag that indicates framing error.</p> <p>Set (1) : Stop bit is not detected</p> <p>Clear (0) : No error; this flag is automatically cleared to 0 when the data is read from the receive buffer.</p>
0	OVE	<p>Overrun Error</p> <p>Status flag that indicates overrun error.</p> <p>Set (1) : Overrun error; Contents of the receive shift register are transferred to the receive buffer before the previous data has been read by the CPU. This will cause an over writing of data and the previous information will be lost.</p> <p>Clear (0) : No error; this flag is automatically cleared to 0 when the data is read from the receive buffer.</p> <p>Because contents of receive shift register are transferred to receive buffer each time one frame of data has been received, if overrun error occurs, next receive data is written over contents of receive buffer, and previous receive data is discarded.</p>

(3) Receive buffers (RXB, RXBL)

RXB are 9-bit buffer registers that hold the receive data. When a 7- or 8-bit character is received, the higher bit of these registers are 0.

When reading 16-bit data from the receive buffer, RXB is specified. When data is read from the lower 8bits, RXBL is specified.

During the state where reception is enabled the receive data is transferred from the receive shift register to the receive buffer synchronizing one complete frame of data has been shifted in.

When the receive data is transferred to the receive buffer, a reception completion interrupt request (INTSR) occurs.

During the state where reception is disabled the data is not transfered into the reception buffer even when one complete frame of data has been shifted in and the data of the reception buffer is retained. In addition, the reception completion interrupt request is not generated. RxB is only possible for reading in 16-bit units and RXBL in 8-/1-bit units.

RXB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address FFFFF0C8H	After reset Undefined
	0	0	0	0	0	0	0	RXEB	RXB7	RXB6	RXB5	RXB4	RXB3	RXB2	RXB1	RXB0		

RXBL	7	6	5	4	3	2	1	0	Address FFFFF0CAH	After reset Undefined
	RXB7	RXB6	RXB5	RXB4	RXB3	RXB2	RXB1	RXB0		

Bit Position	Bit Name	Function
8	RXEB	Receive Extended Buffer Extended bit when 9-bit character is received. These bits are cleared to zero when 7- or 8-bit character is received.
7 to 0	RXB7 to RXB0	Receive Buffer These bits store receive data. RXB7 is cleared to zero when 7-bit character is received.

(4) Transmit shift registers (TXS, TXSL)

TXS are 9-bit shift registers for data transmission. The transmit operation is started when data is written to these registers during transmission enable status.

If data is written to the transmit shift register in the transmission disabled status, the values written are ignored. Transmission complete interrupt request (INTST) is generated after each complete data frame including TXS is transmitted.

In the case of access in 16-bit units, TXS is specified. To access the lower 8bits, TXSL is specified.

TXS can only be written to TXS in 16-bit units, and TXSL in 8-bit units.

TXS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address FFFFFF0CCH	After reset Undefined
	0	0	0	0	0	0	0	TXED	TXS7	TXS6	TXS5	TXS4	TXS3	TXS2	TXS1	TXS0		

TXSL	7	6	5	4	3	2	1	0	Address FFFFFF0CEH	After reset Undefined
	TXS7	TXS6	TXS5	TXS4	TXS3	TXS2	TXS1	TXS0		

Bit Position	Bit Name	Function
8	TXED	Transmit Extended Data Extended bit on transmission of 9-bit/character.
7 to 0	TXS7 to TXS0	Transmit Shifter Writes transmit data.

Caution Since the UART does not have a transmit buffer, an interrupt request due to the end of transmission is not generated but an interrupt request (INTST) is generated in synchronization with the end of transmission of one frame of data.

8.2.4 Interrupt request

UART generates the following three types of interrupt requests:

- Receive error interrupt (INTSER)
- Reception completion interrupt (INTSR)
- Transmission completion interrupt (INTST)

Of these three, the receive error interrupt has the highest default priority, followed by the reception completion interrupt and transmission completion interrupt.

Table 8-1. Default Priority of Interrupts

Interrupt	Priority
Receive error	1
Reception completion	2
Transmission completion	3

(1) Receive error interrupt (INTSER)

A receive error interrupt occurs as a result of ORing the three types of receive errors described in description of the ASIS registers when reception is enabled.

This interrupt does not occur when reception is disabled.

(2) Reception completion interrupt (INTSR)

The reception completion interrupt occurs if data is received in the receive shift register and then transferred to the receive buffer when reception is enabled.

This interrupt also occurs when a receive error occurs, but the receive error interrupt has higher priority.

The reception completion interrupt does not occur when reception is disabled.

(3) Transmission completion interrupt (INTST)

Because the UART does not have a transmit buffer, a transmission completion interrupt occurs when one frame of transmit data including a 7-/8-/9-bit character is shifted out from the transmit shift register.

The transmission completion interrupt is output when the last bit of data has been transmitted.

8.2.5 Operation

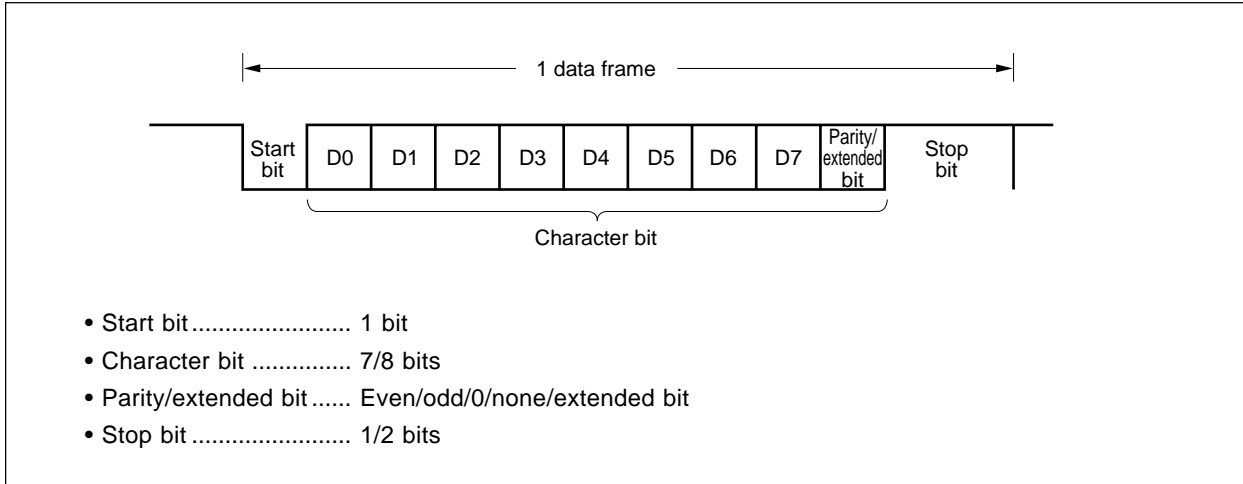
(1) Data format

Full-duplex serial data is transmitted/received.

One data frame of the transmit/receive data consists of a start bit, character bit, parity bit, and stop bit, as shown in Figure 8-2.

The length of the character bit, parity, and the length of the stop bit in one data frame are specified by the asynchronous serial interface mode registers (ASIMn).

Figure 8-2. Format of Transmit/Receive Data of Asynchronous Serial Interface



(2) Transmission

Transmission is started when data is written to the transmit shift registers (TXS or TXSL). The next data is written to the TXS or TXSL registers by the service routine of the transmission completion interrupt processing routine (INTST).

(a) Transmission enabled status

Set using the TXE bit of the ASIM0 register.

TXE = 1 : Transmission enabled status

TXE = 0 : Transmission disabled status

However, to set the transmission enabled status, set both the CTXE0 and CRXE0 bits of the clocked serial interface mode register (CSIM0) to "0".

Because the UART does not have a CTS (transmission enabled signal) input pin, use a general input port when checking whether the other is in the reception enabled status.

(b) Starting transmission

In the transmission enabled status, transmission starts when data is written to the transmission shift register (TXS or TXSL). The transmit data is transferred starting from the start bit with the LSB first. The start bit, parity bit, and stop bit are automatically appended.

Data cannot be written to the transmission shift register in the transmission disabled status, and values written are ignored.

(c) Transmission interrupt request

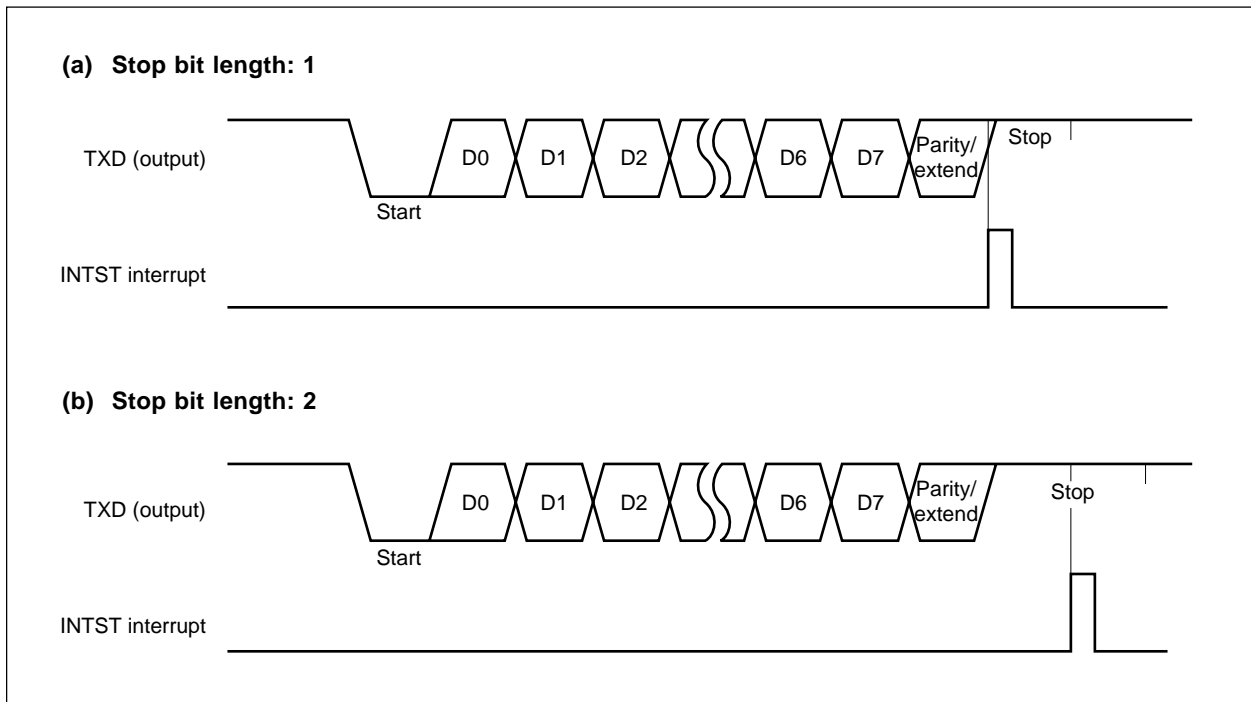
When one frame of data or character has been completely transferred, a transmission completion interrupt request (INTST) occurs.

Unless the data to be transmitted next is written to the TXS or TXSL registers, the transmission is aborted. The communication rate drops unless the next transmit data is written to the TXS or TXSL registers immediately after transmission has been completed.

Cautions 1. Generally, the transmission completion interrupt (INTST) is generated when the transmit shift register (TXS or TXSL) is empty. However, by $\overline{\text{RESET}}$ input, the transmission completion interrupt (INTST) is not generated when the transmit shift register (TXS or TXSL) is empty.

2. During the transmit operation, writing data into the TXS or TXSL register is ignored (the data is discarded) until INTST is generated.

Figure 8-3. Asynchronous Serial Interface Transmission Completion Interrupt Timing



(3) Reception

When reception is enabled, sampling of the RXD pin is started, and reception of data begins when the start bit is detected. Each time one frame of data or character has been received, the reception completion interrupt (INTSR) occurs. Usually, the receive data is transferred from the receive buffer (RXB or RXBL) to memory by this interrupt processing.

(a) Reception enabled status

Reception is enabled when the RXE bits of the ASIM registers are set to 1.

RXE = 1: Reception is enabled

RXE = 0: Reception is disabled

However, to set the reception enabled status, set both the CTXE and CRXE bits of the clocked serial interface mode register (CSIM) to "0".

When reception is disabled, the receive hardware stands by in the initial status.

At this time, the reception completion interrupt/receive error interrupt does not occur, and the contents of the receive buffer are retained.

(b) Starting reception

Reception is started when the start bit is detected.

The RXD pin is sampled with the serial clock from baud rate generator. The RXD pin is sampled again eight clocks after the falling edge of the RXD pin has been detected. If the RXD pin is low at this time, it is recognized as the start bit, and reception is started. After that, the RXD pin is sampled in 16 clock ticks.

If the RXD pin is high eight clocks after the falling edge of the RXD pin has been detected, this falling edge is not recognized as the start bit. The serial clock counter is reinitialized, and the UART waits for the input of the next falling edge or valid start bit.

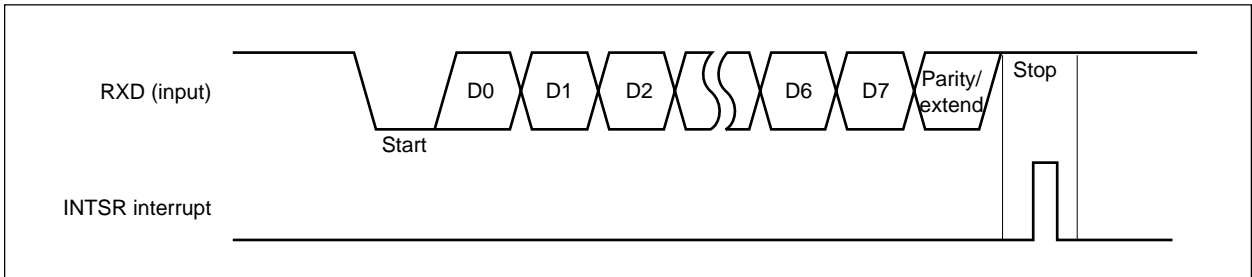
(c) Reception completion interrupt request

When one frame of data has been received with RXE = 1, the receive data in the shift register is transferred to RXB, and a reception completion interrupt request (INTSR) is generated.

If an error occurs, the receive data that contains an error is transferred to the receive buffer (RXB or RXBL), and the transmission completion interrupt (INTSR) and receive error interrupt (INTSER) occur simultaneously.

If the RXE bit is reset (0) during receive operation, the receive operation stops immediately. In this case, the contents of the receive buffer (RXB or RXBL) and the asynchronous serial interface status register (ASIS) do not change, and neither reception completion interrupt (INTSR) nor reception error interrupt (INTSER) is generated.

When RXE = 0 (reception disabled), no reception completion interrupt occurs.

Figure 8-4. Asynchronous Serial Interface Reception Completion Interrupt Timing**(d) Reception error flag**

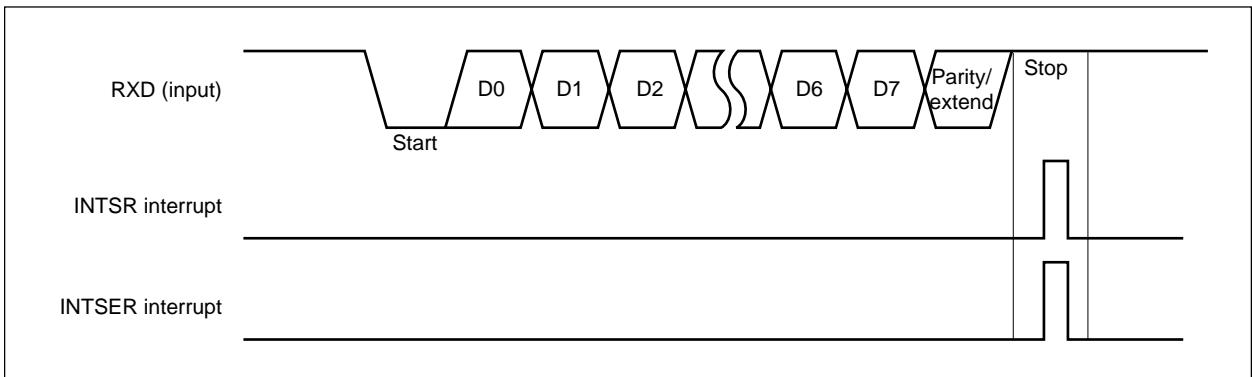
Three error flags, parity error, framing error, and overrun error flags, are related with the reception operation.

The receive error interrupt request occurs as a result of ORing these three error flags.

By reading the contents of the ASIS registers, the error which caused the receive error interrupt (INTSER) can be identified.

The contents of the ASIS registers are reset to 0 when the receive buffer (RXB or RXBL) is read or the next data frame is received (if the next data contains an error, the corresponding error flag is set).

Receive	Error Cause
Parity error	Parity specified during transmission does not coincide with parity of receive data
Framing error	Stop bit is not detected
Overrun error	Next data is completely received before data is read from receive buffer

Figure 8-5. Receive Error Timing

8.3 Clocked Serial Interface 0 to 3 (CSI0 to CSI3)

8.3.1 Features

- Number of channels: 4 channels (CSIn)
- ★ ○ High transfer speed CSI0, CSI2, CSI3: 8.25 Mbps max. ($\phi/4$ use, $\phi = 33$ MHz)
CSI1: 2.00 Mbps max.
- Half duplex communication
- Character length: 8 bits
- MSB first/LSB first selectable
- External serial clock input/internal serial clock output selectable
- 3 wires: SOn : serial data output
SIn : serial data input
SCKn : serial clock I/O
- Interrupt source: 4
 - Transmission/reception completion interrupt (INTCSIn)

Remark n = 0 to 3

ϕ : Internal system clock

8.3.2 Configuration

CSIn is controlled by the clocked serial interface mode register (CSIMn). The transmit/receive data is read/written from/to the serial I/O shift register (SIO_n) (n = 0 to 3).

(1) Clocked serial interface mode registers (CSIM0 to CSIM3)

CSIMn are 8-bit registers that specify the operation of CSIn.

(2) Serial I/O shift registers (SIO0 to SIO3)

SIO_n registers are 8-bit registers that convert serial data into parallel data, and vice versa. SIO_n are used for both transmission and reception.

Data is shifted in (received) or shifted out (transmitted) from the MSB or LSB side.

The actual transmitting and receiving of data is actually performed by writing data to and reading data from the SIO_n registers.

(3) Selector

Selects the serial clock to be used.

(4) Serial clock control circuit

Controls supply of the serial clock to the shift register. When the internal clock is used, it also controls the clock output to the SCKn pin.

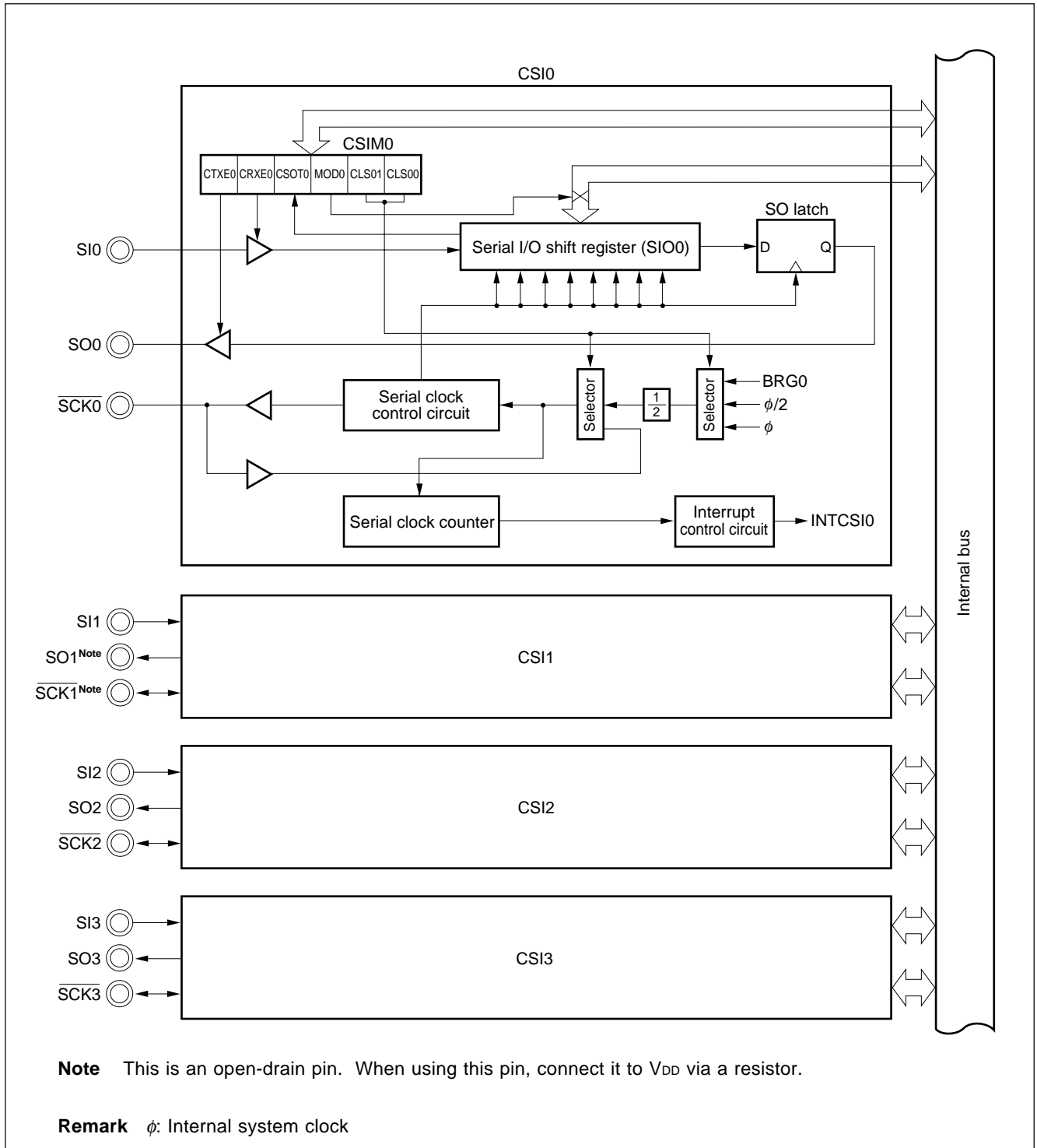
(5) Serial clock counter

Counts the serial clocks being output and the serial clocks received during transmission/reception to check whether 8-bit data has been transmitted or received.

(6) Interrupt control circuit

Controls whether an interrupt request is generated when the serial clock counter has counted eight serial clocks.

Figure 8-6. Block Diagram of Clocked Serial Interface



8.3.3 Control registers

(1) Clocked serial interface mode register 0 to 3 (CSIM0 to CSIM3)

These registers specify the basic operation mode of CSIn.

They can be read/written in 8- or 1-bit units (note, however, that bit 5 can only be read).

	7	6	5	4	3	2	1	0		
CSIM0	CTXE0	CRXE0	CSOT0	0	0	MOD0	CLS01	CLS00	Address FFFFF088H	After reset 00H
CSIM1	CTXE1	CRXE1	CSOT1	0	0	MOD1	CLS11	CLS10	Address FFFFF098H	After reset 00H
CSIM2	CTXE2	CRXE2	CSOT2	0	0	MOD2	CLS21	CLS20	Address FFFFF0A8H	After reset 00H
CSIM3	CTXE3	CRXE3	CSOT3	0	0	MOD3	CLS31	CLS30	Address FFFFF0B8H	After reset 00H

Bit Position	Bit Name	Function
7	CTXEn	CSI Transmit Enable Enables or disables transmission. 0 : Disables transmission 1 : Enables transmission When CTXEn = "0", both SOn and SIn pins go into high-impedance state.
6	CRXEn	CSI Receive Enable Disables or enables reception. 0 : Disables reception 1 : Enables reception If serial clock is received when both transmission is enabled (CTXEn = 1) and reception is disabled, "0" is input to shift register. If this bit is set to reception disabled status (CRXEn = 0) during receive operation, the contents of the SIO register become undefined.
5	CSOTn	CSI Status of Transmission Indicates that transfer operation is in progress. Set (1) : Transmission enable and start timing (writing to SIO0 register) Clear (0) : Transmission cleared and end timing (INTCSI occurs) This bit is used to check whether writing to serial I/O shift register (SIO) is permitted or not. Serial data transfer is started by enabling transmission (CTXEn = 1).
2	MODn	Mode Specifies operation mode. 0 : MSB first 1 : LSB first

Remark n = 0 to 3

Bit Position	Bit Name	Function																							
1, 0	CLS _n 1, CLS _n 0	Clock Source Specifies serial clock.																							
		<table><tr><th>CLS_n1</th><th>CLS_n0</th><th colspan="2">Specifies Serial Clock</th><th>SCK_n pin</th></tr><tr><td>0</td><td>0</td><td colspan="2">External clock</td><td>Input</td></tr><tr><td>0</td><td>1</td><td rowspan="3">Internal clock</td><td>Specified by BPRM_n register^{Note 1}</td><td>Output</td></tr><tr><td>1</td><td>0</td><td>$\phi/4$^{Note 2}</td><td>Output</td></tr><tr><td>1</td><td>1</td><td>$\phi/2$^{Note 2}</td><td>Output</td></tr></table>	CLS _n 1	CLS _n 0	Specifies Serial Clock		SCK _n pin	0	0	External clock		Input	0	1	Internal clock	Specified by BPRM _n register ^{Note 1}	Output	1	0	$\phi/4$ ^{Note 2}	Output	1	1	$\phi/2$ ^{Note 2}	Output
		CLS _n 1	CLS _n 0	Specifies Serial Clock		SCK _n pin																			
		0	0	External clock		Input																			
		0	1	Internal clock	Specified by BPRM _n register ^{Note 1}	Output																			
		1	0		$\phi/4$ ^{Note 2}	Output																			
		1	1		$\phi/2$ ^{Note 2}	Output																			
		Notes 1. For setting of BPRM _n register, refer to section 8.5 Baud Rate Generator 0 to 3 (BRG0 to BRG3) .																							
		2. $\phi/4$ and $\phi/2$ indicate dividing signals (ϕ : internal system clock).																							

Remark n = 0 to 3

Caution Set the CLS_n1 and CLS_n0 bits, in the transmission/reception disable state (CTXEn bit = CRXEn bit = 0). If these bits are set in a state other than transmission/reception disabled, normal operation is not guaranteed.

(2) Serial I/O shift register 0 to 3 (SIO0 to SIO3)

These registers convert 8-bit serial data into parallel data, and vice versa. The actual transmitting and receiving of data is performed by writing data to and reading data from the SIO_n registers.

A shift operation is performed when CTXE = "1" or CRXE = "1".

These registers can be read/written in 8- or 1-bit units.

SIO0	7	6	5	4	3	2	1	0		
	SIO07	SIO06	SIO05	SIO04	SIO03	SIO02	SIO01	SIO00	Address FFFFF08AH	After reset Undefined
SIO1										
	SIO17	SIO16	SIO15	SIO14	SIO13	SIO12	SIO11	SIO10	Address FFFFF09AH	After reset Undefined
SIO2										
	SIO27	SIO26	SIO25	SIO24	SIO23	SIO22	SIO21	SIO20	Address FFFFF0AAH	After reset Undefined
SIO3										
	SIO37	SIO36	SIO35	SIO34	SIO33	SIO32	SIO31	SIO30	Address FFFFF0BAH	After reset Undefined

Bit Position	Bit Name	Function
7 to 0	SIO _n 7 to SIO _n 0 (n = 0 to 3)	Serial I/O Data is shifted in (received) or out (transmitted) from MSB or LSB side.

8.3.4 Basic operation

(1) Transfer format

The CSI performs interfacing by using three lines: one clock line and two data lines.

Serial transfer is started by executing an instruction that writes transfer data to the SIO_n register.

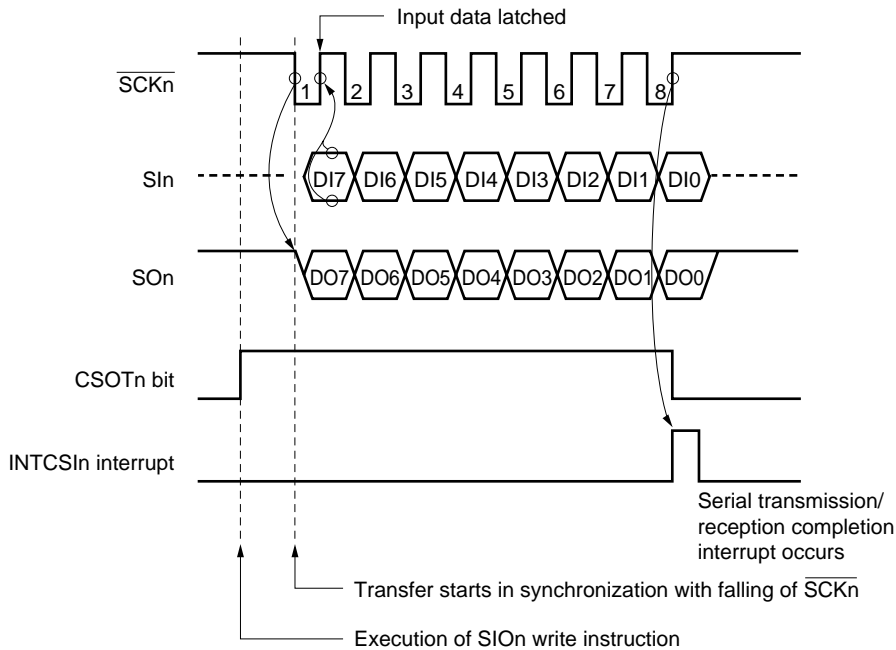
During transmission, the data is output from the SIO_n pin in synchronization with the falling edge of $\overline{\text{SCK}}_n$.

During reception, the data input to the SII_n pin is latched in synchronization with the rising edge of $\overline{\text{SCK}}_n$.

$\overline{\text{SCK}}_n$ stops when the serial clock counter overflows (at the rising edge of the 8th count), and $\overline{\text{SCK}}_n$ remains high until the next data transmission or reception is started. At the same time, a transmission/reception completion interrupt (INTCSI) is generated.

Caution If CTXE is changed from 0 to 1 after the transmit data is sent to the SIO_n registers, serial transfer will not begin.

Remark n = 0 to 3



Remark n = 0 to 3

(2) Enabling transmission/reception

Each CSIn has only one 8-bit shift register and does not have a buffer. Transmission and reception are therefore performed simultaneously.

(a) Transmission/reception enabling condition

The transmission/reception enabling condition of CSIn is specified by the CTXEn and CRXEn bits of the CSIMn register.

CTXEn	CRXEn	Transmission/Reception Operation
0	0	Transmission/reception disabled
0	1	Reception enabled
1	0	Transmission enabled
1	1	Transmission/reception enabled

Remark n = 0 to 3

- Remarks**
1. When CTXEn bit is 0, SOn pin output of CSIn becomes high impedance.
When CTXEn bit is 1, the data of the SIOOn register of CSIn is output.
 2. When CRXEn bit = 0, the shift register input is "0".
When CRXEn bit = 1, the serial input data is input to the shift register.
 3. To receive the transmit data and to check whether bus contention occurs, set CTXEn bit and CRXEn bit to 1.

(b) Starting transmission/reception

Transmission/reception is started by reading/writing the SIOOn registers. Transmission/reception is controlled by setting the transmission enable bit (CTXEn) and reception enable bit (CRXEn) as follows:

CTXEn	CRXEn	Start Condition
0	0	Does not start
0	1	Reads SIOOn registers
1	0	Writes SIOOn registers
1	1	Writes SIOOn registers
0	0 → 1	Rewrites CRXEn bits

Remark n = 0 to 3

In the above table, note that these bits should be set in advance of data transfer. For example, if the CTXEn bit is not changed from 0 to 1 before reading data from or writing data to the SIOOn registers, transfer will not begin. The bottom of the table means that, if the CRXEn bit is changed from 0 to 1 when the CTXEn bit is "0", the serial clock will be generated to initiate receive operation.

8.3.5 Transmission in CSI0 to CSI3

Transmission is started when data is written to the SIO_n register after transmission has been enabled by the clocked serial interface mode register (CSIM_n) ($n = 0$ to 3).

(1) Starting transmission

Transmission is started by writing the transmit data to the shift register (SIO_n) after the CTXE bit of the clocked serial interface mode registers (CSIM_n) has been set (the CRXE bit is cleared to "0").

If the CTXE bit is reset to 0, the SIO_n pin goes into a high-impedance state.

(2) Transmitting data in synchronization with serial clock

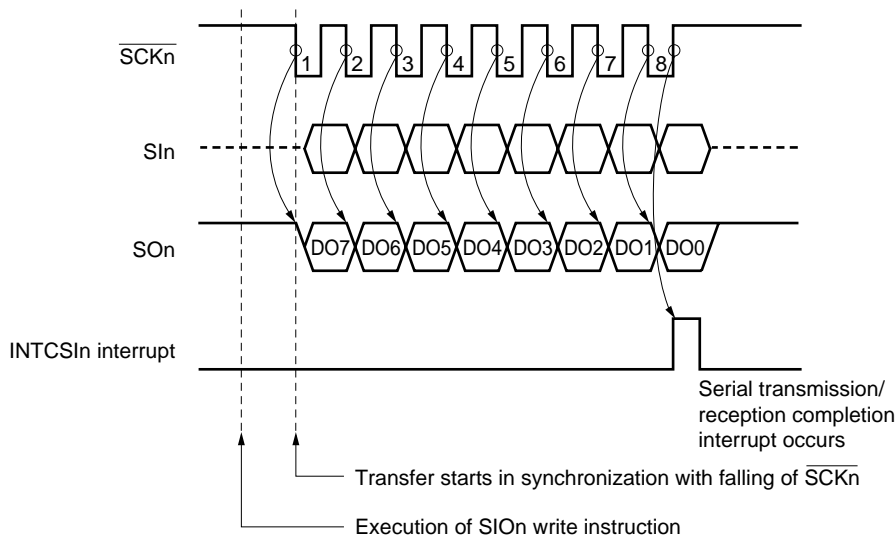
(a) When internal clock is selected as serial clock

When transmission is started, the serial clock is output from the $\overline{\text{SCKn}}$ pin, and at the same time, data is sequentially output to the SIO_n pin from SIO_n in synchronization with the falling edge of the serial clock.

(b) When external clock is selected as serial clock

When transmission is started, the data is sequentially output from SIO_n to the SIO_n pin in synchronization with the falling of the serial clock input to the $\overline{\text{SCKn}}$ pin immediately after transmission has been started. The shift operation is not performed even if the serial clock is input to the $\overline{\text{SCKn}}$ pin if transmission is not enabled, and the output level of the SIO_n pin will not change.

Figure 8-7. Timing of 3-Wire Serial I/O Mode (transmission)



Remark $n = 0$ to 3

8.3.6 Reception in CSI0 to CSI3

Reception is started if the status is changed from reception disabled to reception enabled status by the clocked serial interface mode registers (CSIMn) or if the SIO_n registers are read by the CPU with reception enabled (n = 0 to 3).

(1) Starting reception

Reception can be started in the following two ways:

- <1> Changing the status of the CRXEn bits of the CSIMn registers from "0" (reception disabled) to "1" (reception enabled)
- <2> Reading the receive data from the shift registers (SIO_n) when the CRXEn bits of the CSIMn registers are "1" (reception enabled)

If CRXEn bit of the CSIMn register has already been set to "1", writing "1" to these bits do not initiate receive operation. When bit CRXEn = 0, the shift register inputs are "0".

(2) Receiving data in synchronization with serial clock

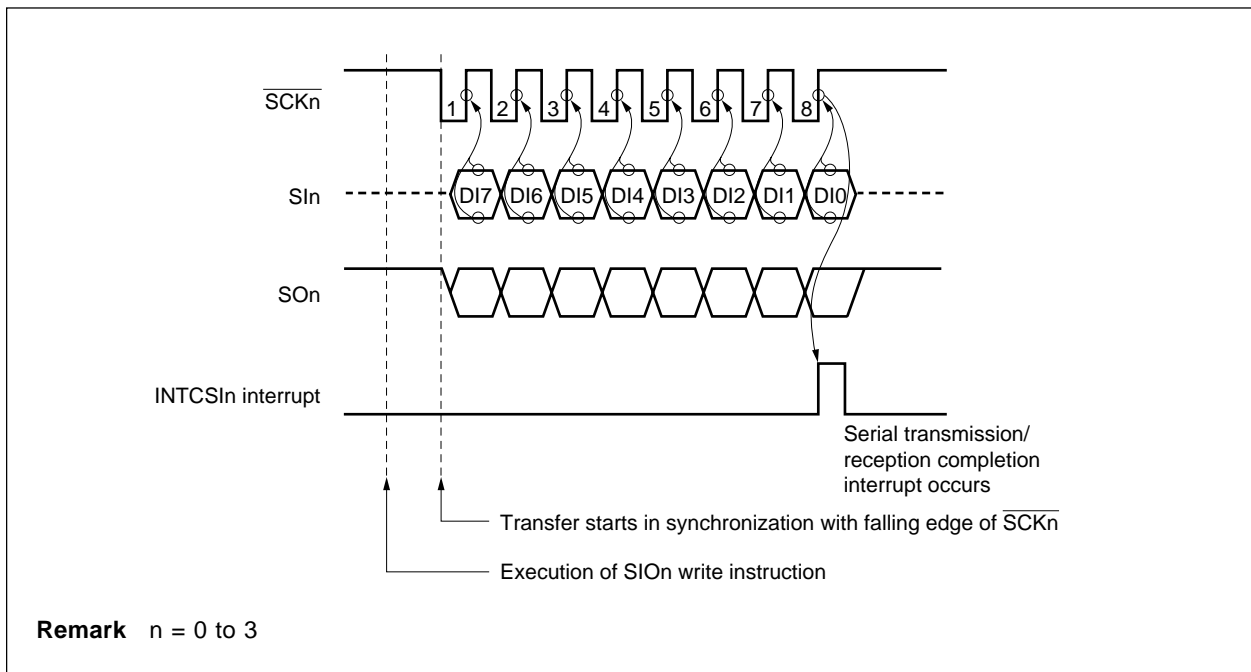
(a) When internal clock is selected as serial clock

When reception is started, the serial clock is output from the $\overline{\text{SCKn}}$ pin, and at the same time, data is sequentially loaded from the SIn pin to SIO_n in synchronization with the rising edge of the serial clock.

(b) When external clock is selected as serial clock

When reception is started, the data is sequentially loaded from the SIn pin to SIO_n in synchronization with the rising of the serial clock input to the $\overline{\text{SCKn}}$ pin immediately after reception has been started. The shift operation is not performed even if the serial clock is input to the $\overline{\text{SCKn}}$ pin when reception is not enabled.

Figure 8-8. Timing of 3-Wire Serial I/O Mode (reception)



8.3.7 Transmission/reception in CSI0 to CSI3

Transmission and reception can be executed simultaneously if both transmission and reception are enabled by the clocked serial interface mode registers (CSIMn) (n = 0 to 3).

(1) Starting transmission/reception

Transmission and reception can be performed simultaneously (transmission/reception operation) when both the CTXEn and CRXEn bits of the clocked serial interface mode registers (CSIMn) are set to 1.

Transmission/reception can be started by writing the transmit data to the shift register n (SIO_n) when both the CTXEn and CRXEn bits of the CSIMn register are "1" (transmission/reception enabled state)

If CRXEn bit of the CSIMn register has already been set to "1", writing "1" to this bit does not initiate transmit/receive operation.

(2) Transmitting data in synchronization with serial clock

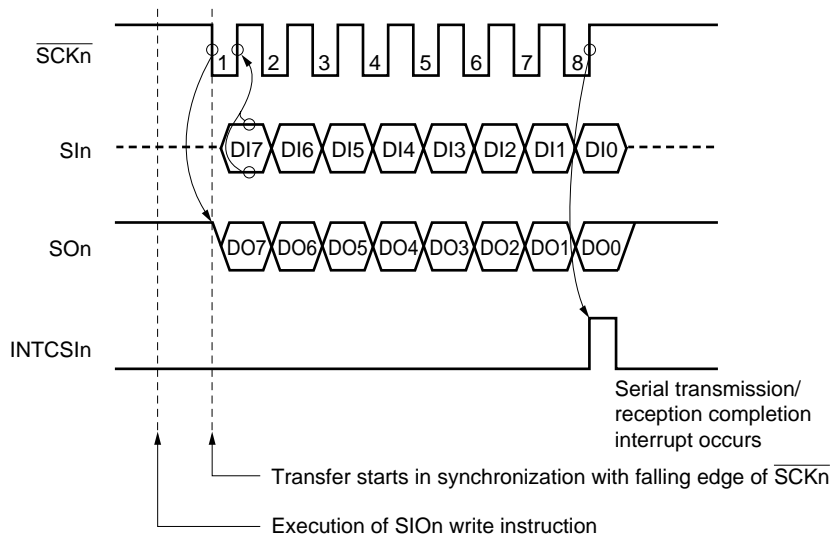
(a) When internal clock is selected as serial clock

When transmission/reception is started, the serial clock is output from the $\overline{\text{SCKn}}$ pin, and at the same time, data is sequentially set to the SOn pin from SIO_n in synchronization with the falling edge of the serial clock. Simultaneously, the data of the SIn pin is sequentially loaded to SIO_n in synchronization with the rising edge of the serial clock.

(b) When external clock is selected as serial clock

When transmission/reception is started, the data is sequentially output from SIO_n to the SOn pin in synchronization with the falling edge of the serial clock input to the $\overline{\text{SCKn}}$ pin immediately after transmission/reception has been started. The data of the SIn pin is sequentially loaded to SIO_n in synchronization with the rising edge of the serial clock. The shift operation is not performed even if the serial clock is input to the $\overline{\text{SCKn}}$ pin when transmission/reception is not enabled, and the output level of the SOn pin does not change.

Figure 8-9. Timing of 3-Wire Serial I/O Mode (transmission/reception)



Remark $n = 0$ to 3

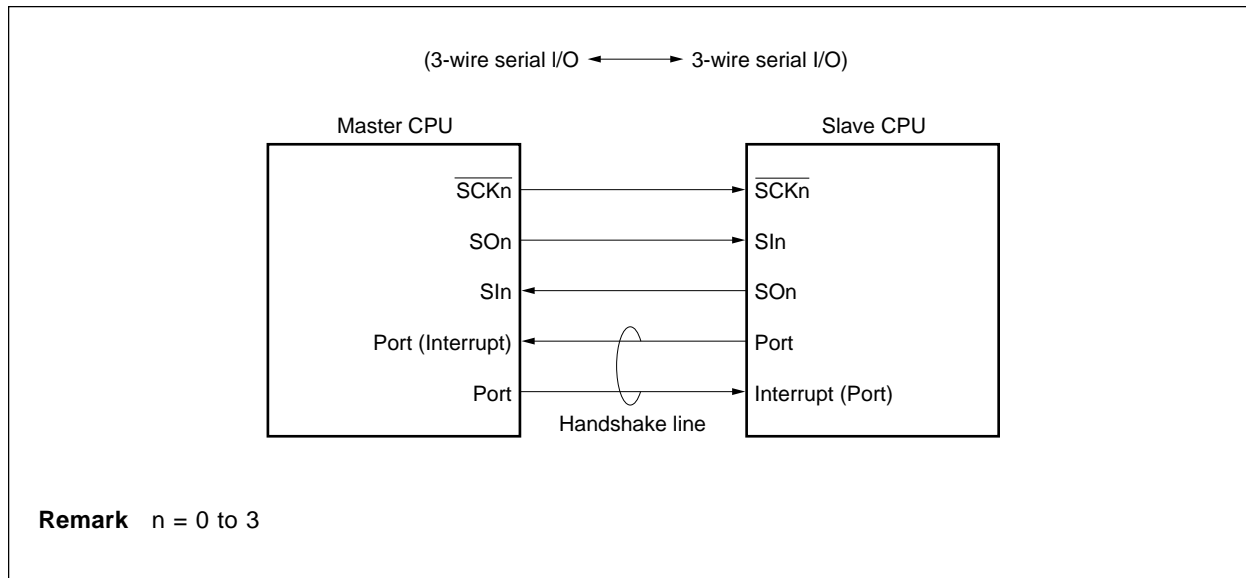
8.3.8 System configuration example

Data 8 bits long is transferred by using three types of signal lines: serial clock ($\overline{\text{SCKn}}$), serial input (SIn), and serial output (SOn). This feature is effective for connecting peripheral I/Os and display controllers that have a conventional clocked serial interface.

To connect two or more devices, a handshake line is necessary.

Various devices can be connected, because it can be specified whether the data is transmitted starting from the MSB or LSB.

Figure 8-10. Example of CSI System Configuration



8.4 I²C Bus (μ PD703008Y and 70F3008Y only)

8.4.1 Features

- ☐ I²C bus format
- ☐ Multi-master serial bus
- ☐ Serial data automatic discrimination function
 - Transfer speed: standard mode : 100 Kbps max.
 - high-speed mode : 400 Kbps max.
- ☐ Chip select by address
- ☐ Wake-up function
- ☐ Acknowledge signal ($\overline{\text{ACK}}$) control function
- ☐ Wait signal ($\overline{\text{WAIT}}$) control function
- ☐ Arbitration control function
- ☐ Conflict detection function

8.4.2 Functions

The following two modes are available for I²C bus.

- Operation stop mode
- I²C (Inter IC) bus mode (supports multi-master)

(1) Operation stop mode

Used when serial transfer is not carried out, reduces power consumption.

(2) I²C bus mode (supports multi-master)

Performs 8-bit data transfer with more than one device, using two lines, each for the serial clock (SCL) and the serial data bus (SDA).

Conforming to I²C bus format, either “start condition”, “data”, or “stop condition” can be output onto serial data bus in transmission. These data can be automatically detected by hardware in reception.

Because SCL and SDA are open drain outputs, pull-up resistors are required for the serial clock line and the serial data bus line.

Figure 8-11. Example of Serial Bus Configuration Using I²C Bus

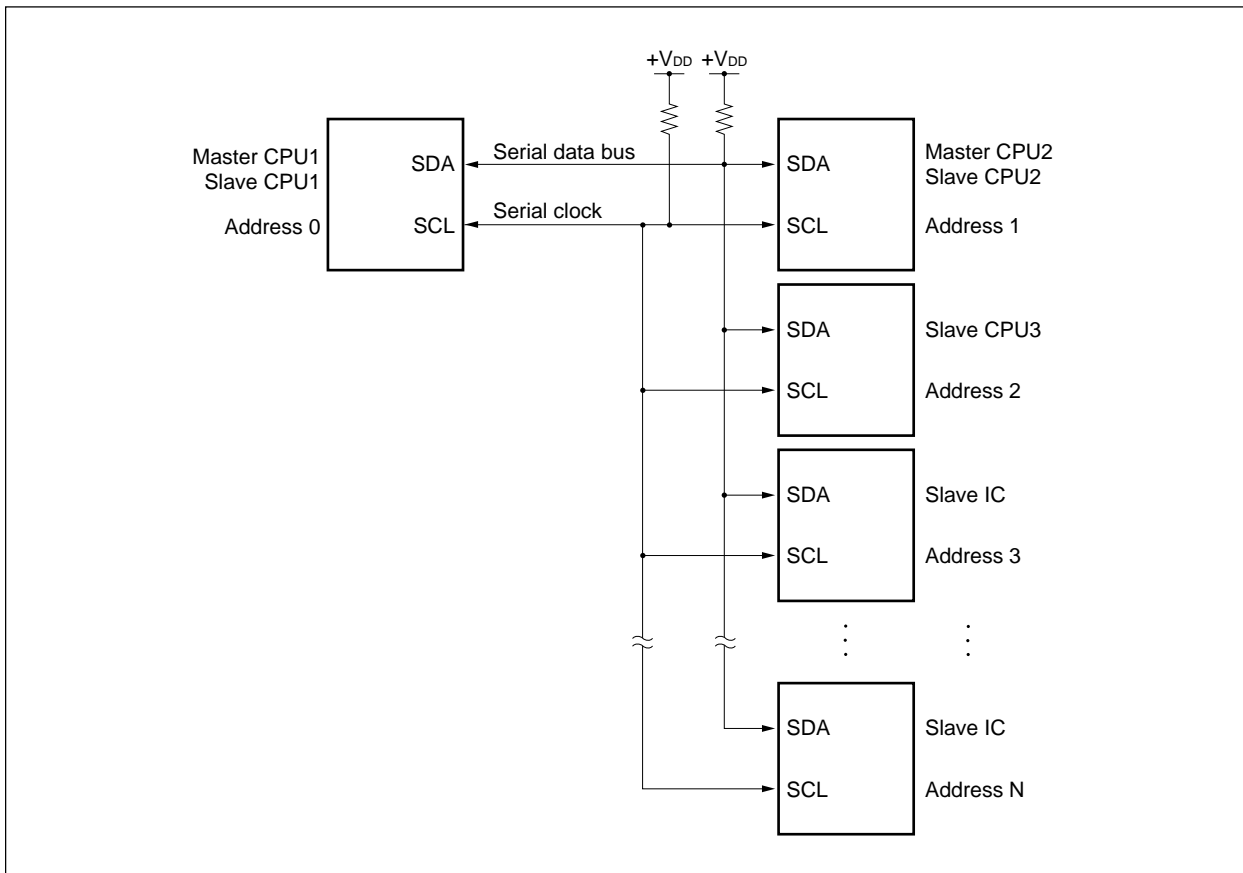
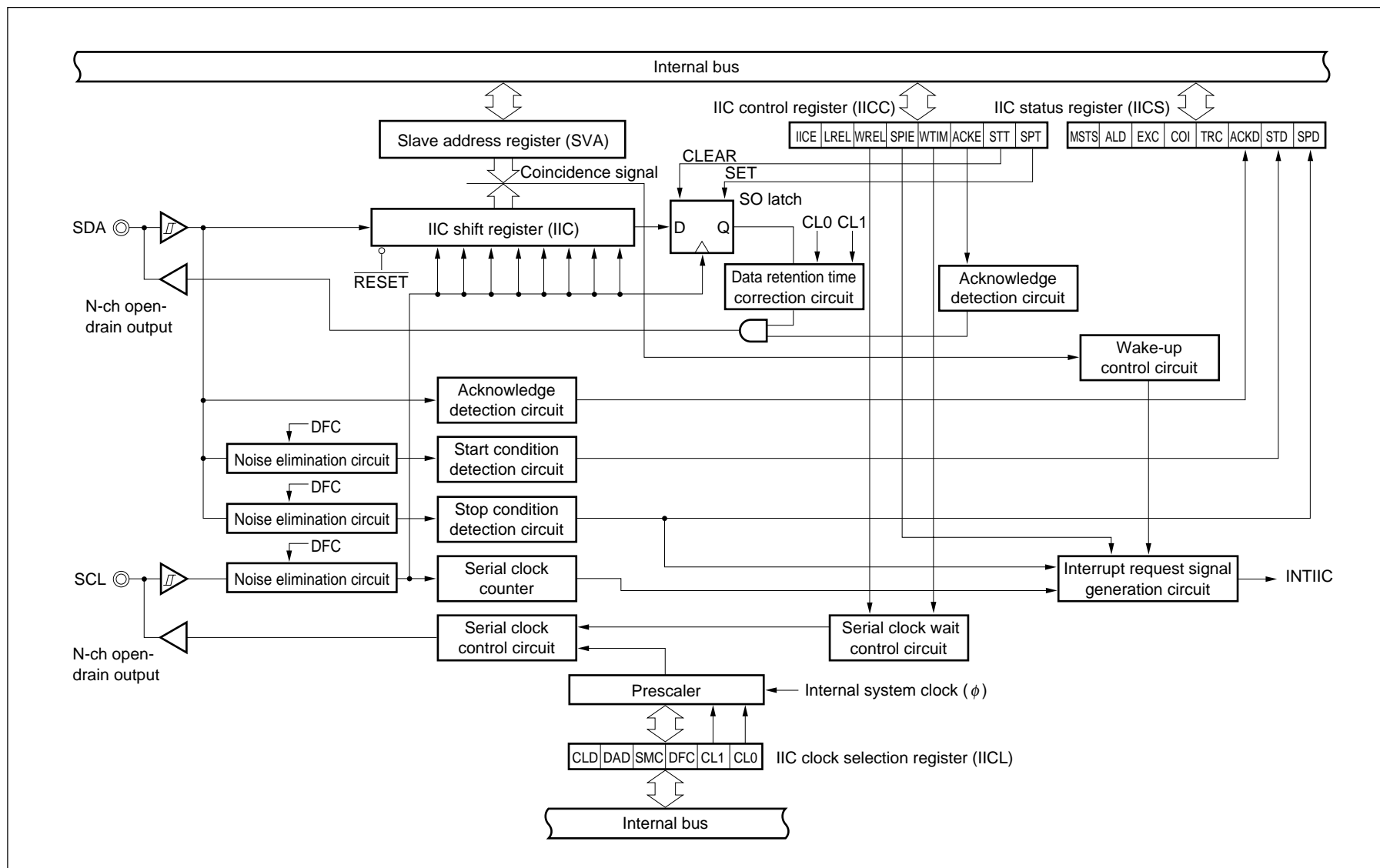


Figure 8-12. Block Diagram of I²C Bus

8.4.3 Configuration

The I²C bus is configured with the following hardware.

Table 8-2. I²C Bus Configuration

Item	Configuration
Register	IIC shift register (IIC) Slave address register (SVA)
Control register	IIC clock selection register (IICCL) IIC status register (IICS) IIC control register (IICC)

(1) IIC shift register (IIC)

IIC is a register that converts 8-bit serial data into parallel data, and vice versa. IIC is used both for transmission and reception.

The actual transmission and reception of data is performed by writing data to and reading data from the IIC shift register.

This register is set by 8-bit memory manipulation instruction. It becomes 00H by $\overline{\text{RESET}}$ input.

(2) Slave address register (SVA)

SVA is a register that sets the local address with 8-bit memory manipulation instruction when used as a slave. It becomes 00H by $\overline{\text{RESET}}$ input.

(3) SO latch

Retains SDA pin output level.

(4) Wake-up control circuit

Generates interrupt requests when the address value set in the slave address register (SVA) and the reception address coincide or when an extension code is received.

(5) Clock selector

Selects the sampling clock to be used.

(6) Serial clock counter

Counts the serial clocks to be output or input in transmission/reception and checks whether 8-bit data has been transmitted/received.

(7) Interrupt request signal generation circuit

Controls generation of interrupt request signals.

I²C interrupt is generated by the following two triggers.

- The eighth or the ninth count of the serial clock (set by WTIM bit^{Note}).
- The generation of an interrupt by the stop condition detection (set by SPIE bit^{Note}).

Note WTIM bit : bit 3 of IIC control register (IICC)
SPIE bit : bit 4 of IIC control register (IICC)

(8) Serial clock control circuit

Generates clocks to be output to SCL pin from the sampling clock in the master mode.

(9) Serial clock wait control circuit

Controls wait timings.

(10) Acknowledge output circuit, stop condition detection circuit, start condition detection circuit, acknowledge detection circuit

Performs output and detection of various control signals.

(11) Data retention time correction circuit

Generates data retention time for the fall of the serial clock.

8.4.4 Serial interface control register

I²C bus is controlled by the following three registers.

- IIC control register (IICC)
- IIC status register (IICS)
- IIC clock selection register (IICCL)

The following registers are also used.

- IIC shift register (IIC)
- Slave address register (SVA)

(1) IIC control register (IICC)

This register performs enabling/disabling I²C operation, setting of wait timing, and other settings of I²C operation.

This register is set by 1- or 8-bit memory manipulation instruction.

It becomes 00H by RESET input.

IICC	7	6	5	4	3	2	1	0	Address FFFFF0E0H	After reset 00H
	IICE	LREL	WREL	SPIE	WTIM	ACKE	STT	SPT		

Bit Position	Bit Name	Function
7	IICE	<p>I²C Enable</p> <p>Enables or disables I²C operation. The data in IICC is not cleared.</p> <p>0 : Disables I²C operation. Presets I²C status register (IICS) and disables internal operation.</p> <p>1 : Enables I²C operation</p> <p>Set condition : Instruction</p> <p>Clear condition : Instruction, reset input</p>
6	LREL	<p>Line Release</p> <p>Exits from the communication in progress, releases the bus, and waits for the start of the next communication.</p> <p>0 : Normal operation</p> <p>1 : Exits from communication and enters wait status</p> <p>This bit is used when an extension code not related to the local register is received. SCL and SDA lines go into high-impedance status. The following flags are cleared.</p> <p>EXC, ACKD, COI, MSTs, TRC, STD</p> <p>Set condition : Instruction</p> <p>Clear condition : Reset input, or automatically cleared after execution.</p>
5	WREL	<p>Wait Release</p> <p>Selects whether releasing wait or not.</p> <p>0 : Does not release wait</p> <p>1 : Releases wait</p> <p>Set condition : Instruction</p> <p>Clear condition : Reset input, or automatically cleared after execution.</p> <p>Caution If wait is released when TRC = 1 and WREL are set to the ninth clock, TRC is cleared and SDA line goes into high impedance status.</p>
4	SPIE	<p>Stop Condition Interrupt Enable</p> <p>Disable or enables generation of INTIIC interrupt request by stop condition detection.</p> <p>0 : Disables</p> <p>1 : Enables</p> <p>Set condition : Instruction</p> <p>Clear condition : Instruction, reset input</p>

Bit Position	Bit Name	Function
3	WTIM	<p>Wait Timing Controls generation of wait and interrupt request.</p> <p>0 : Interrupt request generates at the fall of the eighth clock For master : Waits keeping clock output in low level after outputting eight clocks For slave : Waits for master setting clock output in low level after inputting eight clocks</p> <p>1 : Interrupt request generates at the fall of the ninth clock For master : Waits keeping clock output in low level after outputting nine clocks For slave : Waits for master setting clock output in low level after inputting nine clocks</p> <p>The setting of this bit becomes invalid while transferring address. When EXC = 1, wait is compulsorily inserted at the eighth clock, and when COI = 1, wait is compulsorily inserted at the ninth clock, and then the setting of this bit becomes valid. For master, wait is inserted at the ninth clock while transferring address. The slave which has received the local address enters wait status at the fall of the ninth clock after the generation of acknowledge.</p> <p>Set condition : Instruction Clear condition : Instruction, reset input</p>
2	ACKE	<p>Acknowledge Enable Controls acknowledge.</p> <p>0 : Disables acknowledge 1 : Enables automatic acknowledge output. SDA line becomes low level during the 9-clock period. However, it is invalid while transferring address and valid when EXC = 1.</p> <p>Set condition : Instruction Clear condition : Instruction, reset input</p>
1	STT	<p>Start Condition Trigger Selects whether generating start condition or not.</p> <p>0 : Does not generate start condition 1 : Generates start condition</p> <p>When bus is released (stop status): generates start condition by changing SDA line from high-level to low-level (starts up as master). And then, secures specification time and sets SCL to low level.</p> <p>When not joining bus (STT is set after STD =1 is set): this bit functions as a start condition reservation flag. When this bit is set, it automatically generates start condition after bus is released.</p> <p>Set condition : Instruction Clear condition : Instruction, reset input, when start condition is detected for master, (MSTS = 1 and STD = 1), or when defeated in arbitration.</p>
0	SPT	<p>Stop Condition Trigger Selects whether generating stop condition or not.</p> <p>If this bit is set in the early stage of communication, it outputs low-level to SDA line and generates stop condition.</p> <p>0 : Does not generate stop condition 1 : Generates stop condition</p> <p>Sets SCL line to high level after setting SDA line to low level, or waits SCL becomes high level. And then, it secures specification time, changes SDA line from low level to high level, and generates stop condition.</p> <p>Set condition : Instruction Clear condition : Instruction, reset input, when stop condition is detected, or when defeated in arbitration.</p>

Caution When performing transmission/reception of master between enabling operation (IICE = 1) and the first stop condition detection, generate a stop condition once by setting the SPT bit.

(2) IIC status register (IICS)

IIC status register indicates the I²C status.

This register is set by 1- or 8-bit memory manipulation instruction. It can only be read.

It becomes 00H by $\overline{\text{RESET}}$ input.

	7	6	5	4	3	2	1	0	Address	After reset
IICS	MSTS	ALD	EXC	COI	TRC	ACKD	STD	SPD	FFFFF0E2H	00H

Bit Position	Bit Name	Function
7	MSTS	<p>Master Status Indicates master status. 0 : Slave status or communication wait status 1 : Master status</p> <p>Set condition : Start condition generation Clear condition : Stop condition detection, ALD = 1, LREL = 1, IICE = 1 -> 0, or reset input</p>
6	ALD	<p>Arbitration Defeat Detects arbitration defeat. 0 : Arbitration has not occurred, or win in arbitration 1 : Defeat in arbitration. MSTS flag is cleared.</p> <p>Set condition : Arbitration defeat Clear condition : IICE = 0, reset input, or after IICS read. A bit manipulation instruction is executed to another bit of the IICS register.</p>
5	EXC	<p>Extension Code Indicates reception of extension code. 0 : Extension code is not received 1 : Extension code is received</p> <p>Set condition : The higher 4 bits of the received address are 0000 or 1111 (set at the rise of the eighth clock). Clear condition : Start condition detection, stop condition detection, LREL= 1, IICE = 0, or reset input</p>
4	COI	<p>Coincident Address Indicates coincidence of received address and local address. 0 : Addresses do not coincide 1 : Addresses coincide</p> <p>Set condition : Coincidence of received address and local address (SVA) (set at the rise of the eighth clock) Clear condition : Start condition detection, LREL = 1, IICE = 0, or reset input</p>

Bit Position	Bit Name	Function
3	TRC	<p>Transmit/Receive Condition Indicates current communication status.</p> <p>0 : Receiving status (status other than transmitting status). SDA line goes into high-impedance state.</p> <p>1 : Transmitting status. The value of SO latch can be output to SDA line (valid after the fall of the ninth clock of the first byte).</p> <p>Set condition : Start condition generation (STD = 1 and MSTs = 1) for master. 1 is input to the LSB (transfer direction specification bit) of the first byte for slave.</p> <p>Clear condition : LREL = 1, IICE = 0, ALD = 1, reset input, stop condition detection. 1 is output to the LSB (transfer direction specification bit) of the first byte for master.</p> <p>Start condition detection (STD = 1 and MSTs = 0) for slave when not joining communication.</p>
2	ACKD	<p>Acknowledge Detected Indicates detection of acknowledge signal.</p> <p>0 : Not detected 1 : Detected</p> <p>Set condition : SDA line becomes low-level at the rise of the ninth clock of SCL.</p> <p>Clear condition : LREL = 1, the rise of the first clock of the next byte, stop condition detection, IICE = 0, or reset input</p>
1	STD	<p>Start Condition Detected Indicates detection of start condition.</p> <p>0 : Start condition not detected 1 : Start condition detected. Indicates address transfer period.</p> <p>Set condition : Start condition detection</p> <p>Clear condition : Stop condition detection, LREL = 1, the rise of the first clock of the byte following the address transfer period, IICE = 0, or reset input</p>
0	SPD	<p>Stop Condition Detected Indicates detection of stop condition.</p> <p>0 : Stop condition not detected 1 : Stop condition detected. Communication in the master ends. Bus is released.</p> <p>Set condition : Stop condition detection</p> <p>Clear condition : The rise of the first clock of the address transfer byte after start condition detection and after setting this bit, IICE = 0, or reset input. Cleared with clock input even without start condition.</p>

(3) IIC clock selection register (IICCL)

IICCL is a register that sets the transfer clock of I²C.

This register is set by 1- or 8-bit memory manipulation instruction.

It becomes 00H by $\overline{\text{RESET}}$ input.

	7	6	5	4	3	2	1	0		
IICCL	0	0	CLD ^{Note}	DAD ^{Note}	SMC	DFC	CL1	CL0	Address FFFFF0E4H	After reset 00H

Bit Position	Bit Name	Function																																																	
5	CLD	SCL Level Detected Indicates SCL line level detection result. Valid only when IICE = 1. 0 : SCL line is low level. 1 : SCL line is high level.																																																	
4	DAD	SDA Level Detected Indicates the SDA line level detection result. Valid only when IICE = 1. 0 : SDA line is low level. 1 : SDA line is high level.																																																	
3	SMC	Speed Mode Control Switches operation mode. 0 : Standard mode 1 : High-speed mode																																																	
2	DFC	Digital Filter Condition Enables or disables digital filter operation. 0 : OFF 1 : ON Digital filter can be used in high-speed mode. The response becomes slow when digital filter is used.																																																	
1, 0	CL1, CL0	Clock Selects internal clock according to the system clock. <table><tr><th rowspan="3">CL1</th><th rowspan="3">CL0</th><th colspan="3">Standard Mode</th><th colspan="3">High-speed Mode</th></tr><tr><th colspan="2">Transfer clock</th><th rowspan="2"></th><th colspan="2">Transfer clock</th></tr><tr><th>DFC=0</th><th>DFC=1</th><th>DFC=0</th><th>DFC=1</th></tr><tr><td>0</td><td>0</td><td>ϕ = 4.0 to 8.0 MHz</td><td>$\phi/88$</td><td>$\phi/92$</td><td>ϕ = 8.0 to 16.0 MHz</td><td>$\phi/48$</td><td>$\phi/48$</td></tr><tr><td>0</td><td>1</td><td>ϕ = 10.0 to 16.0 MHz</td><td>$\phi/172$</td><td>$\phi/176$</td><td>ϕ = 8.0 to 16.0 MHz</td><td>$\phi/48$</td><td>$\phi/48$</td></tr><tr><td>1</td><td>0</td><td>ϕ = 16.0 to 33.0 MHz</td><td>$\phi/344$</td><td>$\phi/352$</td><td>ϕ = 16.0 to 33.0 MHz</td><td>$\phi/96$</td><td>$\phi/96$</td></tr><tr><td>1</td><td>1</td><td>Setting prohibited</td><td>—</td><td>—</td><td>Setting prohibited</td><td>—</td><td>—</td></tr></table> Remark ϕ : Internal system clock	CL1	CL0	Standard Mode			High-speed Mode			Transfer clock			Transfer clock		DFC=0	DFC=1	DFC=0	DFC=1	0	0	ϕ = 4.0 to 8.0 MHz	$\phi/88$	$\phi/92$	ϕ = 8.0 to 16.0 MHz	$\phi/48$	$\phi/48$	0	1	ϕ = 10.0 to 16.0 MHz	$\phi/172$	$\phi/176$	ϕ = 8.0 to 16.0 MHz	$\phi/48$	$\phi/48$	1	0	ϕ = 16.0 to 33.0 MHz	$\phi/344$	$\phi/352$	ϕ = 16.0 to 33.0 MHz	$\phi/96$	$\phi/96$	1	1	Setting prohibited	—	—	Setting prohibited	—	—
CL1	CL0	Standard Mode			High-speed Mode																																														
		Transfer clock				Transfer clock																																													
		DFC=0	DFC=1	DFC=0		DFC=1																																													
0	0	ϕ = 4.0 to 8.0 MHz	$\phi/88$	$\phi/92$	ϕ = 8.0 to 16.0 MHz	$\phi/48$	$\phi/48$																																												
0	1	ϕ = 10.0 to 16.0 MHz	$\phi/172$	$\phi/176$	ϕ = 8.0 to 16.0 MHz	$\phi/48$	$\phi/48$																																												
1	0	ϕ = 16.0 to 33.0 MHz	$\phi/344$	$\phi/352$	ϕ = 16.0 to 33.0 MHz	$\phi/96$	$\phi/96$																																												
1	1	Setting prohibited	—	—	Setting prohibited	—	—																																												

★

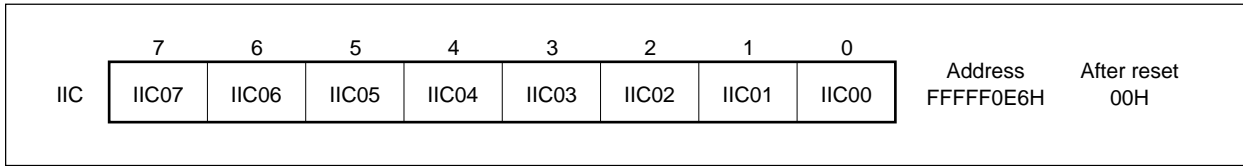
Note Bit 4 and bit 5 are Read Only bits.

(4) IIC shift register (IIC)

IIC shift register performs serial transmission/reception (shift operation) in synchronization with the serial clock.

This register can be read/written in 8-/1-bit units. However, do not write data to IIC register during data transfer.

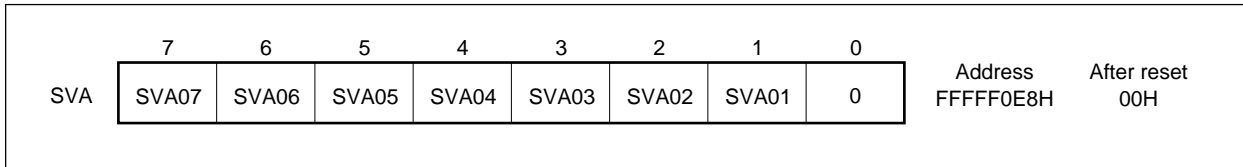
- ★ **Caution** In operations during restart, carry out writing of address data to the IIC shift register after the start conditions trigger is cleared and the start conditions are detected.



(5) Slave address register (SVA)

Slave address register stores slave address of I²C bus.

This register can be read/written in 8-/1-bit units. However, bit 0 is fixed to 0.



8.4.5 I²C bus functions

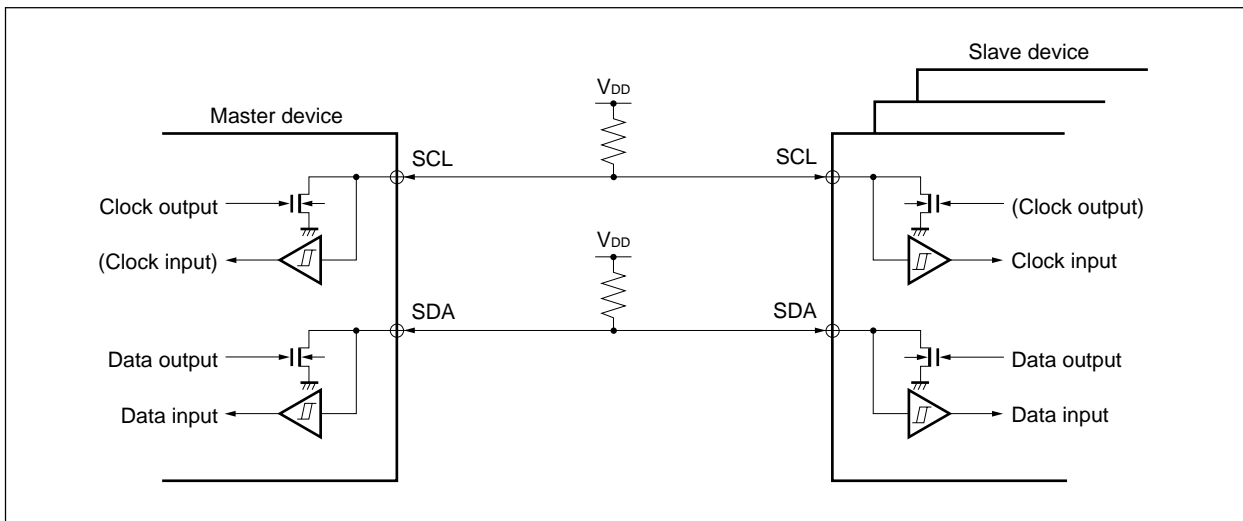
(1) Pin configuration

The configuration of the serial clock pin (SCL) and the serial data bus pin (SDA) is as follows.

- (a) SCL Pin to input/output serial clock
Output is N-ch open drain both for master and slave. Input is Schmitt input.
- (b) SDA I/O multiplexed pin for serial data
Output is N-ch open drain both for master and slave. Input is Schmitt input.

Because the outputs of serial clock line and the serial data bus line are N-ch open drain, external reset pull-up resistors are required.

Figure 8-13. Pin Configuration

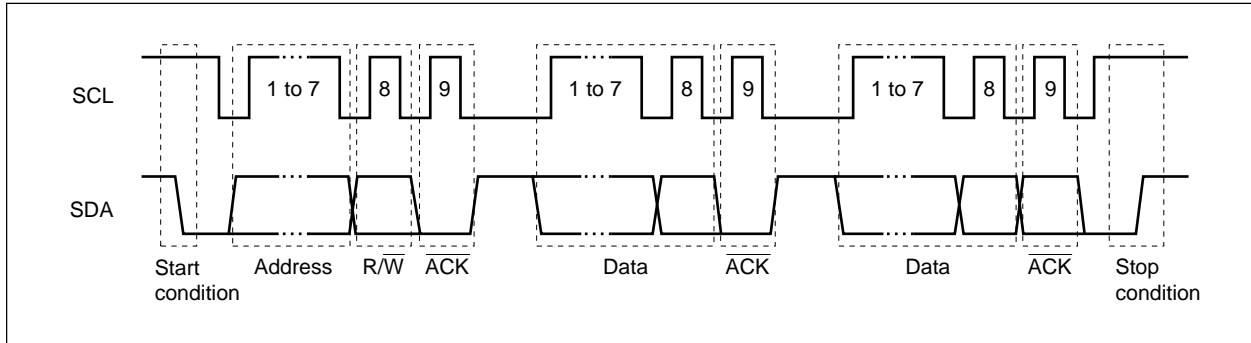


8.4.6 Definition and controls of I²C bus

The serial data communication format of I²C bus and the signals used are explained below.

Figure 8-14 shows each transfer timing of “start condition”, “data”, and “stop condition”, which are output onto the serial data bus of I²C bus.

Figure 8-14. Serial Data Transfer Timing of I²C Bus



Start condition, slave address, and stop condition are output from the master.

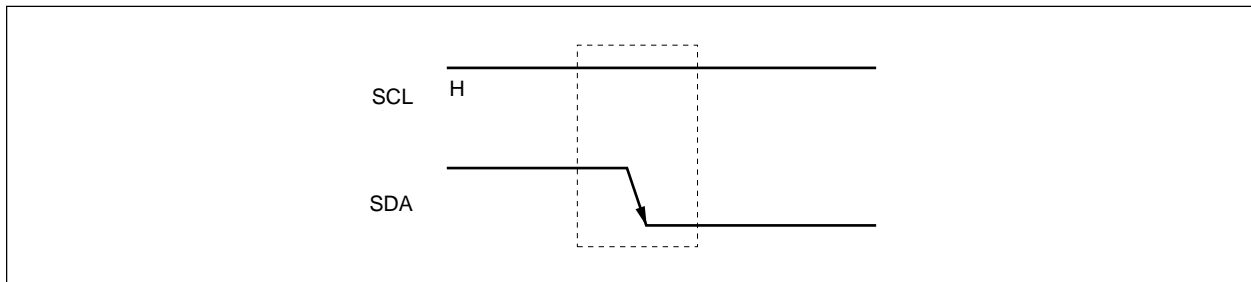
The acknowledge signal ($\overline{\text{ACK}}$) is output either from the master or the slave (normally, it is output from the reception side of 8-bit data)

The serial clock (SCL) is kept being output from the master. However, the slave can extend the low level period of SCL and insert wait.

(1) Start condition

The start condition is generated when the SDA pin changes from high level to low level while the SCL pin is high level. The start condition of the SCL pin and the SDA pin is a signal which is the master outputs to the slave when a serial transfer starts. The slave is provided with the hardware to detect the start condition.

Figure 8-15. Start Condition



Start condition is output by setting (1) the STT bit of the IICC register in the stop condition detection status (the SPD bit of the IICS register = 1). When the start condition is detected, the STD bit of the IICS register is set (1).

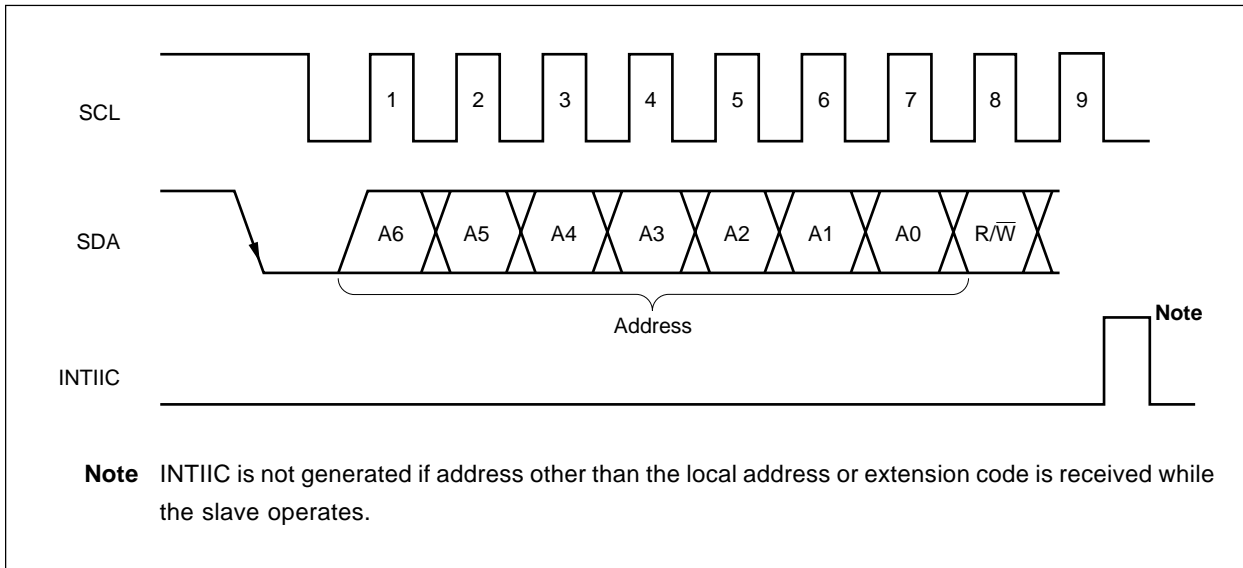
(2) Address

The 7-bit data following the start condition is defined as an address.

The address is an 7-bit data which the master outputs to select a specific slave from the two or more slaves connected to the bus line. Therefore, the slaves on the bus line must be assigned different addresses.

The slave detects this condition by hardware, and, in addition, checks if the 7-bit data coincides with the slave address register (SVA). When the 7-bit data and the value of SVA coincide, a slave is selected, and the slave performs communication with the master until the master transmits a start or stop condition.

Figure 8-16. Address



The address is output when the 8-bit address consisting of the slave address and the transfer direction explained in (3) Transfer direction specification are written to the shift register (IIC). The received address is written to IIC.

The slave address is assigned to the higher 7 bits of IIC.

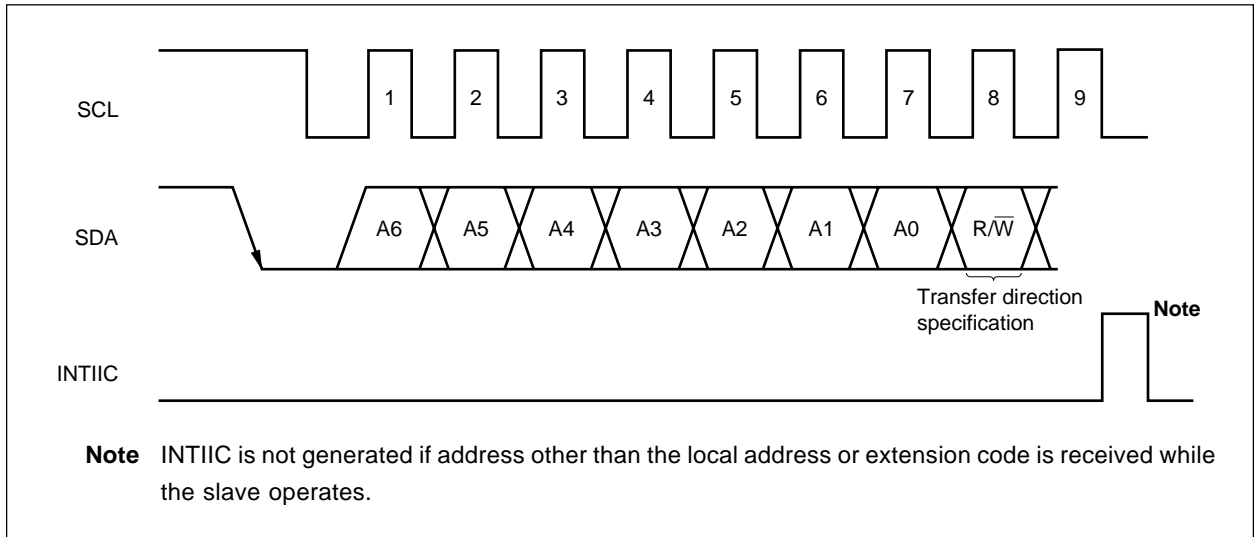
(3) Transfer direction specification

The master transmits 1-bit data because it specifies the transmit direction following the 7-bit address.

When the transmit direction specification bit is 0, the master transmits data to the slave.

When the transmit direction specification bit is 1, the master receives data from the slave.

Figure 8-17. Transfer Direction Specification



(4) Acknowledge signal ($\overline{\text{ACK}}$)

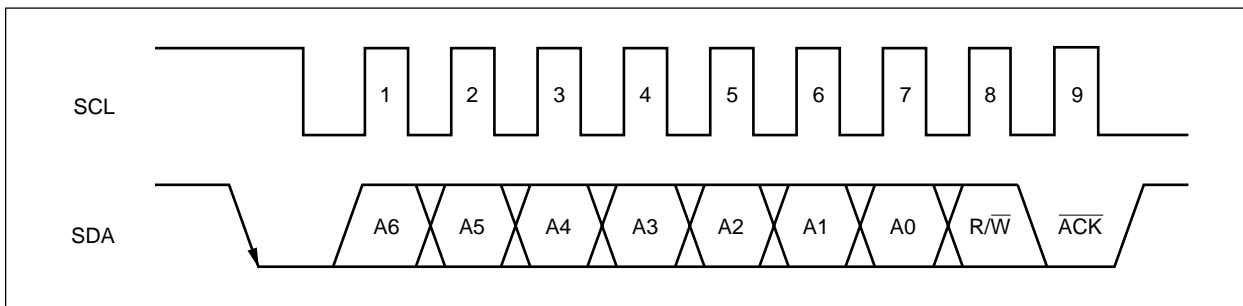
The acknowledge signal is a signal for checking serial data reception in the transmit and receive sides. The receive side sends back the acknowledge signal each time it receives an 8-bit data. The transmit side receives the acknowledge signal after transmitting the 8-bit data. However, in the case the master is the receive side, no acknowledge signal is output if the master receives the final data. The transmit side detects whether the receive side has sent the acknowledge signal back to the transmit side after transmitting 8 bits. If the acknowledge signal is sent back, the transmit side continues processing considering that reception has been performed correctly. If the slave does not send back the acknowledge signal, the reception has not been performed correctly. Therefore, the master outputs a stop condition or restart condition and aborts the transmission. If the acknowledge signal is not sent back, the following two factors can be considered.

- <1> The receptions has not been performed correctly.
- <2> The final data has been received.

When the receive side sets the SDA line to low level at the ninth clock, the acknowledge signal ($\overline{\text{ACK}}$) becomes active (normal reception response).

When ACKE of the IICC register = 1, the acknowledge signal automatic generation enable status is set. The TRC bit of the IICS register is set according to the data of the eighth bit following the 7-bit address information. However, when the value of the TRC bit is 0, set ACKE = 1, because it is receive status. In the slave receive operation (TRC = 0), if the slave side has received two or more bytes and needs the next data, set ACKE = 0 so that the master side is disabled to start the next transfer. Similarly, in the master receive operation (TRC = 0), if the master side receives two or more bytes and needs the next data, set ACKE = 0 to output the restart condition or the stop condition so that the $\overline{\text{ACK}}$ signal does not generate. This prevents the MSB data from being output to the SDA line in the slave transmit operation (transmission stops).

Figure 8-18. Acknowledge Signal



When receiving the local address, the acknowledge signal is automatically output in synchronization with the fall of the eighth clock of SCL regardless of the value of the ACKE. The acknowledge signal is not output when receiving an address other than the local address.

The output methods of the acknowledge signal are as follows according to the setting of the wait timing.

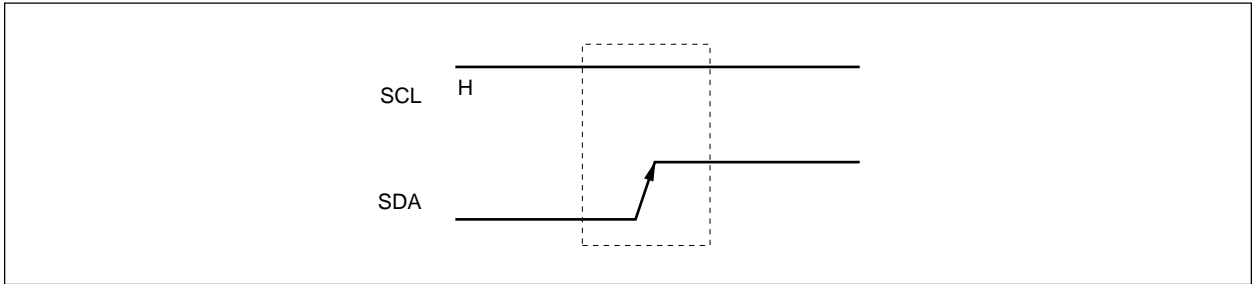
- When selecting 8-clock wait : acknowledge signal is output by setting ACKE = 1 before releasing wait.
- When selecting 9-clock wait : acknowledge signal is automatically output in synchronization with the fall of the eighth clock of SCL by setting ACKE = 1 beforehand.

(5) Stop condition

The stop condition is generated when the SDA pin changes from low level to high level while the SCL pin is high level.

The stop condition is a signal which the master outputs to the slave when a serial transfer has ended. The slave is provided with the hardware to detect the stop condition.

Figure 8-19. Stop Condition



The stop condition is generated by setting (to 1) bit 0 (SPT) of the IICC control register (IICC). When the stop condition is detected, bit 0 (SPD) of the IICC status register (IICS) is set (1). When bit 4 (SPIE) of IICC is set (1), INTIIC is generated.

(6) Wait signal ($\overline{\text{WAIT}}$)

The wait signal is a signal by which the master or the slave informs the other that it is preparing for transmitting/receiving data (wait status).

The master of the slave informs the wait status to the other by inputting the low level to the SCL pin. Both the master and slave can start the next transfer when the wait status is released.

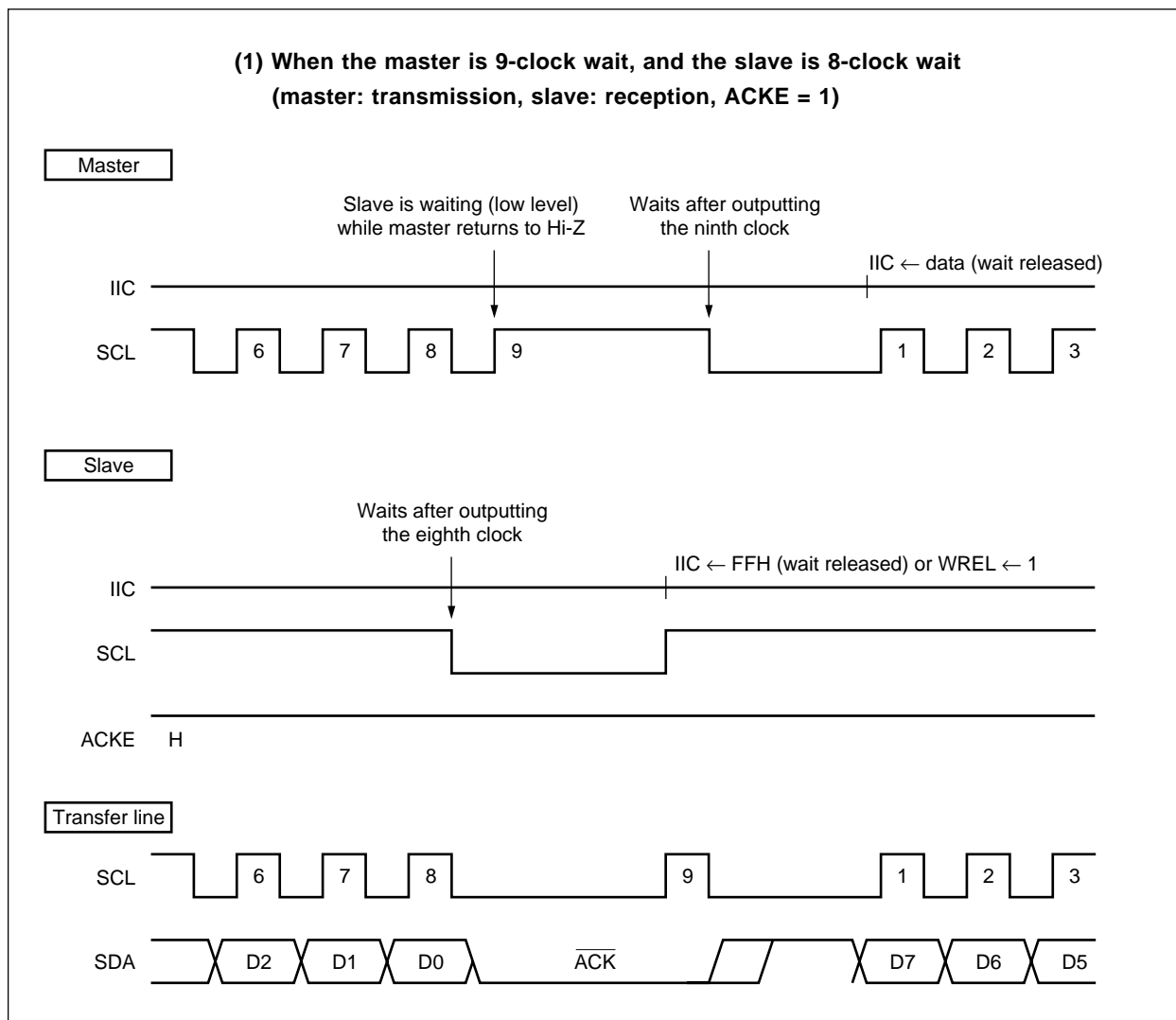
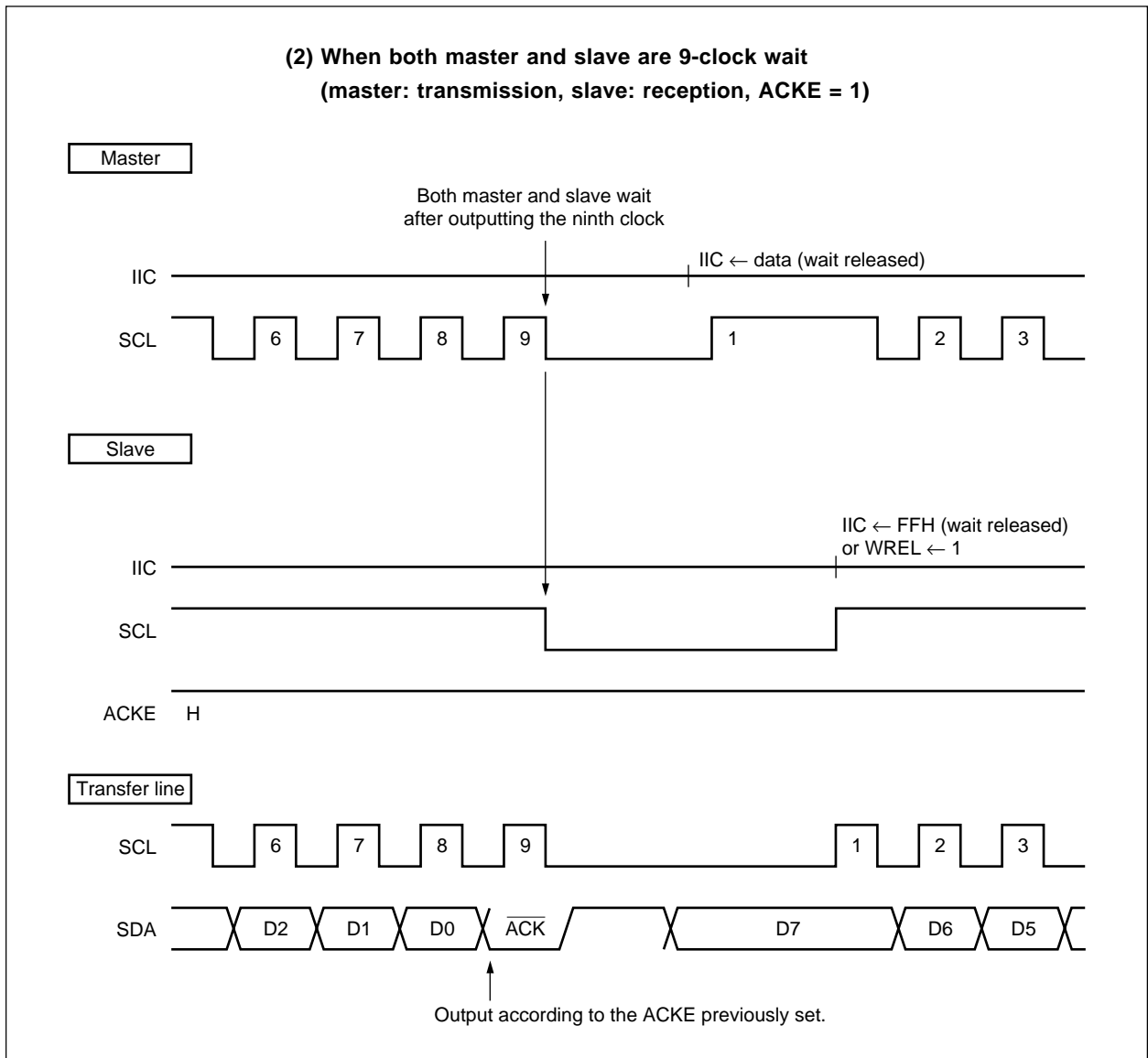
Figure 8-20. Wait Signal (1/2)

Figure 8-20. Wait Signal (2/2)



The wait of the IICC register automatically generates according to the setting of WTIM.

Normally, the receive side releases wait when WREL = 1 or when FFH is written to IIC, and the transmit side releases wait when data is written to IIC.

For the master, wait can be released also with the following method.

- STT = 1
- SPT = 1

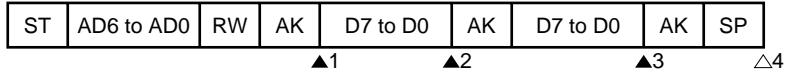
(7) I²C interrupt (INTIIC)

The following shows the INTIIC interrupt request generation timing and the value of the IIC status register (IICS) in INTIIC interrupt timing.

(a) Master operation

(i) Start-Address-Data-Data-Stop (normal transmission/reception)

<1> When WTIM = 0



▲ 1: IICS = 10xxx110 B

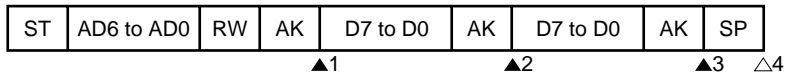
▲ 2: IICS = 10xxx000 B

▲ 3: IICS = 10xxx000 B

△ 4: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

<2> When WTIM = 1



▲ 1: IICS = 10xxx110 B

▲ 2: IICS = 10xxx100 B

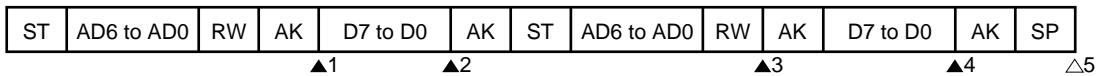
▲ 3: IICS = 10xxx000 B

△ 4: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

(ii) Start-Address-Data-Start-Address-Data-Stop (restart)

<1> When WTIM = 0



▲ 1: IICS = 10xxx110 B

▲ 2: IICS = 10xxx000 B

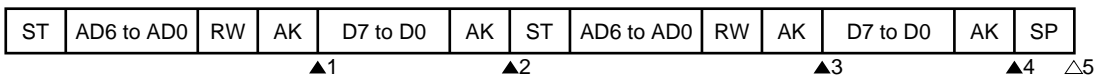
▲ 3: IICS = 10xxx110 B

▲ 4: IICS = 10xxx000 B

△ 5: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

<2> When WTIM = 1



▲ 1: IICS = 10xxx110 B

▲ 2: IICS = 10xxxx00 B

▲ 3: IICS = 10xxx110 B

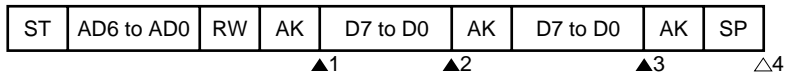
▲ 4: IICS = 10xxxx00 B

△ 5: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

(iii) Start-Code-Data-Data-Stop (extension code transmission)

<1> When WTIM = 0



▲ 1: IICS = 1010x110 B

▲ 2: IICS = 1010x000 B

▲ 3: IICS = 1010x000 B

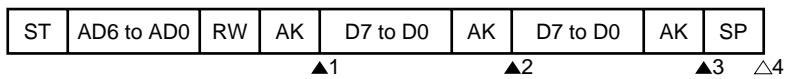
△ 4: IICS = 00000001 B

Remark ▲ always generates

△ generates only when SPIE = 1

x don't care

<2> When WTIM = 1



▲ 1: IICS = 1010x110 B

▲ 2: IICS = 1010x100 B

▲ 3: IICS = 1010xx00 B

△ 4: IICS = 00000001 B

Remark ▲ always generates

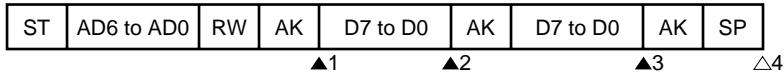
△ generates only when SPIE = 1

x don't care

(b) Slave operation (when receiving slave address data (SVA coincides))

(i) Start-Address-Data-Data-Stop

<1> When WTIM = 0



▲ 1: IICS = 0001x110 B

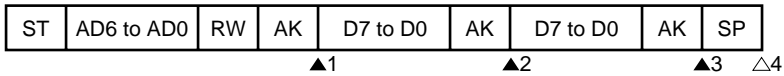
▲ 2: IICS = 0001x000 B

▲ 3: IICS = 0001x000 B

△ 4: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

<2> When WTIM = 1



▲ 1: IICS = 0001x110 B

▲ 2: IICS = 0001x100 B

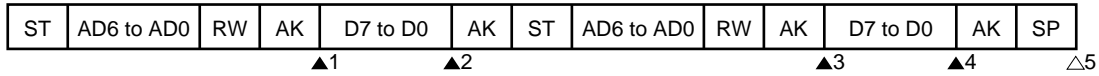
▲ 3: IICS = 0001xx00 B

△ 4: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

(ii) Start-Address-Data-Start-Address-Data-Stop

<1> When WTIM = 0 (SVA coincides after restart)



▲ 1: IICS = 0001x110 B

▲ 2: IICS = 0001x000 B

▲ 3: IICS = 0001x110 B

▲ 4: IICS = 0001x000 B

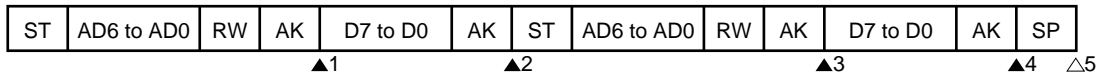
△ 5: IICS = 00000001 B

Remark ▲ always generates

△ generates only when SPIE = 1

x don't care

<2> When WTIM = 1 (SVA coincides after restart)



▲ 1: IICS = 0001x110 B

▲ 2: IICS = 0001xx00 B

▲ 3: IICS = 0001x110 B

▲ 4: IICS = 0001xx00 B

△ 5: IICS = 00000001 B

Remark ▲ always generates

△ generates only when SPIE = 1

x don't care

(iii) Start-Address-Data-Start-Code-Data-Stop

<1> When WTIM = 0 (receives extension code after restart)



▲ 1: IICS = 0001x110 B

▲ 2: IICS = 0001xx00 B

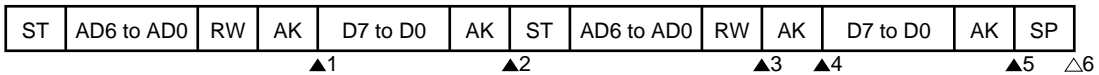
▲ 3: IICS = 0010x010 B

▲ 4: IICS = 0010xx00 B

△ 5: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

<2> When WTIM = 1 (receives extension code after restart)



▲ 1: IICS = 0001x110 B

▲ 2: IICS = 0001xx00 B

▲ 3: IICS = 0010x010 B

▲ 4: IICS = 0010x110 B

▲ 5: IICS = 0010xx00 B

△ 6: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

(iv) Start-Address-Data-Start-Address-Data-Stop

<1> When WTIM = 0 (address does not coincide after restart (except extension code))



▲ 1: IICS = 0001x110 B

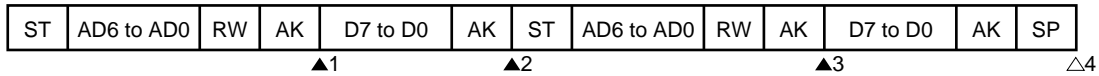
▲ 2: IICS = 0001x000 B

▲ 3: IICS = 0000xx10 B

△ 4: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

<2> When WTIM = 1 (address does not coincide after restart (except extension code))



▲ 1: IICS = 0001x110 B

▲ 2: IICS = 0001xx00 B

▲ 3: IICS = 0000xx10 B

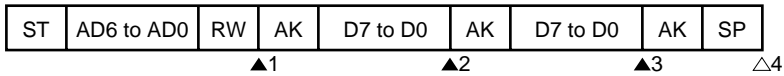
△ 4: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

(c) Slave operation (when receiving extension code)

(i) Start-Code-Data-Data-Stop

<1> When WTIM = 0



▲ 1: IICS = 0010x010 B

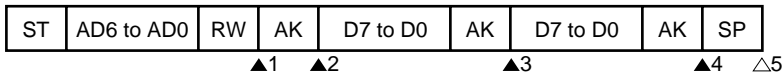
▲ 2: IICS = 0010x000 B

▲ 3: IICS = 0010x000 B

△ 4: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

<2> When WTIM = 1



▲ 1: IICS = 0010x010 B

▲ 2: IICS = 0010x110 B

▲ 3: IICS = 0010xx00 B

▲ 4: IICS = 0010xx00 B

△ 5: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

(ii) Start-Code-Data-Start-Address-Data-Stop

<1> When WTIM = 0 (SVA coincides after restart)



▲ 1: IICS = 0010x010 B

▲ 2: IICS = 0010x000 B

▲ 3: IICS = 0001x110 B

▲ 4: IICS = 0001x000 B

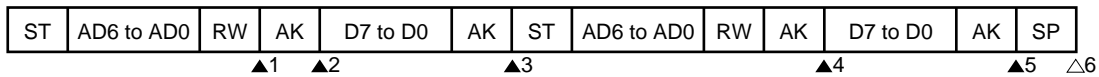
△ 5: IICS = 00000001 B

Remark ▲ always generates

△ generates only when SPIE = 1

x don't care

<2> When WTIM = 1 (SVA coincides after restart)



▲ 1: IICS = 0010x010 B

▲ 2: IICS = 0010x110 B

▲ 3: IICS = 0010xx00 B

▲ 4: IICS = 0001x110 B

▲ 5: IICS = 0001xx00 B

△ 6: IICS = 00000001 B

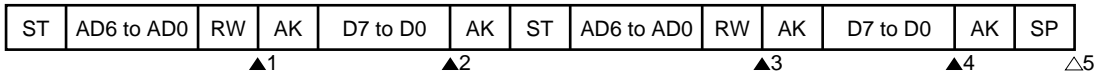
Remark ▲ always generates

△ generates only when SPIE = 1

x don't care

(iii) **Start-Code-Data-Start-Code-Data-Stop**

<1> When WTIM = 0 (receives extension code after restart)



▲ 1: IICS = 0010x010 B

▲ 2: IICS = 0010x000 B

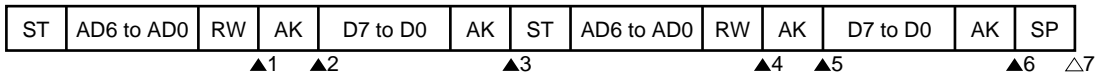
▲ 3: IICS = 0010x010 B

▲ 4: IICS = 0010x000 B

△ 5: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

<2> When WTIM = 1 (receives extension code after restart)



▲ 1: IICS = 0010x010 B

▲ 2: IICS = 0010x110 B

▲ 3: IICS = 0010xx00 B

▲ 4: IICS = 0010x010 B

▲ 5: IICS = 0010x110 B

▲ 6: IICS = 0010xx00 B

△ 7: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

(iv) Start-Code-Data-Start-Address-Data-Stop

<1> When WTIM = 0 (address does not coincides after restart (except extension code))



▲ 1: IICS = 0010x010 B

▲ 2: IICS = 0010x000 B

▲ 3: IICS = 00000x10 B

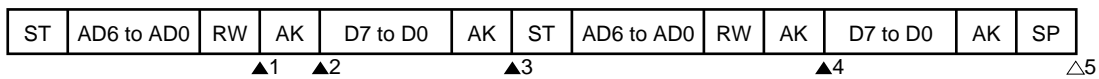
△ 4: IICS = 00000001 B

Remark ▲ always generates

△ generates only when SPIE = 1

x don't care

<2> When WTIM = 1 (address does not coincides after restart (except extension code))



▲ 1: IICS = 0010x010 B

▲ 2: IICS = 0010x110 B

▲ 3: IICS = 0010xx00 B

▲ 4: IICS = 00000x10 B

△ 5: IICS = 00000001 B

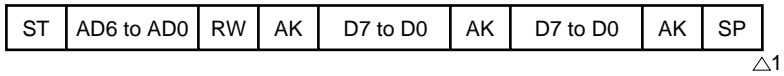
Remark ▲ always generates

△ generates only when SPIE = 1

x don't care

(d) Operation of not joining communication

(i) Start-Code-Data-Data-Stop



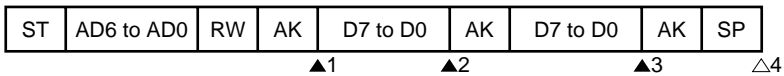
△ 1: IICS = 00000001 B

Remark △ generates only when SPIE = 1

(e) Operation of arbitration defeat (operates as a slave after arbitration defeat)

(i) When defeated in arbitration during slave address data transmission

<1> When WTIM = 0



▲ 1: IICS = 0101x110 B (example: reads ALD during interrupt processing)

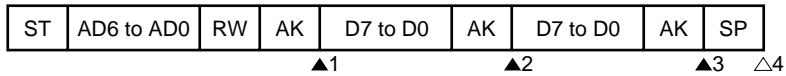
▲ 2: IICS = 0001x000 B

▲ 3: IICS = 0001x000 B

△ 4: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

<2> When WTIM = 1



▲ 1: IICS = 0101x110 B (example: reads ALD during interrupt processing)

▲ 2: IICS = 0001x100 B

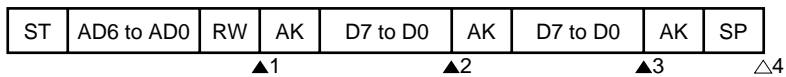
▲ 3: IICS = 0001xx00 B

△ 4: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

(ii) When defeated in arbitration during transmitting extension code

<1> When WTIM = 0



▲ 1: IICS = 0110x010 B (example: reads ALD during interrupt processing)

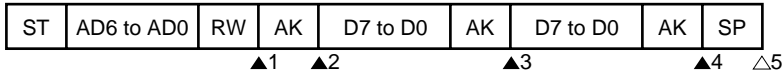
▲ 2: IICS = 0010x000 B

▲ 3: IICS = 0010x000 B

△ 4: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

<2> When WTIM = 1



▲ 1: IICS = 0110x010 B (example: reads ALD during interrupt processing)

▲ 2: IICS = 0010x110 B

▲ 3: IICS = 0010x100 B

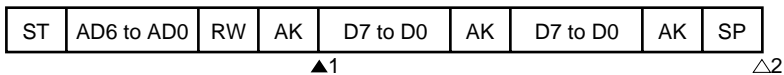
▲ 4: IICS = 0010xx00 B

△ 5: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

(f) Operation of arbitration defeat (does not join after arbitration defeat)

(i) When defeated in arbitration during transmitting slave address data

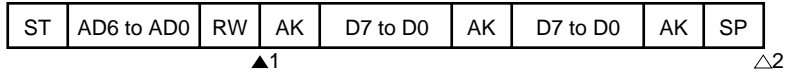


▲ 1: IICS = 01000110 B (example: reads ALD during interrupt processing)

△ 2: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1

(ii) When defeated in arbitration during transmitting extension code



▲ 1: IICS = 0110x010 B (example: reads ALD during interrupt processing)

Set LREL =1 by software (when not joining communication)

△ 2: IICS = 00000001 B

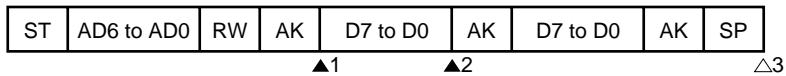
Remark ▲ always generates

△ generates only when SPIE = 1

x don't care

(iii) When defeated in arbitration during transferring data

<1> When WTIM = 0



▲ 1: IICS = 10001110 B

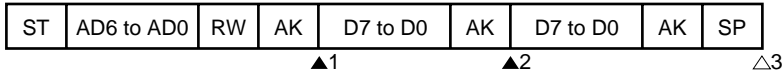
▲ 2: IICS = 01000000 B (example: reads ALD during interrupt processing)

△ 3: IICS = 00000001 B

Remark ▲ always generates

△ generates only when SPIE = 1

<2> When WTIM = 1



▲ 1: IICS = 10001110 B

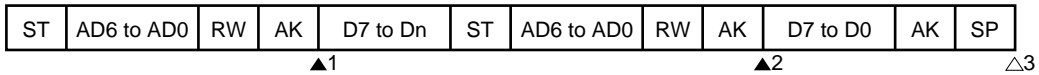
▲ 2: IICS = 01000100 B (example: reads ALD during interrupt processing)

△ 3: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1

(iv) When defeated in restart condition during transferring data

<1> Except extension code (example: SVA does not coincide)



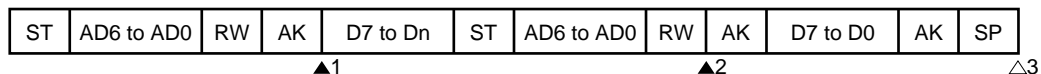
▲ 1: IICS = 1000x110 B

▲ 2: IICS = 01000110 B (example: reads ALD during interrupt processing)

△ 3: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care
 n = 0 to 6

<2> Extension code



▲ 1: IICS = 1000x110 B

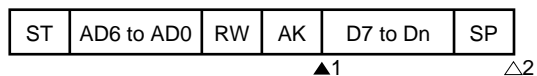
▲ 2: IICS = 0110x010 B (example: reads ALD during interrupt processing)

Set IICC : LREL = 1 by software (when not joining communication)

△ 3: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care
 n = 0 to 6

(v) When defeated in stop condition during transferring data



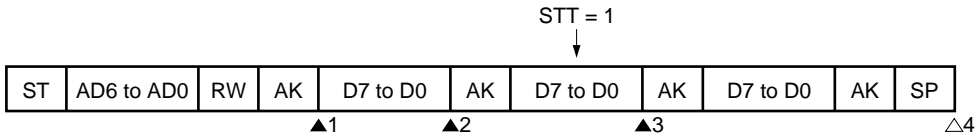
▲ 1: IICS = 1000x110 B

△ 2: IICS = 01000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care
 n = 0 to 6

- (vi) When attempting to generate restart condition and defeated in arbitration because the data is low level

<1> When WTIM = 0



▲ 1: IICS = 1000x110 B

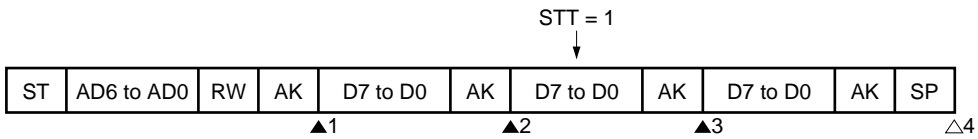
▲ 2: IICS = 1000x000 B

▲ 3: IICS = 01000000 B (example: reads ALD during interrupt processing)

△ 4: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

<2> When WTIM = 1



▲ 1: IICS = 1000x110 B

▲ 2: IICS = 1000xx00 B

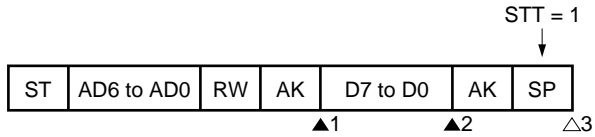
▲ 3: IICS = 01000100 B (example: reads ALD during interrupt processing)

△ 4: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

(vii) When attempting to generate restart condition and defeated in arbitration at stop condition because the data is low level

<1> When WTIM = 0



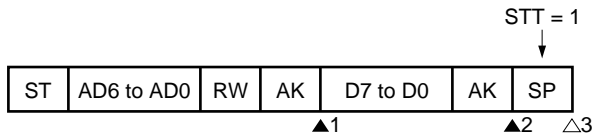
▲ 1: IICS = 1000x110 B

▲ 2: IICS = 1000x000 B

△ 3: IICS = 01000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

<2> When WTIM = 1



▲ 1: IICS = 1000x110 B

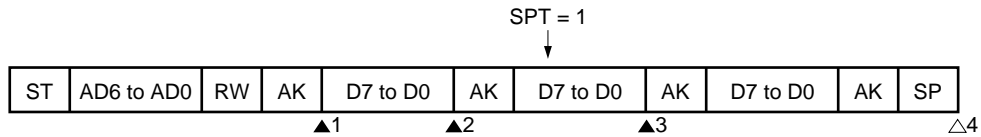
▲ 2: IICS = 1000xx00 B

△ 3: IICS = 01000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

(viii) When attempting to generate stop condition and defeated in arbitration because the data is low level

<1> When WTIM = 0



▲ 1: IICS = 1000x110 B

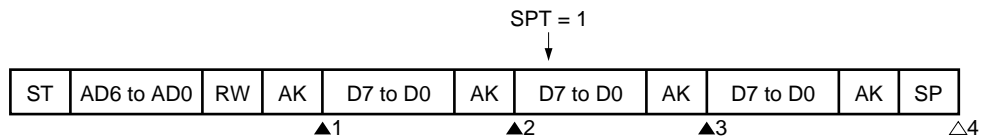
▲ 2: IICS = 1000x000 B

▲ 3: IICS = 01000000 B (example: reads ALD during interrupt processing)

△ 4: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

<2> When WTIM = 1



▲ 1: IICS = 1000x110 B

▲ 2: IICS = 1000xx00 B

▲ 3: IICS = 01000000 B (example: reads ALD during interrupt processing)

△ 4: IICS = 00000001 B

Remark ▲ always generates
 △ generates only when SPIE = 1
 x don't care

(8) Interrupt request (INTIIC) generation timing and wait control

INTIIC generates and wait control is performed by the settings of the WTIM bit of the IIC control register (IICC) at the timings shown in Table 8-3.

Table 8-3. INTIIC Generation Timing and Wait Control

WTIM	In Slave Operation			In Master Operation		
	Address	Data Reception	Data Transmission	Address	Data Reception	Data Transmission
0	9 ^{Notes 1, 2}	8 ^{Note 2}	8 ^{Note 2}	9	8	8
1	9 ^{Notes 1, 2}	9 ^{Note 2}	9 ^{Note 2}	9	9	9

- Notes**
1. INTIIC signal and wait of the slave generate at the fall of the ninth clock only when they coincide with the address set in the slave address register (SVA).
At this time, \overline{ACK} is output regardless of the setting of ACKE. The slave which has received an extension code generates INTIIC at the fall of the eighth clock.
 2. Neither INTIIC nor wait generates when SVA and the received address do not coincide.

Remark The numbers in the table represent the number of the clocks of the serial clock. Both the interrupt request and the wait control synchronize with the fall of the serial clock.

(a) When transmitting/receiving address

- In slave operation : The interrupt and the wait timings are determined regardless of the WTIM bit.
- In master operation : The interrupt and the wait timings generates at the fall of the ninth clock regardless of the WTIM bit.

(b) When receiving data

- In master/slave operation: The interrupt and the wait timings are determined by the WTIM bit.

(c) When transmitting data

- In master/slave operation: The interrupt and the wait timings are determined by the WTIM bit.

(d) Wait release

The following four methods are available for releasing wait.

- Set WREL of the control register (IICC) = 1
- Write operation of IIC shift register (IIC)
- Start condition (STT) set
- Stop condition (SPT) set

When 8-clock wait (WTIM = 0) is selected, the output level of \overline{ACK} should be determined before wait release.

(e) Stop condition detection

INTIIC generates when stop condition is detected.

(9) Address coincidence detection

The I²C bus can select the specific slave device when the master transmits the slave address.

Address coincidence detection can be automatically performed by hardware. If the local address is set to the slave address register (SVA), INTIIC interrupt request generates only when the slave address transmitted from the master and the address set in SVA coincide or when an extension code is received.

(10) Error detection

The I²C bus can detect transmission errors by comparing the IIC data before transmission starts and that after transmission ends because the status of the serial bus during transmission (SDA) is captured also to IIC shift register (IIC) of the transmitting device. In this case, if the two data differ, it is judged that a transmission error has occurred.

(11) Extension code

- (a) Interrupt request (INTIIC) is issued at the fall of the eighth clock by setting the extension code reception flag (EXC) regarding it as reception of exception code when the higher 4 bits of the reception address is either "0000" or "1111".

The local address stored in the slave address register (SVA) is not affected.

- (b) The following is set when "111110xx" is set to SVA by 10-bit address transfer and "111110xx0" is transferred from the master. However, interrupt request (INTIIC) generates at the fall of the eighth clock.

- Coincidence of the higher 4-bit data: EXC = 1
- Coincidence of the 7-bit data : COI = 1

- (c) The processing after interrupt request is issued differs depending on the data following the extension code. Therefore, it is performed by software.

For example, LREL is set to 1 and the next communication wait status enters not to operate a device as a slave after receiving extension code.

Table 8-4. Definition of Extension Code Bit

Slave Address	R/W Bit	Description
0000 000	0	General call address
0000 000	1	Start byte
0000 001	x	CBUS address
0000 010	x	Address reserved for different bus format
1111 0xx	x	10-bit slave address specification

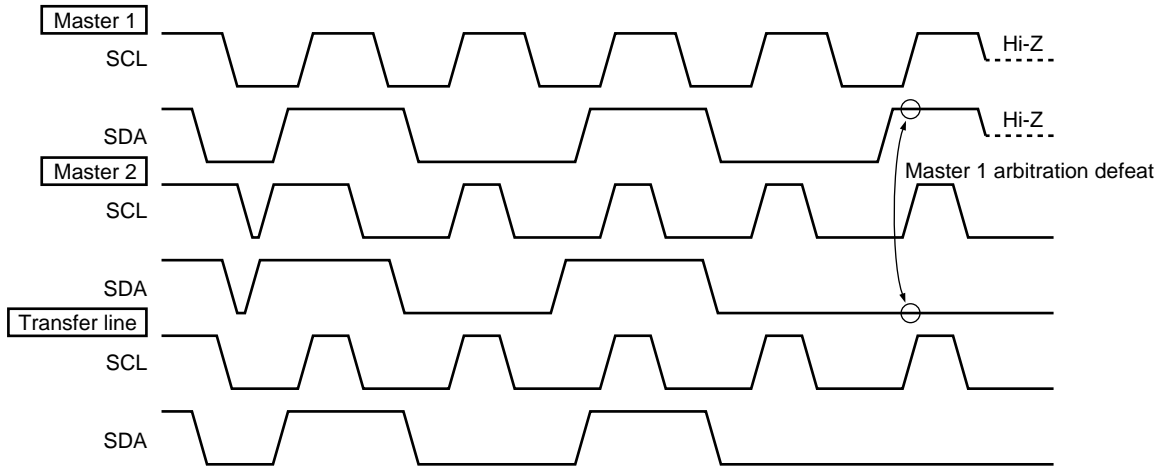
(12) Arbitration

When more than one master simultaneously output start conditions (when setting STT =1 before STD = 1 is set), master communication continues until the data differs while adjusting the clock. This operation is called arbitration.

The master which is defeated in arbitration sets the ALD bit of the IIC status register (IICS) at the timing at which the master is defeated in the arbitration, sets both SCL and SDA lines in Hi-Z status, and releases bus. The arbitration defeat is detected by software when ALD =1 at the next interrupt request generation timing (the eighth or ninth clock, stop condition detection, etc.).

For the interrupt generation timing, refer to **(7) I²C interrupt (INTIIC)**.

Figure 8-21. Example of Arbitration Timing



Status when Arbitration Occurs	Interrupt Request Issue Timing
Address transmitting	Fall of the eighth or ninth clock after byte transfer ^{Note 1}
Read/write information after address transmission	
Transferring extension code	
Read/write information after extension code transmission	
Transmitting data	
ACK transfer period after data transmission	
Transferring data, restart condition detection	
Transferring data, stop condition detection	Stop condition output (SPIE = 1) ^{Note 2}
Attempted to output restart condition but data is low level	Fall of the eighth or ninth clock after byte transfer ^{Note 1}
Attempted to output restart condition but stop condition is detected	
Attempted to output stop condition but data is low level	Stop condition output (SPIE = 1) ^{Note 2}
Attempted to restart condition but SCL is low level	

Notes 1. When WTIM (bit 3 of the IIC control register (IICC)) = 1, interrupt generates at the fall of the ninth clock. When WTIM = 0 and when slave address of extension code is received, interrupt generates at the fall of the eighth clock.

2. If arbitration may occur, set SPIE = 1 in master operation.

(13) Wake-up function

Wake-up function generates interrupt request (INTIIC) when the local address and an extension code are received in the slave function of I²C.

When address does not coincide, unnecessary interrupt does not generate, so that efficient processing is possible.

When start condition is detected, wake-up wait status is set. Even a master can become a slave as a result of arbitration defeat (in the case start condition is output), it enters wake-up wait status while transmitting address.

However, when a stop condition is detected, interrupt enable/disable is determined according to the setting of the SPIE bit regardless of the wake-up function.

(14) Communication reservation

- When a device could become neither a master or slave in arbitration.
- When a device does not operate as a slave receiving an extension code (when not sending back $\overline{\text{ACK}}$ and releasing bus with LREL of IICC = 1).

When the STT bit of the IICC is set in the status not joining the bus, a start condition is automatically generated and wait status is entered after the bus is released (stop condition detection).

When the bus release is detected (stop condition detection), address transfer as a master is started by IIC write manipulation. At this time the SPIE bit of the IICC should be set.

When STT is set, whether it is operates as start condition or as communication reservation is determined by the bus status.

- When bus is released : start condition generation
- When bus is not released (wait status) : communication reservation

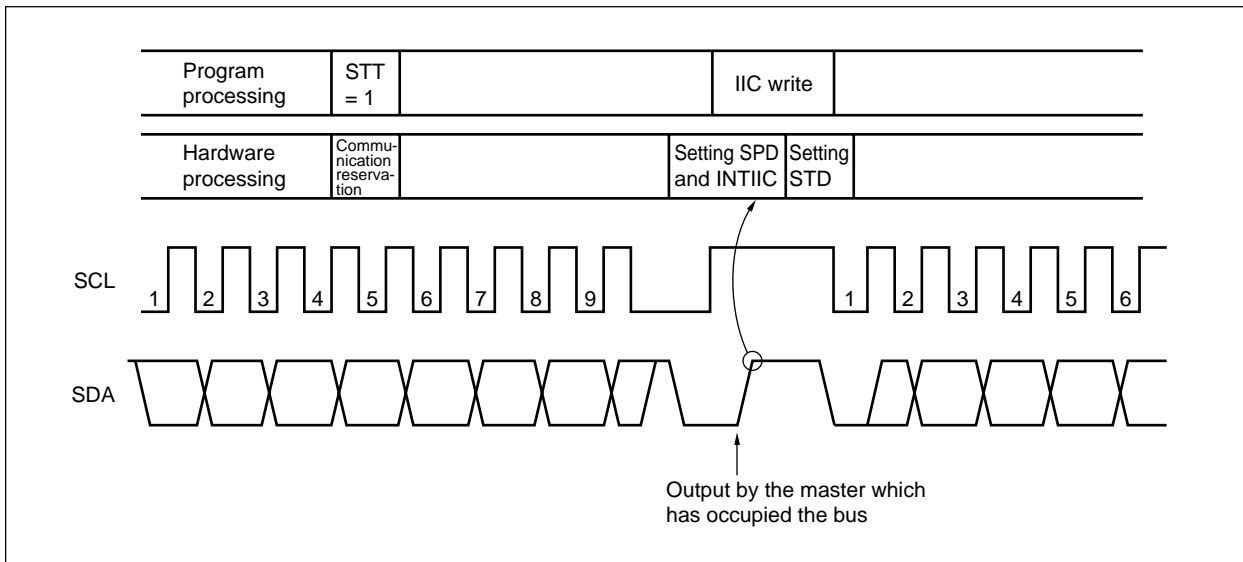
Which operation STT has performed is detected by checking the STT bit again after setting STT and giving wait time.

Secure the wait time as shown in Table 8-5 by software. Wait time can be set by SMC, CL0, and CL1 of IICCL.

Table 8-5. Wait Time

SMC	CL1	CL0	Wait Time
0	0	0	26 clocks
0	0	1	46 clocks
0	1	0	
0	1	1	37 clocks
1	0	0	16 clocks
1	0	1	
1	1	0	
1	1	1	13 clocks

Figure 8-22. Communication Reservation Timing



The communication reservation is acknowledged at the following timings. The communication reservation is made by setting the STT of IICC = 1 before stop condition detection after STD of IICS = 1 is set.

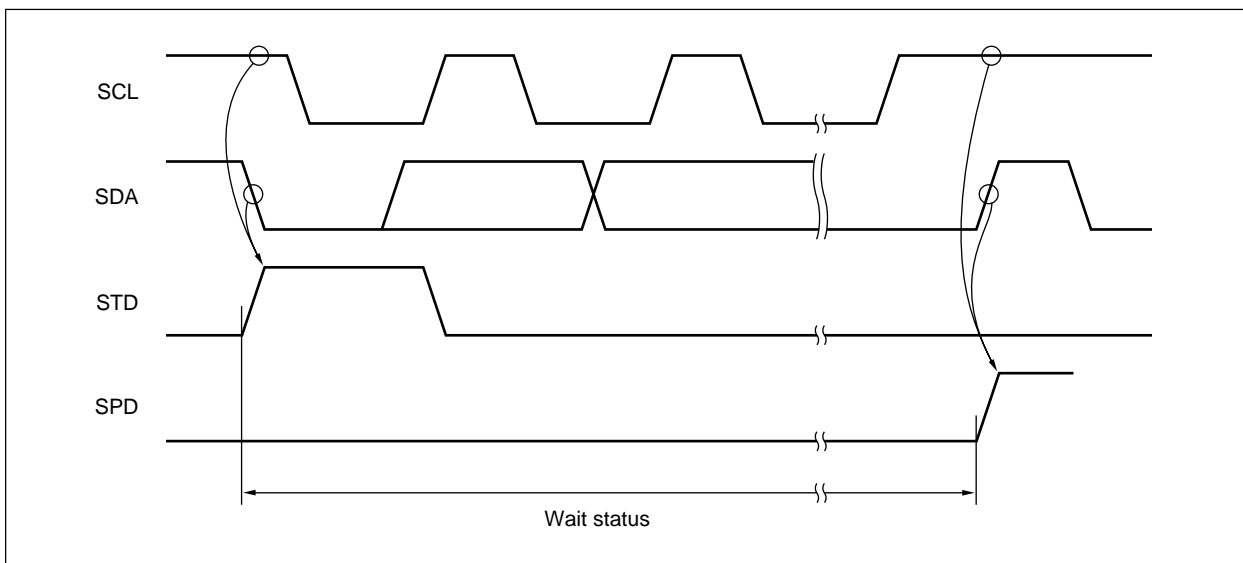
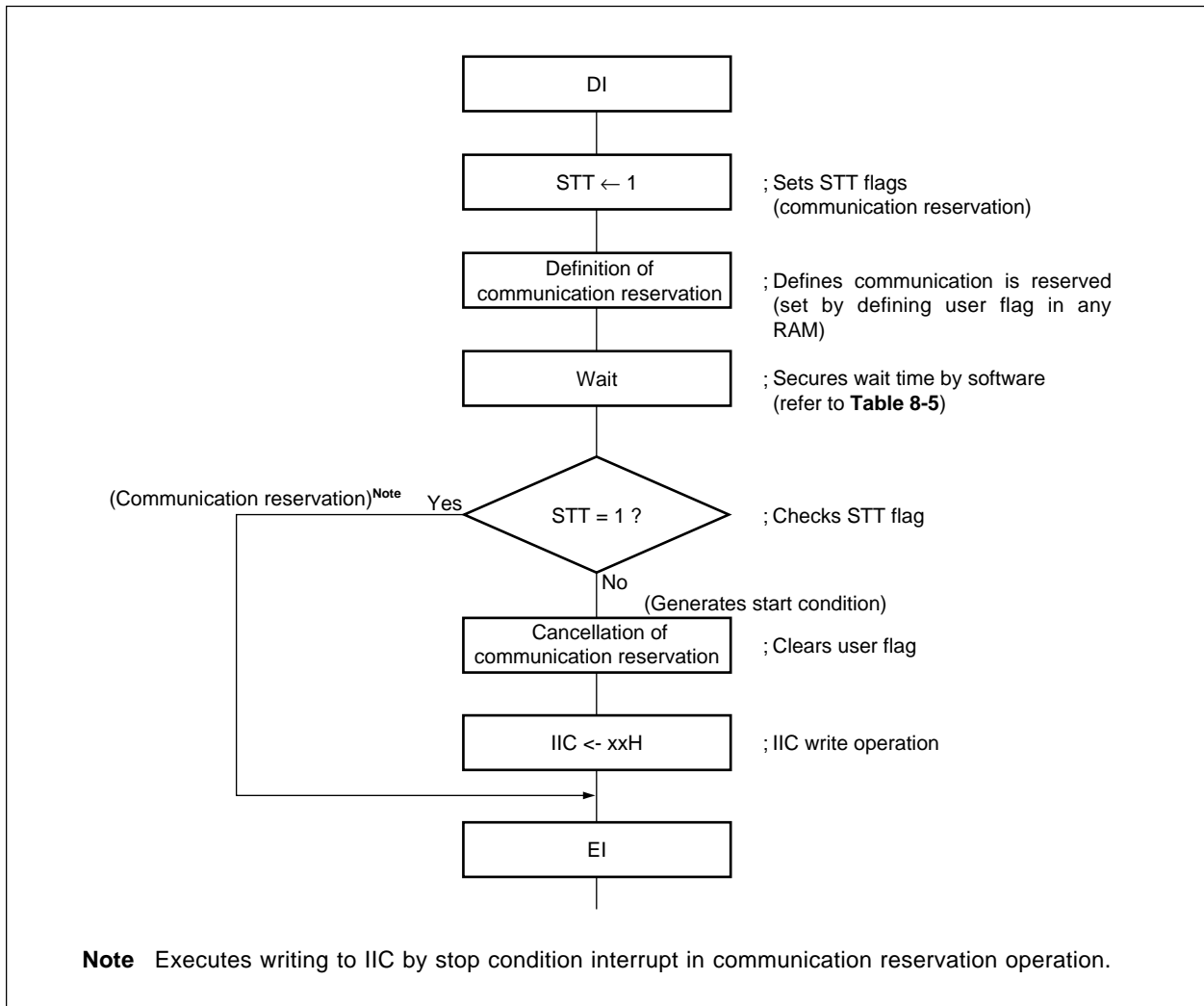


Figure 8-23 shows the communication reservation procedure.

Figure 8-23. Communication Reservation Procedure



(15) Other precautions

(a) Multi-master communication

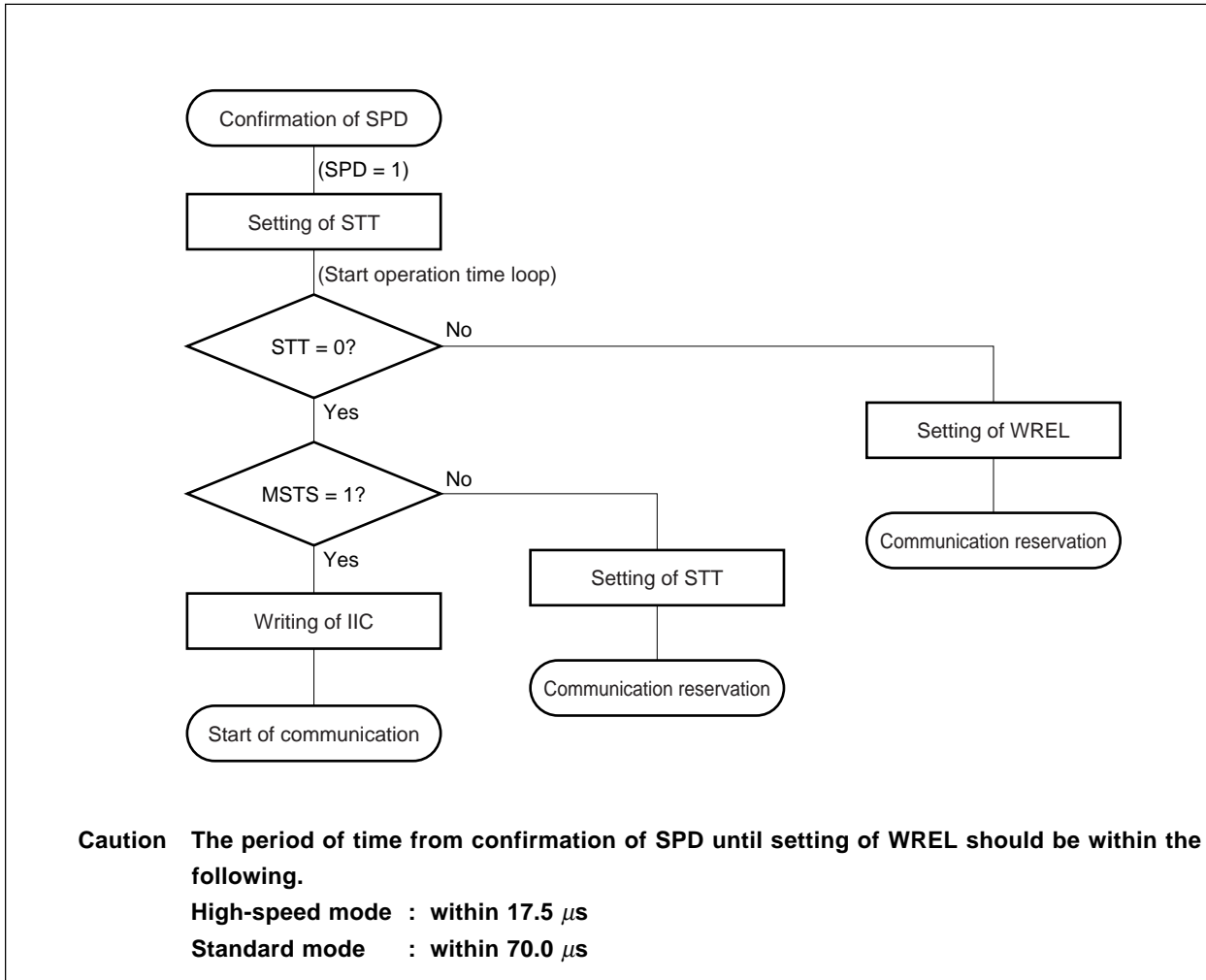
To perform master communication from the status in which stop condition is not detected (bus is not released) after reset, generate stop condition and release bus before starting master communication. In multi-master, master communication cannot be performed in the status in which bus is not released (stop condition is not detected).

Generate stop condition with the following procedure.

- <1> Setting IICCL
- <2> IICE of IICC ← 1
- <3> SPT of IICC ← 1

- ★ (b) **Operation during communication reservation (when a multi-master is used)**
If a slave is selected during communication reservation, when writing a “1” to the WREL bit, write a “0” to the STT bit at the same time. After that, following stop condition detection, write a “1” to the STT bit again.
- ★ (c) **Start operation after communication reservation (when a multi-master is used)**
If the stop condition is detected and the start condition is generated after that, after confirming that the MSTs bit is 1 (master communication state), confirm that the TRC bit is 1 (transmission operation). At this time, if the TRC bit is 0, set LREL to withdraw from communication, and carry out communication reservation (STT = 1) again after the stop condition is detected.
- ★ (d) **STT setting timing (when a multi-master is used)**
Arrange the program as shown in Figure 8-24.

Figure 8-24. STT Setting Timing Procedure

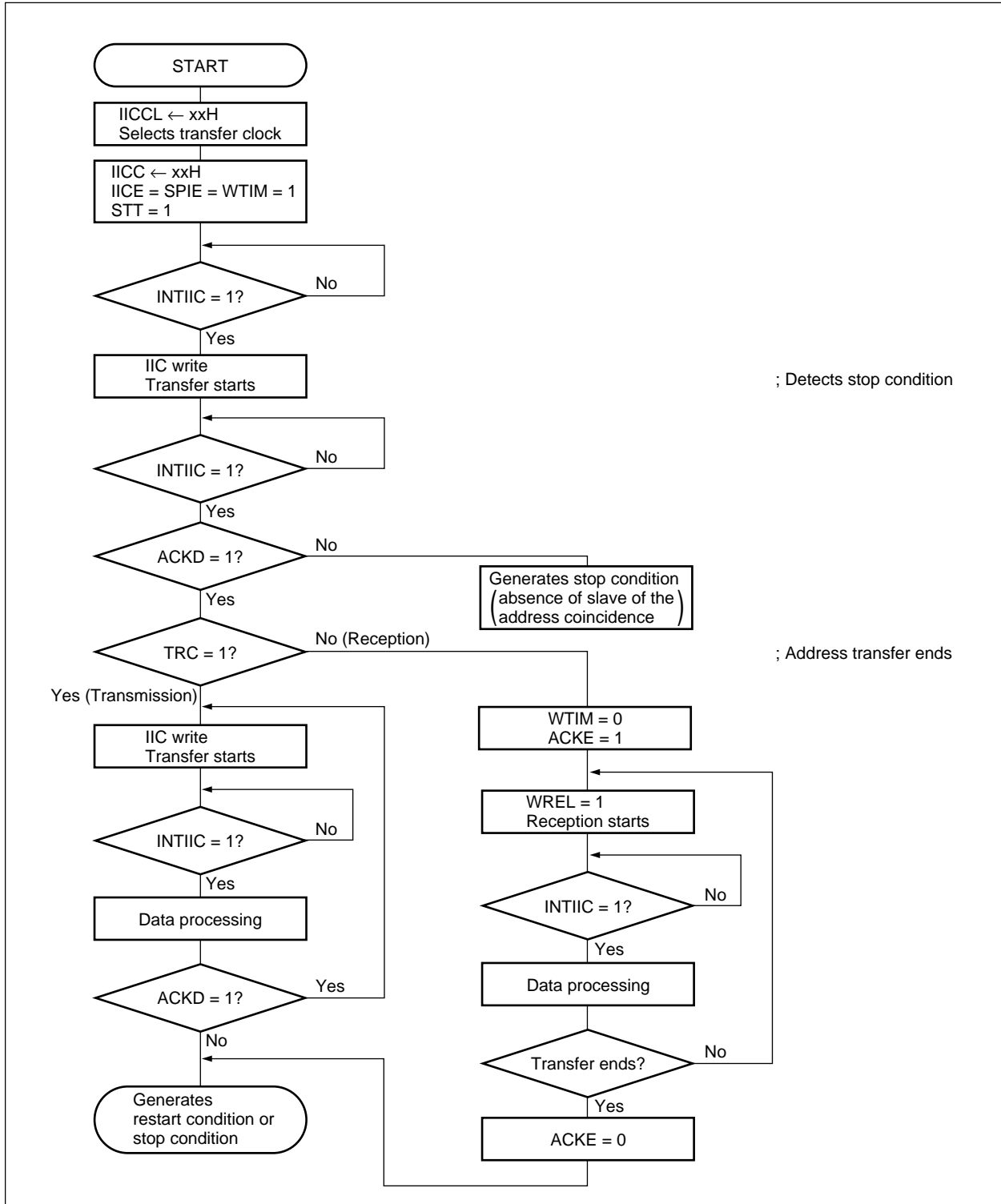


8.4.7 Communication operation

(1) Master operation

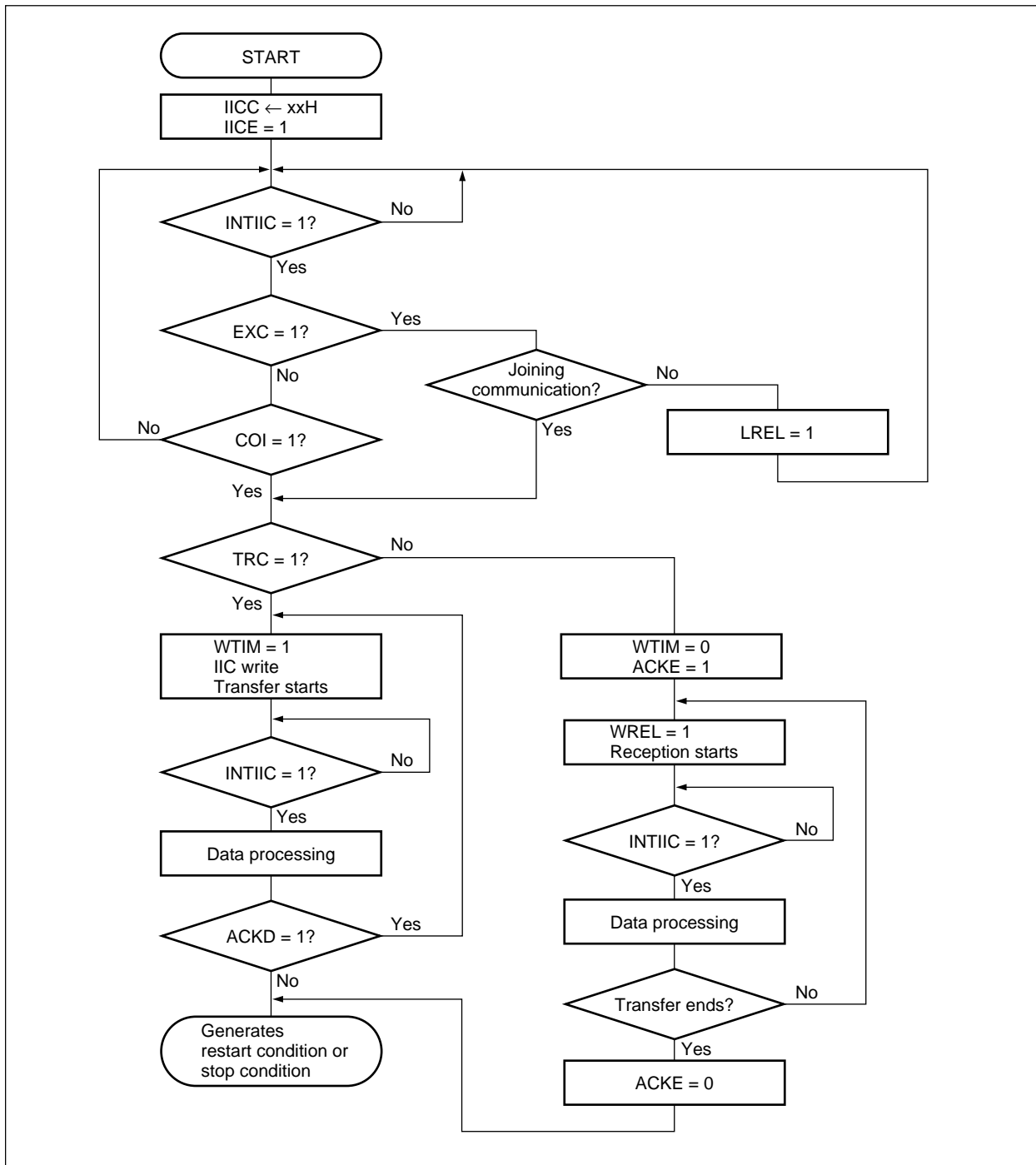
The following shows the master communication procedure.

Figure 8-25. Master Operation Procedure



(2) Slave operation

The following shows the slave communication procedure.

Figure 8-26. Slave Operation Procedure

8.4.8 Timing chart

In the I²C bus mode, a target slave device is selected from more than one slave device when the master outputs an address to the serial bus.

The master transmits the TRC bit that indicates the transfer direction of data following the slave address and starts serial communication with the slave.

Figures 8-27 and 8-28 show the timing charts of data communication.

The shift operation of the shift register (IIC) is performed in synchronization with the fall of the serial clock (SCK), the transmitted data is transferred to the SO latch, and output from the SDA pin with the MSB first.

The data input to the SDA pin at the rise of SCL is captured by IIC.

Figure 8-27. Example of Master→Slave Communication
(9-clock wait is selected both for master and slave) (1/3)

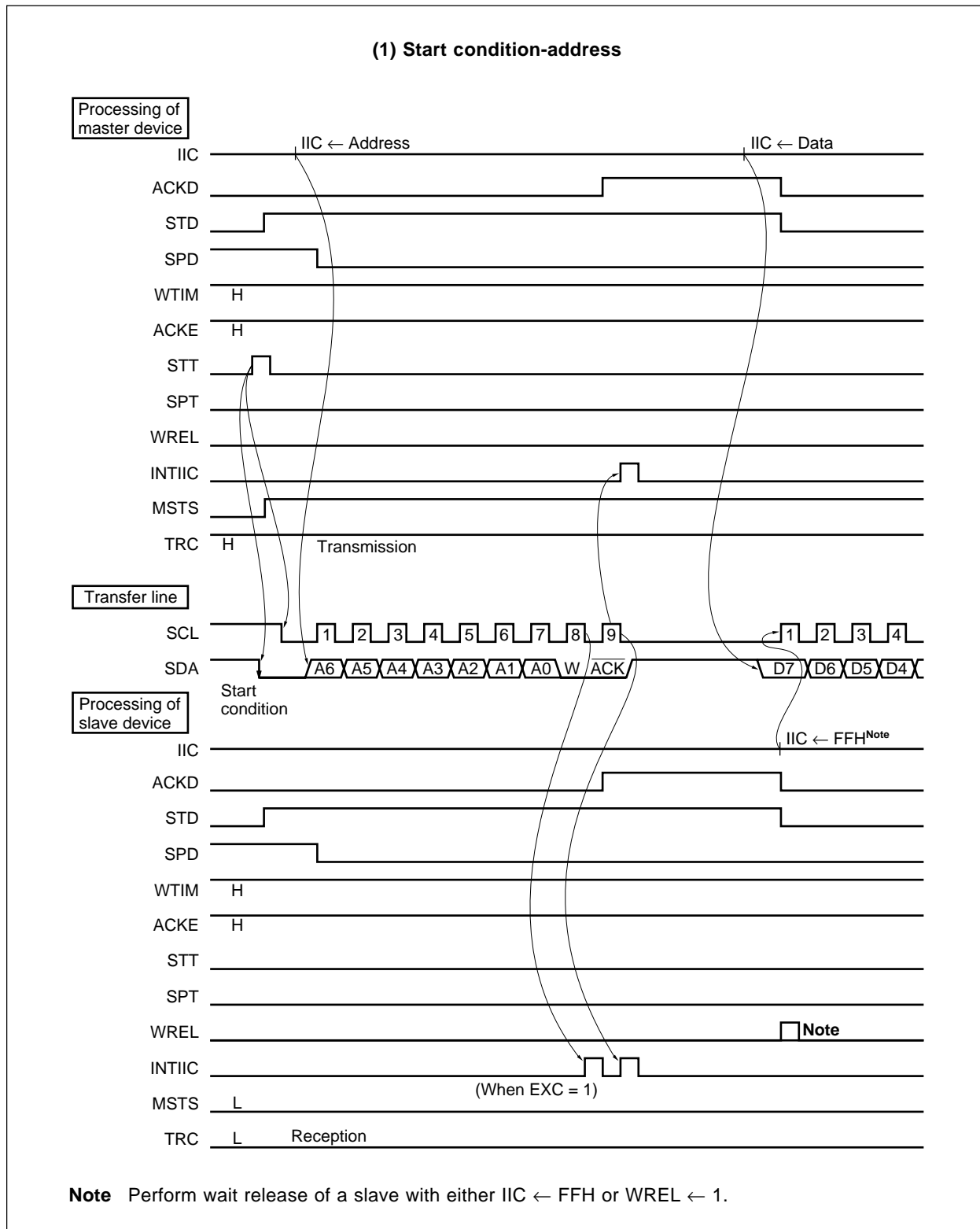


Figure 8-27. Example of Master → Slave Communication
(9-clock wait is selected both for master and slave) (2/3)

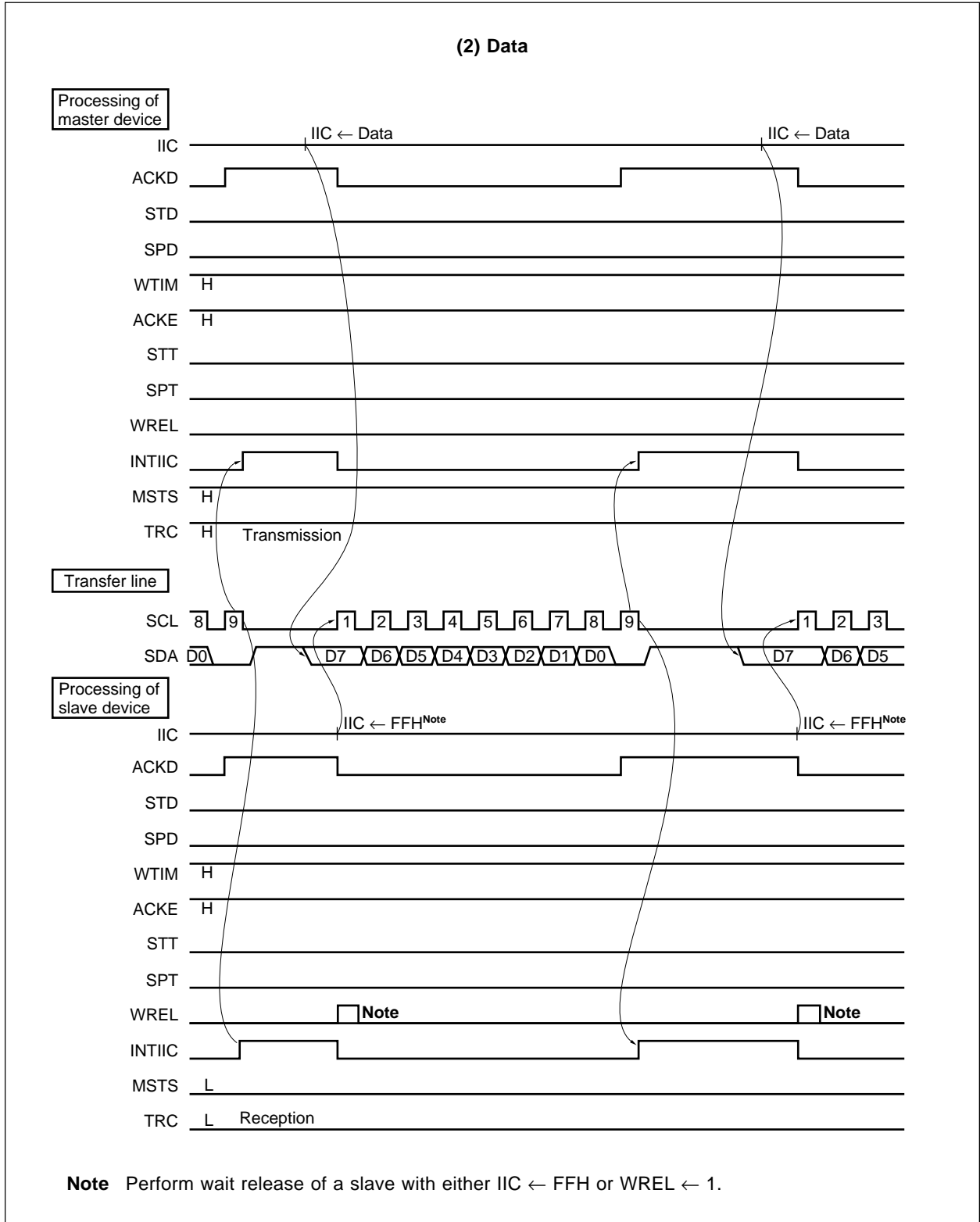


Figure 8-27. Example of Master → Slave Communication
(9-clock wait is selected both for master and slave) (3/3)

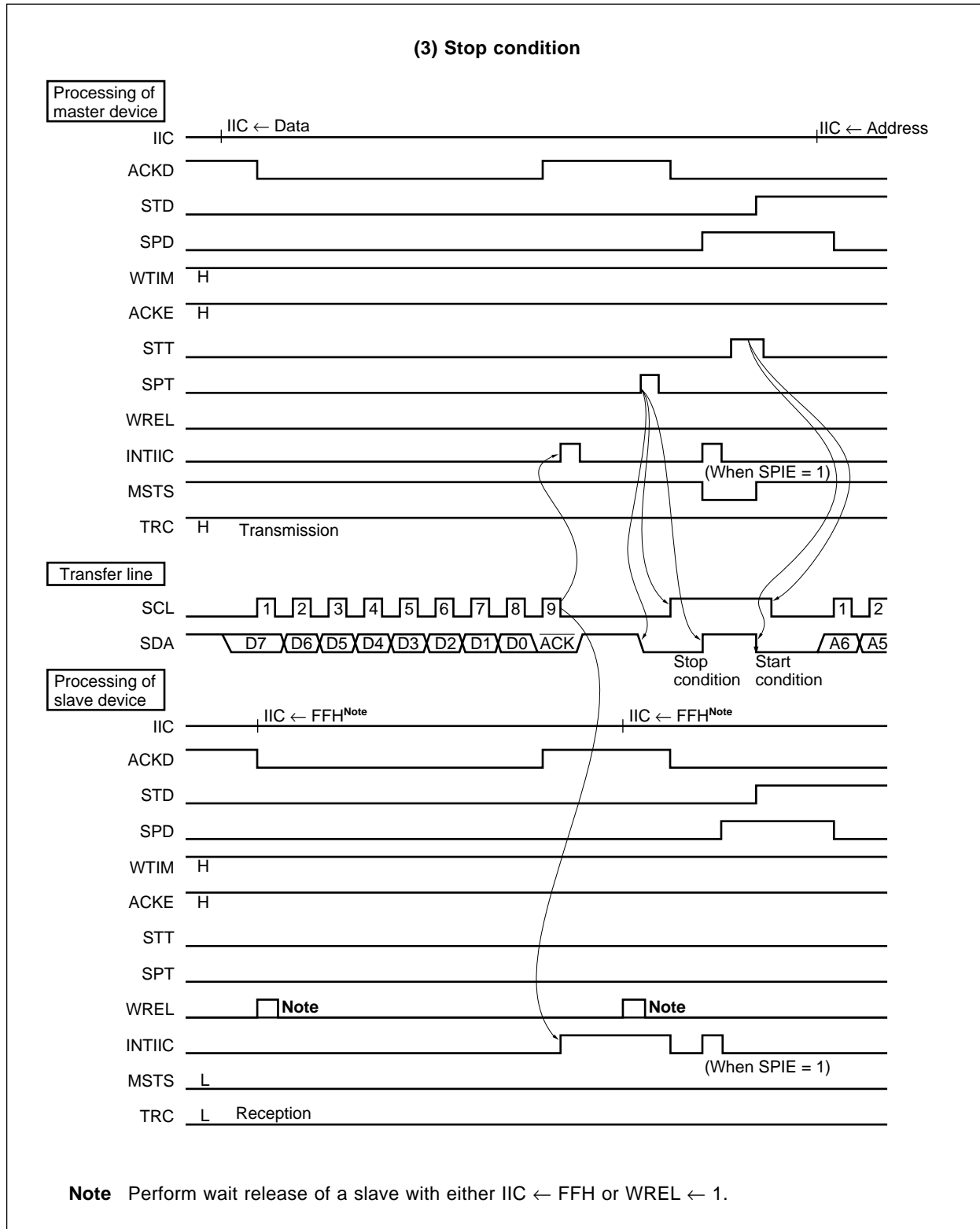


Figure 8-28. Example of Slave → Master Communication
(9-clock wait is selected both for master and slave) (1/3)

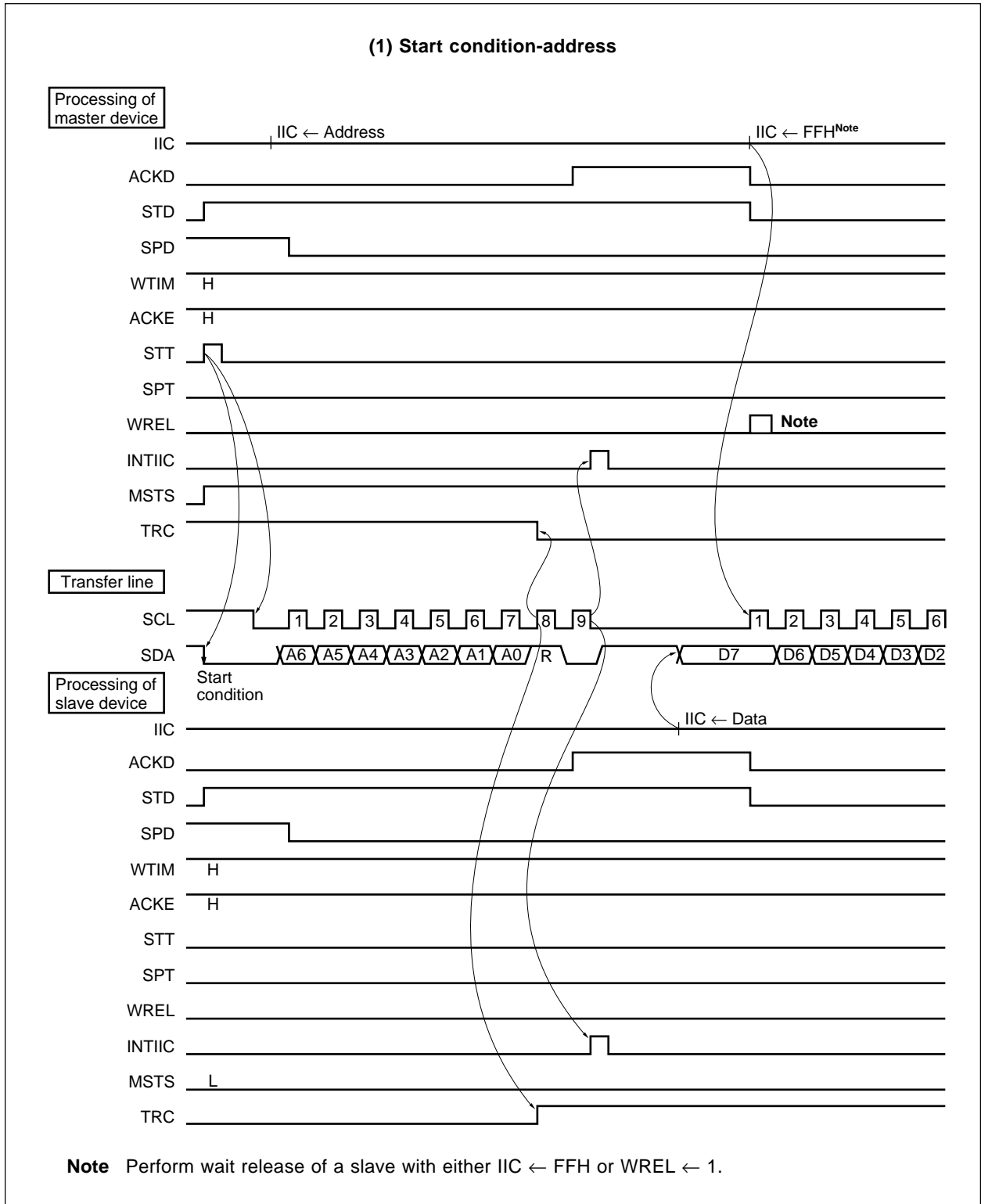
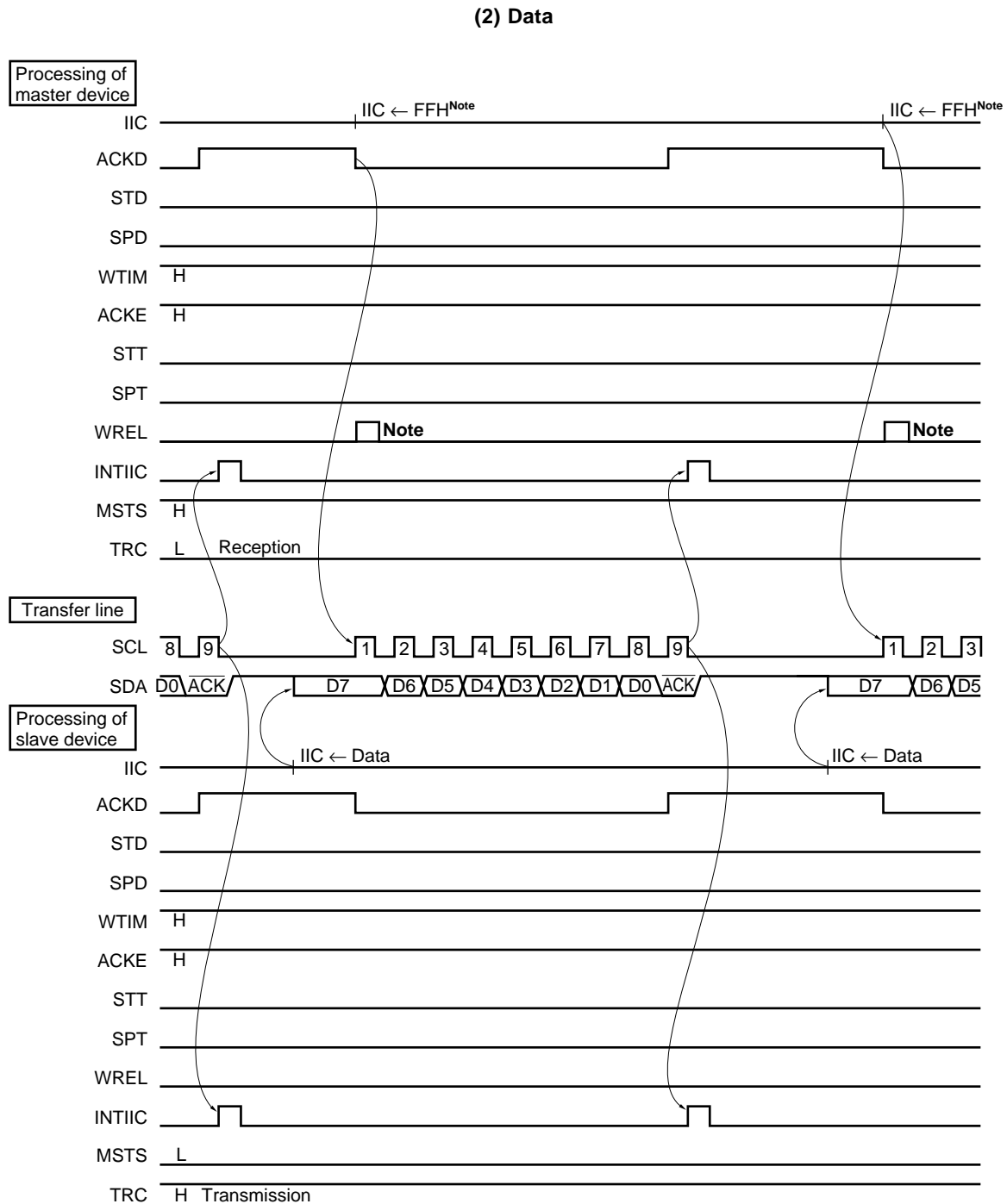
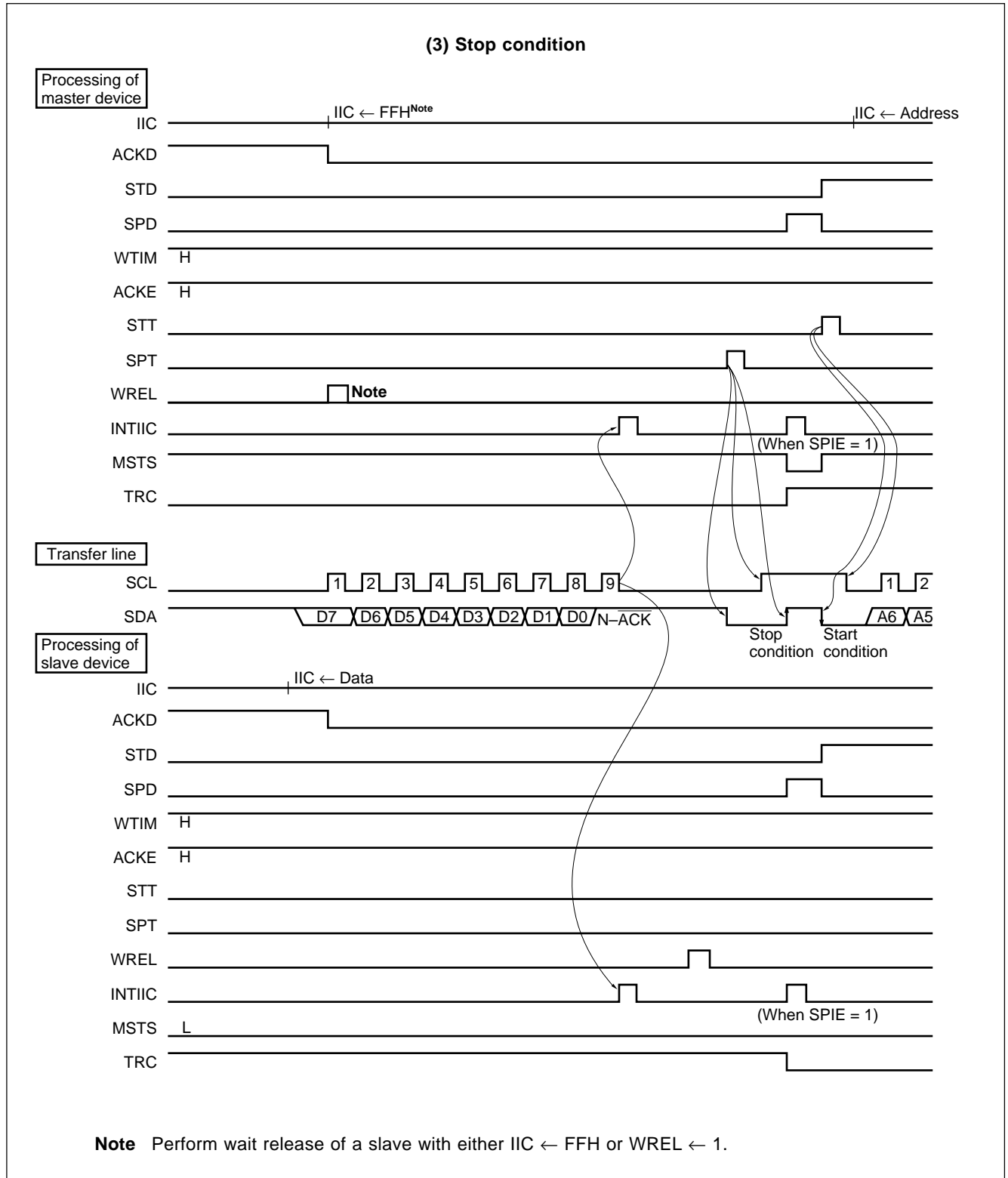


Figure 8-28. Example of Slave → Master Communication
(9-clock wait is selected both for master and slave) (2/3)



Note Perform wait release of a slave with either $IIC \leftarrow FFH$ or $WREL \leftarrow 1$.

Figure 8-28. Example of Slave → Master Communication
(9-clock wait is selected both for master and slave) (3/3)



8.5 Baud Rate Generator 0 to 3 (BRG0 to BRG3)

8.5.1 Configuration and function

The serial clock of the serial interface can be selected from the baud rate generator output or ϕ (internal system clock) for each channel.

A baud rate generator is provided with the following four systems, which can be set independently.

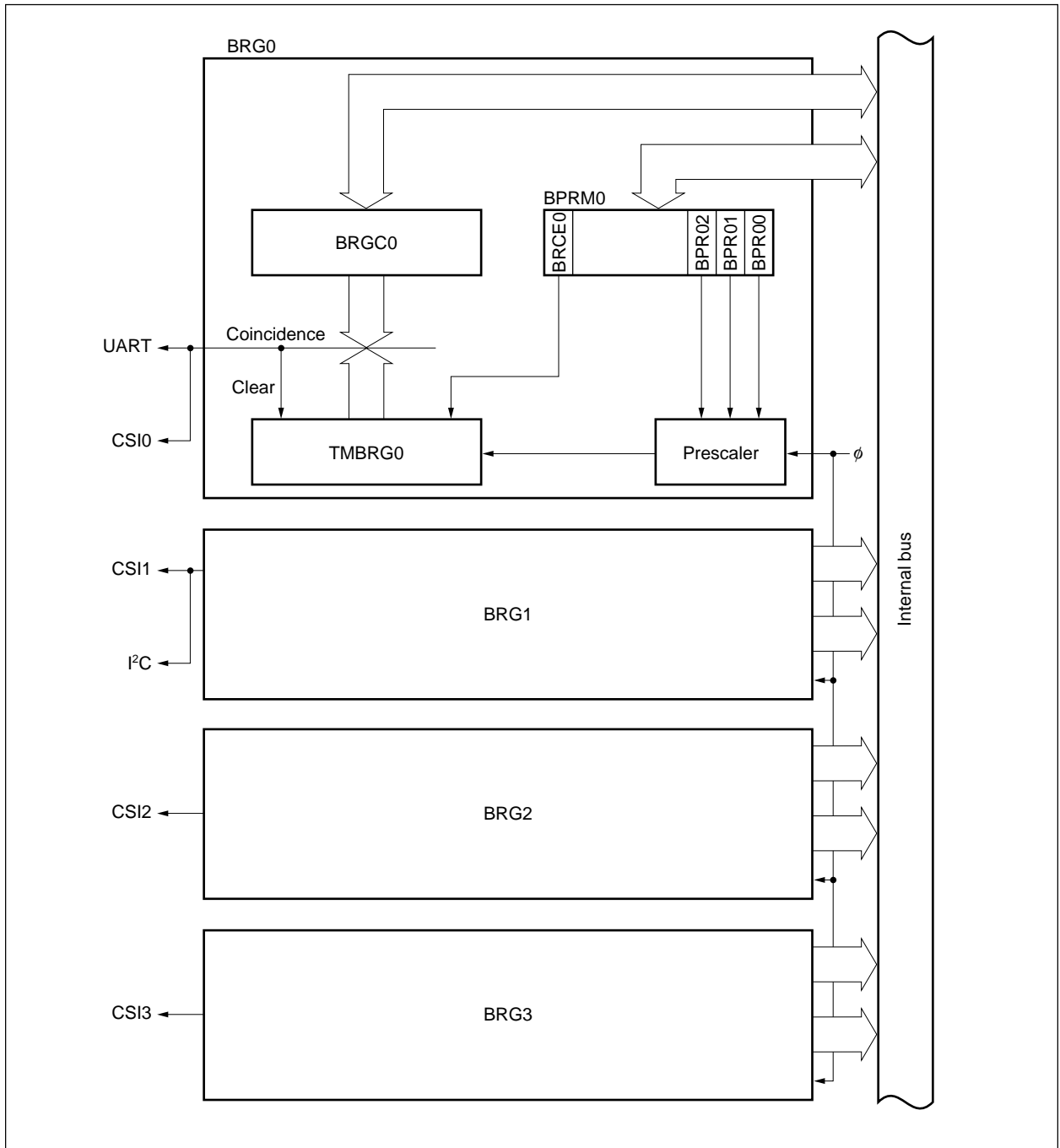
- For UART/CSI0 (BRG0)
- For I²C/CSI1 (BRG1)
- For CSI2 (BRG2)
- For CSI3 (BRG3)

The serial clock source for the UART is specified by the SCLS bits of the ASIMn registers. The serial clock source for the CSI is specified by the CLS bits of the CSIMn registers.

When the output of the baud rate generator is specified, the baud rate generator will be used as the clock source.

Because the serial clock for transmission/reception is shared by both the transmission and reception portions, the same baud rate is used for both transmission and reception.

Figure 8-29. Block Diagram of Baud Rate Generator



(1) Dedicated baud rate generators (BRG0 to BRG3)

The dedicated baud rate generators (BRGn) consist of an 8-bit timer (TMBRGn) that generates a serial clock for transmission/reception, a compare register (BRGCn), and a prescaler (n = 0 to 3).

(a) Input clock

Internal system clock (ϕ) is input to the BRGn.

(b) Set-up value of BRGn

(i) UART

If the dedicated baud rate generator is specified for UART as a serial clock source, the actual baud rate can be calculated by the following expression, because a sample rate of x16 is used:

$$\text{Baud rate} = \frac{\phi}{m \times 2^k \times 16 \times 2} \quad [\text{bps}]$$

where,

ϕ : Internal system clock frequency [Hz]

m: BRGC0 set-up value ($1 \leq m \leq 256^{\text{Note}}$)

k: BPR00 to BPR02 prescaler set-up value

Note 256 is set by writing 0 to the BRGC0 register.

(ii) CSI0 to CSI3

If the dedicated baud rate generator is specified for CSIn, the actual baud rate can be calculated by the following expression (n = 0 to 3):

$$\text{Baud rate} = \frac{\phi}{m \times 2^k \times 2} \quad [\text{bps}]$$

where,

ϕ : Internal system clock frequency [Hz]

m: BRGCn set-up value ($1 \leq m \leq 256^{\text{Note 1}}$)

k: BPRn0 to BPRn2 prescaler set-up value^{Note 2}

Notes 1. m = 256 is set by writing 0 to the BRGCn register.

2. Setting k = 0 is prohibited.

Table 8-6 shows the setup values of the baud rate generator when the typical clocks are used.

Table 8-6. Baud Rate Generators 0 to 3 Set-up Values (when typical clocks are used) (1/2)

(a) UART

Baud Rate [bps]	$\phi = 33 \text{ MHz}$			$\phi = 25 \text{ MHz}$			$\phi = 16 \text{ MHz}$			$\phi = 12.5 \text{ MHz}$		
	BPR	BRGC	Error	BPR	BRGC	Error	BPR	BRGC	Error	BPR	BRGC	Error
110	—	—	—	5	222	0.02%	5	142	0.03%	4	222	0.02%
150	5	215	0.07%	5	163	0.15%	4	208	0.16%	4	163	0.15%
300	4	215	0.07%	4	163	0.15%	3	208	0.16%	3	163	0.15%
600	3	215	0.07%	3	163	0.15%	2	208	0.16%	2	163	0.15%
1200	2	215	0.07%	2	163	0.15%	1	208	0.16%	1	163	0.15%
2400	1	215	0.07%	1	163	0.15%	0	208	0.16%	0	162	0.47%
4800	0	215	0.07%	0	163	0.15%	0	104	0.16%	0	82	0.76%
9600	0	107	0.39%	0	81	0.47%	0	52	0.16%	0	40	1.73%
10400	0	100	0.84%	0	75	0.16%	0	48	0.16%	0	38	1.16%
19200	0	54	0.54%	0	41	0.72%	0	26	0.16%	0	20	1.73%
31250	0	33	0.00%	0	25	0.00%	0	16	0.00%	0	13	3.85%
38400	0	27	0.54%	0	20	1.73%	0	13	0.16%	0	10	1.73%
76800	0	13	3.29%	0	10	1.73%	0	6	6.99% ^{Note}	0	5	1.73%
153600	0	7	1.30%	0	5	1.73%	0	3	8.51% ^{Note}	—	—	—

Baud Rate [bps]	$\phi = 19.660 \text{ MHz}$			$\phi = 14.746 \text{ MHz}$			$\phi = 12.288 \text{ MHz}$			$\phi = 9.830 \text{ MHz}$		
	BPR	BRGC	Error	BPR	BRGC	Error	BPR	BRGC	Error	BPR	BRGC	Error
110	5	176	0.83%	5	131	0.07%	4	218	0.08%	4	176	0.02%
150	5	128	0.00%	4	192	0.00%	4	160	0.00%	4	128	0.00%
300	4	128	0.00%	3	192	0.00%	3	160	0.00%	3	128	0.00%
600	3	128	0.00%	2	192	0.00%	2	160	0.00%	2	128	0.00%
1200	2	128	0.00%	1	192	0.00%	1	160	0.00%	1	128	0.00%
2400	1	128	0.00%	0	192	0.00%	0	160	0.00%	0	128	0.00%
4800	0	128	0.00%	0	96	0.00%	0	80	0.00%	0	64	0.00%
9600	0	64	0.00%	0	48	0.00%	0	40	0.00%	0	32	0.00%
10400	0	60	1.54%	0	44	0.70%	0	37	0.21%	0	30	1.54%
19200	0	32	0.00%	0	24	0.00%	0	20	0.00%	0	16	0.00%
31250	0	20	1.70%	0	15	1.69%	0	12	2.40%	0	10	1.70%
38400	0	16	0.00%	0	12	0.00%	0	10	0.00%	0	8	0.00%
76800	0	8	0.00%	0	6	0.00%	0	5	0.00%	0	4	0.00%
153600	0	4	0.00%	0	3	0.00%	—	—	—	0	2	0.00%
307200	0	2	0.00%	—	—	—	—	—	—	0	1	0.00%
614400	0	1	0.00%	—	—	—	—	—	—	—	—	—

Note Cannot be used because the error is too great.

Remark ϕ : Internal system clock

Table 8-6. Baud Rate Generators 0 to 3 Set-up Values (when typical clocks are used) (2/2)

(b) CSI

Baud Rate [bps]	$\phi = 33 \text{ MHz}$			$\phi = 25 \text{ MHz}$			$\phi = 16 \text{ MHz}$			$\phi = 12.5 \text{ MHz}$		
	BPR	BRGC	Error	BPR	BRGC	Error	BPR	BRGC	Error	BPR	BRGC	Error
1760	—	—	—	5	222	0.02%	5	142	0.03%	4	222	0.02%
2400	5	215	0.07%	5	163	0.15%	4	208	0.16%	4	163	0.15%
4800	4	215	0.07%	4	163	0.15%	3	208	0.16%	3	163	0.15%
9600	3	215	0.07%	3	163	0.15%	2	208	0.16%	2	163	0.15%
19200	2	215	0.07%	2	163	0.15%	1	208	0.16%	1	163	0.15%
38400	1	215	0.07%	1	163	0.15%	1	104	0.16%	1	81	0.47%
76800	1	107	0.39%	1	81	0.47%	1	52	0.16%	1	41	0.76%
153600	1	54	0.54%	1	41	0.76%	1	26	0.16%	1	20	1.73%
166400	1	50	0.84%	1	38	1.16%	1	24	0.16%	1	19	1.16%
307200	1	27	0.54%	1	20	1.73%	1	13	0.16%	1	10	1.73%
614400	1	13	3.29%	1	10	1.73%	1	7	6.99% ^{Note}	1	5	1.73%
1228800	1	7	4.09%	1	5	1.73%	—	—	—	1	3	15.2% ^{Note}
2457600	1	3	11.30% ^{Note}	1	2	27.2% ^{Note}	—	—	—	—	—	—

Baud Rate [bps]	$\phi = 20 \text{ MHz}$			$\phi = 14.746 \text{ MHz}$			$\phi = 12.288 \text{ MHz}$			$\phi = 9.830 \text{ MHz}$		
	BPR	BRGC	Error	BPR	BRGC	Error	BPR	BRGC	Error	BPR	BRGC	Error
1760	5	178	0.25%	5	131	0.07%	4	218	0.08%	4	176	0.26%
2400	5	130	0.16%	4	192	0.00%	4	160	0.00%	4	128	0.00%
4800	4	130	0.16%	3	192	0.00%	3	160	0.00%	3	128	0.00%
9600	3	130	0.16%	2	192	0.00%	2	160	0.00%	2	128	0.00%
19200	2	130	0.16%	1	192	0.00%	1	160	0.00%	1	128	0.00%
38400	1	130	0.16%	1	96	0.00%	1	80	0.00%	1	64	0.00%
76800	1	65	0.16%	1	48	0.00%	1	40	0.00%	1	32	0.00%
153600	1	33	1.36%	1	24	0.00%	1	20	0.00%	1	16	0.00%
166400	1	30	0.16%	1	22	0.70%	1	18	2.60%	1	15	1.50%
307200	1	16	1.73%	1	12	0.00%	1	10	0.00%	1	8	0.00%
614400	1	8	1.73%	1	6	0.00%	1	5	0.00%	1	4	0.00%
1228800	1	4	1.73%	1	3	0.00%	1	3	16.7% ^{Note}	1	2	0.00%
2457600	1	2	1.73%	1	2	25% ^{Note}	—	—	—	1	1	0.00%

Note Cannot be used because the error is too great.

Remark ϕ : Internal system clock

(c) Error of baud rate

The error of the baud rate is calculated as follows:

$$\text{Error [\%]} = \left(\frac{\text{Actual baud rate (baud rate with error)}}{\text{Desired baud rate (normal baud rate)}} - 1 \right) \times 100$$

Example: $(9520/9600 - 1) \times 100 = -0.833 \text{ [\%]}$
 $(5000/4800 - 1) \times 100 = +4.167 \text{ [\%]}$

(2) Allowable error range of baud rate

The allowable error range depends on the number of bits of one frame.

The basic limit is $\pm 5\%$ of baud rate error and $\pm 4.5\%$ of sample timing with an accuracy of 16 bits. However, the practical limit should be $\pm 2.3 \%$ of baud rate error, assuming that both the transmission and reception sides contain an error.

8.5.2 Baud rate generator compare registers 0 to 3 (BRGC0 to BRGC3)

These are 8-bit compare registers that set a timer/count value for the dedicated baud rate generator.

These registers can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
BRGC0	BRG07	BRG06	BRG05	BRG04	BRG03	BRG02	BRG01	BRG00	Address FFFFF084H	After reset Undefined
BRGC1	BRG17	BRG16	BRG15	BRG14	BRG13	BRG12	BRG11	BRG10	Address FFFFF094H	After reset Undefined
BRGC2	BRG27	BRG26	BRG25	BRG24	BRG23	BRG22	BRG21	BRG20	Address FFFFF0A4H	After reset Undefined
BRGC3	BRG37	BRG36	BRG35	BRG34	BRG33	BRG32	BRG31	BRG30	Address FFFFF0B4H	After reset Undefined

Caution The internal timer (TMBRGN) is cleared by writing the BRGC registers. Therefore, do not rewrite or program the BRGCn registers during transmission/reception operation.

Remark n = 0 to 3

8.5.3 Baud rate generator prescaler mode registers 0 to 3 (BPRM0 to BPRM3)

These registers control the timer/count operation of the dedicated baud rate generator and select a count clock. They can be read/written in 8- or 1-bit units.

BPRM0	7	6	5	4	3	2	1	0	Address FFFFF086H	After reset 00H
	BRCE0	0	0	0	0	BPR02	BPR01	BPR00		
BPRM1	7	6	5	4	3	2	1	0	Address FFFFF096H	After reset 00H
	BRCE1	0	0	0	0	BPR12	BPR11	BPR10		
BPRM2	7	6	5	4	3	2	1	0	Address FFFFF0A6H	After reset 00H
	BRCE2	0	0	0	0	BPR22	BPR21	BPR20		
BPRM3	7	6	5	4	3	2	1	0	Address FFFFF0B6H	After reset 00H
	BRCE3	0	0	0	0	BPR32	BPR31	BPR30		

Bit Position	Bit Name	Function																																
7	BRCEn	Baud Rate Generator Count Enable Controls count operation of BRGn. 0 : Stops count operation with cleared 1 : Enables count operation																																
2 to 0	BPRn3 to BPRn0	Baud Rate Generator Prescaler Specifies count clock input to internal timer (TMBRGn). <table border="1"><thead><tr><th>BPRn2</th><th>BPRn1</th><th>BPRn0</th><th>Count Clock</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>ϕ (k = 0): CSI use disabled</td></tr><tr><td>0</td><td>0</td><td>1</td><td>$\phi/2$ (k = 1)</td></tr><tr><td>0</td><td>1</td><td>0</td><td>$\phi/4$ (k = 2)</td></tr><tr><td>0</td><td>1</td><td>1</td><td>$\phi/8$ (k = 3)</td></tr><tr><td>1</td><td>0</td><td>0</td><td>$\phi/16$ (k = 4)</td></tr><tr><td>1</td><td>0</td><td>1</td><td>$\phi/32$ (k = 5)</td></tr><tr><td colspan="3">Others</td><td>Setting prohibited</td></tr></tbody></table> <p>k: Set value of prescaler, ϕ: Internal system clock</p>	BPRn2	BPRn1	BPRn0	Count Clock	0	0	0	ϕ (k = 0): CSI use disabled	0	0	1	$\phi/2$ (k = 1)	0	1	0	$\phi/4$ (k = 2)	0	1	1	$\phi/8$ (k = 3)	1	0	0	$\phi/16$ (k = 4)	1	0	1	$\phi/32$ (k = 5)	Others			Setting prohibited
BPRn2	BPRn1	BPRn0	Count Clock																															
0	0	0	ϕ (k = 0): CSI use disabled																															
0	0	1	$\phi/2$ (k = 1)																															
0	1	0	$\phi/4$ (k = 2)																															
0	1	1	$\phi/8$ (k = 3)																															
1	0	0	$\phi/16$ (k = 4)																															
1	0	1	$\phi/32$ (k = 5)																															
Others			Setting prohibited																															

Caution Do not change the count clock during transmission/reception operation.

Remark n = 0 to 3

8.6 Selection of Operational Serial Interface

CSI0 and CSI1 of the V854 are alternate pins for UART and I²C. Therefore, they are used selecting either UART or I²C.

The selection is made by the following registers.

(1) Selecting CSI0 or UART

The setting is made by the ASIM0 register and the CSIM0 register.

ASIM0 Register		CSIM0 Register		Selection of Operational Peripheral I/O
TXE	RXE	CTXE0	CRXE0	
0	0	0	0	Operation stops
0	1	0	0	Selects UART
1	0	0	0	
1	1	0	0	
0	0	0	1	Selects CSI
0	0	1	0	
0	0	1	1	
Others				Setting prohibited

(2) Selecting CSI1 or I²C

The setting is made by the IICC register and the CSIM1 register.

IICC Register	CSIM1 Register		Selection of Operational Peripheral I/O
IICE	CTXE1	CRXE1	
0	0	0	Operation stops
1	0	0	Selects I ² C
0	0	1	Selects CSI
0	1	0	
0	1	1	
Others			Setting prohibited

[MEMO]

CHAPTER 9 A/D CONVERTER

9.1 Features

- Analog input: 16 channels
- 8-bit A/D converter
- On-chip A/D conversion result register (ADCR0 to ADCR7)
8 bits x 8
- A/D conversion trigger mode
 - A/D trigger mode
 - Timer trigger mode
 - External trigger mode
- Sequential conversion

9.2 Configuration

The A/D converter of the V854 adopts the sequential conversion method, and uses the A/D converter mode registers (ADM0, ADM1), and ADCRn register to perform A/D conversion operations (n = 0 to 7).

(1) Input circuit

Selects the analog input (ANI0 to ANI15) according to the mode set to the ADM0 and ADM1 registers and then sends it to the sample and hold circuit.

(2) Sample and hold circuit

Samples the analog input sent from the input circuit one by one and sends it to the comparator. During A/D conversion operations, holds the analog input sampled.

(3) Voltage comparator

Compares the voltage difference between the input analog input and voltage tap of the serial resistor string output.

(4) Serial resistor string

Generates voltage to coincide with analog input.

The serial resistor string is connected between the reference voltage pin for A/D converter (AV_{REF}) and GND pin for A/D converter (AV_{SS}). The serial resistor consists of 255 equivalent resistors and two resistors with half the resistance so that the connection between the two pins is made of 256 equal voltage steps.

The voltage tap of the serial resistor string is selected by a tap selector controlled by the successive approximation register (SAR).

(5) Successive approximation register (SAR)

8-bit register for setting data for which the value of the voltage tap of the serial resistor string coincides with the voltage value of the analog input from the most significant bit (MSB) in 1-bit units.

When the setting is made to the least significant bit (LSB) (A/D conversion ends), the contents of the SAR (conversion result) are held in the A/D conversion result register (ADCRn).

(6) A/D Conversion Result Register n (ADCRn)

8-bit register for retaining the A/D conversion result. The conversion result is loaded from the sequential conversion register (SAR) each time A/D conversion ends.

This register becomes undefined by $\overline{\text{RESET}}$ input.

(7) Controller

Selects the analog input, generates the sample hold circuit operation timing, and controls the conversion trigger according to the mode set to the ADM0/ADM1 register.

(8) ANI0 to ANI15 pins

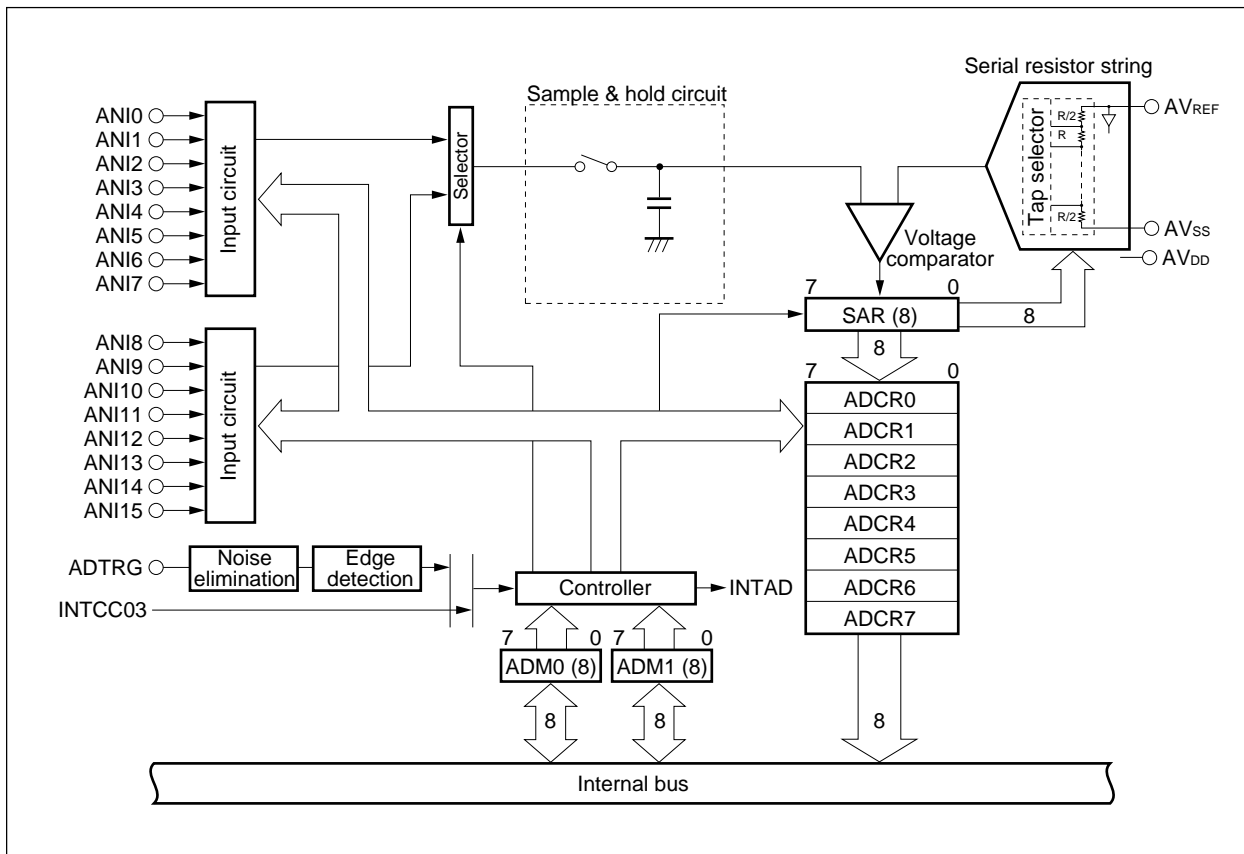
16-channel analog input pins for the A/D converter. Input the analog signal to be A/D converted.

Caution Use ANI0 to ANI15 input voltages within the specification. Especially, if the voltage exceeding V_{DD} or less than V_{SS} (even if it is within the range of the absolute maximum rating) is input, the conversion value of the channel may become undefined or the conversion value of other channels may be affected.

(9) AVREF pin

Pin for inputting the reference voltage of the A/D converter. Converts signals input to the ANI0 to ANI15 pins to digital signals based on the voltage applied between AV_{REF} and AV_{SS} .

Figure 9-1. Block Diagram of A/D Converter



9.3 Control Register

(1) A/D converter mode register 0 (ADM0)

The ADM0 register is an 8-bit register which executes the selection of the analog input pin, specification of the operation mode, and conversion operations.

This register can be read/written in 8- or 1-bit units. However, when the data is written to the ADM0 register during A/D conversion operations, the conversion operation is initialized and conversion is executed from the beginning. Bit 6 cannot be written in and writing executed is ignored.

	7	6	5	4	3	2	1	0		
ADM0	CE	CS	BS	MS	PS	ANIS2	ANIS1	ANIS0	Address FFFFFF380H	After reset 00H

Bit Position	Bit Name	Function
7	CE	Convert Enable Enables or disables A/D conversion operation. 0: Disabled 1: Enabled
6	CS	Converter Status Indicates the status of A/D converter. This bit is read only. 0: Stops 1: Operates
5	BS	Buffer Select Specifies buffer mode in the select mode. 0: 1-buffer mode 1: 4-buffer mode
4	MS	Mode Select Specifies operation mode of A/D converter. 0: Scan mode 1: Select mode
3	PS	Pin Select Switches the analog input pin. 0: Selects ANI0 to ANI7 1: Selects ANI8 to ANI15

Bit Position	Bit Name	Function				
2 to 0	ANIS2 to ANIS0	Analog Input Select Specifies analog input pin to A/D convert.				
		ANIS2	ANIS1	ANIS0	Select Mode	Scan Mode
		0	0	0	ANI0/ANI8	ANI0/ANI8
		0	0	1	ANI1/ANI9	ANI0, ANI1/ANI8, ANI9
		0	1	0	ANI2/ANI10	ANI0 to ANI2/ANI8 to ANI10
		0	1	1	ANI3/ANI11	ANI0 to ANI3/ANI8 to ANI11
		1	0	0	ANI4/ANI12	ANI0 to ANI4/ANI8 to ANI12
		1	0	1	ANI5/ANI13	ANI0 to ANI5/ANI8 to ANI13
		1	1	0	ANI6/ANI14	ANI0 to ANI6/ANI8 to ANI14
		1	1	1	ANI7/ANI15	ANI0 to ANI7/ANI8 to ANI15

Caution When the CE bit is 1 in the timer trigger mode and external trigger mode, the trigger signal standby state is set. To clear the CE bit, write “0” or reset.

In the A/D trigger mode, the conversion trigger is set by writing 1 to the CE bit. After the operation, when the mode is changed to the timer trigger mode or external trigger mode without clearing the CE bit, the trigger input standby state is set immediately after the change.

(2) A/D converter mode register 1 (ADM1)

The ADM1 register is an 8-bit register which specifies the conversion operation time and trigger mode.

This register can be read/written in 8- or 1-bit units. However, when the data is written to the ADM1 register during A/D conversion, the conversion operation is initialized and conversion is executed from the beginning again.

	7	6	5	4	3	2	1	0		
ADM1	0	0	TRG1	TRG0	0	FR2	FR1	FR0	Address FFFFF382H	After reset 07H

Bit Position	Bit Name	Function
5 and 4	TRG1 and TRG0	Trigger Mode Specifies trigger mode.
2 to 0	FR2 to FR0	Frequency Specifies conversion operation time.

(3) A/D conversion result register (ADCR0 to ADCR7)

The ADCRn register is an 8-bit register holding the A/D conversion results. It is provided with eight 8-bit registers.

This register can only be read in 8-/1-bit units.

	7	6	5	4	3	2	1	0		
ADCRn	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	Address FFFFF390H to FFFFF39EH	After reset Undefined

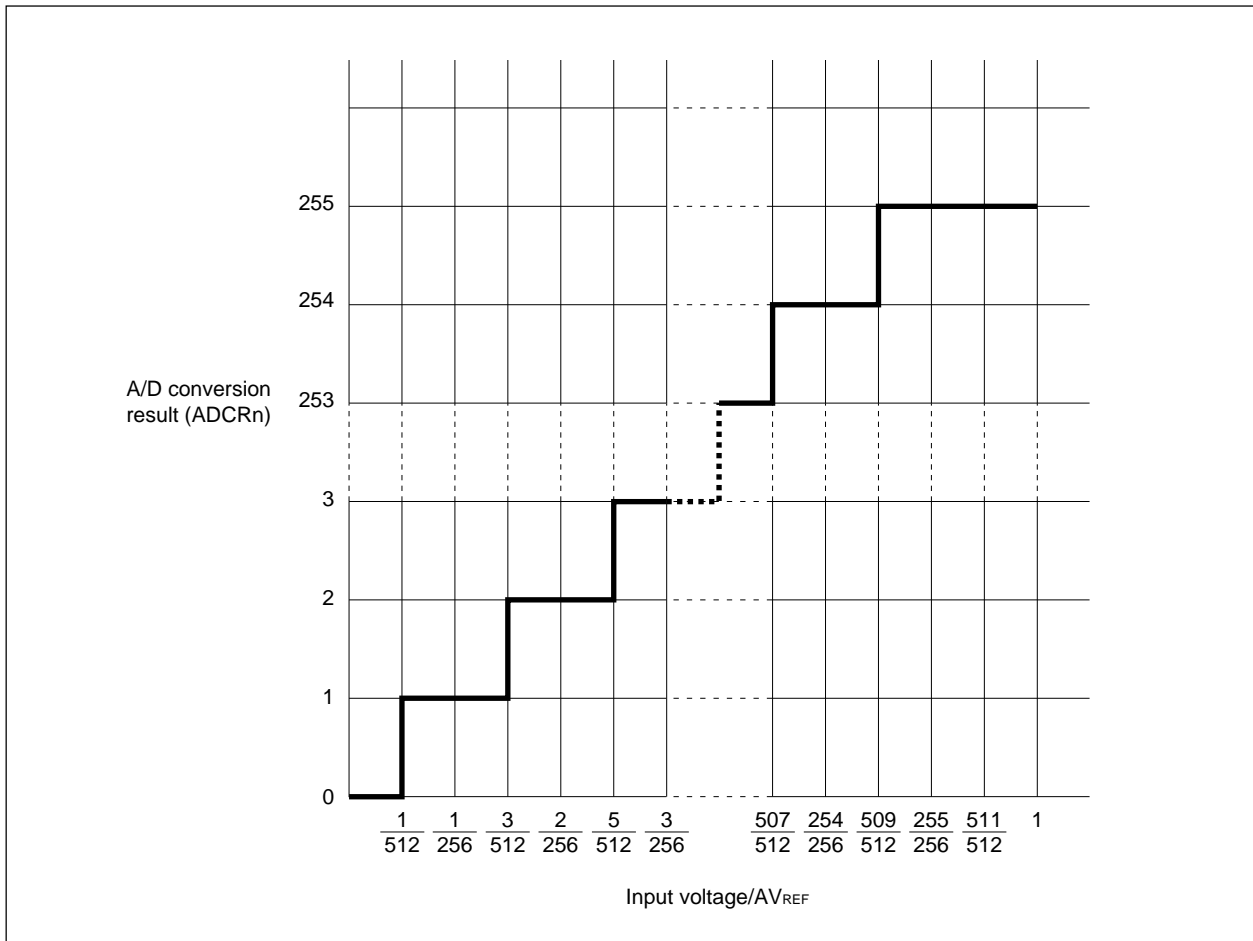
Remark n = 0 to 7

The following shows the correspondence of each analog input pin to the ADCRn register (except 4-buffer mode).

Analog Input Pin		ADCRn Register
PS = 0	PS =1	
ANI0	ANI8	ADCR0
ANI1	ANI9	ADCR1
ANI2	ANI10	ADCR2
ANI3	ANI11	ADCR3
ANI4	ANI12	ADCR4
ANI5	ANI13	ADCR5
ANI6	ANI14	ADCR6
ANI7	ANI15	ADCR7

Figure 9-2 shows the relation between the analog input voltage and the A/D conversion result.

Figure 9-2. Relation between Analog Input Voltage and A/D Conversion Result



9.4 A/D Converter Operation

9.4.1 Basic operation of A/D converter

A/D conversion is executed in the following order.

- (1) The selection of the analog input and specification of the operation mode and trigger mode, etc., should be set in the ADMn register^{Note 1} (n = 0, 1).
When the CE bit of the ADM0 register is set (1), A/D conversion starts during the A/D trigger mode. During the timer trigger mode and external trigger mode, the trigger standby state^{Note 2} is set.
- (2) The voltage generated from the voltage tap of the serial resistor string and analog input are compared by the comparator.
- (3) When the comparison of the 8 bits ends, the conversion results are stored in the ADCRn register. When A/D conversion is performed for the specified number of times, the A/D conversion end interrupt (INTAD) is generated (n = 0 to 7).

- Notes**
1. When the ADMn register (n = 0, 1) is changed during A/D conversion, the A/D conversion operation started before the change is stopped and the conversion results are not stored in the ADCRn register (n = 0 to 7).
 2. During the timer trigger mode and external trigger mode, if the CE bit of the ADM0 register is set to 1, the mode changes to the trigger standby state. The A/D conversion operation is started by the trigger signal, and the trigger standby state is returned when the A/D conversion operation ends.

9.4.2 Operation mode and trigger mode

The A/D converter can specify various conversion operations by specifying the operation mode and trigger mode. The operation mode and trigger mode are set by the ADMn register (n = 0, 1).

The following shows the relation between the operation mode and trigger mode.

	Trigger Mode	Operation Mode		Setting Value		Analog Input
				ADM0	ADM1	
★	A/D trigger	Select	1 buffer	xx01xxxxB	00000xxxB	ANI0 to ANI15
			4 buffers	xx11xxxxB	00000xxxB	
		Scan		xxx0xxxxB	00000xxxB	
★	Timer trigger	Select	1 buffer	xx01xxxxB	00010xxxB	
			4 buffers	xx11xxxxB	00010xxxB	
		Scan		xxx0xxxxB	00010xxxB	
★	External trigger	Select	1 buffer	xx01xxxxB	00100xxxB	
			4 buffers	xx11xxxxB	00100xxxB	
		Scan		xxx0xxxxB	00100xxxB	

(1) Trigger mode

There are three types of trigger modes which serve as the start timing of A/D conversion processing: A/D trigger mode, timer trigger mode, and external trigger mode. These trigger modes are set by the ADM0 register.

(a) A/D trigger mode

Generates the conversion timing of the analog input for the ANI0 to ANI15 pins inside the A/D converter unit.

(b) Timer trigger mode

Specifies the conversion timing of the analog input set for the ANI0 to ANI15 pins using the values set to the RPU compare register.

This register creates the analog input conversion timing by generating the coincidence interrupts of the capture/compare registers (CC03) connected to the 24-bit TM10.

(c) External trigger mode

Mode which specifies the conversion timing of the analog input to the ANI0 to ANI15 pins using the ADTRG pin.

(2) Operation mode

There are two types of operation modes which set the ANI0 to ANI15 pins: select mode and scan mode. The select mode has sub-modes including the one-buffer mode and four-buffer mode. These modes are set by the ADM0 register.

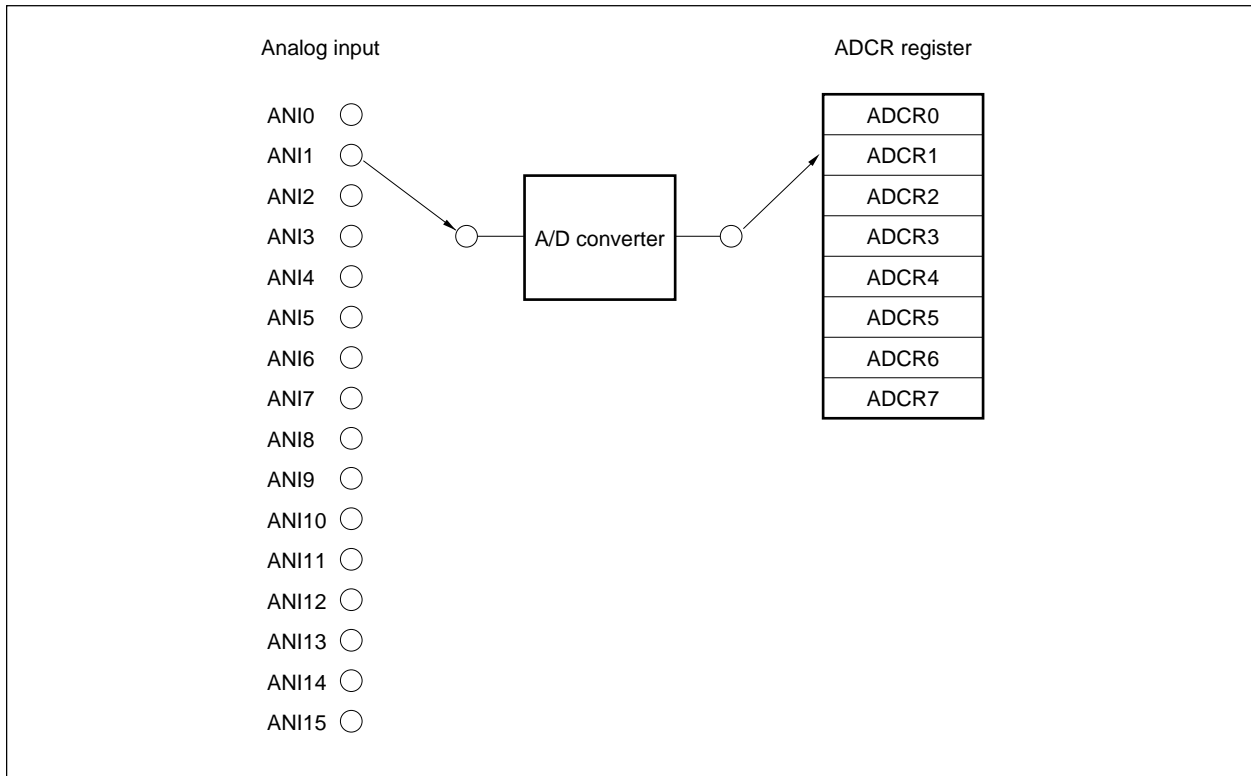
(a) Select mode

A/D converts one analog input specified by the ADM0 register. The conversion results are stored in the ADCRn register corresponding to the analog input (n = 0 to 7). For this mode, the one-buffer mode and four-buffer mode are provided for storing the A/D conversion results.

- **One-buffer mode**

A/D converts one analog input specified by the ADM0 register. The conversion results are stored in the ADCRn register corresponding to the analog input. The analog input and ADCRn register correspond one to one, and an A/D conversion end interrupt (INTAD) is generated each time one A/D conversion ends.

Figure 9-3. Operation Timing Example of Select Mode: 1-Buffer Mode (ANI1)



- **Four-buffer mode**

A/D converts one analog input four times and stores the results in the four registers corresponding to analog input. The A/D conversion end interrupt (INTAD) is generated when the four A/D conversions end.

Figure 9-4. Operation Timing Example of Select Mode: 4-Buffer Mode (ANI6) (1/2)

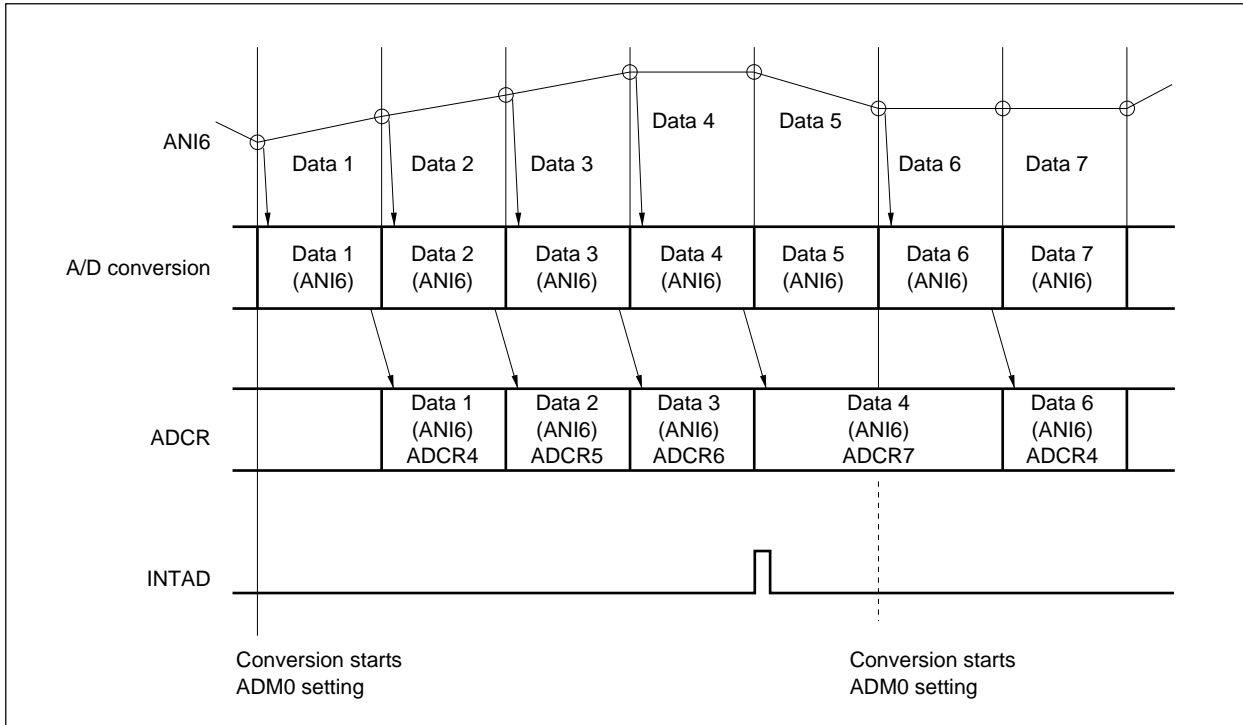
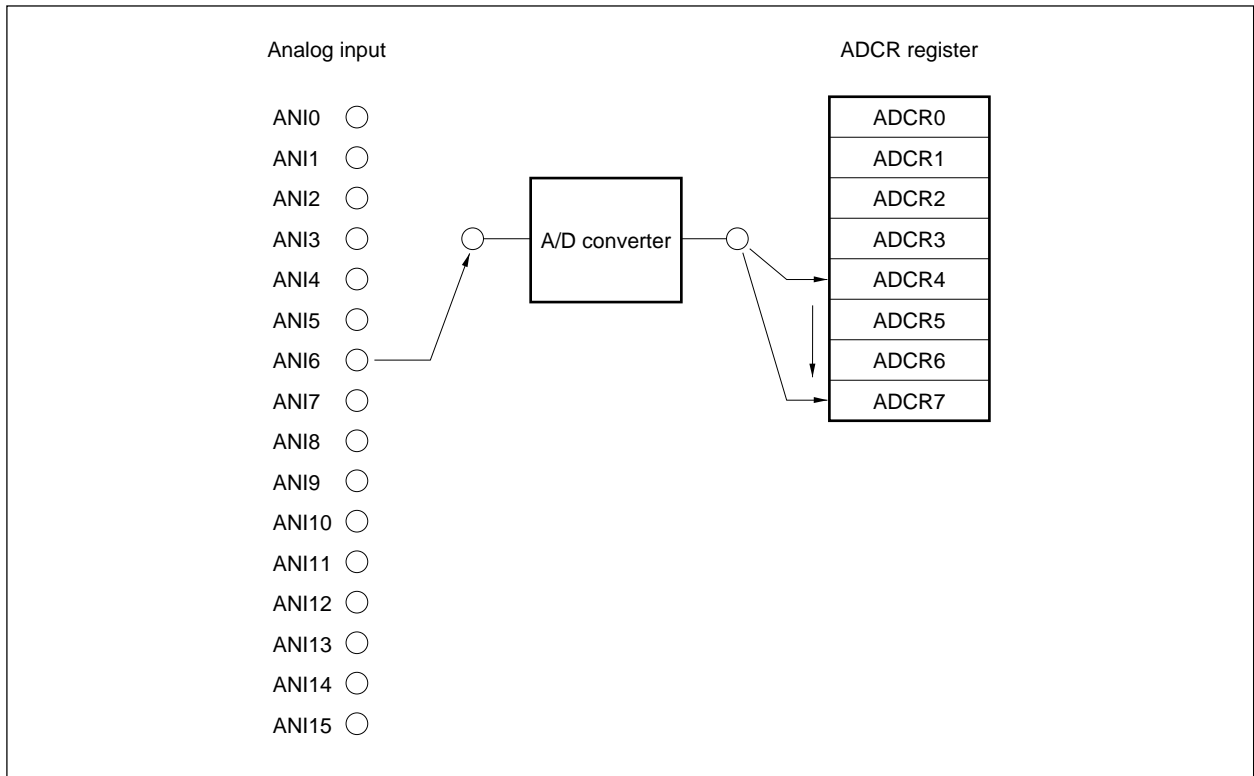


Figure 9-4. Operation Timing Example of Select Mode: 4-Buffer Mode (ANI6) (2/2)

(b) Scan mode

Selects the analog inputs specified by the ADM0 register sequentially from the ANI0 pin, and A/D conversion is executed. The A/D conversion results are stored in the ADCRn register corresponding to the analog input. When the conversion of the specified analog input ends, the INTAD interrupt is generated (n = 0 to 7).

Figure 9-5. Operation Timing Example of Scan Mode: 4-Channel Scan (ANI0 to ANI3) (1/2)

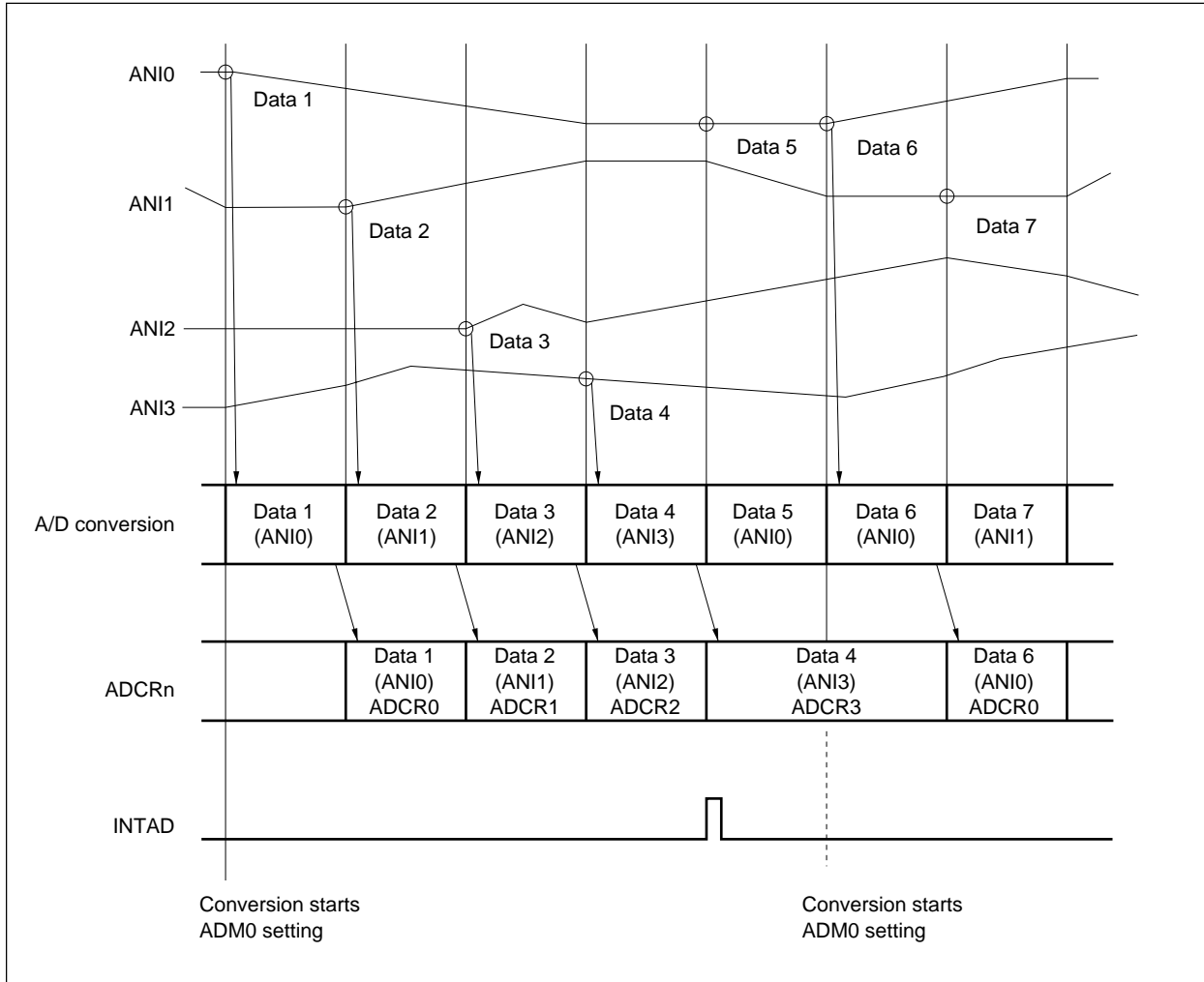
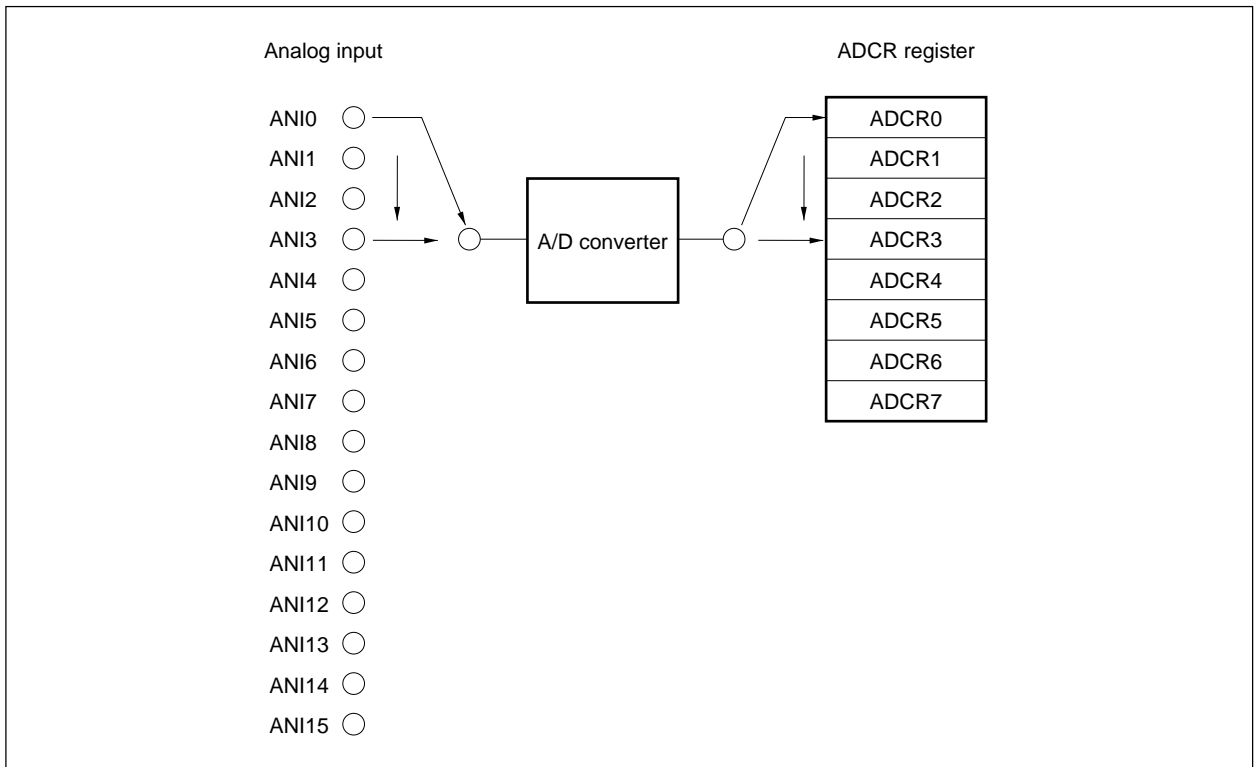


Figure 9-5. Operation Timing Example of Scan Mode: 4-Channel Scan (ANI0 to ANI3) (2/2)

9.5 Operation in the A/D Trigger Mode

When the CE bit of the ADM0 register is set to 1, A/D conversion is started.

9.5.1 Select mode operation

The A/D converter converts the analog input specified by the ADM0 register. The conversion results are stored in the ADCRn register corresponding to the analog input. In the select mode, the one-buffer mode and four-buffer mode are supported according to the storing method employed for the A/D conversion results (n = 0 to 7).

(1) 1-buffer mode (A/D trigger select: 1-buffer)

The A/D converter converts one analog input once. The conversion results are stored in one ADCRn register. The analog input and ADCRn register correspond one to one. (Refer to **Table 9-1**, **Figure 9-6**.)

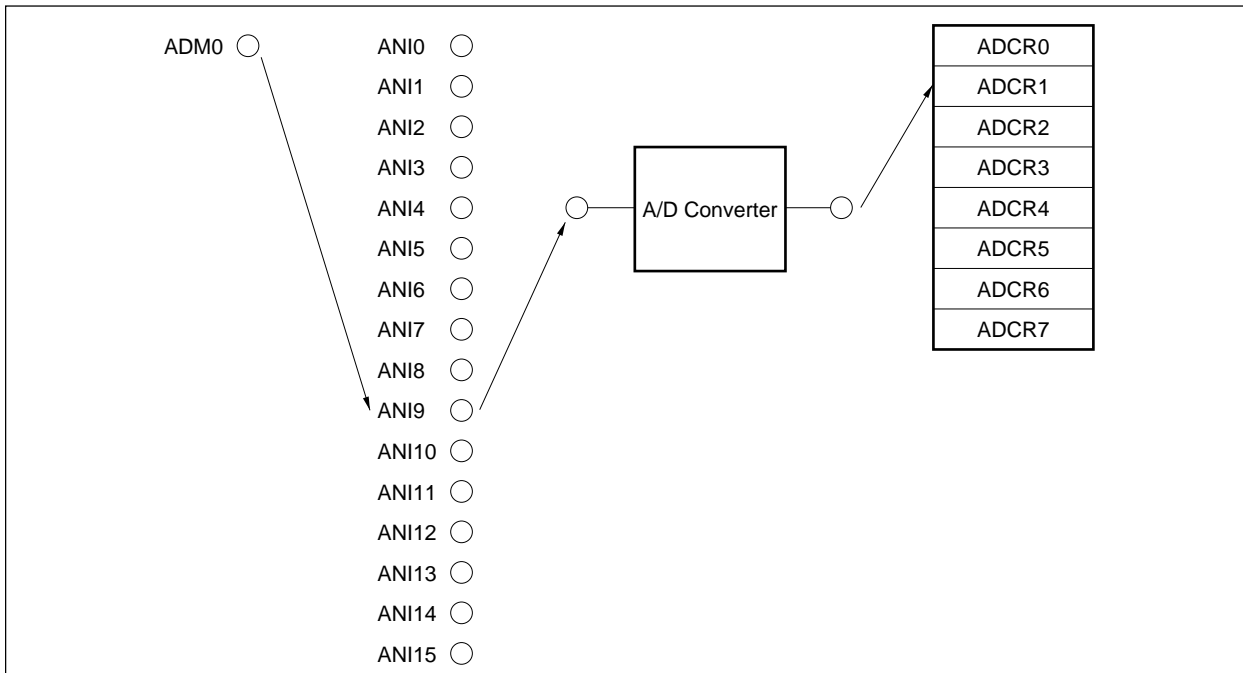
Each time an A/D conversion is executed, an INTAD interrupt is generated and the AD conversion terminates. When 1 is written to the CE bit of the ADM0 register, A/D conversion can be restarted.

This mode is suitable for applications which read out the result in each A/D conversion.

★ **Table 9-1. Correspondence between Analog Input Pin and ADCRn Register (1-buffer mode (A/D trigger select 1-buffer))**

Analog Input	A/D Conversion Results Register
ANI0/ANI8	ADCR0
ANI1/ANI9	ADCR1
ANI2/ANI10	ADCR2
ANI3/ANI11	ADCR3
ANI4/ANI12	ADCR4
ANI5/ANI13	ADCR5
ANI6/ANI14	ADCR6
ANI7/ANI15	ADCR7

★ **Figure 9-6. Example of 1-Buffer Mode (A/D trigger select 1-buffer) Operation**



(2) 4-buffer mode (A/D trigger select: 4-buffer)

The A/D converter converts one analog input four times and stores the results in four ADCRn registers. (Refer to **Table 9-2, Figure 9-7.**) When A/D conversion ends four times, an INTAD interrupt is generated and the A/D conversion terminates.

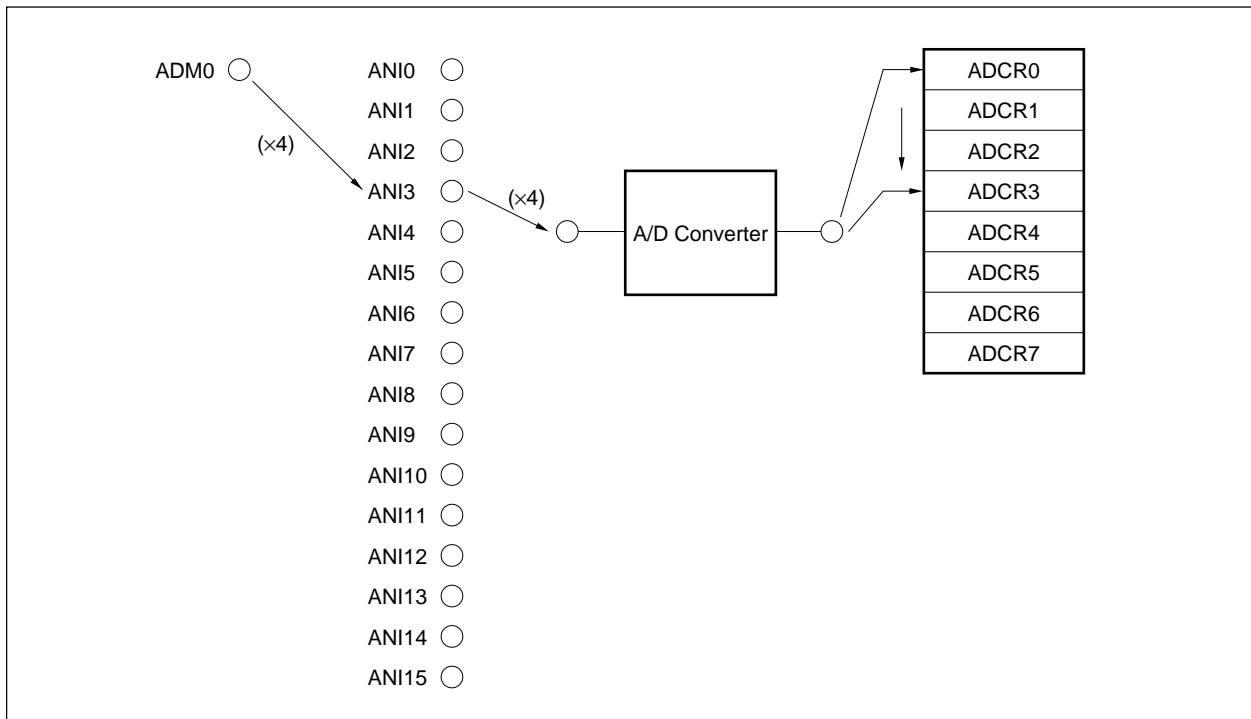
When 1 is written to the CE bit of the ADM0 register, A/D conversion is ended.

This mode is suitable for applications which calculate the average of the A/D conversion result.

**Table 9-2. Correspondence between Analog Input Pin and ADCRn Register
(4-buffer mode (A/D trigger select 4-buffer))**

Analog Input	A/D Conversion Results Register
ANI0 to ANI3/ANI8 to ANI11	ADCR0 (First time)
	ADCR1 (Second time)
	ADCR2 (Third time)
	ADCR3 (Fourth time)
ANI4 to ANI7/ANI12 to ANI15	ADCR4 (First time)
	ADCR5 (Second time)
	ADCR6 (Third time)
	ADCR7 (Fourth time)

Figure 9-7. Example of 4-Buffer Mode (A/D trigger select 4-buffer) Operation



9.5.2 Scan mode operation

The analog inputs from ANI0/ANI8 to the analog input specified with the ADM0 register are selected sequentially and converted to digital. The A/D conversion results are stored in the ADCRn register corresponding to the analog input. (Refer to **Table 9-3**, **Figure 9-8**.)

When the conversion of all the specified analog inputs ends, the INTAD interrupt is generated, and A/D conversion is ended.

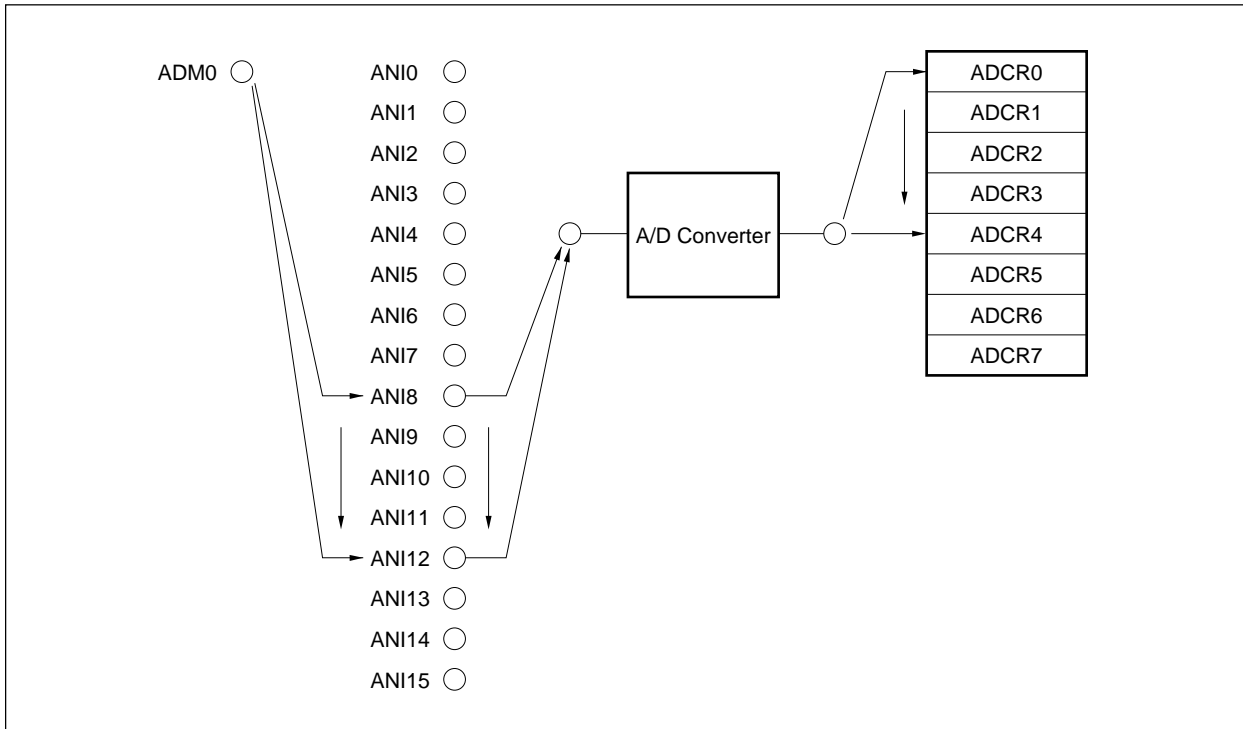
When 1 is written to the CE bit of the ADM0 register, A/D conversion can be restarted.

This mode is suitable for applications which always monitor two or more analog inputs.

★ **Table 9-3. Correspondence between Analog Input Pin and ADCRn Register (scan mode (A/D trigger scan))**

Analog Input	A/D Conversion Results Register
ANI0/ANI8	ADCR0
ANI1/ANI9	ADCR1
ANI2/ANI10	ADCR2
ANI3/ANI11	ADCR3
ANI4/ANI12	ADCR4
ANI5/ANI13	ADCR5
ANI6/ANI14	ADCR6
ANI7/ANI15	ADCR7

★ **Figure 9-8. Example of Scan Mode (A/D trigger scan) Operation**



9.6 Operation in the Timer Trigger Mode

The A/D converter can set conversion timings with the coincidence interrupt signals of the RPU compare register. TM0 and the capture/compare register (CC03) are used for the timer for specifying the analog conversion trigger. The following two modes are provided according to the specification of the TMC00 register.

(1) One-shot mode

To use the one-shot mode, 1 should be set to the OST0 bit of the TMC00 register (one-shot mode).

When the A/D conversion period is longer than the TM0 period, the TM0 generates an overflow, holds 000000H and stops. Thereafter, TM0 does not output the coincidence interrupt signal INTCC03 (A/D conversion trigger) of the compare register, and the A/D converter goes into the A/D conversion standby state. The TM0 count operation restarts when the valid edge of the TCLR0 pin input is detected or when 1 is written to the CE0 bit of the TMC00 register.

(2) Loop mode

To use the loop mode, 0 should be set to the OST0 bit (normal mode) of the TMC00 register.

When the TM0 generates an overflow, the TM0 starts counting from 000000H again, and the coincidence interrupt signal INTCC03 (A/D conversion trigger) of the compare register is repeatedly output and A/D conversion is also repeated.

Coincidence of the compare register can also clear TM0 and restart it.

9.6.1 Select mode operation

The A/D converter converts an analog input (ANI0 to ANI15) specified by the ADM0 register. The conversion results are stored in the ADCRn register corresponding to the analog input. For the select mode, the one-buffer mode and four-buffer mode are provided according to the storing method employed for the A/D conversion results.

(1) 1-buffer mode operation (Timer trigger select: 1-buffer)

The A/D converter converts one analog input once and stores the conversion results in one ADCRn register (Refer to **Table 9-4**, **Figure 9-9**).

The A/D converter converts one analog input once using the trigger of the coincidence interrupt signal (INTCC03) and stores the results in one ADCRn register.

An INTAD interrupt is generated for each A/D conversion and the A/D conversion is ended.

When TM0 is set to the one-shot mode, A/D conversion is ended after one conversion operation. To restart the A/D conversion, input the valid edge to the TCLR0 pin or write 1 to the CE0 bit of the TMC00 register.

When TM0 is set to the loop mode, A/D conversion is repeated each time the coincidence interrupt is generated, unless the CE bit of the ADM0 register is set to 0.

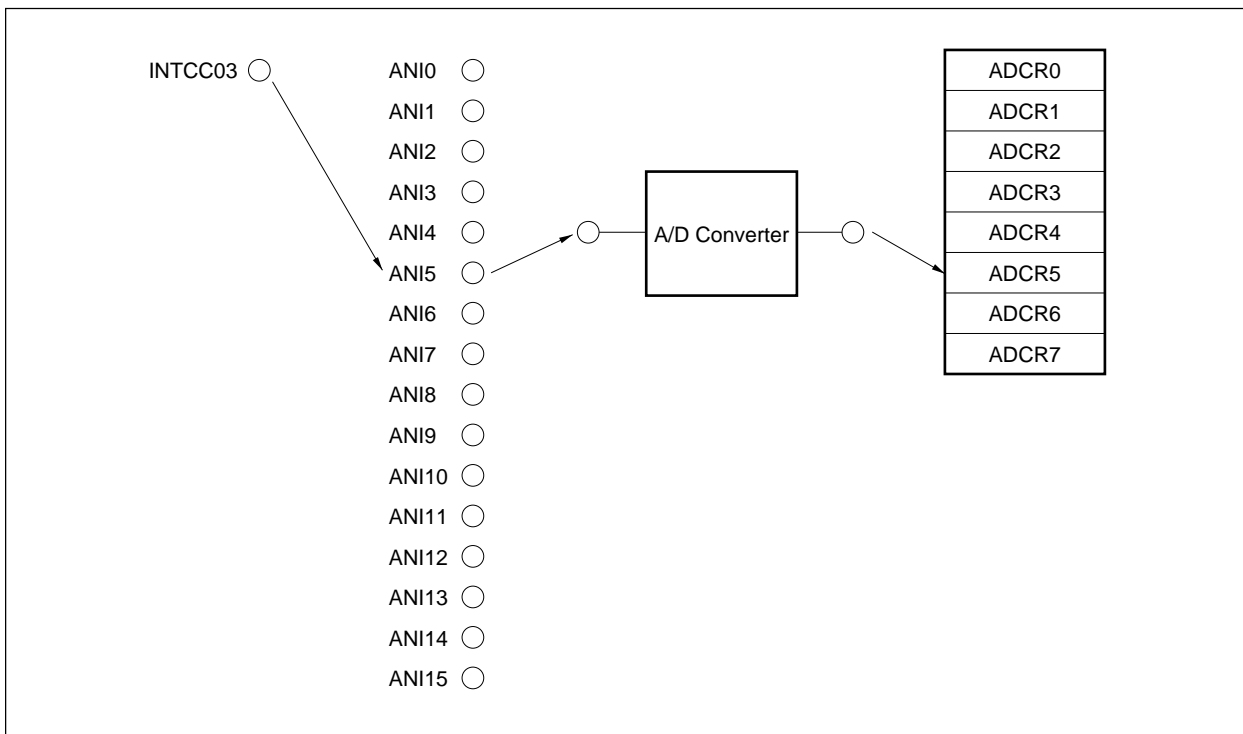
★

**Table 9-4. Correspondence between Analog Input Pin and ADCRn Register
(1-buffer mode (timer trigger select 1-buffer))**

Trigger	Analog Input	A/D Conversion Results Register
INTCC03 interrupt	ANI0/ANI8	ADCR0
INTCC03 interrupt	ANI1/ANI9	ADCR1
INTCC03 interrupt	ANI2/ANI10	ADCR2
INTCC03 interrupt	ANI3/ANI11	ADCR3
INTCC03 interrupt	ANI4/ANI12	ADCR4
INTCC03 interrupt	ANI5/ANI13	ADCR5
INTCC03 interrupt	ANI6/ANI14	ADCR6
INTCC03 interrupt	ANI7/ANI15	ADCR7

★

Figure 9-9. Example of 1-Buffer Mode (timer trigger select 1-buffer) Operation



(2) 4-buffer mode operation (Timer trigger select: 4-buffer)

A/D conversion of one analog input is executed four times, and the results are stored in the ADCRn register (Refer to **Table 9-5**, **Figure 9-10**).

The A/D converter converts one analog input four times using the coincidence interrupt signal (INTCC03) as a trigger, and stores the results in four ADCRn registers.

An INTAD interrupt is generated when the four A/D conversion operations end, and the A/D conversion is ended.

When the TM0 is set to the one-shot mode, and less than four coincidence interrupts are generated, if the CE bit is set to 1, the INTAD interrupt is not generated and the standby state is set.

This mode is suitable for applications which calculate the average of the A/D conversion result.

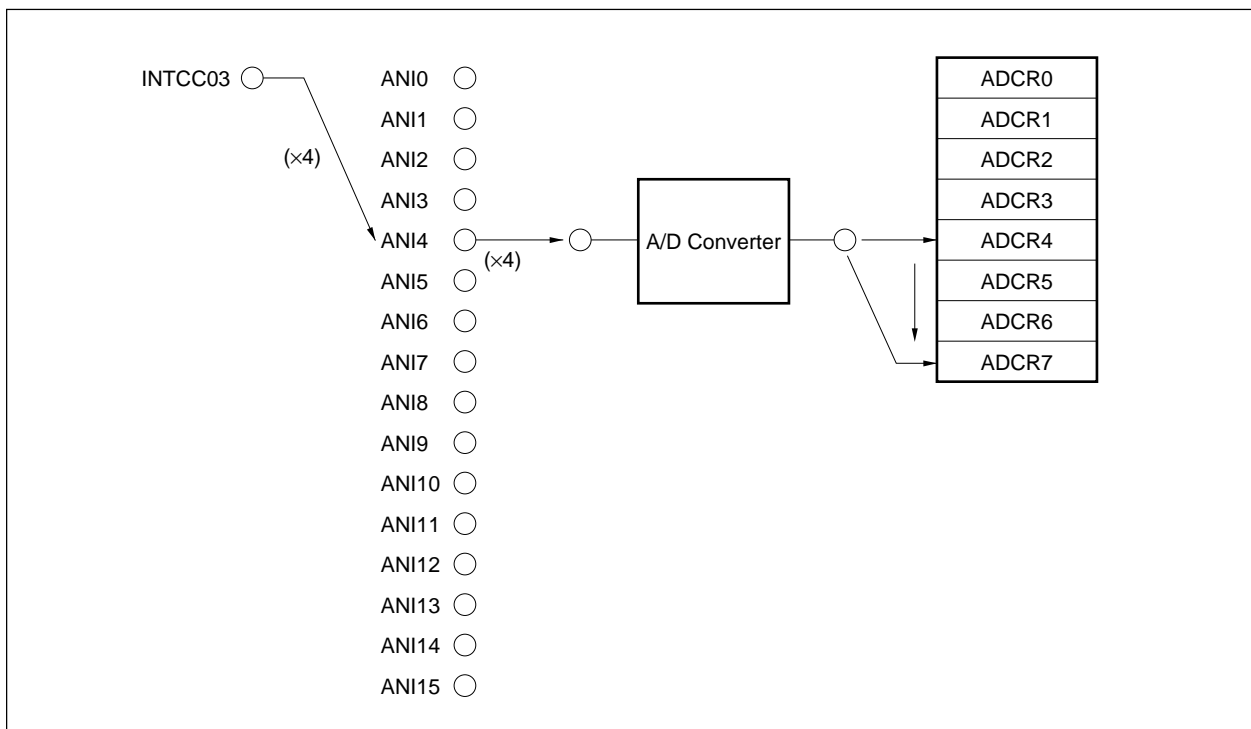
★

**Table 9-5. Correspondence between Analog Input Pin and ADCRn Register
(4-buffer mode (timer trigger select 4-buffer))**

Trigger	Analog Input	A/D Conversion Results Register
INTCC03 interrupt	ANI0 to ANI3/ANI8 to ANI11	ADCR0 (First time)
		ADCR1 (Second time)
		ADCR2 (Third time)
		ADCR3 (Fourth time)
INTCC03 interrupt	ANI4 to ANI7/ANI12 to ANI15	ADCR4 (First time)
		ADCR5 (Second time)
		ADCR6 (Third time)
		ADCR7 (Fourth time)

★

Figure 9-10. Example of Operation in 4-Buffer Mode (timer trigger select 4-buffer)



9.6.2 Scan mode operation

The analog inputs from ANI0/ANI8 to the analog input specified with the ADM0 register are selected sequentially, and A/D conversion is executed the number of times specified using the coincidence interrupt as trigger.

The conversion results are stored in the ADCRn register corresponding to the analog input (refer to **Table 9-6**, **Figure 9-11**). When the conversion of all the specified analog inputs has been ended, the INTAD interrupt is generated and A/D conversion is ended. When the coincidence interrupt is generated after all the specified A/D conversion operations end, A/D conversion is restarted.

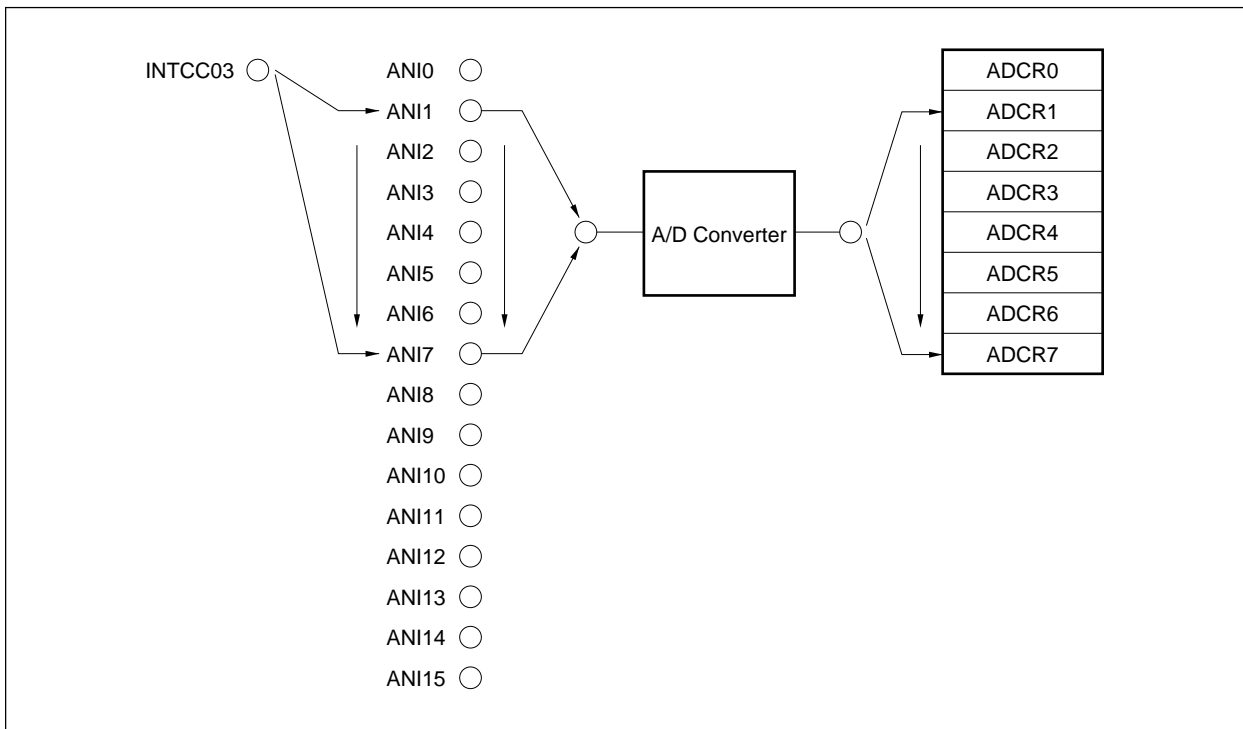
When TM0 is set to the one-shot mode, and less than the specified number of coincidence interrupts are generated the INTAD interrupt is not generated and the standby state is set if the CE bit is set to 1.

This mode is suitable for applications which always monitor two or more analog inputs.

★ **Table 9-6. Correspondence between Analog Input Pin and ADCRn Register (scan mode (timer trigger scan))**

Trigger	Analog Input	A/D Conversion Results Register
INTCC03 interrupt	ANI0/ANI8	ADCR0
INTCC03 interrupt	ANI1/ANI9	ADCR1
INTCC03 interrupt	ANI2/ANI10	ADCR2
INTCC03 interrupt	ANI3/ANI11	ADCR3
INTCC03 interrupt	ANI4/ANI12	ADCR4
INTCC03 interrupt	ANI5/ANI13	ADCR5
INTCC03 interrupt	ANI6/ANI14	ADCR6
INTCC03 interrupt	ANI7/ANI15	ADCR7

★ **Figure 9-11. Example of Scan Mode (timer trigger scan) Operation**



9.7 Operation in the External Trigger Mode

In the external trigger mode, the analog inputs (ANI0 to ANI3) are A/D converted by the ADTRG pin input timing.

The ADTRG pin is also used as the P22 pin. To set the external trigger mode, set the PMC22 bit of the PMC2 register to 1 and bits TRG1 to TRG0 of the ADM1 register to 10.

For the valid edge of the external input signal during the external trigger mode, the rising edge, falling edge, or both rising and falling edges can be specified using the ESAD1 and ESAD0 bits of the INTM5 register. For details, refer to **5.3.8 (2) External interrupt mode registers 1 to 6 (INTM1 to INTM6)**.

9.7.1 Select mode operation (External trigger select)

The A/D converter converts one analog input (ANI0 to ANI15) specified by the ADM0 register. The conversion results are stored in the ADCRn register corresponding to the analog input. Two select modes, one-buffer mode and four-buffer mode are available for storing the conversion results.

(1) 1-buffer mode (External trigger select: 1-buffer)

The A/D converter converts one analog input using the ADTRG signal as a trigger. The conversion results are stored in one ADCRn register (refer to **Table 9-7, Figure 9-12**). The analog input and the A/D conversion results register correspond one to one. An INTAD interrupt is generated after one A/D conversion, and A/D conversion ends.

While the CE bit of the ADM0 register is 1, A/D conversion is repeated every time a trigger is input from the ADTRG pin.

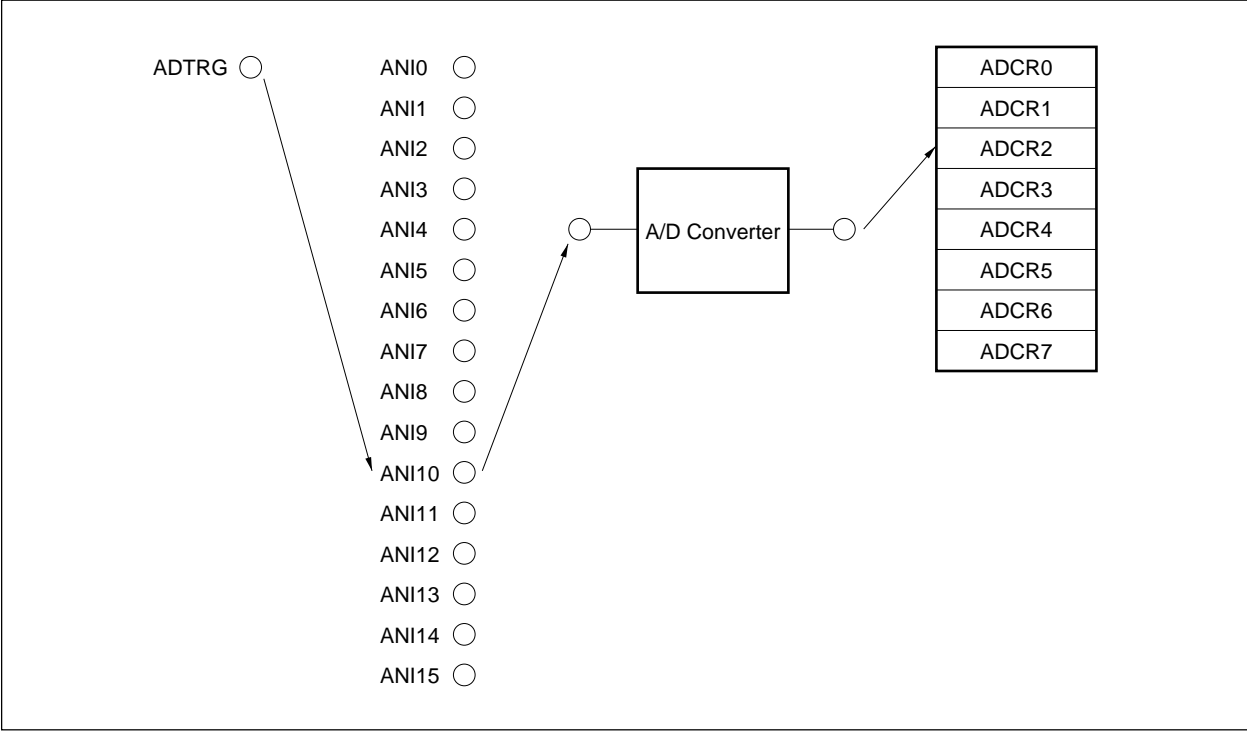
This mode is suitable for applications which read out the result in each A/D conversion.

★

**Table 9-7. Correspondence between Analog Input Pin and ADCRn Register
(1-buffer mode (external trigger select 1-buffer))**

Trigger	Analog Input	A/D Conversion Results Register
ADTRG signal	ANI0/ANI8	ADCR0
ADTRG signal	ANI1/ANI9	ADCR1
ADTRG signal	ANI2/ANI10	ADCR2
ADTRG signal	ANI3/ANI11	ADCR3
ADTRG signal	ANI4/ANI12	ADCR4
ADTRG signal	ANI5/ANI13	ADCR5
ADTRG signal	ANI6/ANI14	ADCR6
ADTRG signal	ANI7/ANI15	ADCR7

★ **Figure 9-12. Example of 1-Buffer Mode (external trigger select 1-buffer) Operation**



(2) 4-buffer mode (External trigger select: 4-buffer)

The A/D converter converts one analog input four times using the ADTRG signal as a trigger and stores the results in four ADCRn registers (refer to **Table 9-8, Figure 9-13**). The INTAD interrupt is generated and conversion ends when the four A/D conversions end.

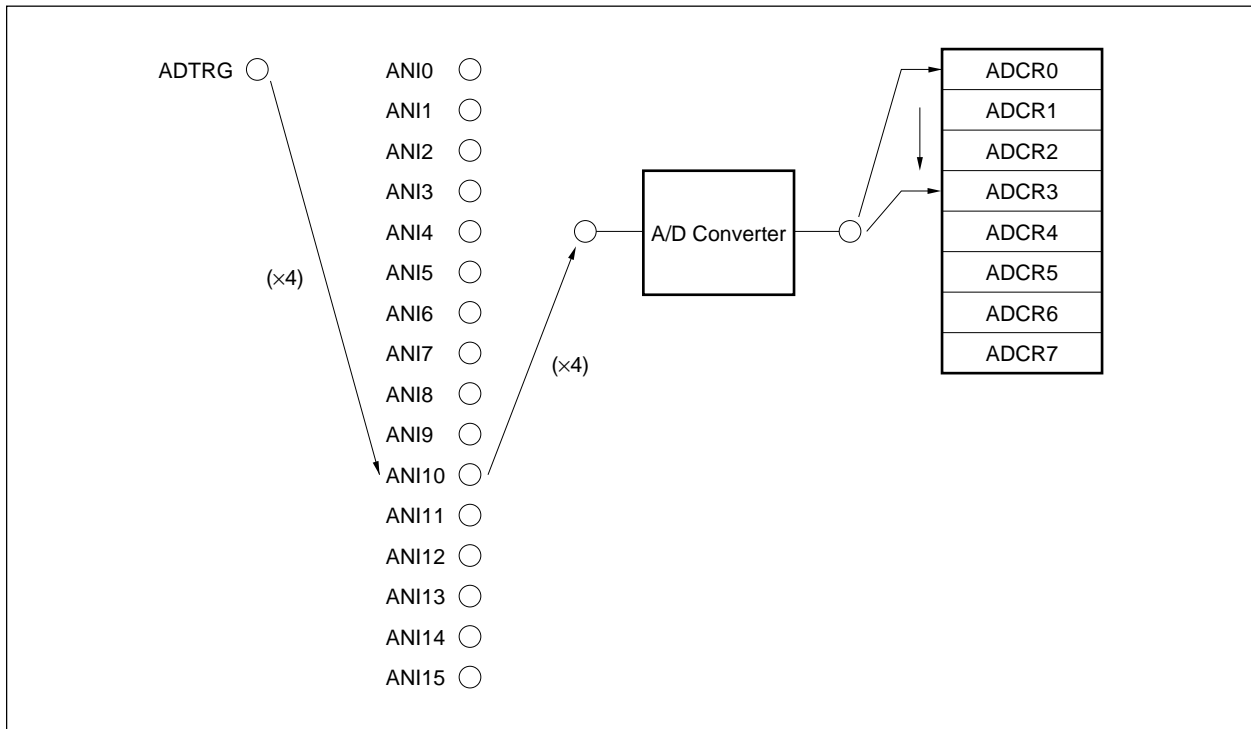
While the CE bit of the ADM0 register is 1, A/D conversion is repeated every time a trigger is input from the ADTRG pin.

This mode is suitable for applications which calculate the average of the A/D conversion result.

**Table 9-8. Correspondence between Analog Input Pin and ADCRn Register
(4-buffer mode (external trigger select 4-buffer))**

Trigger	Analog Input	A/D Conversion Results Register
ADTRG signal	ANI0 to ANI3/ANI8 to ANI11	ADCR0 (First time)
		ADCR1 (Second time)
		ADCR2 (Third time)
		ADCR3 (Fourth time)
ADTRG signal	ANI4 to ANI7/ANI12 to ANI15	ADCR4 (First time)
		ADCR5 (Second time)
		ADCR6 (Third time)
		ADCR7 (Fourth time)

Figure 9-13. Example of 4-Buffer Mode (external trigger select 4-buffer) Operation



9.7.2 Scan mode operation (External trigger scan)

The analog inputs from ANI0/ANI8 to the analog input specified with the ADM0 register are selected sequentially and converted to digital when triggered by the ADTRG signal. The A/D conversion results are stored in the ADCRn register corresponding to the analog input (refer to **Table 9-9, Figure 9-14**). When the conversion of all the specified analog inputs ends, the INTAD interrupt is generated and A/D conversion is ended.

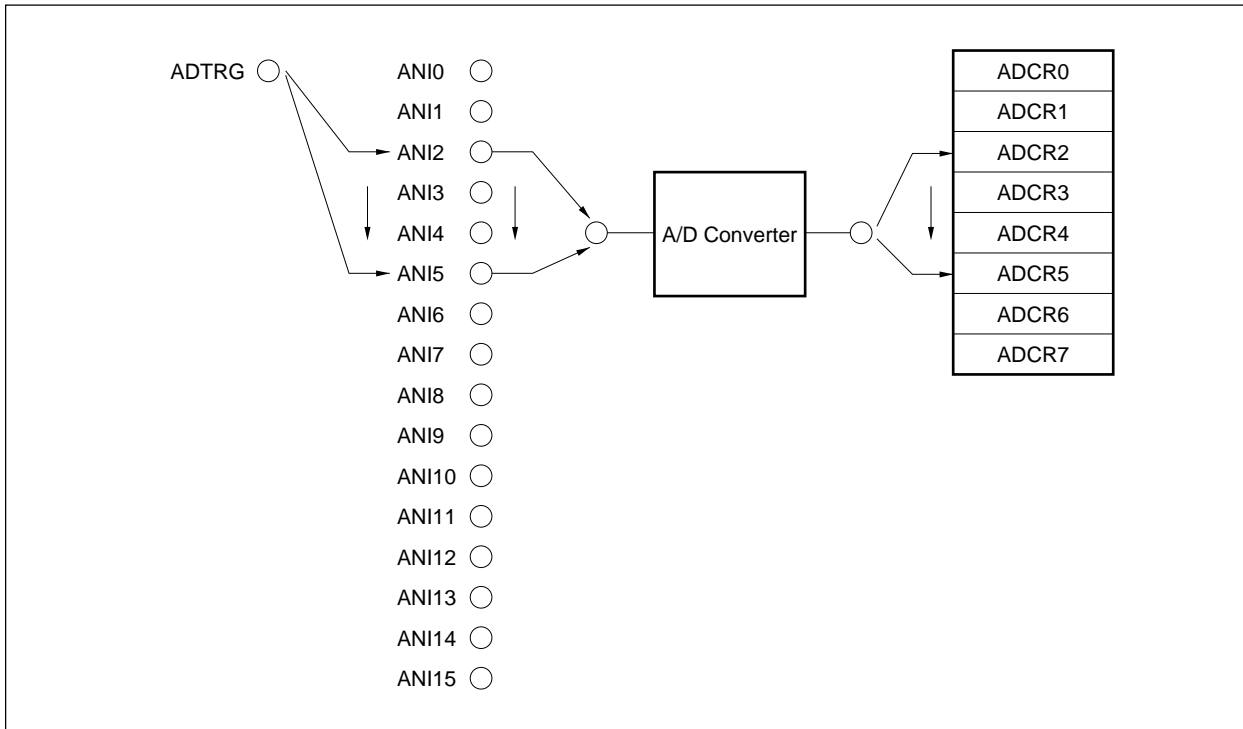
While the CE bit of the ADM0 register is 1, A/D conversion is restarted every time a trigger is input from the ADTRG pin.

This mode is suitable for applications which always monitor two or more analog inputs.

★ **Table 9-9. Correspondence between Analog Input Pin and ADCRn Register (scan mode (external trigger scan))**

Trigger	Analog Input	A/D Conversion Results Register
ADTRG signal	ANI0/ANI8	ADCR0
ADTRG signal	ANI1/ANI9	ADCR1
ADTRG signal	ANI2/ANI10	ADCR2
ADTRG signal	ANI3/ANI11	ADCR3
ADTRG signal	ANI4/ANI12	ADCR4
ADTRG signal	ANI5/ANI13	ADCR5
ADTRG signal	ANI6/ANI14	ADCR6
ADTRG signal	ANI7/ANI15	ADCR7

★ **Figure 9-14. Example of Scan Mode (external trigger scan) Operation**



9.8 Precautions Regarding Operations

9.8.1 Stop of conversion operations

When 0 is written to the CE bit of the ADM0 register during conversion, conversion stops and the conversion results are not stored in the ADCRn register (n = 0 to 7).

★ 9.8.2 Interval of the external/timer trigger

Set the interval (input time interval) of the trigger during the external or timer trigger mode longer than the conversion time specified by the FR2 to FR0 bits of the ADM1 register.

When $0 < \text{interval} \leq \text{conversion operation time}$

When the next external trigger or timer trigger is input during conversion, conversion stops and conversion starts according to the last timer trigger input.

When conversion operations are stopped, the conversion results are not stored in the ADCRn register (n = 0 to 7). However, the number of triggers input are counted, and when an interrupt is generated, the value at which conversion ended is stored in the ADCRn register.

9.8.3 Operation in the standby mode

(1) HALT mode

Continues A/D conversion operations. When canceled by NMI input, the ADM0/ADM1 register and ADCRn register hold the value (n = 0 to 7).

(2) IDLE mode, STOP mode

As clock supply to the A/D converter is stopped, no conversion operations are performed. When canceled using NMI input, the ADM0/ADM1 register and the ADCRn register hold the value (n = 0 to 7). However, when these modes are set during conversion, conversion stops. At this time, if canceled using the NMI input, the conversion operation resumes, but the conversion result written to the ADCRn register will become undefined. In the IDLE and STOP modes, operation of the serial resistor string is also stopped to reduce the power consumption. To further reduce current consumption, set the voltage of the AV_{REF} to V_{SS}.

9.8.4 Compare coincide interrupt in the timer trigger mode

The coincidence interrupt of the compare register becomes the A/D conversion start trigger and conversion operations are started. At this time, the coincidence interrupt of the compare register also functions as the coincidence interrupt of the compare register for the CPU. To prevent generation of the coincidence interrupt of the compare register for the CPU, set interrupt disable using the interrupt mask bit (CC0MK3) of the interrupt control register (CC0IC3).

[MEMO]

CHAPTER 10 REAL-TIME OUTPUT FUNCTION

10.1 Configuration and Function

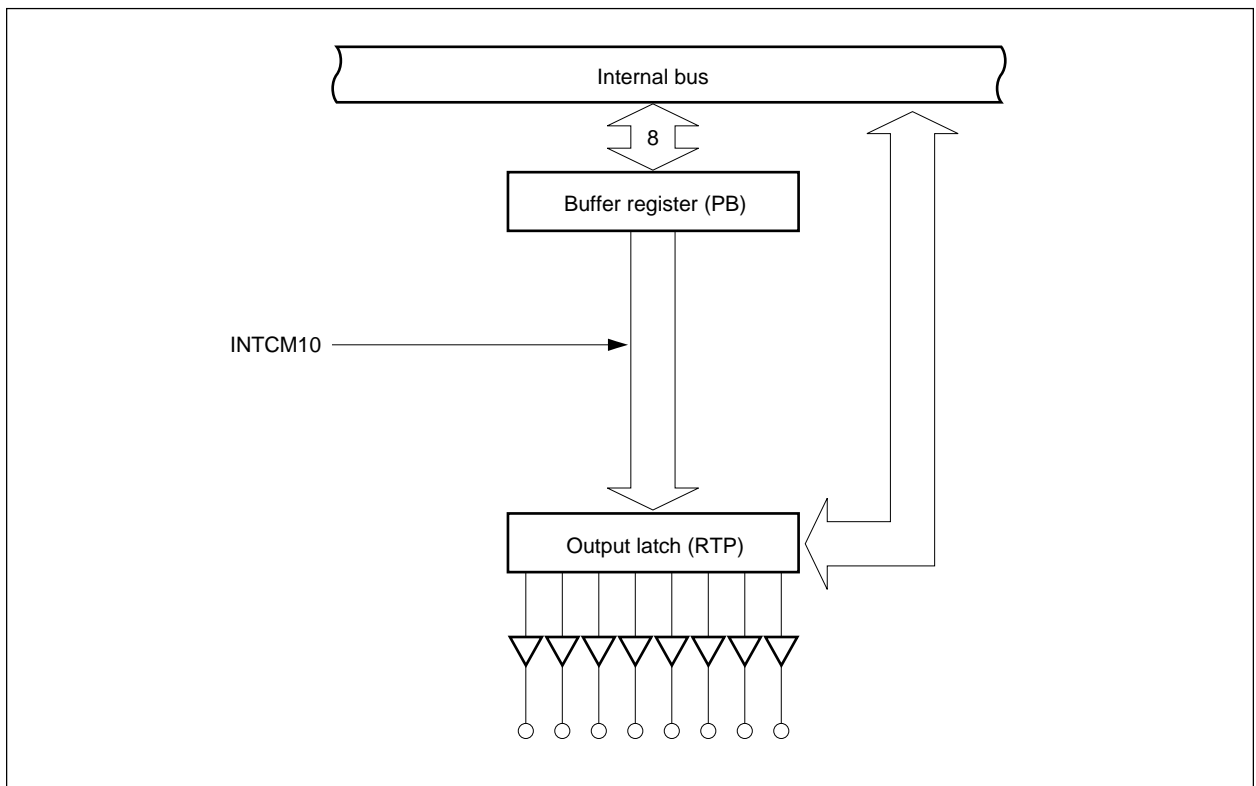
The real-time output function is realized by hardware consisting principally of the buffer register (PB) and the output latch (RTP) as shown in Figure 10-1.

The real-time output function is a procedure that transfers the data previously prepared in the PB register to the output latch by hardware simultaneously with the generation of CM10 coincidence interrupt of timer 1, and outputs it to external. The pins to output the data to external are called a real time output port.

The real-time output function can handle 8-bit real-time output data.

Figure 10-1 shows the block diagram of the real-time output port.

Figure 10-1. Block Diagram of Real-Time Output Port



10.2 Control Register

(1) Buffer register (PB)

The buffer register is a register to which the data to be output from the real-time output port is written beforehand.

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
PB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	Address FFFFFF3C0H	After reset Undefined

(2) Output latch (RTP)

The output latch is a register to which the data of the PB register is transferred by the coincidence signal with the CM10 register. Write the value to be output to external to the RTP register before setting the port as a real-time output port with the PMC13 register.

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
RTP	RTP7	RTP6	RTP5	RTP4	RTP3	RTP2	RTP1	RTP0	Address FFFFFF3C2H	After reset Undefined

10.3 Operation

When the corresponding bit is set to the control mode by the PMC13 register, the output pins can be used as a real-time output port. These pins can be accessed by the PB register and the RTP register.

The data is output by the following procedure.

- <1> The data is written to the PB register.
- <2> The contents of the PB register is transferred to the RTP register at the generation timing of the compare coincidence interrupt of timer (INTCM10).
- <3> The contents of the RTP register is output to the pins set as the real time output port.

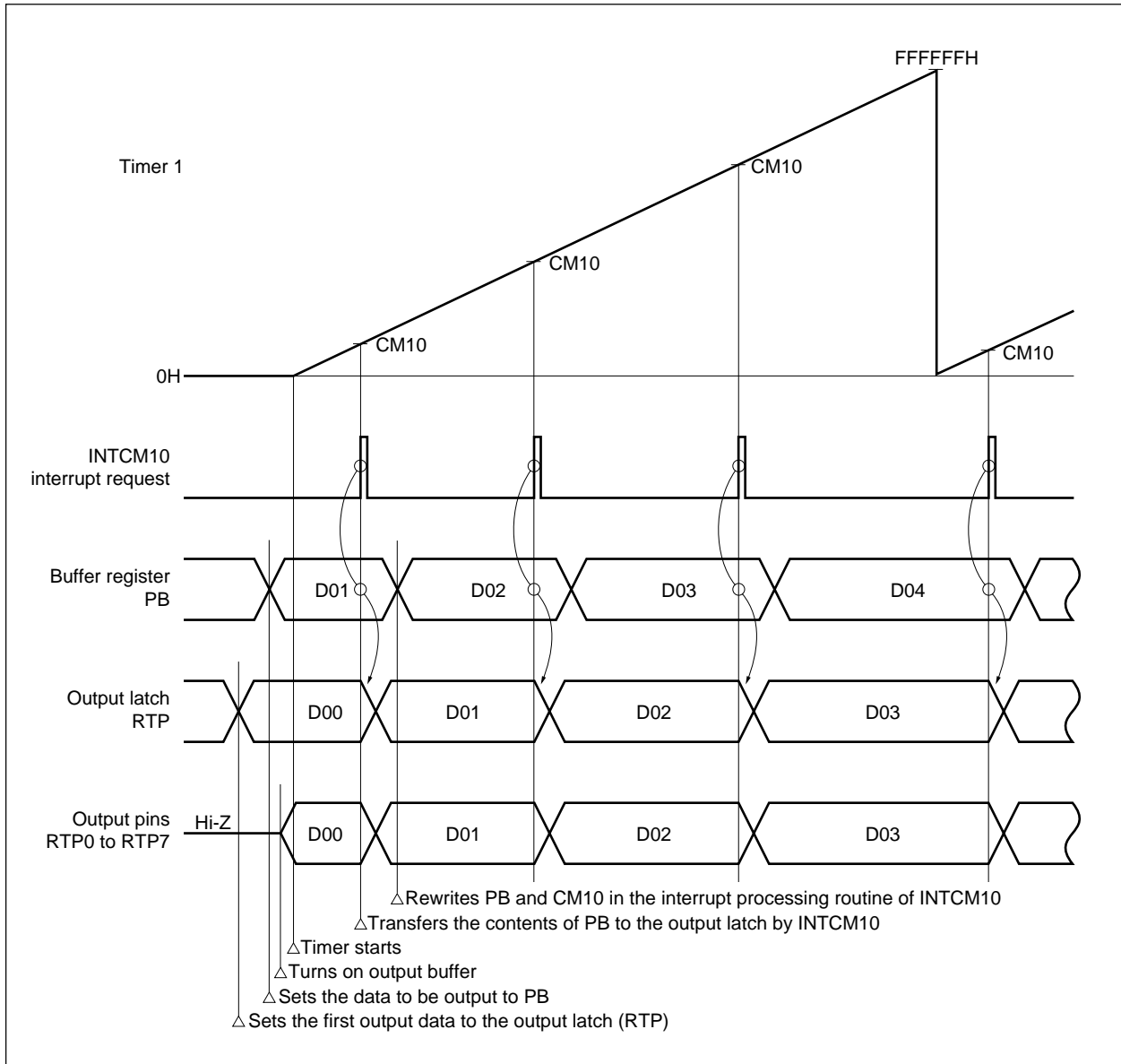
10.4 Example

The following shows an example of using RTP0 to RTP7 as an 8-bit real-time output port.

The contents of the buffer register (PB) is output to RTP0 to RTP7 in each coincidence of the contents of TM1 and CM10 of timer 1. At this time, the interrupt processing routine is generated in which the data to be output next and the timing to change the output next are set (refer to **Figure 10-2**).

For the use of timer 1, refer to **7.2.2 Timer 1**.

Figure 10-2. Operational Timings of Real-Time Output Port



[MEMO]

11.1 Features

- PWMn: 4 channels
- 12- to 16-bit PWM output port
- Main pulse + additional pulse configuration
 - Main pulse 4/5/6/7/8 bits
 - Additional pulse 8 bits
- Repeat frequency: 129 kHz to 2 MHz ($f_{\text{PWM}} = 33 \text{ MHz}$)
- Pulse width overwrite frequency selection: each one pulse/256 pulse
- Active level of the PWM output pulse can be selected.
- Operation clock: Can be selected from ϕ , $\phi/2$, $\phi/4$, $\phi/8$, and $\phi/16$. (ϕ is the internal system clock)

Remark $n = 0$ to 3

11.2 Configuration

Figure 11-1 shows the configuration of the output circuit of PWMn.

(1) Prescaler

Divides the frequency of ϕ and generates PWM operational clock (f_{PWM}). Prescaler output is selected by the PWPn0/PWPn1 bit of the PWPRn register.

(2) Reload control

Controls the reload of the modulo values of x-bit down counter and the 8-bit counter.

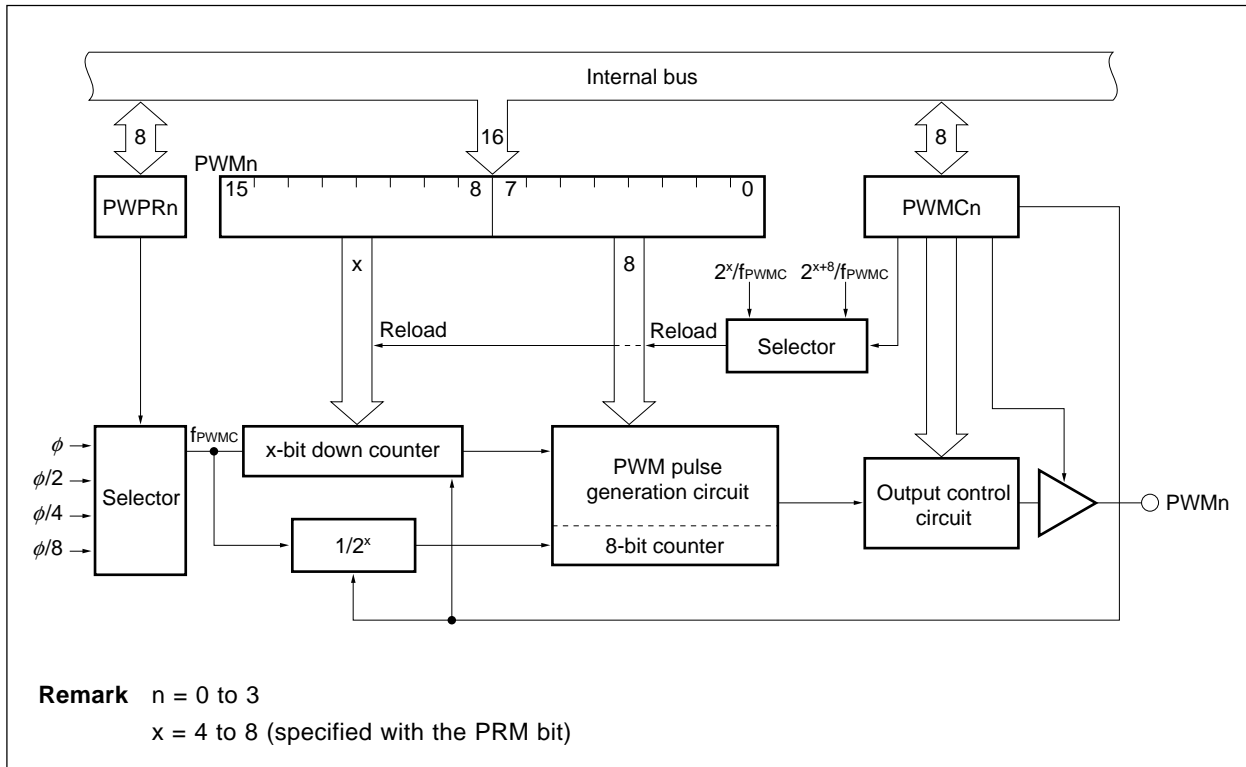
$2^x/f_{\text{PWM}}$ or $2^{x+8}/f_{\text{PWM}}$ is selected by the SYNn bit of the PWMCn register for the reload timing (PWM pulse width rewrite cycle).

(3) x-bit down counter

Controls the output timings of the main pulse.

The value of the modulo H register is loaded to this counter by the reload signal generated in the reload controls and decremented by PWM operational clock (f_{PWM}).

Figure 11-1. Configuration of PWM Unit



11.3 Control Register

(1) PWM control register 0 to 3 (PWMC0 to PWMC3)

Controls PWMn operation, specifies the output active level, and specifies the bit length of the main pulse. This register can be read/written in 8- or 1-bit units. The contents of this register can also be changed during PWMn operation (PWME = 1).

	7	6	5	4	3	2	1	0		
PWMCn	PMPn2	PMPn1	PMPn0	0	0	SYNn	PWME _n	PALV _n	Address FFFFF360H to FFFFF378H	After reset 05H

Bit Position	Bit Name	Function																												
7 to 5	PMPn2 to PMPn0	PWM Main Pulse Specifies bit length of x-bit down counter (main pulse)																												
		<table><tr><th>PMPn2</th><th>PMPn1</th><th>PMPn0</th><th>Bit Length</th></tr><tr><td>0</td><td>0</td><td>0</td><td>8 bits</td></tr><tr><td>0</td><td>0</td><td>1</td><td>7 bits</td></tr><tr><td>0</td><td>1</td><td>0</td><td>6 bits</td></tr><tr><td>0</td><td>1</td><td>1</td><td>5 bits</td></tr><tr><td>1</td><td>0</td><td>0</td><td>4 bits</td></tr><tr><td colspan="3">Others</td><td>Setting prohibited</td></tr></table>	PMPn2	PMPn1	PMPn0	Bit Length	0	0	0	8 bits	0	0	1	7 bits	0	1	0	6 bits	0	1	1	5 bits	1	0	0	4 bits	Others			Setting prohibited
		PMPn2	PMPn1	PMPn0	Bit Length																									
		0	0	0	8 bits																									
		0	0	1	7 bits																									
		0	1	0	6 bits																									
		0	1	1	5 bits																									
		1	0	0	4 bits																									
Others			Setting prohibited																											
2	SYNn	Rewrite Cycle Specifies PWM pulse width rewrite cycle 0: Large cycle (every PWM 2^{x+8} cycles ($2^{x+8}/f_{\text{PWMC}}$)) 1: Small cycle (every PWM 1 cycle ($2^x/f_{\text{PWMC}}$))																												
1	PWME _n	PWM Enable Controls operation/stop of PWM _n 0: Operation stops 1: Operation in progress PWM counter is cleared by changing this bit from 0 to 1.																												
0	PALV _n	PWM Active Level Specifies PWM _n active level 0: Active low 1: Active high																												

Remark n = 0 to 3

x: number of bits set with PRM

(2) PWM prescaler register 0 to 3 (PWPR0 to PWPR3)

This register selects the operation clock (f_{PWM}) of PWMn, and can be read/written in 8- or 1-bit units. Change the contents of this register while the bits of the PWMCn register are 0. If the contents of this register are changed when the setting of the PWME_n bit is 1, the operation cannot be guaranteed.

	7	6	5	4	3	2	1	0		
PWPR _n	0	0	0	0	0	0	PWP _n 1	PWP _n 0	Address FFFFF364H to FFFFF37CH	After reset 00H

Bit Position	Bit Name	Function															
1, 0	PWP _n 1, PWP _n 0	PWM Prescaler Clock Mode Selects operation clock of PWMn <table border="1"> <tr> <th>PWP_n1</th><th>PWP_n0</th><th>Operation Clock (f_{PWM})</th></tr> <tr> <td>0</td><td>0</td><td>ϕ</td></tr> <tr> <td>0</td><td>1</td><td>$\phi/2$</td></tr> <tr> <td>1</td><td>0</td><td>$\phi/4$</td></tr> <tr> <td>1</td><td>1</td><td>$\phi/8$</td></tr> </table> ϕ : Internal system clock	PWP _n 1	PWP _n 0	Operation Clock (f_{PWM})	0	0	ϕ	0	1	$\phi/2$	1	0	$\phi/4$	1	1	$\phi/8$
PWP _n 1	PWP _n 0	Operation Clock (f_{PWM})															
0	0	ϕ															
0	1	$\phi/2$															
1	0	$\phi/4$															
1	1	$\phi/8$															

Remark n = 0 to 3

(3) PWM modulo registers 0 to 3 (PWM0 to PWM3)

The PWM modulo registers 0 to 3 are 16-bit registers used to determine the pulse width of the PWM_n pulse. These registers can be read/written in 16-bit units. These registers consist of the following two parts.

<1> Modulo H register (bit 8 to bit 15)

Indicates the number of bits specified with the PMP_n bit of the PWM_{Cn} register. This value is the accuracy when generating the main pulse.

The pulse width rewrite timing depends on the number of bits of this register.

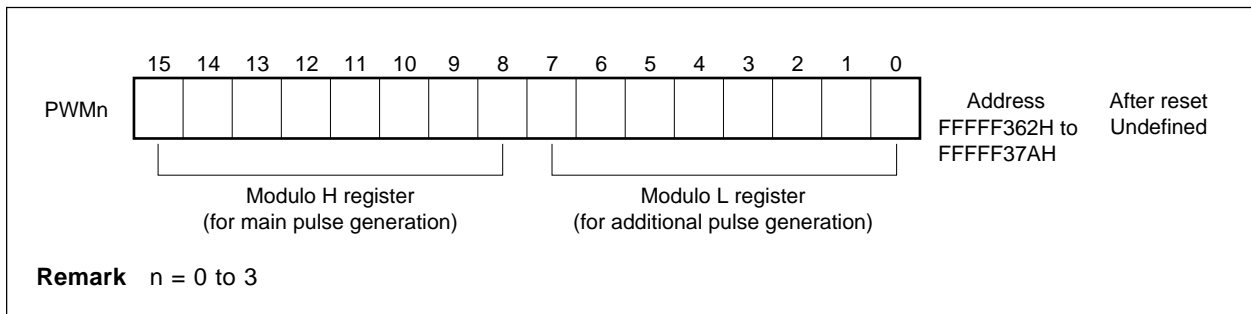
When selecting 4 to 7 bits for the counter with the PMP_n bit, set 0 to the rest of the higher bits.

<2> Modulo L register (bit 0 to bit 7)

The value of this register determines the additional timings of the additional pulse to perform minute adjustment (refer to **Figure 11-3**).

The value of this register becomes undefined by $\overline{\text{RESET}}$ input. Set the data with initialization program before enabling PWM output.

The value from 0000H to FFFFH can be set to the PWM_n register, and PWM output also changes linearly. When 0000H is set, inactive level is retained. When FFFFH is set, one additional pulse ($1/f_{\text{PWMC}}$) becomes inactive by one rewrite cycle ($2^{16}/f_{\text{PWMC}}$) (refer to **Figure 11-4**).



11.4 PWM Operations

11.4.1 Basic operations of PWM

The duty of the PWM pulse output is determined as follows by the value set to the modulo H register of the PWM modulo register (PWMn: n = 0 to 3).

$$\text{Duty of PWM pulse output} = \frac{(\text{Value of modulo H register})^{\text{Note 1}} + 1^{\text{Note 2}}}{2^x}$$

- Notes**
1. $0 \leq (\text{Value of modulo H register}) \leq 2^x - 1$
 2. With additional pulse

Remark $x = 4 \text{ to } 8$

The repeat frequency of the PWM pulse output is the frequency of the 2^x frequency division ($= f_{\text{PWMC}}/2^x$) of the PWM clock (f_{PWMC}) of ϕ to $\phi/4$ set by the PWM prescaler register (PWPR), and the minimum pulse width is $1/f_{\text{PWMC}}$.

The PWM pulse output realizes 12- to 16-bit resolution by repeatedly outputting the PWM signal with 4- to 8-bit resolution and $f_{\text{PWMC}}/2^x$ repeat frequency for 256 times. The PWM pulse signal with 12- to 16-bit resolution is realized in 256 cycles by controlling the addition of the additional pulse ($1/f_{\text{PWMC}}$) to the PWM pulse with 4- to 8-bit resolution determined by the modulo H register according to the value of the modulo L register in 1-cycle units.

Figure 11-2. Basic Operations of PWM

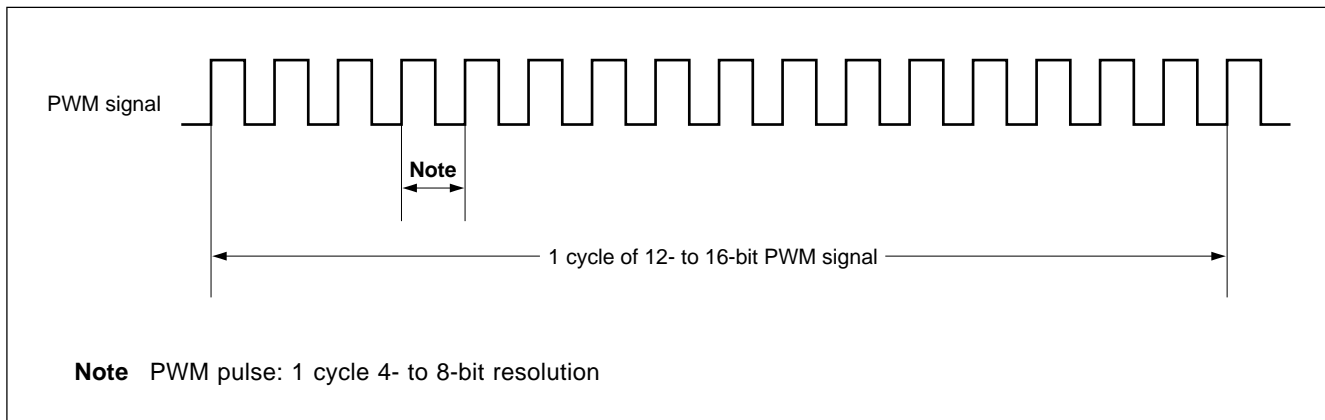


Figure 11-3. Example of PWM Output by Main Pulse and Additional Pulse

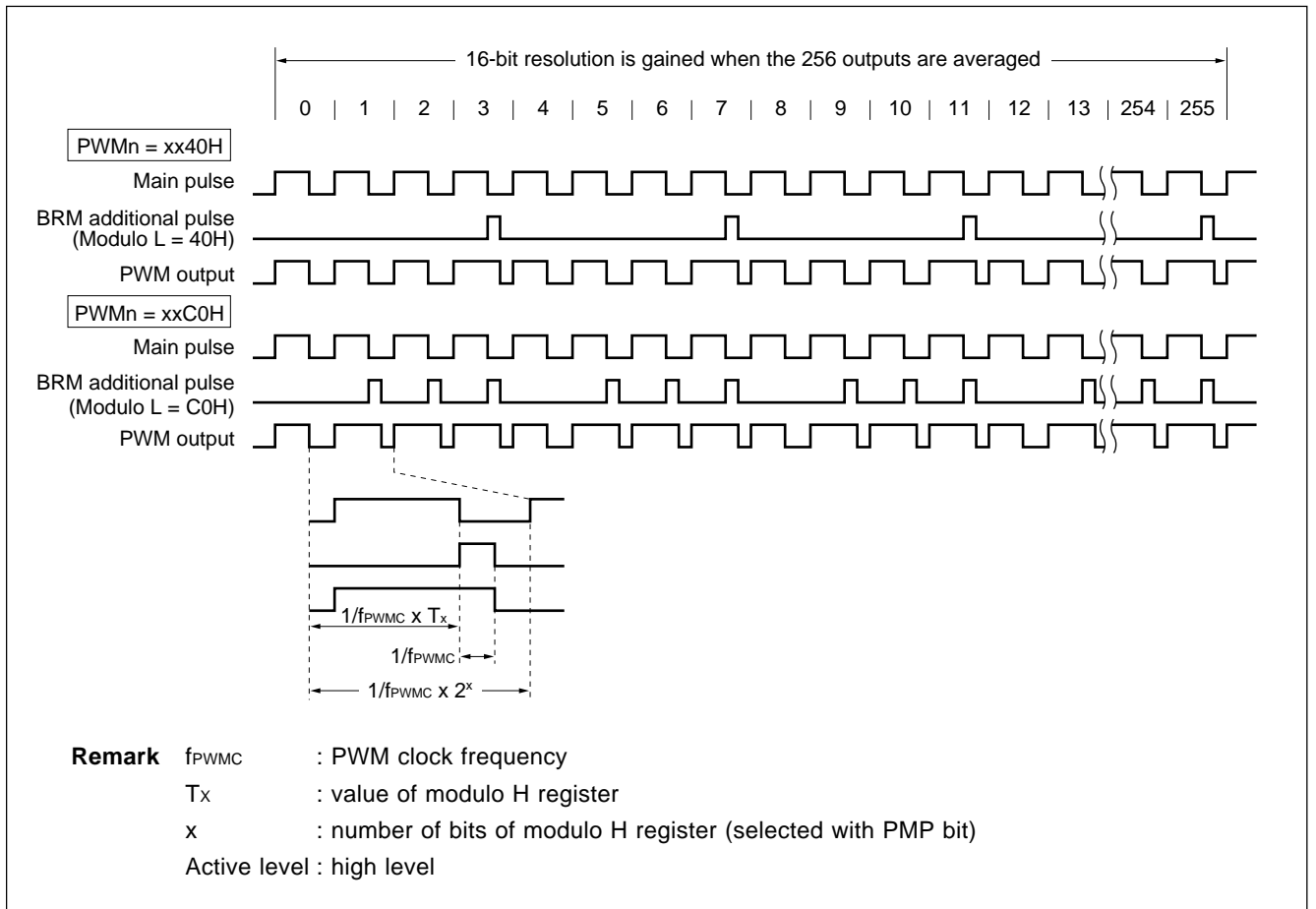
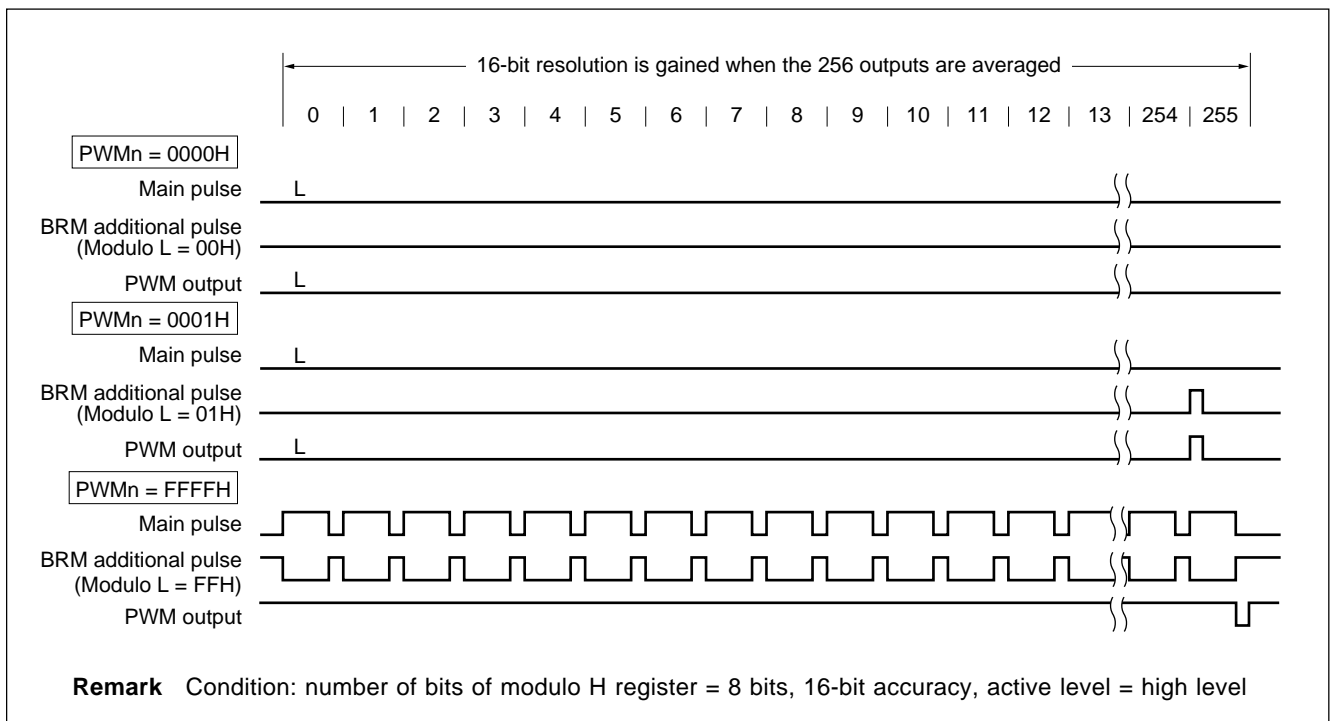


Figure 11-4. Example of PWM Output Operation



11.4.2 Enabling/disabling PWM operation

To output the PWM pulse, the PWME bit of the PWM control register (PWMCn) is set (1) after setting data to the PWM prescaler register (PWPRn) and the PWM modulo register (PWMn) ($n = 0$ to 3).

Thereby, PWM pulse with active level specified by the PALVn bit of the PWMCn register is output from the PWM output pin.

When the PWME bit of the PWMCn register is cleared (0), the PWM output unit immediately stops the PWM output operation, and the PWM output pin becomes inactive.

(1) Setting when PWM operation starts

When the PWME bit of the PWMCn register is set, PWMn goes into operation status. However, the PWM pin maintains the port mode status even after the operation status is set until the reload signal of the PWMn register is generated. In addition, the value of the PWMn register is not loaded to the x-bit down counter. Therefore, when the pulse width rewrite timing is set to 2^{x+8} (large cycle: SYN bit = 0), operation starts in $2^{x+8}/f_{PWM}$ max. after the PWME bit is set. The SYNn bit of the PWMCn register can be rewritten even during PWM output.

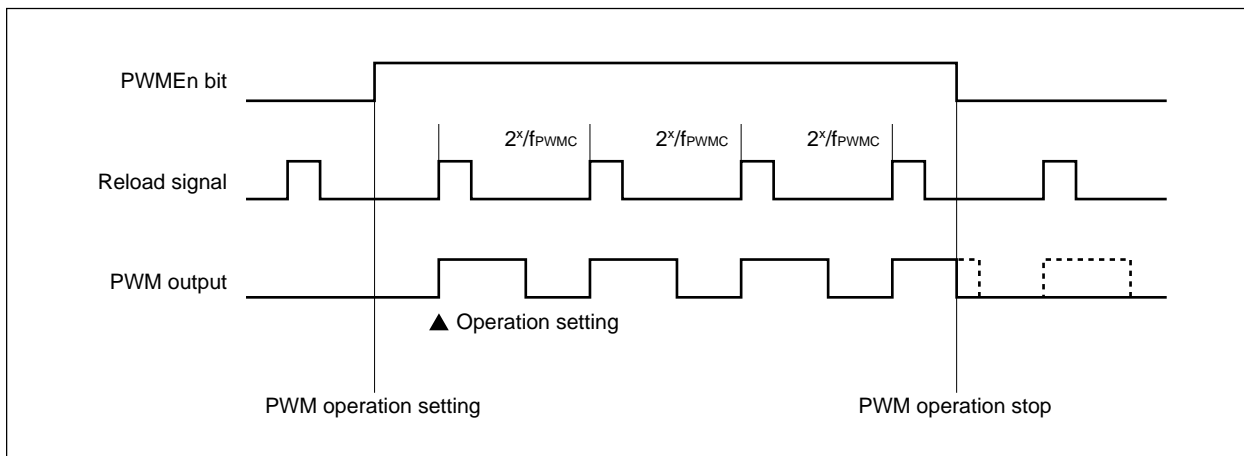
Initialize the following registers before starting PWMn operation.

- PMC10 register : Setting of the control mode
- PWMn register : Setting of the pulse width
- PWPRn register : Specification of the operational clock of the PWM output circuit
- PWMCn register : Specification of the PWM pulse width rewrite cycle, specification of active level of PWM pin, PWM operation control, and selection of the number of bits of the main pulse

(2) Setting when PWM operation stops

When the PWME bit of the PWMCn register is reset, PWM operation immediately stops.

Figure 11-5. Operation Timing of PWM



11.4.3 Specification of active level of PWM pulse

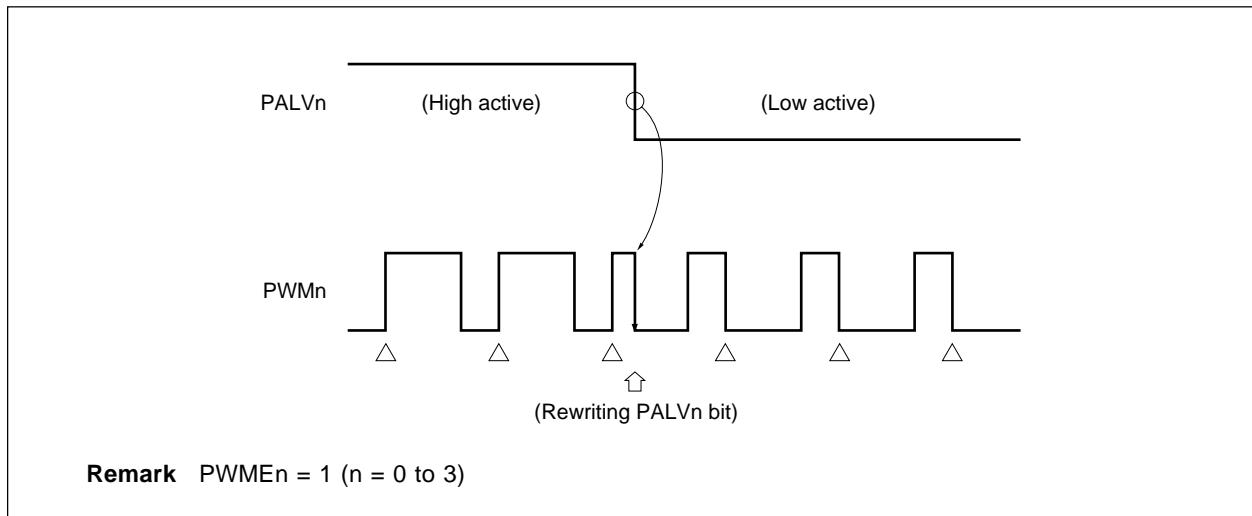
The PALVn bit of the PWM control register (PWMCn) specifies the active level of the PWM pulse output from the PWM output pin ($n = 0$ to 3).

When the PALVn bit is set (1), a pulse with high active level is output, and when it is cleared (0), a pulse with low active level is output.

When the PALVn bit is rewritten, the active level of the PWM output immediately changes. Figure 11-6 shows the active level setting and the pin status of the PWM output.

The active level of the PWM output can be changed by manipulating the PALVn bit, regardless of the setting of the PWME_n bit (enabling/disabling PWM).

Figure 11-6. Setting of Active Level of PWM Output



11.4.4 Specification of PWM pulse width rewrite cycle

Starting PWM output and changing the PWM pulse width are performed in synchronization either with each $2^{(x+8)}$ cycles ($2^x/f_{PWM}$) of the PWM pulse or with each 1 cycle ($2^0/f_{PWM}$) of the PWM pulse. The specification of the PWM pulse width rewrite cycle is performed with the SYNn bit of the PWMCn register ($n = 0$ to 3).

When the SYNn bit is cleared (0), the pulse width is changed at every $2^{(x+8)}$ cycles ($2^{(x+8)}/f_{PWM}$) of the PWM pulse. Therefore, it will take $2^{(x+8)}$ clocks max. before the pulse with the width corresponding to the data written to the PWMn register is output.

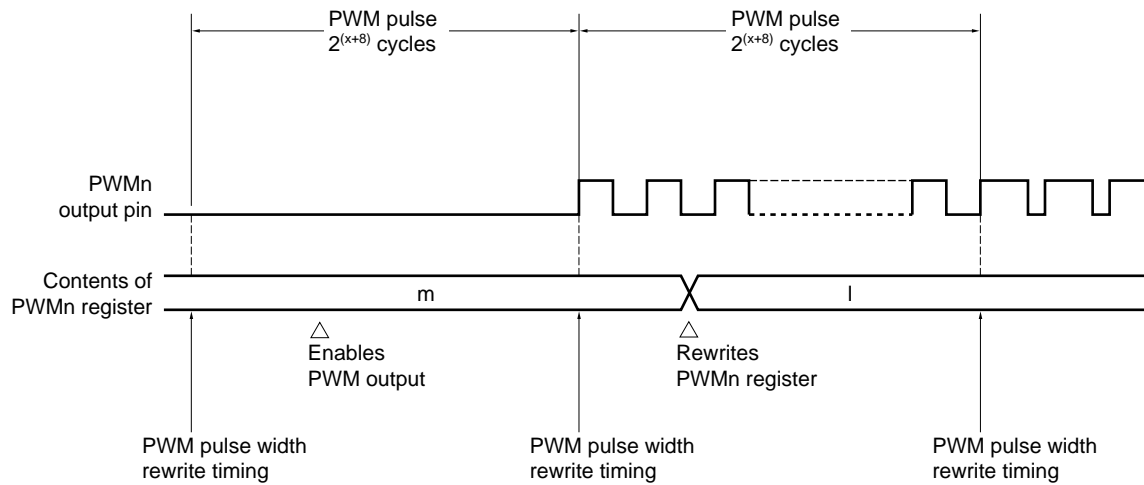
Figure 11-7 shows an example of the PWM output timing.

On the other hand, when the SYNn bit is set (1), the pulse width is changed at every 1 cycle of the PWM pulse ($2^0/f_{PWM}$). In this case, it will take 2^x clocks max. before the pulse with the width corresponding to the data written to the PWMn register is output.

When the PWM pulse rewriting cycle is specified as every $2^x/f_{PWM}$ (when the SYNn bit is set (1)), the accuracy of the PWM pulse gained is x bits or more and $(x+8)$ bits or less, which is lower than the accuracy when the rewriting cycle is specified as $2^{(x+8)}/f_{PWM}$. However, the response is improved because the repeat frequency is increased.

Figure 11-8 shows an example of the PWM output timing when the rewrite timing is $2^x/f_{PWM}$.

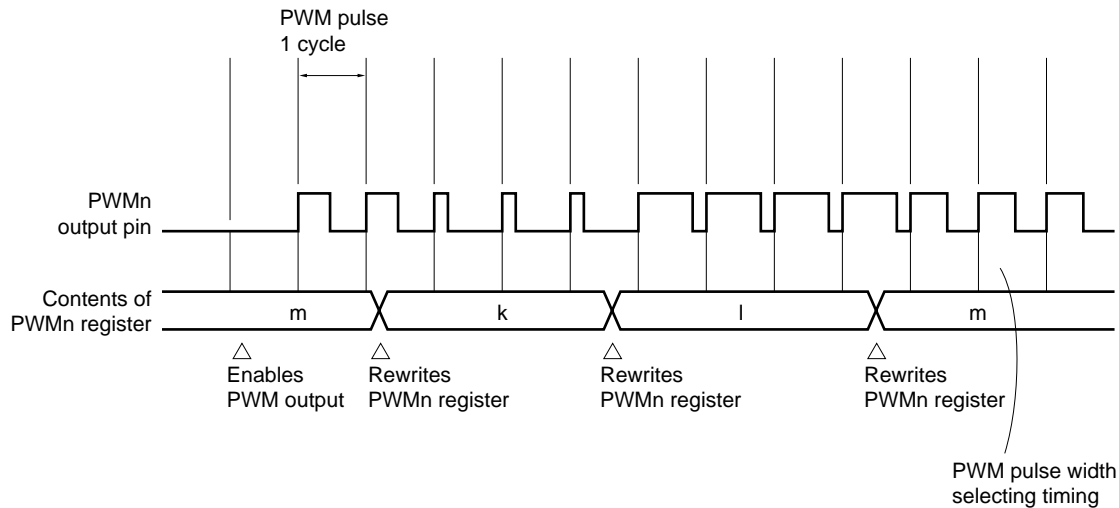
Figure 11-7. Example 1 of PWM Output Timing (PWM pulse width rewrite cycle $2^{(x+8)}/f_{PWM}$)



- Cautions**
1. The pulse width is rewritten at every 256 cycles of the PWM pulse.
 2. The accuracy of the PWM pulse is $(x + 8)$ bits.

- Remarks**
1. m and l are the contents of the PWMn register.
 2. $n = 0$ to 3

Figure 11-8. Example 2 of PWM Output Timing (PWM pulse width rewrite cycle $2^x/f_{PWM}$)



- Cautions**
1. The pulse width is rewritten at every 1 cycle of the PWM pulse.
 2. The accuracy of the PWM pulse is x bits or more and $(x + 8)$ bits or less.

- Remarks**
1. k, l, and m are the contents of the PWMn register.
 2. $n = 0$ to 3

11.4.5 Repetition frequency

The repetition frequency of the PWM_n is shown below (n = 0 to 3).

Main Pulse	Additional Pulse	Repetition Frequency	Pulse Width Rewrite Cycle	
			Large Cycle (SYN _n bit = 0)	Small Cycle (SYN _n bit = 1)
4 bits	8 bits	$f_{\text{PWM}}/16$	$f_{\text{PWM}}/2^{12}$	$f_{\text{PWM}}/2^4$
5 bits	8 bits	$f_{\text{PWM}}/32$	$f_{\text{PWM}}/2^{13}$	$f_{\text{PWM}}/2^5$
6 bits	8 bits	$f_{\text{PWM}}/64$	$f_{\text{PWM}}/2^{14}$	$f_{\text{PWM}}/2^6$
7 bits	8 bits	$f_{\text{PWM}}/128$	$f_{\text{PWM}}/2^{15}$	$f_{\text{PWM}}/2^7$
8 bits	8 bits	$f_{\text{PWM}}/256$	$f_{\text{PWM}}/2^{16}$	$f_{\text{PWM}}/2^8$

f_{PWM} : Select from ϕ , $\phi/2$, $\phi/4$, and $\phi/8$ by the PWPR_n register.

[MEMO]

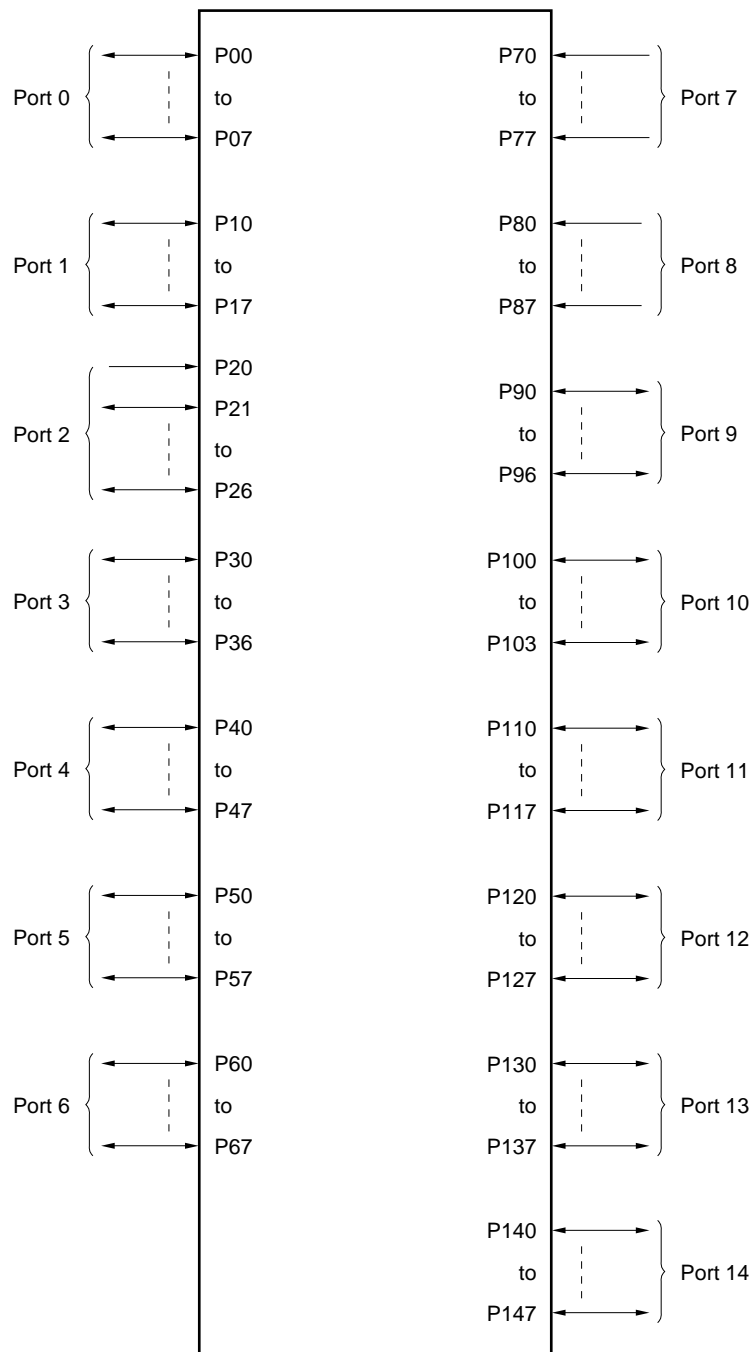
12.1 Features

The ports of the V854 have the following features:

- Number of pins: input: 16
I/O: 96
- Also function as I/O pins of other peripheral functions
- Can be set in input/output mode in 1-bit units

12.2 Basic Configuration of Ports

The V854 is provided with a total of 112 input/output port pins (of which 16 are input-only port pins) that make up ports 0 to 14. The configuration of the V854's ports is shown below. (P20 cannot be used for a port function.)



(1) Function of each port

The ports of the V854 have the functions shown in the table below.

Each port can be manipulated in 8- or 1-bit units and perform various types of control operations. In addition to port functions, the ports also have functions as internal hardware input/output pins, when placed in the control mode.

For the details, refer to the description of each port. Figure 12-1 to 12-11 show the block diagram of the ports.

Port	Pin	Port Function	Function in Control Mode
Port 0	P00 to P07	8-bit I/O	Real time pulse unit (RPU) input/output External interrupt request input (capture trigger input)
Port 1	P10 to P17	8-bit I/O	RPU input/output External interrupt request input (capture trigger input) P17 is only for port.
Port 2	P20 to P26 ^{Note}	6-bit I/O	Non-maskable interrupt request input External interrupt request input (capture trigger input) Analog trigger input
Port 3	P30 to P36	7-bit I/O	Serial interface input/output (UART, CSI, I ² C) P36 is only for port.
Port 4	P40 to P47	8-bit I/O	Address/data bus for external memory
Port 5	P50 to P57		
Port 6	P60 to P67	8-bit I/O	Address bus for external memory
Port 7	P70 to P77	8-bit input	Analog input to A/D converter (only for input in the port mode)
Port 8	P80 to P87		
Port 9	P90 to P96	7-bit I/O	Control signal input/output for external memory
Port 10	P100 to P103	4-bit I/O	PWM control signal output
Port 11	P110 to P117	8-bit I/O	RPU input/output External interrupt request input
Port 12	P120 to P127	8-bit I/O	Serial interface input/output Clock output P126 is only for port.
Port 13	P130 to P137	8-bit I/O	Real-time output port
Port 14	P140 to P147	8-bit I/O	Only for port

Note P20 cannot be used for a port function.

Caution when outputting in the control mode or switching a port that operates as an input/output pin to the control mode, take the following steps.

- (1) Set the corresponding bit of port n (Pn)(n = 0, 1, 3 to 6, 9 to 13) to the inactive level of the output signal in the control mode.
- (2) Switch to the control mode with a port n mode control register (PMCn).

If (1) above is omitted, the contents of port n (Pn) may momentarily be output when switching from the port mode to control mode.

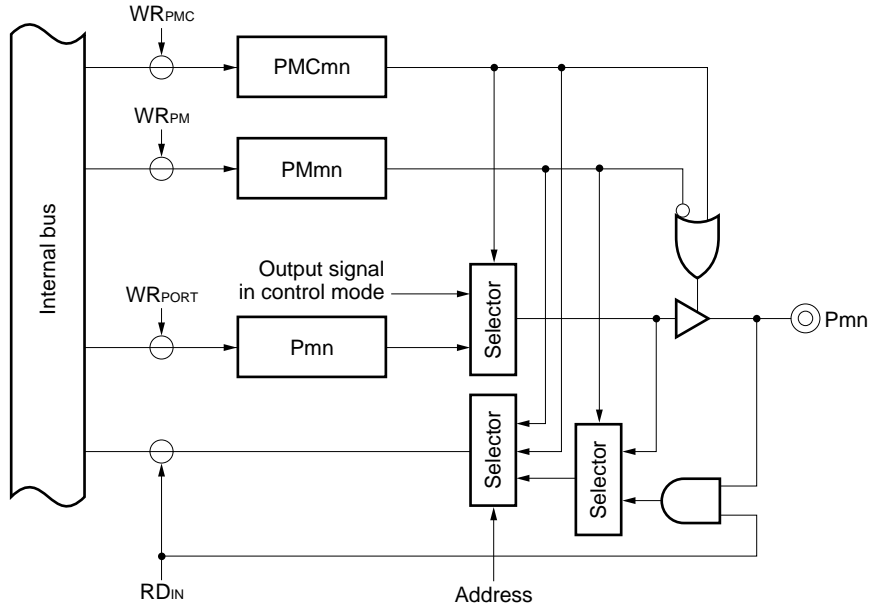
(2) Register for setting function at reset and port/control mode of each port pin

(1/2)

Port Name	Pin Name	Function after Reset (Input/output is shown in parentheses)				Register for Setting Mode	
		In Single-Chip Mode 1	In Single-Chip Mode 2	In ROM-less Mode 1	In ROM-less Mode 2		
Port 0	P00/TO00	P00 (input)				PMC0	
	P01/TO01	P01 (input)					
	P02/INTP00	P02 (input)					
	P03/INTP01	P03 (input)					
	P04/INTP02	P04 (input)					
	P05/INTP03	P05 (input)					
	P06/INTP04/TCLR0	P06 (input)					
	P07/INTP05/TI0	P07 (input)					
Port 1	P10/INTP10	P10 (input)				PMC1	
	P11/INTP11	P11 (input)					
	P12/INTP12	P12 (input)					
	P13/INTP13	P13 (input)					
	P14/INTP14/TI1	P14 (input)					
	P15/TO20	P15 (input)					
	P16/INTP20/TI20	P16 (input)					
	P17	P17 (input)					
Port 2	P20/NMI	NMI (input)				—	
	P21/INTP30	P21 (input)					PMC2
	P22/ADTRG	P22 (input)					
	P23/INTP50	P23 (input)					
	P24/INTP51	P24 (input)					
	P25/INTP52	P25 (input)					
	P26/INTP53	P26 (input)					
Port 3	P30/SO0/TDX	P30 (input)				PMC3	
	P31/SI0/RXD	P31 (input)					
	P32/̄SCK0	P32 (input)					
	P33/SO1/SDA	P33 (input)					
	P34/SI1	P34 (input)					
	P35/̄SCK1/SCL	P35 (input)					
	P36	P36 (input)					
Port 4	P40/AD0 to P47/AD7	P40 to P47 (all input)		AD0 to AD7 (all input/output)		MM	
Port 5	P50/AD8 to P57/AD15	P50 to P57 (all input)		AD8 to AD15 (all input/output)		MM	
Port 6	P60/A16 to P67/A23	P60 to P67 (all input)		AD16 to A23 (all output)		MM	
Port 7	P70/ANI0 to P77/ANI7	P70/ANI0 to P77/ANI7 (all input)				—	
Port 8	P80/ANI8 to P87/ANI15	P80ANI8 to P87ANI15 (all input)				—	

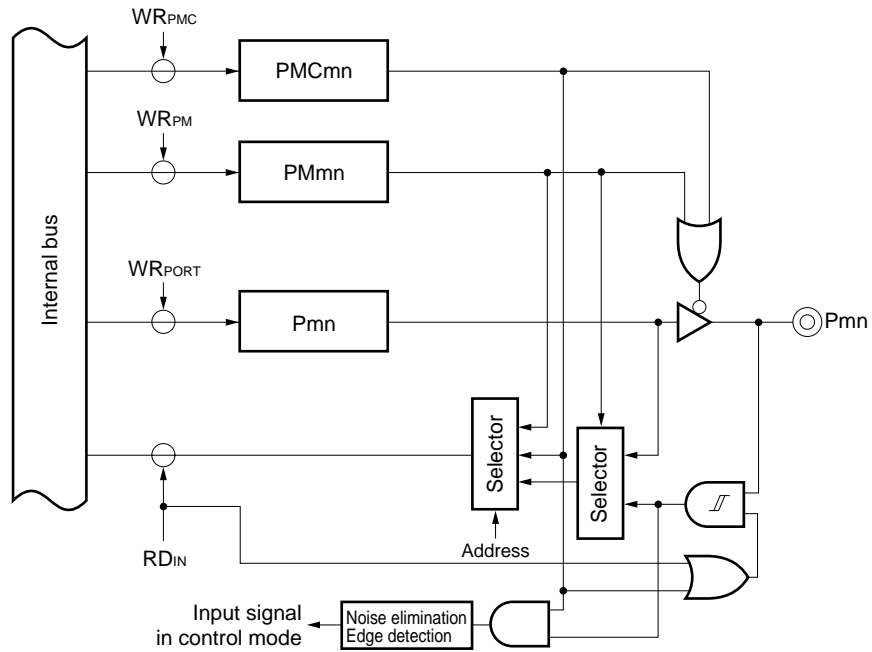
Port Name	Pin Name	Function after Reset (Input/output is shown in parentheses)				Register for Setting Mode
		In Single-Chip Mode 1	In Single-Chip Mode 2	In ROM-less Mode 1	In ROM-less Mode 2	
Port 9	P90/ $\overline{\text{LBEN}}$ / $\overline{\text{WRL}}$	P90 (input)		$\overline{\text{LBEN}}$ (output)	$\overline{\text{WRL}}$ (output)	MM
	P91/ $\overline{\text{UBEN}}$	P91 (input)		$\overline{\text{UBEN}}$ (output)		
	P92/R/ $\overline{\text{W}}$ / $\overline{\text{WRH}}$	P92 (input)		R/ $\overline{\text{W}}$ (output)	$\overline{\text{WRH}}$ (output)	
	P93/ $\overline{\text{DSTB}}$ / $\overline{\text{RD}}$	P93 (input)		$\overline{\text{DSTB}}$ (output)	$\overline{\text{RD}}$ (output)	
	P94/ $\overline{\text{ASTB}}$	P94 (input)		$\overline{\text{ASTB}}$ (output)		
	P95/ $\overline{\text{HLDK}}$	P95 (input)				
	P96/ $\overline{\text{HLDRQ}}$	P96 (input)				
Port 10	P100/PWM0	P100 (input)				PMC10
	P101/PWM1	P101 (input)				
	P102/PWM2	P102 (input)				
	P103/PWM3	P103 (input)				
Port 11	P110/TO21	P110 (input)				PMC11
	P111/INTP21/TI21	P111 (input)				
	P112/TO22	P112 (input)				
	P113/INTP22/TI22	P113 (input)				
	P114/TO23	P114 (input)				
	P115/INTP23/TI23	P115 (input)				
	P116/TO24	P116 (input)				
	P117/INTP24/TI24	P117 (input)				
Port 12	P120/SO2	P120 (input)				PMC12
	P121/SI2	P121 (input)				
	P122/ $\overline{\text{SCK2}}$	P122 (input)				
	P123/SO3	P123 (input)				
	P124/SI3	P124 (input)				
	P125/ $\overline{\text{SCK3}}$	P125 (input)				
	P126	P126 (input)				
	P127/CLO	P127 (input)				
Port 13	P130/RTP0 to P137/RTP7	P130 to P137 (all input)				PMC13
Port 14	P140 to P147	P140 to P147 (all input)				—

Figure 12-1. Block Diagram of Type A



Remark m: port number
n: bit number

Figure 12-2. Block Diagram of Type B



Remark m: port number
n: bit number

Figure 12-3. Block Diagram of Type C

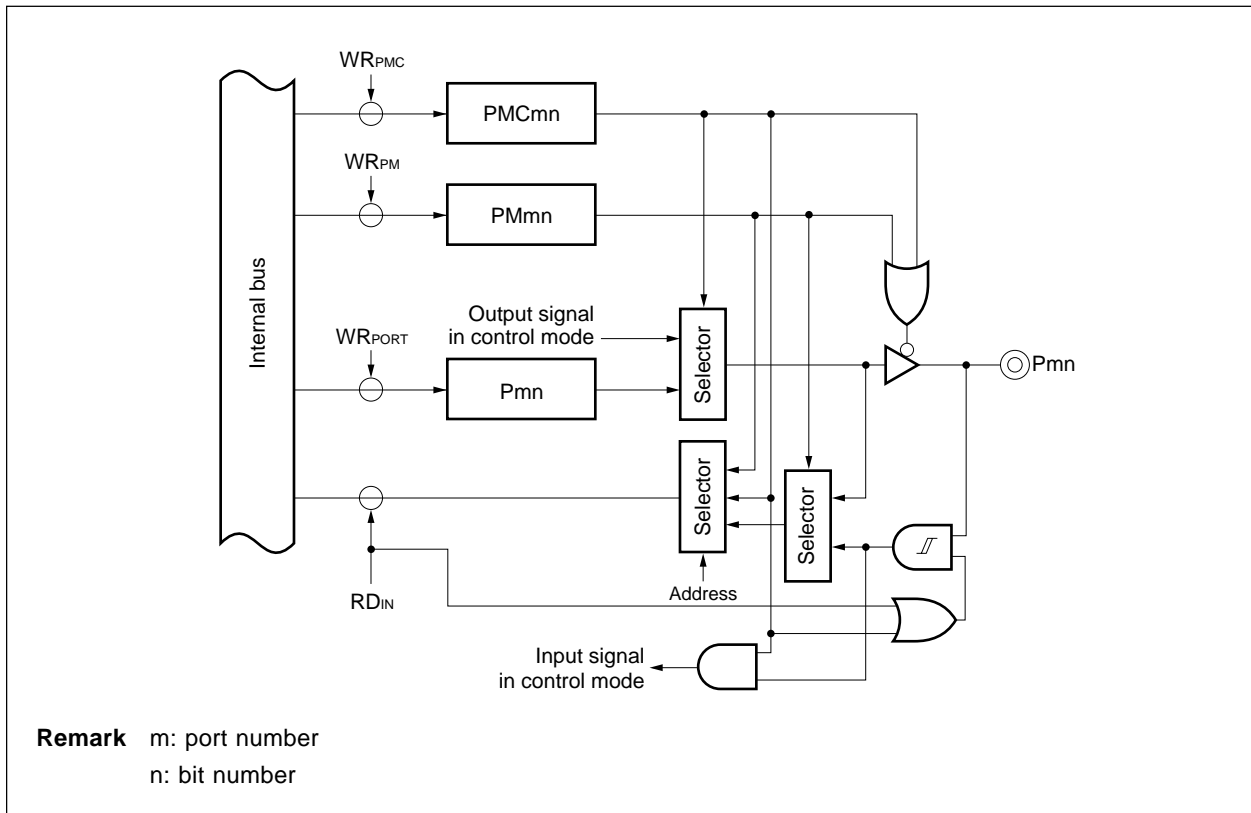


Figure 12-4. Block Diagram of Type D

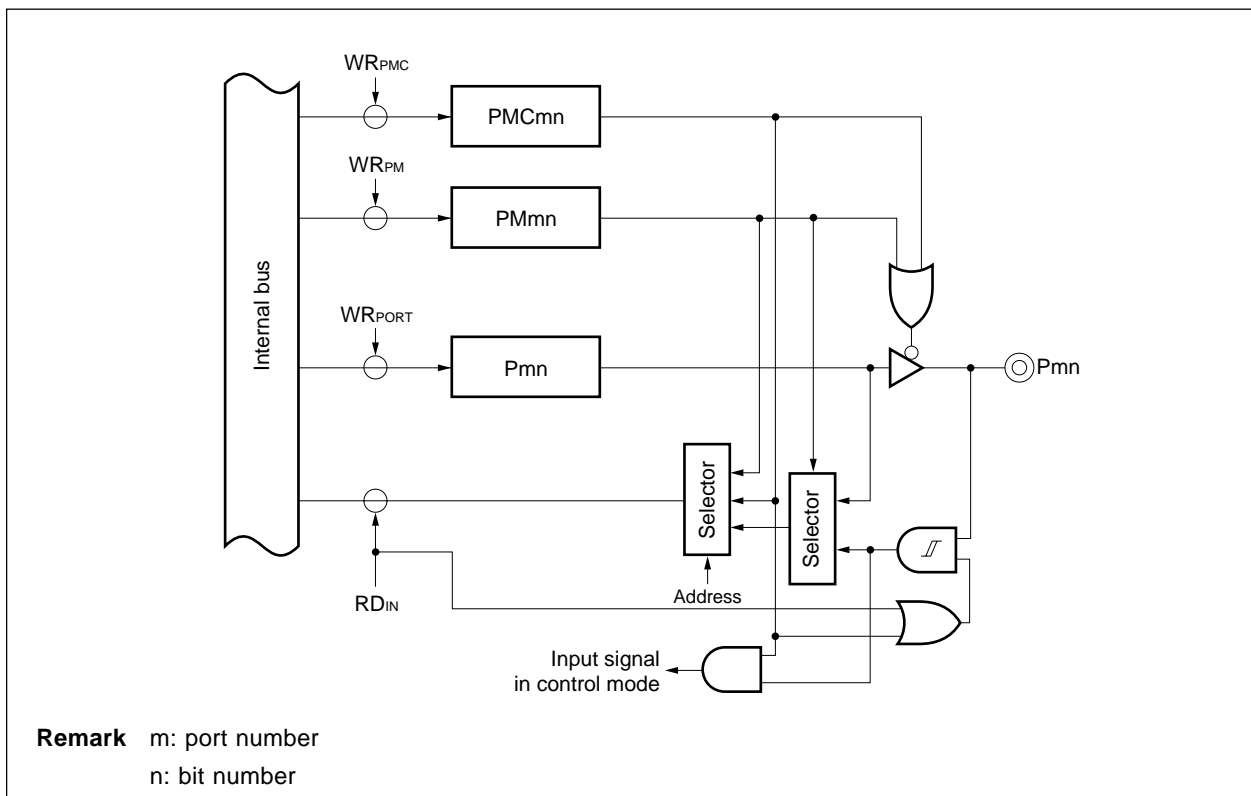
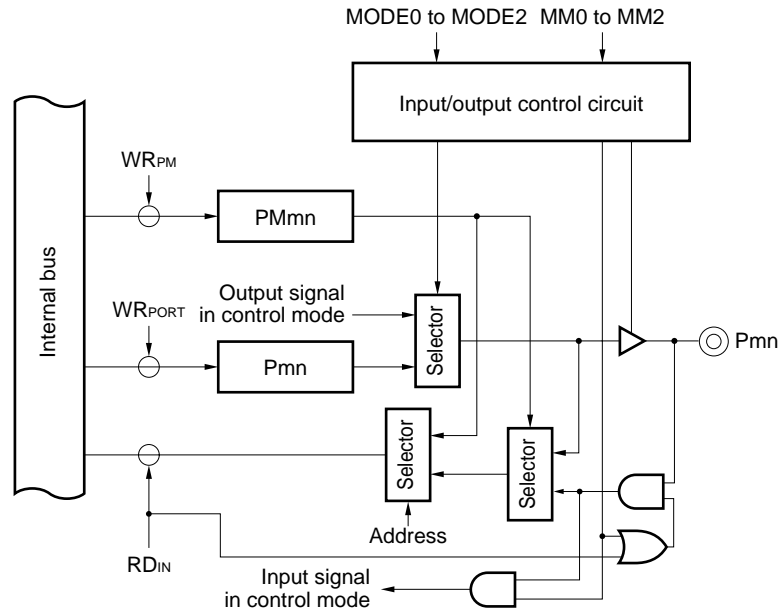
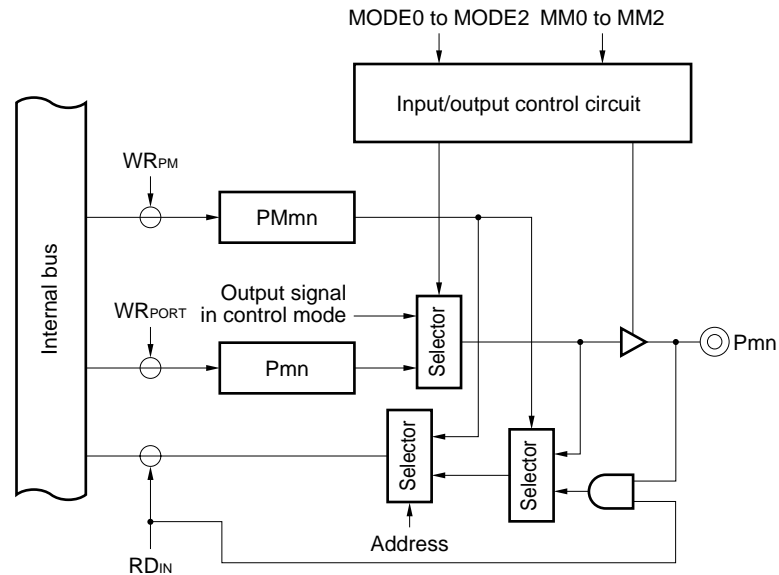


Figure 12-5. Block Diagram of Type E



Remark m: port number
n: bit number

Figure 12-6. Block Diagram of Type F



Remark m: port number
n: bit number

Figure 12-7. Block Diagram of Type G

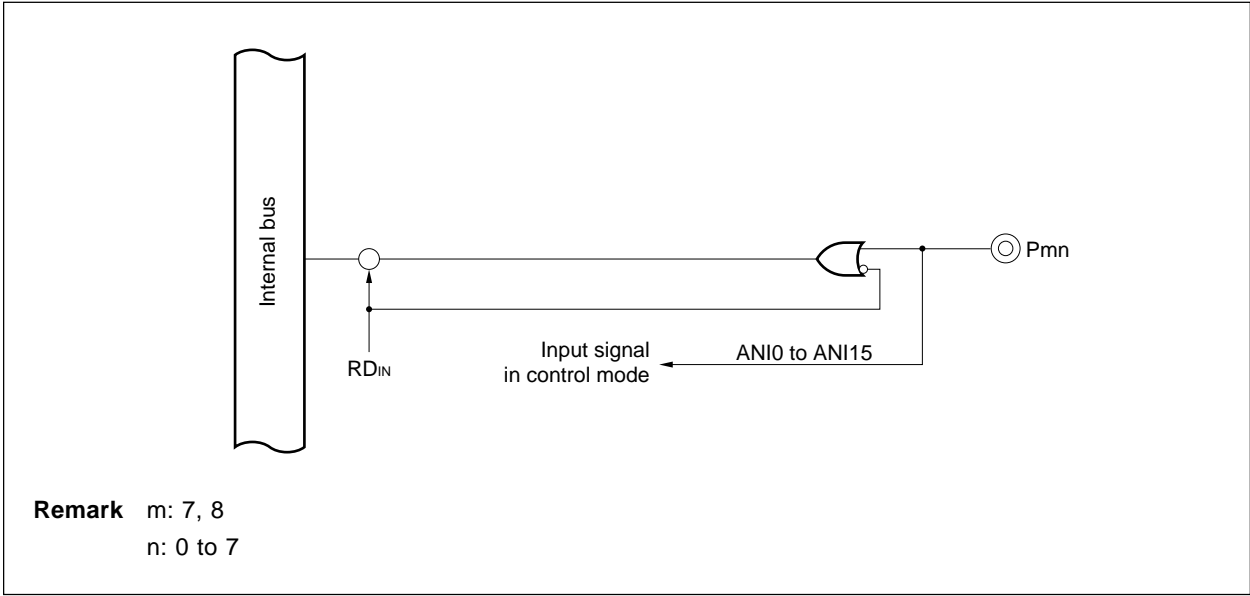


Figure 12-8. Block Diagram of Type H

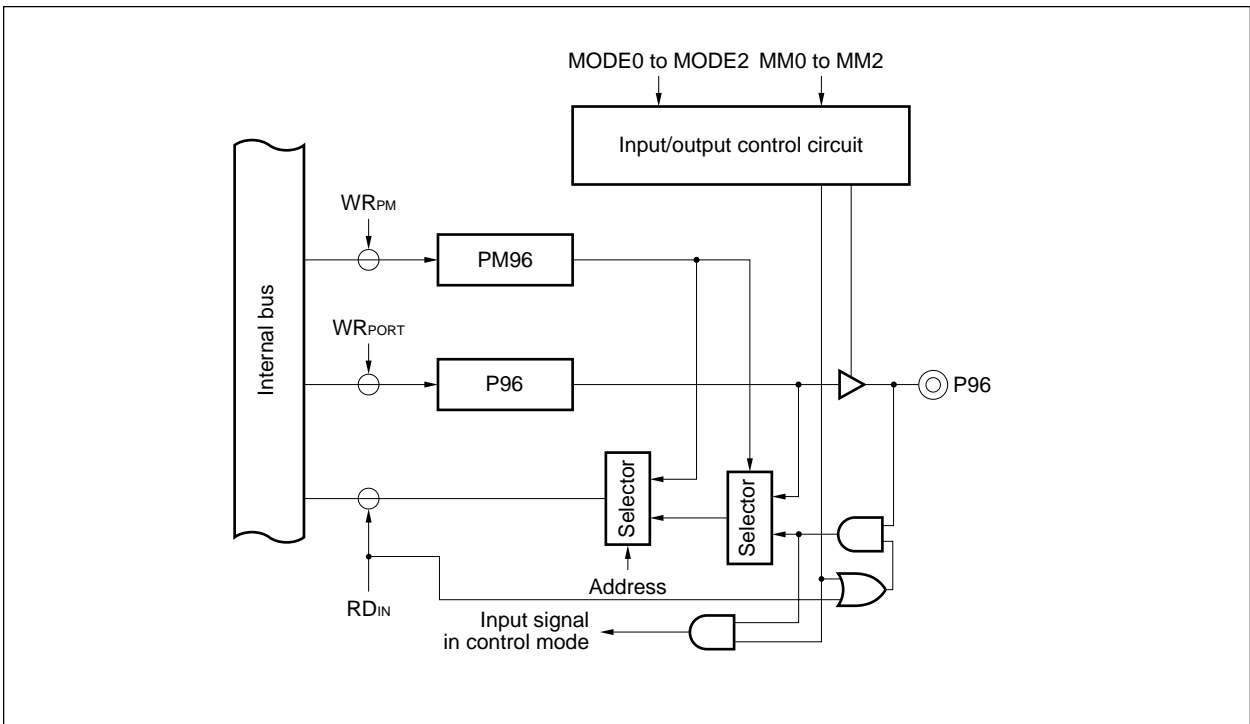


Figure 12-9. Block Diagram of Type I

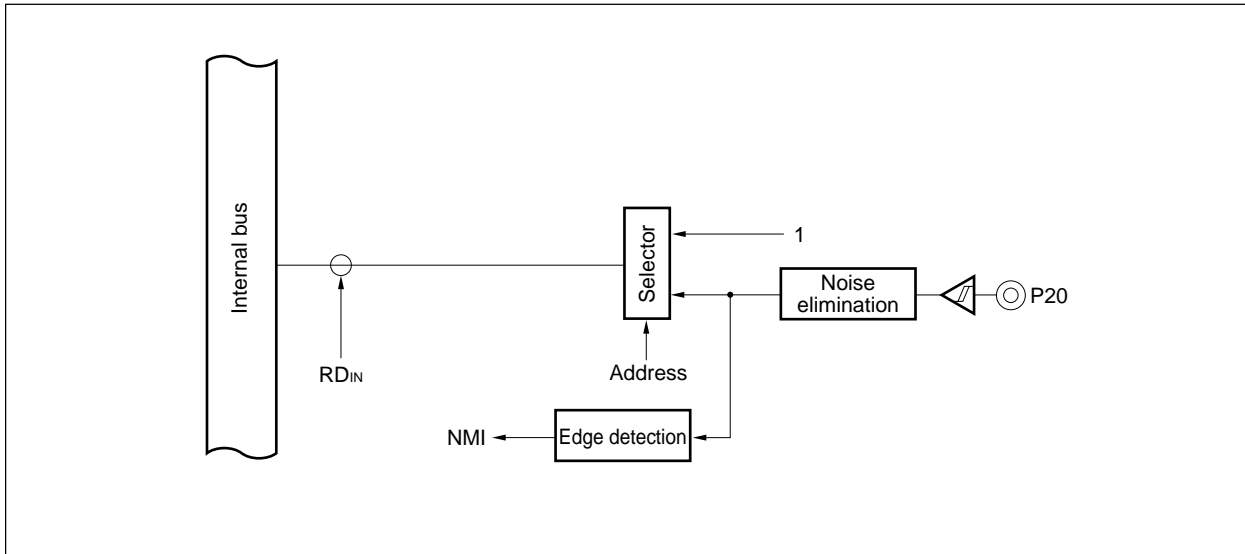


Figure 12-10. Block Diagram of Type J

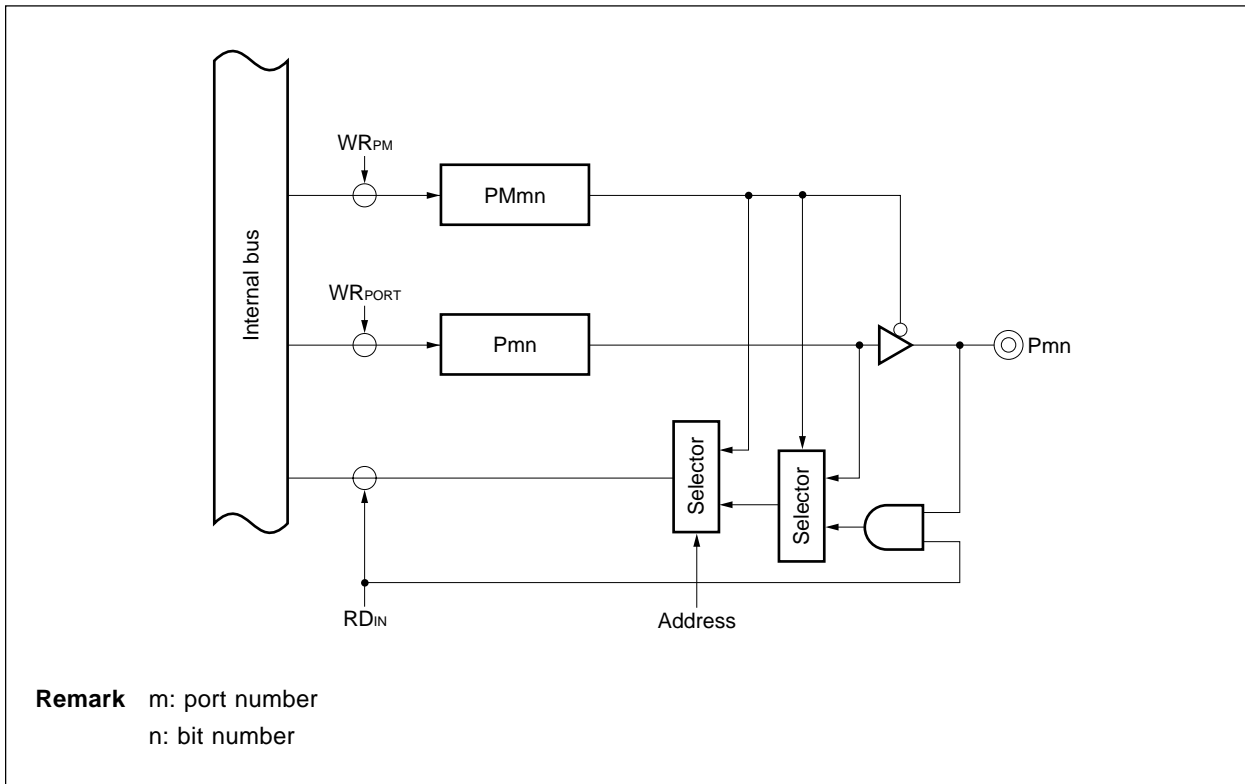
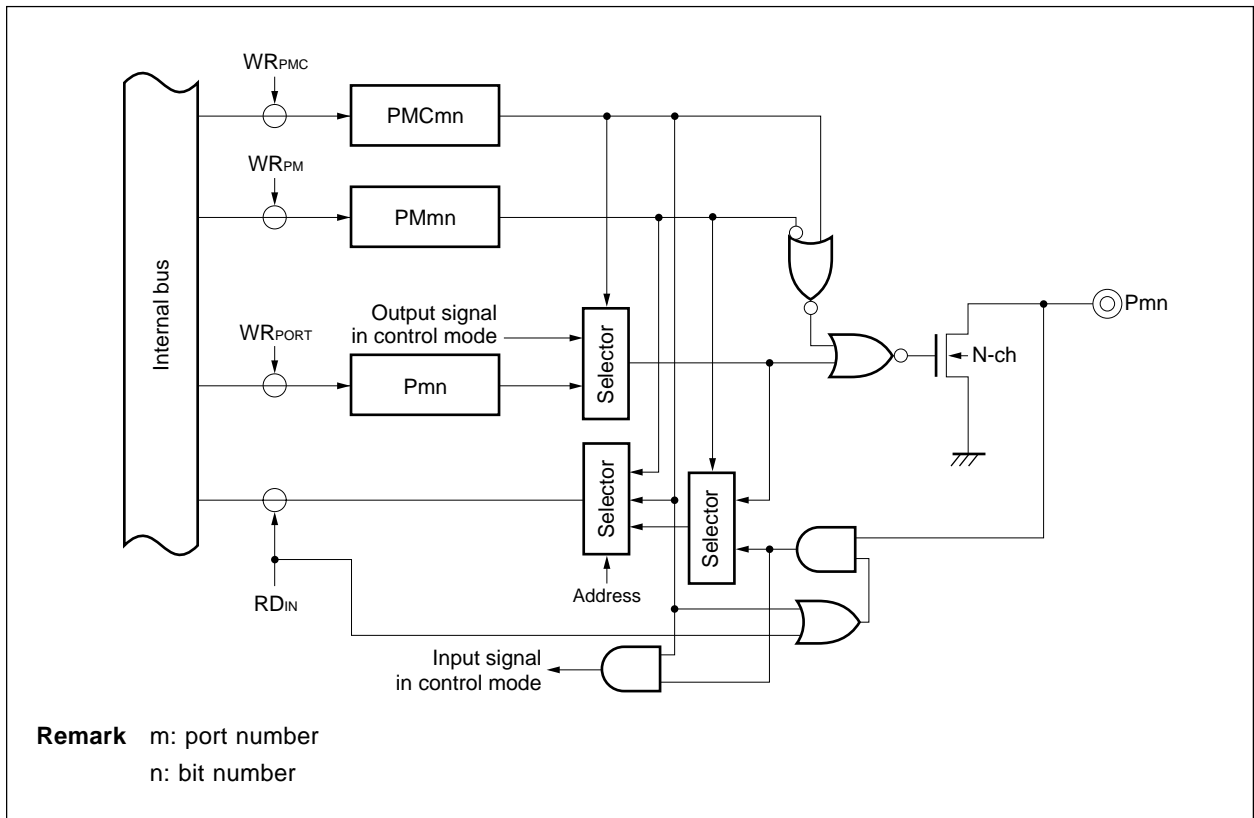


Figure 12-11. Block Diagram of Type K



12.3 Port Pin Function

12.3.1 Port 0

Port 0 is an 8-bit input/output port that can be set to the input or output mode in 1-bit units.

	7	6	5	4	3	2	1	0		
P0	P07	P06	P05	P04	P03	P02	P01	P00	Address FFFFF000H	After reset Undefined

Bit Position	Bit Name	Function
7 to 0	P0n (n = 7 to 0)	Port 0 I/O port

In addition to the function as a general I/O port, this port can also be used to input/output signals of the real-time pulse unit (RPU) and input external interrupt requests, when placed in the control mode.

(1) Operations in control mode

Port		Control Mode	Function in Control Mode	Block Type
Port 0	P00	TO00	RPU output	A
	P01	TO01		
	P02	INTP00	External interrupt request input/RPU capture trigger input	B
	P03	INTP01		
	P04	INTP02		
	P05	INTP03		
	P06	TCLR0/INTP04	External interrupt request input/RPU input	
	P07	TI0/INTP05		

(2) Setting input/output mode and control mode

The input/output mode of port 0 is set by port mode register 0 (PM0). The control mode is set by port mode control register 0 (PMC0).

Port 0 mode register (PM0)

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
PM0	PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00	Address FFFFFF020H	After reset FFH

Bit Position	Bit Name	Function
7 to 0	PM00 to PM07	Port Mode Sets P00 to P07 pins in input/output mode. 0: Output mode (output buffer ON) 1: Input mode (output buffer OFF)

Port 0 mode control register (PMC0)

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
PMC0	PMC07	PMC06	PMC05	PMC04	PMC03	PMC02	PMC01	PMC00	Address FFFFFF040H	After reset 00H

Bit Position	Bit Name	Function
7	PMC07	Port mode Control Specifies operation mode of P07 pin. 0: I/O port mode 1: External interrupt request input (INTP05)/TI0 input mode
6	PMC06	Port Mode Control Specifies operation mode of P06 pin. 0: I/O port mode 1: External interrupt request input (INTP04)/TCLR0 input mode
5 to 2	PMC05 to PMC02	Port Mode Control Specifies operation mode of P05 to P02 pins. 0: I/O port mode 1: External interrupt request input (INTP03 to INTP00)
1	PMC01	Port Mode Control Specifies operation mode of P01 pin. 0: I/O port mode 1: TO01 output mode
0	PMC00	Port Mode Control Specifies operation mode of P00 pin. 0: I/O port mode 1: TO00 output mode

12.3.2 Port 1

Port 1 is an 8-bit input/output port that can be set in the input or output mode in 1-bit units.

	7	6	5	4	3	2	1	0		
P1	P17	P16	P15	P14	P13	P12	P11	P10	Address FFFFF002H	After reset Undefined

Bit Position	Bit Name	Function
7 to 0	P1n (n = 7 to 0)	Port 1 I/O port

In addition to the function as a general I/O port, this port can also be used to input/output signals of the real-time pulse unit (RPU), and to input external interrupts when placed in the control mode.

(1) Operations in control mode

Port		Control Mode	Function in Control Mode	Block Type
Port 1	P10	INTP10	External interrupt request input/RPU capture trigger input	B
	P11	INTP11		
	P12	INTP12		
	P13	INTP13		
	P14	TI1/INTP14	External interrupt request input	A
	P15	TO20	RPU output	
	P16	TI20/INTP20	External interrupt request input/RPU input	
	P17	—	Port only	J

(2) Setting input/output mode

The input/output mode of port 1 is set by port mode register 1 (PM1). The control mode is set by port mode control register 1 (PMC1).

Port 1 mode register (PM1)

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	Address FFFFFF022H	After reset FFH

Bit Position	Bit Name	Function
7 to 0	PM1n (n = 7 to 0)	Port Mode Sets P1n pin in input/output mode. 0: Output mode (output buffer ON) 1: Input mode (output buffer OFF)

Port 1 mode control register (PMC1)

This register can be read/written in 8- or 1-bit units. However, bit 7 is fixed to “0” and ignored when “1” is written.

	7	6	5	4	3	2	1	0		
PMC1	0	PMC16	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	Address FFFFFF042H	After reset 00H

Bit Position	Bit Name	Function
6	PMC16	Port Mode Control Specifies operation mode of P16 pin. 0: I/O port mode 1: External interrupt request input (INTP20)/TI20 input mode
5	PMC15	Port Mode Control Specifies operation mode of P15 pin. 0: I/O port mode 1: TO20 output mode
4	PMC14	Port Mode Control Specifies operation mode of P14 pin. 0: I/O port mode 1: External interrupt request input (INTP14)/TI1 input mode
3 to 0	PMC13 to PMC10	Port Mode Control Specifies operation mode of P13 to P10 pins. 0: I/O port mode 1: External interrupt request input (INTP13 to INTP10)

12.3.3 Port 2

Port 2 is an 8-bit input/output port that can be set in the input or output mode in 1-bit units. P20, however, always operates as the NMI input when an edge is input.

	7	6	5	4	3	2	1	0		
P2	–	P26	P25	P24	P23	P22	P21	P20	Address FFFFF004H	After reset Undefined

Bit Position	Bit Name	Function
6 to 1	P2n (n = 6 to 1)	Port 2 I/O port
0	P20	NMI input level

In addition to the function as a port, this port can also be used as the external interrupt request input, when placed in the control mode.

When port 2 is accessed in 8-bit units for write, the data in the higher 1 bit is ignored. When it is accessed in 8-bit units for read, undefined data is read.

(1) Operations in control mode

Port	Control Mode	Function in Control Mode	Block Type
Port 2	P20	NMI	Non-maskable interrupt request input
	P21	INTP30	External interrupt request input (capture trigger input)
	P22	ADTRG	A/D converter trigger input
	P23	INTP50	External interrupt request input
	P24	INTP51	
	P25	INTP52	
	P26	INTP53	

(2) Setting input/output mode and control mode

The input/output mode of port 2 is set by port mode register 2 (PM2). The control mode is set by port mode control register 2 (PMC2). P20 is fixed to NMI input.

Port 2 mode register (PM2)

This register can be read/written in 8- or 1-bit units. However, bit 0 and bit 7 are fixed to “1” by hardware and ignored when 0 is written in.

	7	6	5	4	3	2	1	0		
PM2	1	PM26	PM25	PM24	PM23	PM22	PM21	1	Address FFFFFF024H	After reset FFH

Bit Position	Bit Name	Function
6 to 1	PM2n (n = 6 to 1)	Port Mode Sets P2n pin in input/output mode. 0: Output mode (output buffer ON) 1: Input mode (output buffer OFF)

Port 2 mode control register (PMC2)

This register can be read/written in 8- or 1-bit units. However, bit 0 is fixed to “1” by hardware, and ignored when “0” is written. Bit 7 is fixed to “0” by hardware, and ignored when “1” is written.

	7	6	5	4	3	2	1	0		
PMC2	0	PMC26	PMC25	PMC24	PMC23	PMC22	PMC21	1	Address FFFFFF044H	After reset 01H

Bit Position	Bit Name	Function
6 to 3	PMC26 to PMC23	Port Mode Control Sets operation mode of P26 to P23 pins. 0: I/O port mode 1: External interrupt request input (INTP53 to INTP50)
2	PMC22	Port Mode Control Sets operation mode of P22 pin. 0: I/O port mode 1: AD converter trigger input (ADTRG)
1	PMC21	Port Mode Control Sets operation mode of P21 pin. 0: I/O port mode 1: External interrupt request input (INTP30)

Remark Bit 0 is fixed to NMI input mode.

12.3.4 Port 3

Port 3 is a 7-bit input/output port that can be set in the input or output mode in 1-bit units.

	7	6	5	4	3	2	1	0		
P3	–	P36	P35	P34	P33	P32	P31	P30	Address FFFFFF06H	After reset Undefined

Bit Position	Bit Name	Function
6 to 0	P3n (n = 6 to 0)	Port 3 I/O port

In addition to the function as a port, this port can also be used as the input/output lines of the serial interface (UART, CSI, I²C), when placed in the control mode. P33 and P35 are multiplexed with SDA and SCL pin of I²C bus, respectively, and output is N-ch open drain.

When port 3 is accessed in 8-bit units for write, the data in the higher 1 bit is ignored. When it is accessed in 8-bit units for read, undefined data is read.

(1) Operations in control mode

Port		Control Mode	Function in Control Mode	Block Type
Port 3	P30	SO0/TXD	Serial interface I/O (UART, CSI, I ² C)	A
	P31	SI0/RXD		D
	P32	$\overline{\text{SCK0}}$		C
	P33	SO1/SDA		K
	P34	SI1		D
	P35	$\overline{\text{SCK1/SCL}}$		K
	P36	–	Port only	J

(2) Setting input/output mode and control mode

The input/output mode of port 3 is set by port mode register 3 (PM3). The control mode is set by port mode control register 3 (PMC3).

Port 3 mode register (PM3)

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
PM3	1	PM36	PM35	PM34	PM33	PM32	PM31	PM30	Address FFFFFF026H	After reset FFH

Bit Position	Bit Name	Function
6 to 0	PM3n (n = 6 to 1)	Port Mode Sets P3n pin in input/output mode. 0: Output mode (output buffer ON) 1: Input mode (output buffer OFF)

Port 3 mode control register (PMC3)

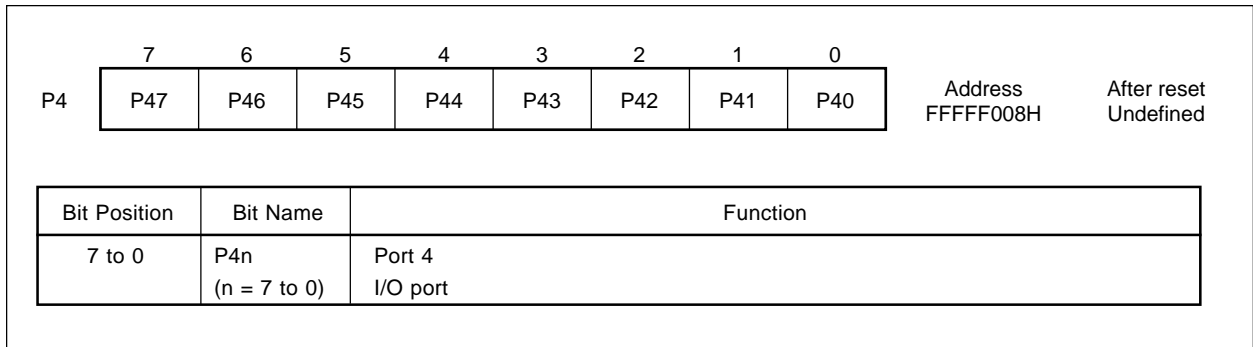
This register can be read/written in 8- or 1-bit units. However, the higher 2 bits are fixed to “0” by hardware, and ignored when “1” is written in.

	7	6	5	4	3	2	1	0		
PMC3	0	0	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30	Address FFFFF046H	After reset 00H

Bit Position	Bit Name	Function
5	PMC35	Port Mode Control Sets operation mode of P35 pin. 0: I/O port mode 1: SCK1/SCL output mode
4	PMC34	Port Mode Control Sets operation mode of P34 pin. 0: I/O port mode 1: SI1 input mode
3	PMC33	Port Mode Control Sets operation mode of P33 pin. 0: I/O port mode 1: SO1/SDA output mode
2	PMC32	Port Mode Control Sets operation mode of P32 pin. 0: I/O port mode 1: SCK0 I/O mode
1	PMC31	Port Mode Control Sets operation mode of P31 pin. 0: I/O port mode 1: SI0/RXD input mode
0	PMC30	Port Mode Control Sets operation mode of P30 pin. 0: I/O port mode 1: SO0/TXD output mode

12.3.5 Port 4

Port 4 is an 8-bit input/output port that can be set in the input or output mode in 1-bit units.



In addition to the function as a general I/O port, this port also serves as an external address/data bus for external memory expansion, when placed in the control mode (external expansion mode).

(1) Operation in control mode

Port		Control Mode	Function in Control Mode	Block Type
Port 4	P40 to P47	AD0 to AD7	Address/data bus for external memory	E

(2) Setting input/output mode and control mode

The input/output mode of port 4 is set by port mode register 4 (PM4). The control mode (external expansion mode) is set by mode specification pins MODE and memory expansion mode register (MM: refer to **3.4.6 (1)**) (n = 0 to 2).

Port 4 mode register (PM4)

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
PM4	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	Address FFFFFF028H	After reset FFH

Bit Position	Bit Name	Function
7 to 0	PM4n (n = 7 to 0)	Port Mode Sets P4n pin in input/output mode. 0: Output mode (output buffer ON) 1: Input mode (output buffer OFF)

Operation mode of port 4

Bit of MM Register			Operation Mode							
MM2	MM1	MM0	P40	P41	P42	P43	P44	P45	P46	P47
0	0	0	Port							
0	1	1	Address/data bus (AD0 to AD7)							
1	0	0								
1	0	1								
1	1	1								
Others			RFU (reserved)							

For the details of mode selection by the MODE pins, refer to **3.3.2 Specifying operation mode**.

In the ROM-less mode, MM0 to MM2 bits are initialized to 111 at system reset, enabling the external expansion mode. External expansion can be disabled by programming the MM0 to MM2 bits and setting the port mode. If MM0 to MM2 are cleared to 000, the subsequent external instruction cannot be fetched.

12.3.6 Port 5

Port 5 is an 8-bit input/output port that can be set in the input or output mode in 1-bit units.

	7	6	5	4	3	2	1	0		
P5	P57	P56	P55	P54	P53	P52	P51	P50	Address FFFFFF00AH	After reset Undefined

Bit Position	Bit Name	Function
7 to 0	P5n (n = 7 to 0)	Port 5 I/O port

In addition to the function as a general I/O port, this port also serves as an external address/data bus for external memory expansion, when placed in the control mode (external expansion mode).

(1) Operation in control mode

Port		Control Mode	Function in Control Mode	Block Type
Port 5	P50 to P57	AD8 to AD15	Address/data bus for external memory	E

(2) Setting input/output mode and control mode

The input/output mode of port 5 is set by port mode register 5 (PM5). The control mode (external expansion mode) is set by mode specification pins MODEn and memory expansion mode register (MM: refer to 3.4.6 (1)) (n = 0 to 2).

Port 5 mode register (PM5)

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
PM5	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	Address FFFFFF02AH	After reset FFH

Bit Position	Bit Name	Function
7 to 0	PM5n (n = 7 to 0)	Port Mode Sets P5n pin in input/output mode. 0: Output mode (output buffer ON) 1: Input mode (output buffer OFF)

Operation mode of port 5

Bit of MM Register			Operation Mode							
MM2	MM1	MM0	P50	P51	P52	P53	P54	P55	P56	P57
0	0	0	Port Address/data bus (AD8 to AD15)							
0	1	1								
1	0	0								
1	0	1								
1	1	1								
Others			RFU (reserved)							

12.3.7 Port 6

Port 6 is an 8-bit input/output port that can be set in the input or output mode in 1-bit units.

P6	7	6	5	4	3	2	1	0	Address FFFFFF00CH	After reset Undefined
	P67	P66	P65	P64	P63	P62	P61	P60		

Bit Position	Bit Name	Function
7 to 0	P6n (n = 7 to 0)	Port 6 I/O port

In addition to the function as a general I/O port, this port also serves as an external address bus for external memory expansion, when placed in the control mode (external expansion mode).

(1) Operation in control mode

Port		Control Mode	Function in Control Mode	Block Type
Port 6	P60 to P67	A16 to A23	Address bus for external memory expansion	F

(2) Setting input/output mode and control mode

The input/output mode of port 6 is set by port mode register 6 (PM6). The control mode (external expansion mode) is set by mode specification pins MODE_n and memory expansion mode register (MM: refer to 3.4.6 (1)) (n = 0 to 2).

Port 6 mode register (PM6)

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
PM6	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	Address FFFFFF02CH	After reset FFH

Bit Position	Bit Name	Function
7 to 0	PM6 _n (n = 7 to 0)	Port Mode Sets P6 _n pin in input/output mode. 0: Output mode (output buffer ON) 1: Input mode (output buffer OFF)

Operation mode of port 6

Bit of MM Register			Operation Mode							
MM2	MM1	MM0	P60	P61	P62	P63	P64	P65	P66	P67
0	0	0	Port							
0	1	1								
1	0	0								
1	0	1								
1	1	0								
1	1	1								
Others			RFU (reserved)							

12.3.8 Port 7, port 8

Port 7 and port 8 are 8-bit input only ports and all pins of port 7 and port 8 are fixed in the input mode.

	7	6	5	4	3	2	1	0		
P7	P77	P76	P75	P74	P73	P72	P71	P70	Address FFFFFF00EH	After reset Undefined
	7	6	5	4	3	2	1	0		
P8	P87	P86	P85	P84	P83	P82	P81	P80	Address FFFFFF010H	After reset Undefined

In addition to the function as input ports, these ports can also always be used as analog input for the A/D converter.

These ports are used also as the analog input pins (ANI0 to ANI7 and ANI8 to ANI15), but the input port and analog input pin cannot be switched. The status of each pin can be read by reading out ports.

(1) Normal operation

Port		Control Mode	Function in Control Mode	Block Type
Port 7	P70 to P77	ANI0 to ANI7	Analog input to A/D converter (only for input in port mode)	G
Port 8	P80 to P87	ANI8 to ANI15		

12.3.9 Port 9

Port 9 is a 7-bit input/output port that can be set in the input or output mode in 1-bit units.

	7	6	5	4	3	2	1	0		
P9	–	P96	P95	P94	P93	P92	P91	P90	Address FFFFFF012H	After reset Undefined

Bit Position	Bit Name	Function
6 to 0	P9n (n = 6 to 0)	Port 9 I/O port

In addition to the function as a general I/O port, this port can also be used to output external bus control signals and output bus hold control signals, when placed in the control mode (external expansion mode). When port 9 is accessed in 8-bit units for write, the higher 1 bit is ignored. When it is accessed in 8-bit units for read, undefined data is read.

(1) Operations in control mode

Port		Control Mode	Function in Control Mode	Block Type
Port 9	P90	$\overline{\text{LBEN}}/\overline{\text{WRL}}$	Control signal output for external memory	F
	P91	$\overline{\text{UBEN}}$		
	P92	$\text{R}/\overline{\text{W}}/\overline{\text{WRH}}$		
	P93	$\overline{\text{DSTB}}/\overline{\text{RD}}$		
	P94	$\overline{\text{ASTB}}$		
	P95	$\overline{\text{HLDAK}}$	Bus hold acknowledge signal output	H
	P96	$\overline{\text{HLDRQ}}$	Bus hold request signal input	

(2) Setting input/output mode and control mode

The input/output mode of port 9 is set by port mode register 9 (PM9). The control mode (external expansion mode) is set by the mode specification pin MODEn and the memory expansion mode register (MM: refer to 3.4.6 (1)) (n = 0 to 2).

Port 9 mode register (PM9)

This register can be read/written in 8- or 1-bit units. However, bit 7 is ignored during write access, and undefined during read access.

PM9	7	6	5	4	3	2	1	0	Address FFFFFF032H	After reset FFH
	–	PM96	PM95	PM94	PM93	PM92	PM91	PM90		

Bit Position	Bit Name	Function
6 to 0	PM9n (n = 6 to 0)	Port Mode Sets P9n pin in input/output mode. 0: Output mode (output buffer ON) 1: Input mode (output buffer OFF)

Operation mode of port 9

P90 to P94

Bit of MM Register			Operation Mode				
MM2	MM1	MM0	P90	P91	P92	P93	P94
0	0	0	Port				
0	1	1	LBEN, WRL	UBEN	R/W, WRH	DSTB, RD	ASTB
1	0	0					
1	0	1					
1	1	1					
Others			RFU (reserved)				

P95, P96

MM3	Operation Mode	P95	P96
0	Port mode	Port	
1	External expansion mode	HLD $\overline{\text{AK}}$	HLD $\overline{\text{RQ}}$

12.3.10 Port 10

Port 10 is a 4-bit input/output port that can be set in the input or output mode in 1-bit units.

P10	7	6	5	4	3	2	1	0	Address FFFFF014H	After reset Undefined
	—	—	—	—	P103	P102	P101	P100		

Bit Position	Bit Name	Function
3 to 0	P10n (n = 3 to 0)	Port 10 I/O port

When port 10 is accessed in 8-bit units for write, the data in the higher 4 bits is ignored. When it is accessed in 8-bit units for read, undefined data is read.

In addition to the function as a general I/O port, this port can also be used to output the PWMn.

(1) Operations in control mode

Port		Control Mode	Function in Control Mode	Block Type
Port 10	P100	PWM0	PWM control signal output	A
	P101	PWM1		
	P102	PWM2		
	P103	PWM3		

(2) Setting input/output mode and control mode

The input/output mode of port 10 is set by port mode register 10 (PM10). The control mode is set by port mode control register 10 (PMC10).

Port 10 mode register (PM10)

This register can be read/written in 8- or 1-bit units. However, the higher 4 bits are fixed to “0” by hardware and ignored when 0 is written in.

	7	6	5	4	3	2	1	0		
PM10	1	1	1	1	PM103	PM102	PM101	PM100	Address FFFFF034H	After reset FFH

Bit Position	Bit Name	Function
3 to 0	PM10n (n = 3 to 0)	Port Mode Sets P10n pin in input/output mode. 0: Output mode (output buffer ON) 1: Input mode (output buffer OFF)

Port 10 mode control register (PMC10)

This port can be read/written in 8- or 1-bit units. However, the higher 4 bits are fixed to “0” and ignored if “1” is written in.

	7	6	5	4	3	2	1	0		
PMC10	0	0	0	0	PMC103	PMC102	PMC101	PMC100	Address FFFFF054H	After reset 00H

Bit Position	Bit Name	Function
3 to 0	PMC10n (n = 3 to 0)	Port Mode Control Sets operation mode of P10n pin. 0: I/O port mode 1: PWMn output mode

12.3.11 Port 11

Port 11 is an 8-bit input/output port that can be set in the input or output mode in 1-bit units.

P11	7	6	5	4	3	2	1	0	Address FFFFF016H	After reset Undefined
	P117	P116	P115	P114	P113	P112	P111	P110		

Bit Position	Bit Name	Function
7 to 0	P11n (n = 7 to 0)	Port 11 I/O port

In addition to the function as a port, this port can also be used to input/output signals of the real-time pulse unit (RPU) and to input external interrupt requests, when placed in the control mode.

(1) Operations in control mode

Port		Alternate Function	Function in Control Mode	Block Type
Port 11	P110	TO21	RPU output	A
	P111	TI21/INTP21	RPU input/external interrupt request input	B
	P112	TO22	RPU output	A
	P113	TI22/INTP22	RPU input/external interrupt request input	B
	P114	TO23	RPU output	A
	P115	TI23/INTP23	RPU input/external interrupt request input	B
	P116	TO24	RPU output	A
	P117	TI24/INTP24	RPU input/external interrupt request input	B

(2) Setting input/output mode and control mode

The input/output mode of port 11 is set by port mode register 11 (PM11). The control mode is set by port mode control register 11 (PMC11).

Port 11 mode register (PM11)

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
PM11	PM117	PM116	PM115	PM114	PM113	PM112	PM111	PM110	Address FFFFF036H	After reset FFH

Bit Position	Bit Name	Function
7 to 0	PM11n (n = 7 to 0)	Port Mode Sets P11n pin in input/output mode. 0: Output mode (output buffer ON) 1: Input mode (output buffer OFF)

Port 11 mode control register (PMC11)

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
PMC11	PMC117	PMC116	PMC115	PMC114	PMC113	PMC112	PMC111	PMC110	Address FFFFF056H	After reset 00H

Bit Position	Bit Name	Function
7	PMC117	Port Mode Control Sets P117 pin in input/output mode. 0: I/O port mode 1: External interrupt request input (INTP24)/TI24 input mode
6	PMC116	Port Mode Control Sets P116 pin in input/output mode. 0: I/O port mode 1: TO24 output mode
5	PMC115	Port Mode Control Sets P115 pin in input/output mode. 0: I/O port mode 1: External interrupt request input (INTP23)/TI23 input mode
4	PMC114	Port Mode Control Sets P114 pin in input/output mode. 0: I/O port mode 1: TO23 output mode
3	PMC113	Port Mode Control Sets P113 pin in input/output mode. 0: I/O port mode 1: External interrupt request input (INTP22)/TI22 input mode
2	PMC112	Port Mode Control Sets P112 pin in input/output mode. 0: I/O port mode 1: TO22 output mode
1	PMC111	Port Mode Control Sets P111 pin in input/output mode. 0: I/O port mode 1: External interrupt request input (INTP21)/TI21 input mode
0	PMC110	Port Mode Control Sets P110 pin in input/output mode. 0: I/O port mode 1: TO21 output mode

12.3.12 Port 12

Port 12 is an 8-bit input/output port that can be set in the input or output mode in 1-bit units.

	7	6	5	4	3	2	1	0		
P12	P127	P126	P125	P124	P123	P122	P121	P120	Address FFFFF018H	After reset Undefined

Bit Position	Bit Name	Function
7 to 0	P12n (n = 7 to 0)	Port 12 I/O port

In addition to the function as a port, this port can also be used as the input/output lines of the serial interface when placed in the control mode.

(1) Operation in control mode

Port	Alternate-Function Pin	Function in Control Mode	Block Type
Port 12	P120	SO2	Serial interface output
	P121	SI2	Serial interface input
	P122	$\overline{\text{SCK2}}$	Serial interface output
	P123	SO3	Serial interface output
	P124	SI3	Serial interface input
	P125	$\overline{\text{SCK3}}$	Serial interface output
	P126	–	Only for port
	P127	CLO	Clock output

(2) Setting input/output mode and control mode

The input/output mode of port 12 is set by the port mode register 12 (PM12). The control mode is set by the port mode control register 12 (PMC12).

Port 12 mode register (PM12)

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
PM12	PM127	PM126	PM125	PM124	PM123	PM122	PM121	PM120	Address FFFFF038H	After reset FFH

Bit Position	Bit Name	Function
7 to 0	PM12n (n = 7 to 0)	Port Mode Set P12n pin in input/output mode. 0: Output mode (output buffer ON) 1: Input mode (output buffer ON)

Port 12 mode control register (PMC12)

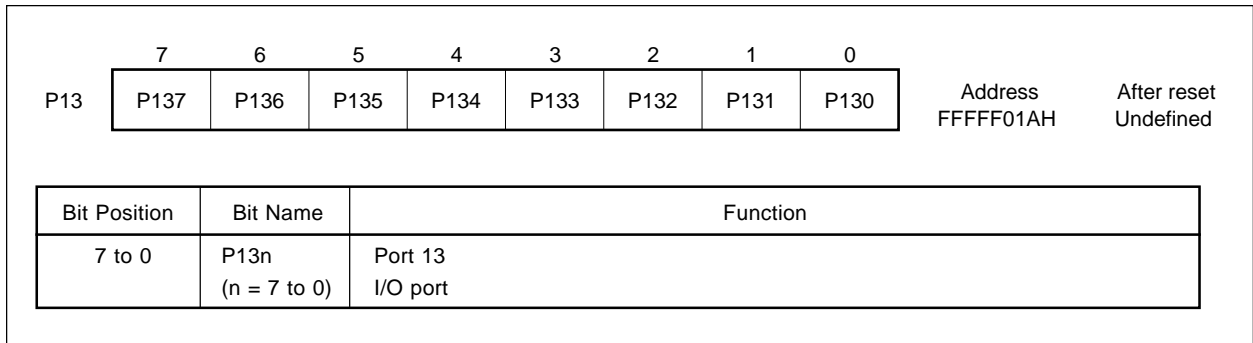
Port 12 can be read/written in 8- or 1-bit units. However, bit 6 is fixed to “0” by hardware and ignored if “1” is written in.

	7	6	5	4	3	2	1	0		
PMC12	PMC127	0	PMC125	PMC124	PMC123	PMC122	PMC121	PMC120	Address FFFFF058H	After reset 00H

Bit Position	Bit Name	Function
7	PMC127	Port Mode Control Sets P127 pin in input/output mode. 0: I/O port mode 1: CLO output mode
5	PMC125	Port Mode Control Sets P125 pin in input/output mode. 0: I/O port mode 1: SCK3 input/output mode
4	PMC124	Port Mode Control Sets P124 pin in input/output mode. 0: I/O port mode 1: SI3 input mode
3	PMC123	Port Mode Control Sets P123 pin in input/output mode. 0: I/O port mode 1: SO3 output mode
2	PMC122	Port Mode Control Sets P122 pin in input/output mode. 0: I/O port mode 1: SCK2 input/output mode
1	PMC121	Port Mode Control Sets P121 pin in input/output mode. 0: I/O port mode 1: SI2 input mode
0	PMC120	Port Mode Control Sets P120 pin in input/output mode. 0: I/O port mode 1: SO2 output mode

12.3.13 Port 13

Port 13 is an 8-bit input/output port that can be set in the input or output mode in 1-bit units.



In addition to the function as a port, this port can also be used as the output of real time output port.

(1) Operation in control mode

Port		Alternate-Function Pin	Function in Control Mode	Block Type
Port 13	P130 to P137	RTP0 to RTP7	Real time output port	A

(2) Setting input/output mode and control mode

The input/output mode of port 13 is set by port mode register 13 (PM13). The control mode is set by port mode control register 13 (PMC13).

Port 13 mode register (PM13)

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
PM13	PM137	PM136	PM135	PM134	PM133	PM132	PM131	PM130	Address FFFFF03AH	After reset FFH

Bit Position	Bit Name	Function
7 to 0	PM13n (n = 7 to 0)	Port Mode Sets P13n pin in input/output mode. 0: Output mode (output buffer ON) 1: Input mode (output buffer OFF)

Port 13 mode control register (PMC13)

This register can be read/written in 8- or 1-bit units.

	7	6	5	4	3	2	1	0		
PMC13	PMC137	PMC136	PMC135	PMC134	PMC133	PMC132	PMC131	PMC130	Address FFFFF05AH	After reset 00H

Bit Position	Bit Name	Function
7 to 0	PMC13n (n = 7 to 0)	Port Mode Control Sets P13n pin in input/output mode. 0: I/O port mode 1: RTPn output mode

Caution When each bit is set to 1, the output buffer of the corresponding port is turned on, regardless of the contents of the PM13 register, and the contents of the RTP register are output. Therefore, initialize the contents of the RTP register before setting each bit to 1.

12.3.14 Port 14

Port 14 is an 8-bit input/output port that can be set in the input or output mode in 1-bit units.

P14	7	6	5	4	3	2	1	0	Address FFFFF01CH	After reset Undefined
	P147	P146	P145	P144	P143	P142	P141	P140		

Bit Position	Bit Name	Function
7 to 0	P14n (n = 7 to 0)	Port 14 I/O port

Port 14 can be used only as a port.

(1) Operation in control mode

Port	Alternate-Function Pin	Function in Control Mode	Block Type
Port 14	P140 to P147	–	Port only

(2) Setting input/output mode and control mode

The input/output mode of port 14 is set by port mode register 14 (PM14). Port 14 does not have port mode control register 14 (PMC14) because it is not provided with the control mode.

Port 14 mode register (PM14)

This register can be read/written in 8- or 1-bit units.

PM14	7	6	5	4	3	2	1	0	Address FFFFF03CH	After reset FFH
	PM147	PM146	PM145	PM144	PM143	PM142	PM141	PM140		

Bit Position	Bit Name	Function
7 to 0	PM14n (n = 7 to 0)	Port Mode Sets P14n pin in input/output mode. 0: Output mode (output buffer ON) 1: Input mode (output buffer OFF)

[MEMO]

CHAPTER 13 RESET FUNCTION

When the low-level is input to the $\overline{\text{RESET}}$ pin, the system is reset and each on-chip hardware is initialized to the initial state.

When the $\overline{\text{RESET}}$ pin changes from low-level to high-level, the reset state is released and the CPU starts executing the program. Initialize the contents of each register in the program as necessary.

13.1 Features

- Analog noise elimination circuit (delay of approx. 60 ns) provided on reset pin

13.2 Pin Function

★ During the reset state, all the pins (except CLKOUT, $\overline{\text{RESET}}$, X2, V_{DD}, V_{SS}, CV_{DD}, CV_{SS}, AV_{DD}, AV_{SS} and AV_{REF} pins) are in the high-impedance state.

When an external memory is connected, a pull-up (or pull-down) resistor must be connected to each pin of ports 4, 5, 6, and 9. Otherwise, the memory contents may be lost if these pins go into a high-impedance state.

Also treat signal outputs of the on-chip peripheral I/O function and the output port so that they will not be affected.

In the ROM-less mode and single-chip mode 2, the CLKOUT signal is output even during the reset period (low level output). In single-chip mode 1, the CLKOUT signal is not output until the PSC register is set. In the flash memory programming mode, the CLKOUT signal is not output (low level output).

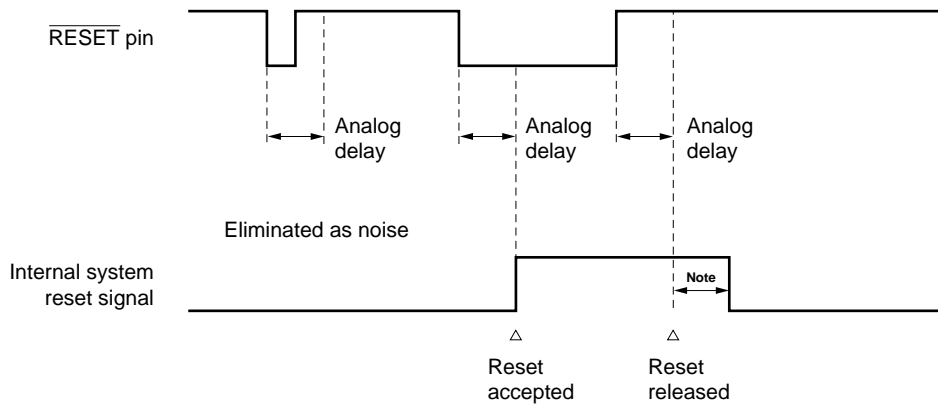
Table 13-1 shows the operating status of each pin during the reset period.

Table 13-1. Operating Status of I/O and Output Pins During Reset Period

I/O or Output Pin	Pin Status				
	In Single-Chip Mode 1	In Single-Chip Mode 2	In ROM-less Mode 1	In ROM-less Mode 2	In Flash Memory Programming Mode
P00 to P07, P10 to P17, P21 to P26, P30 to P37, P95, P96, P100 to P103, P110 to P117, P120 to P127, P130 to P137, P140 to P147	(Input)				Hi-Z
P40 to P47, P50 to P57, P69 to P67, P90 to P94	(Input)		(Control Mode)		
AD0 to AD15, A16 to A23	(Port mode)		Hi-Z		
$\overline{\text{LBEN}}$	(P90)		Hi-Z	$(\overline{\text{WRL}})$	
$\overline{\text{WRL}}$	(P90)		$(\overline{\text{LBEN}})$	Hi-Z	
$\overline{\text{UBEN}}$	(P91)		Hi-Z		
R/ $\overline{\text{W}}$	(P92)		Hi-Z	$(\overline{\text{WRH}})$	
$\overline{\text{WRH}}$	(P92)		R/ $\overline{\text{W}}$	Hi-Z	
$\overline{\text{DSTB}}$	(P93)		Hi-Z	$(\overline{\text{RD}})$	
$\overline{\text{RD}}$	(P93)		$(\overline{\text{DSTB}})$	Hi-Z	
ASTB	(P94)		Hi-Z		
$\overline{\text{HLD\text{AK}}}$	(Port mode)				
CLKOUT	L	Operates			L
SO0, SO2, TXD	(Port mode)				Operation
TO00, TO01, TO20 to TO24, RTP0 to RTP7, SDA, SDL, SO1, SO3, PWM0 to PWM3	(Port mode)				Hi-Z

Remark Hi-Z : High impedance
L : Low-level output

(1) Accepting reset signal



Note The internal system reset signal remains active for the duration of at least 4 system clocks after the reset condition is removed from the $\overline{\text{RESET}}$ pin.

(2) Power-ON reset

For the reset operations at power-on it is necessary to secure an oscillation stabilization time of 10 ms or more from when the power supply starts until reset is accepted by the low-level width of the $\overline{\text{RESET}}$ pin. Furthermore,

★

it is also necessary to secure oscillation stabilization time when an external clock is used in the direct mode.

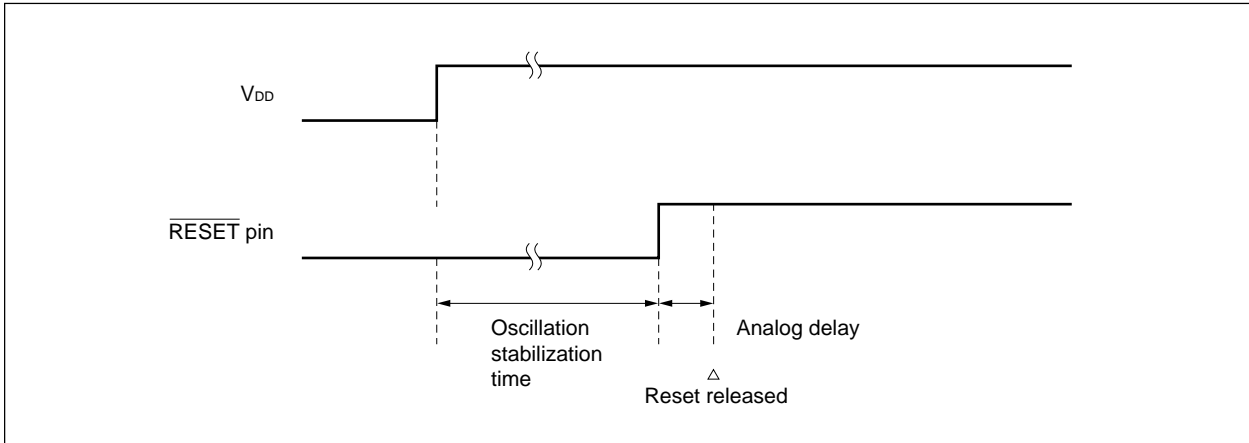
**13.3 Initialize**

Table 13-2 shows the initial value of each register after reset.

The contents of the registers must be initialized in the program as necessary. Especially, set the following registers as necessary because they are related to system setting:

- Power save control register (PSC) ... X1 and X2 pin function, CLKOUT pin operation, etc.
- Data wait control register (DWC) ... Number of data wait states

Table 13-2. Initial Values after Reset of Each Register (1/2)

Register		Initial Value after Reset
r0		00000000H
r1 to r31		Undefined
PC		00000000H
PSW		00000020H
EIPC		Undefined
EIPSW		Undefined
FEPC		Undefined
FEPSW		Undefined
ECR		00000000H
Internal RAM		Undefined
Port	Output latch (P0 to P6, P9 to P14)	Undefined
	Mode register (PM0 to PM6, PM9 to PM14)	FFH
	Mode control register (PMC0, PMC1, PMC3, PMC10 to PMC13) (PMC2)	00H 01H
	Memory expansion mode register (MM)	00H/07H
Clock generator	System status register (SYS)	0000000xB
Clock output	Clock output mode register (CLOM)	00H
Real-time pulse unit	Timer control register (TMC01, TMC02) (TMC00, TMC1, TMC20 to TMC24, TMC3)	00H 01H
	Timer output control register (TOC0, TOC1)	00H
	Capture/compare register (CC00 to CC03, CC00L to CC03L, CC3)	Undefined
	Compare register (CM10, CM11, CM10L, CM11L, CM20 to CM24)	Undefined
	Capture register (CP10 to CP13, CP10L to CP13L, CP3)	Undefined
	Timer register (TM0, TM1, TM0L, TM1L, TM20 to TM24, TM3)	0000H
	Timer overflow status register (TOVS)	00H
A/D converter	A/D converter mode register (ADM0, ADM1)	07H
	A/D conversion result register (ADCR0 to ADCR7)	Undefined

Caution “Undefined” means an undefined value due to power-on reset or data corruption when a falling edge of $\overline{\text{RESET}}$ coincides with a data write operation. The previous status of data is retained by a falling edge of $\overline{\text{RESET}}$ in cases other than the above.

Table 13-2. Initial Values after Reset of Each Register (2/2)

	Register	Initial Value after Reset
Real-time output function	Port 13 buffer register (PB)	Undefined
	Output latch register (RTP)	Undefined
Serial interface	Asynchronous serial interface mode register (ASIM0)	80H
	Asynchronous serial interface mode register (ASIM1)	00H
	Asynchronous serial interface status register (ASIS)	00H
	Receive buffer (RXB, RXBL)	Undefined
	Transmit shift register (TXS, TXSL)	Undefined
	Clocked serial interface mode register (CSIM0 to CSIM3)	00H
	Serial I/O shift register (SIO0 to SIO3)	Undefined
	Baud rate generator compare register (BRGC0 to BRGC3)	Undefined
	Baud rate generator prescaler mode register (BPRM0 to BPRM3)	00H
	IIC control register (IICC)	00H
	IIC status register (IICS)	00H
	IIC clock selection register (IICCL)	00H
	IIC shift register (IIC)	00H
	Slave address register (SVA)	00H
PWM	PWM control register (PWMC0 to PWMC3)	05H
	PWM prescaler register (PWPR0 to PWPR3)	00H
	PWM modulo register (PWM0 to PWM3)	Undefined
Interrupt/exception processing function	Interrupt control register (xxICn)	47H
	In-service priority register (ISPR)	00H
	External interrupt mode register (INTM0 to INTM7)	00H
	Event divide counter (EDV0 to EDV2)	00H
	Event divide control register (EDVC0 to EDVC2)	01H
	Event selection register (EVS)	00H
Memory management function	Data wait control register (DWC)	FFFFH
	Bus cycle control register (BCC)	AAAAH
	System control register (SYC)	00H/01H
Power save control	Command register (PRCMD)	Undefined
	Power save control register (PSC)	00H/C0H
	Clock control register (CKC)	00H

Caution “Undefined” means an undefined value due to power-on reset or data corruption when a falling edge of $\overline{\text{RESET}}$ coincides with a data write operation. The previous status of data is retained by a falling edge of $\overline{\text{RESET}}$ in cases other than the above.

[MEMO]

CHAPTER 14 FLASH MEMORY (μ PD70F3008 AND 70F3008Y ONLY)

The μ PD70F3008 and 70F3008Y of the V854 are provided with a 128-Kbyte flash memory. In the instruction fetch to this flash memory, 4 bytes can be accessed by a single clock as well as the mask ROM version.

Writing to a flash memory can be performed with memory mounted on the target system (on board). The dedicated flash writer is connected to the target system to perform writing.

The followings can be considered as the development environment and the applications using a flash memory.

- Software can be altered after the V854 is solder mounted on the target system.
- Small scale production of various models is made easier by differentiating software.
- Data adjustment in starting mass production is made easier.

14.1 Features

- 4-byte/1-clock access (in instruction fetch access)
- All area one-shot erase
- Communication through serial interface from the dedicated flash writer
- ★ • Erase/writing voltage: $V_{PP} = 7.8 \text{ V}$
- On-board programming
- Number of rewrite: 100 times (target)

14.2 Writing by Flash Writer

Writing can be performed either on-board or off-board by the dedicated flash writer.

(1) On-board programming

The contents of the flash memory is rewritten after the V854 is mounted on the target system. Mount connectors, etc., on the target system to connect the dedicated flash writer.

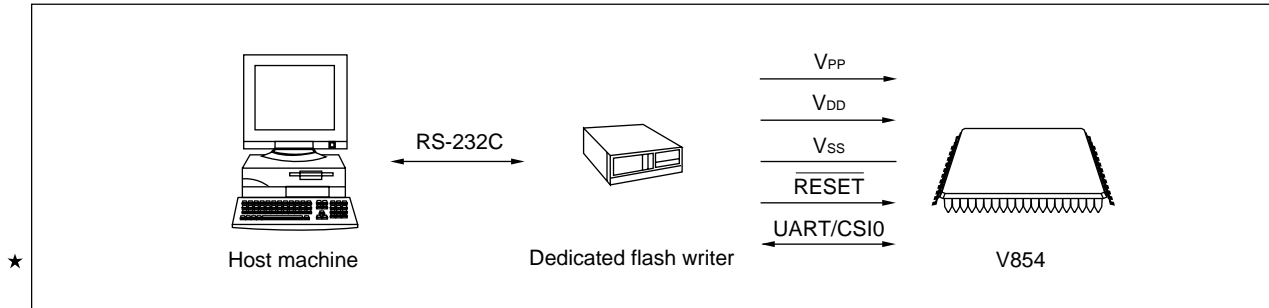
(2) Off-board programming

Writing to a flash memory is performed by the dedicated program adapter (FA Series **Note**), etc., before mounting the V854 on the target system.

Note FA Series program adapters are made by Naito Densei Machidaseisakusho Co., Ltd.

14.3 Programming Environment

The following shows the environment required for writing programs to the flash memory of the V854.



A host machine is required for controlling the dedicated flash writer.

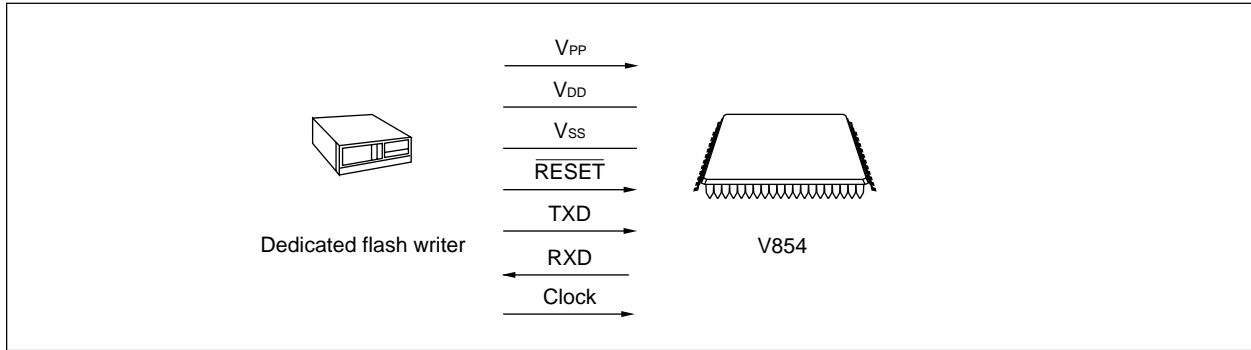
UART or CSI is used as the interface between the dedicated flash writer and the V854 to perform writing, erasing, etc. A dedicated program adapter (FA Series) is required for off-board writing.

14.4 Communication System

- ★ The communication between the dedicated flash writer and the V854 is performed by serial communication using UART or CSIO.

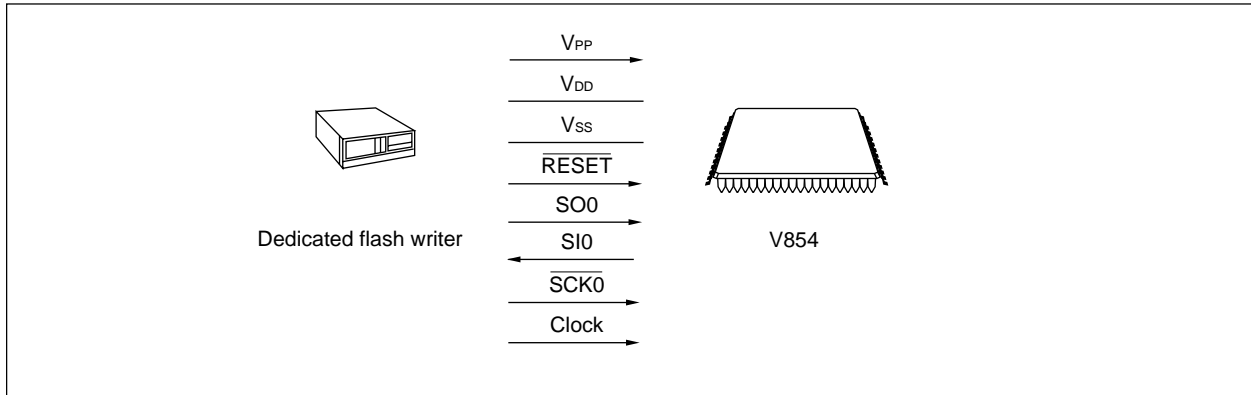
(1) UART

Transfer rate: 1200 to 76800 bps (LSB first)



(2) CSIO

Transfer rate: up to 8.25 Mbps (MSB first)



The dedicated flash writer outputs the transfer clock, and the V854 operates as a slave.

When Flashpro II is used as the dedicated flash writer, it generates the following signals to the V854. For the details, refer to the Flashpro II manual.

Remark Flashpro II is a product of Naitou Densai Machidaseisakusho Co., Ltd.

Flashproll			V854	Measurement when connected	
Signal Name	I/O	Pin Function	Pin Name	CSIn	UART
V _{PP}	Output	Writing voltage	V _{PP}	◎	◎
V _{DD}	I/O	V _{DD} voltage generation/ voltage monitoring	V _{DD}	◎	◎
GND	—	Ground	V _{SS}	◎	◎
CLK	Output	Clock output to V854	X1 ^{Note}	○	○
RESET	Output	Reset signal	RESET	◎	◎
★ SI/RxD	Input	Receive signal	SO0/TxD	◎	◎
★ SO/TxD	Output	Transmit signal	SI0/RxD	◎	◎
★ SCK	Output	Transfer clock	SCK0	◎	x

Note Only for off-board writing

Remark ◎ : Always connected

○ : Does not need to connect, if generated on the target board

x : Does not need to connect

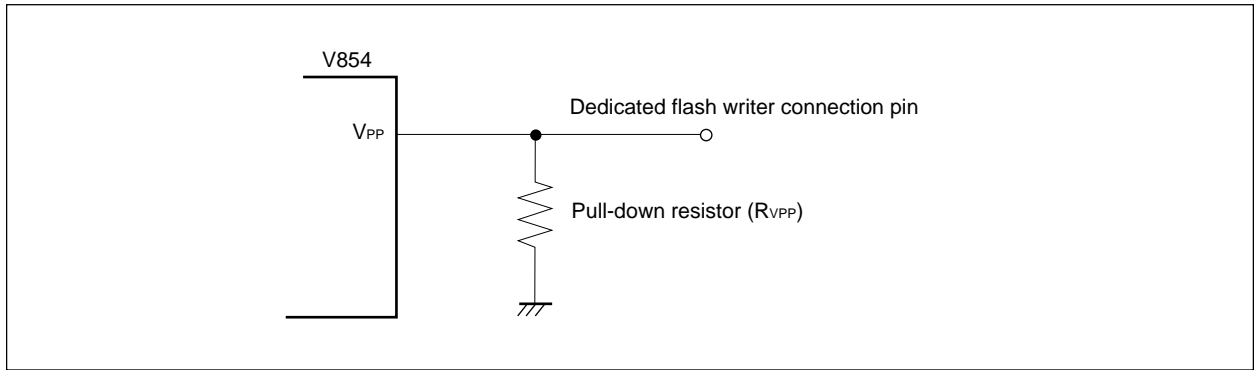
14.5 Pin Handling

When performing on-board writing, install a connector on the target system to connect to the dedicated flash writer. Also, install the function on-board to switch from the normal operation mode to the flash memory programming mode.

When switched to the flash memory programming mode, all the pins not used for the flash memory programming become the same status as that immediately after reset of single-chip mode 1. Therefore, all the ports become high-impedance status, so that pin handling is required when the external device does not acknowledge the high-impedance status.

14.5.1 V_{PP} pin

- ★ In the normal operation mode, 0 V is input to V_{PP} pin. In the flash memory programming mode, 7.8-V writing voltage is supplied to V_{PP} pin. The following shows an example of the connection of V_{PP} pin.



★ 14.5.2 Serial interface pin

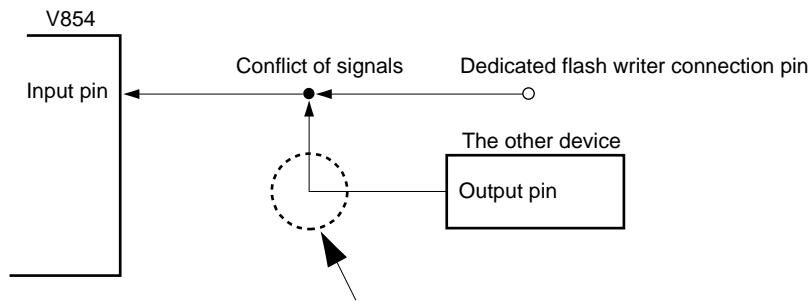
The following shows the pins used by each serial interface.

Serial Interface	Pins Used
CSI0	SO0, SI0, $\overline{\text{SCK0}}$
UART	TXD, RXD

When connecting a dedicated flash writer to a serial interface pin which is connected to other devices on-board, care should be taken to the conflict of signals and the malfunction of other devices, etc.

(1) Conflict of signals

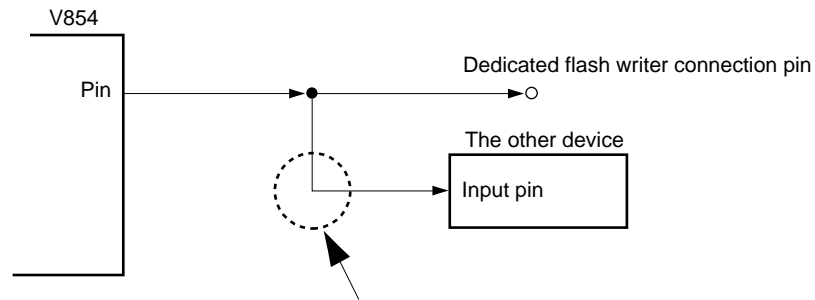
When connecting a dedicated flash writer (output) to a serial interface pin (input) which is connected to another device (output), conflict of signals occurs. To avoid the conflict of signals, isolate the connection to the other device or set the other device to the high-impedance status.



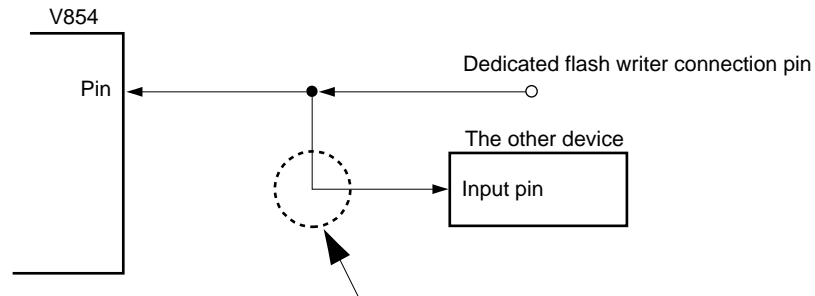
In the flash memory programming mode, the signal that the dedicated flash writer sends out conflicts with signals the other device outputs. Therefore, isolate the signals on the other device side.

(2) Malfunction of the other device

When connecting a dedicated flash writer (output or input) to a serial interface pin (input or output) connected to another device (input), the signal output to the other device may cause the device to malfunction. To avoid this, isolate the connection to the other device or make the setting so that the input signal to the other device is ignored.



In the flash memory programming mode, if the signal the V854 outputs affects the other device, isolate the signal on the other device side.

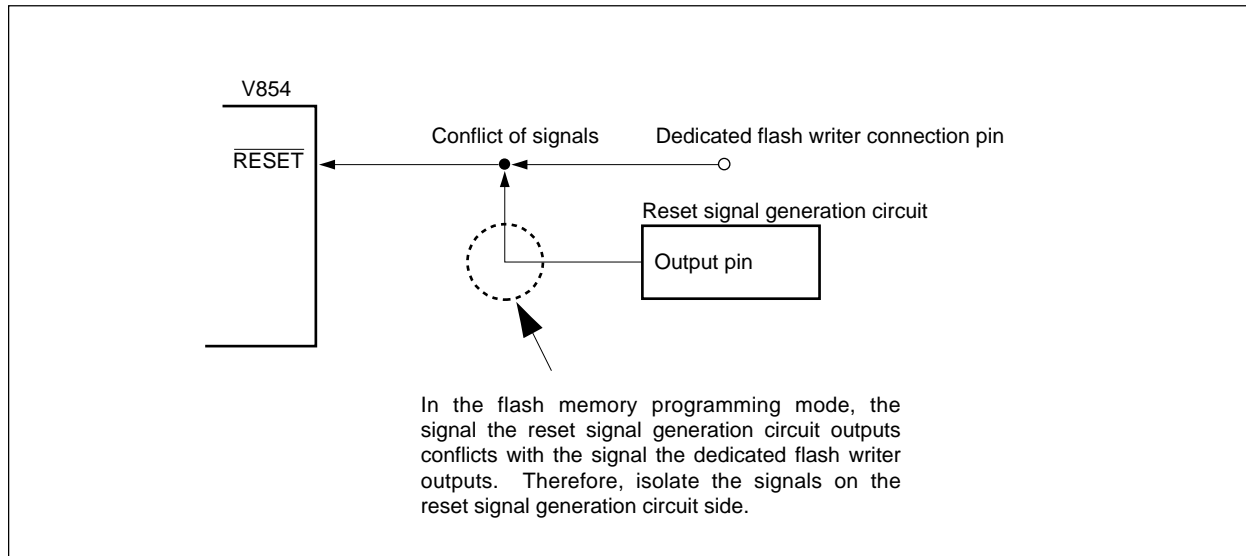


In the flash memory programming mode, if the signal the dedicated flash writer outputs affects the other device, isolate the signal on the other device side.

14.5.3 Reset pin

When connecting the reset signals of the dedicated flash writer to the $\overline{\text{RESET}}$ pin which is connected to the reset signal generation circuit on-board, conflict of signals occurs. To avoid the conflict of signals, isolate the connection to the reset signal generation circuit.

When reset signal is input from the user system during the flash memory programming mode, programming operation will not be performed correctly. Therefore, do not input signals other than the reset signals from the dedicated flash writer.



14.5.4 NMI pin

Do not change the input signal to the NMI pin during the flash memory programming mode. If the NMI pin is changed during the flash memory programming mode, the programming may not be performed correctly.

14.5.5 Mode pin

To switch to the flash memory programming mode, change MODE0 through MODE2 to "111" with a jumper, etc., applies writing voltage to V_{PP} pin, and release the reset.

14.5.6 Port pin

When the flash memory programming mode is set, all the port pins except the pins which communicate with the dedicated flash writer become output high-impedance status. The treatment of these port pins are not necessary. If problems such as disabling output high-impedance status should occurs to the external devices connected to the port, connect them to V_{DD} or V_{SS} through resistors.

14.5.7 Other signal pin

Connect X1, X2, CKSEL, PLLSEL, and AV_{REF} to the same status as that in the normal operation mode.

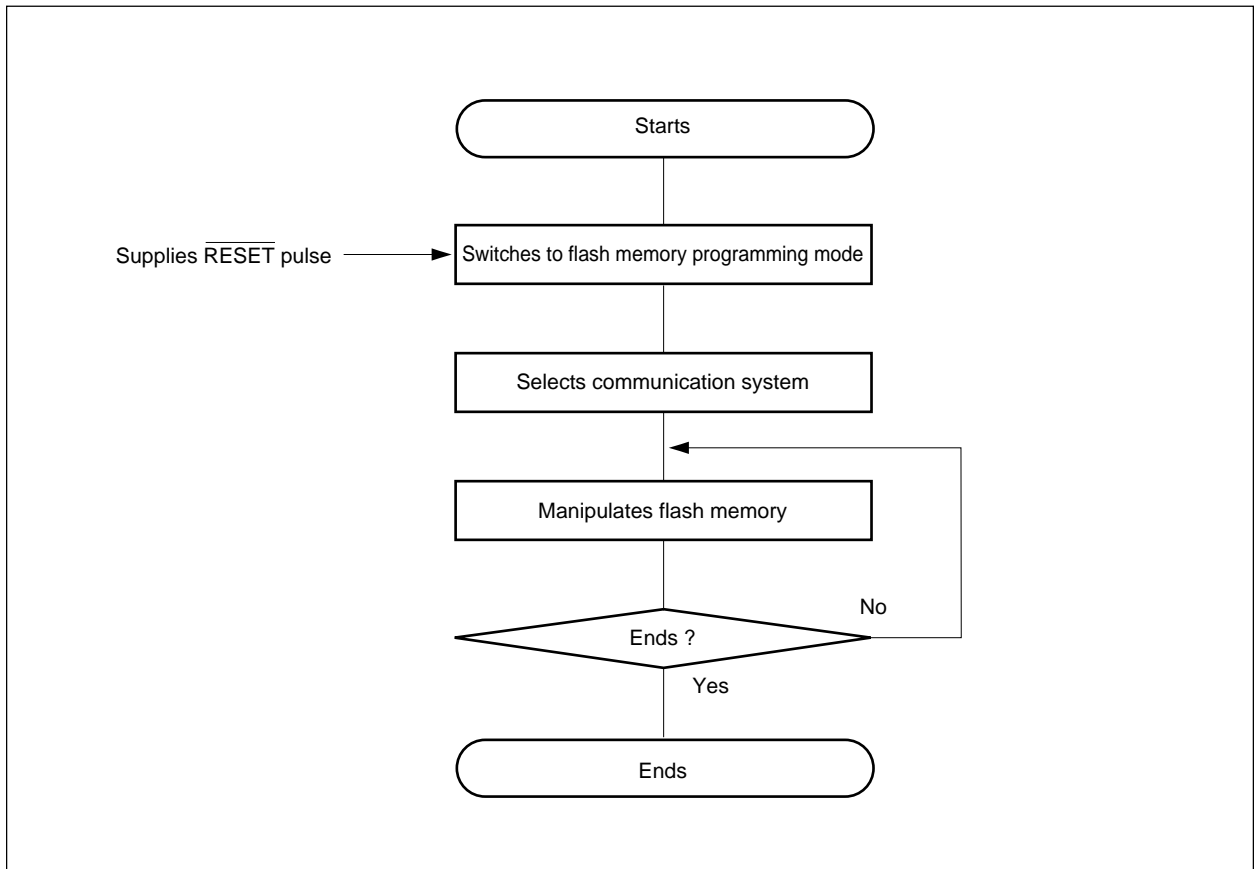
14.5.8 Power supply

- ★ Supply the same power supplies (V_{DD} , V_{SS} , AV_{DD} , AV_{SS} , CV_{DD} , CV_{SS}) as those in the normal operation mode. Connect V_{DD} and GND of the dedicated flash writer to V_{DD} and V_{SS} . (The V_{DD} dedicated flash writer is provided with a power supply monitoring function.)

14.6 Programming Method

14.6.1 Flash memory control

The following shows the procedure that this firmware manipulates the flash memory.



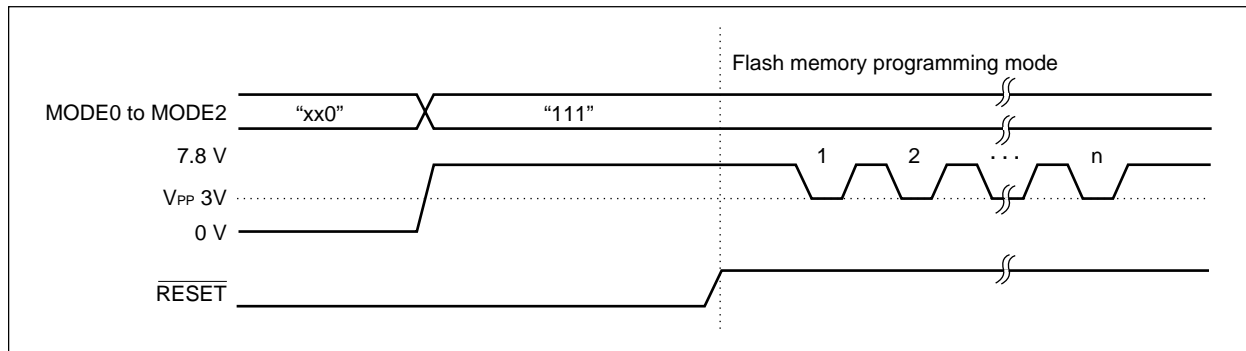
14.6.2 Flash memory programming mode

When rewriting the contents of a flash memory using the dedicated flash writer, set the V854 in the flash memory programming mode. When switching to modes, set MODE0 through MODE2 and V_{PP} pin before releasing reset.

When performing on-board writing, change modes using a jumper, etc.

V _{PP}	MODE2	MODE1	MODE0	Operation Mode	
0 V	0	0	0	Normal operation mode	ROM-less mode 1
0 V	0	0	1		ROM-less mode 2
0 V	0	1	0		Single-chip mode 1
0 V	0	1	1		Single-chip mode 2
7.8 V	1	1	1	Flash memory programming mode	
Other than the above				Setting prohibited	

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14.6.3 Selection of communication mode

In the V854, a communication system is selected by inputting pulse (16 pulses max.) to V_{PP} pin after switching to the flash memory programming mode. The V_{PP} pulse is generated by the dedicated flash writer.

The following shows the relation between the number of pulses and the communication systems.

Table 14-1. List of Communication Systems

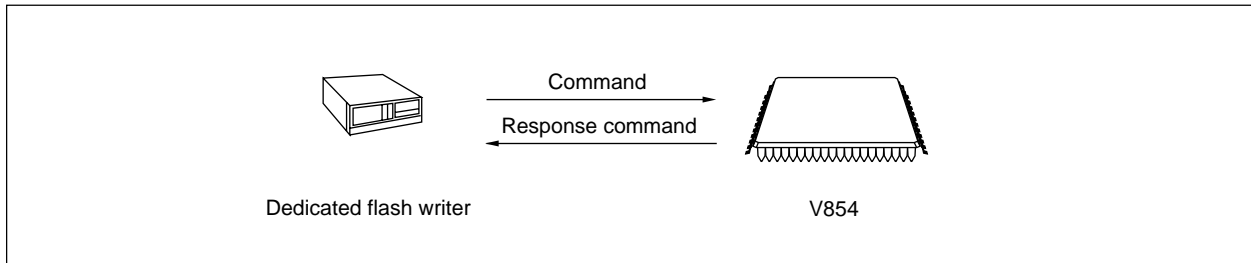
V _{PP} pulse	Communication System	Remarks
0	CSI0	V854 performs slave operation, MSB first
8	UART	Communication rate: 9600 bps (at reset), LSB first
Others	RFU	Setting prohibited

Caution When UART is selected, the receive clock is calculated based on the reset command sent from the dedicated flash writer after receiving V_{PP} pulse.

★

14.6.4 Communication command

The V854 communicates with the dedicated flash writer by means of commands. The command sent from the dedicated flash writer to the V854 is called a “command”. The response signal sent from the V854 to the dedicated flash writer is called a “response command”.



The following shows the command for flash memory control of the V854. All of these commands are issued from the dedicated flash writer, and the V854 performs the various processings corresponding to the commands.

Category	Command Name	Function
★ Verify	One-shot verify command	Compares the contents of the entire memory and the input data.
★ Erase	One-shot erase command	Erases the contents of the entire memory.
★ Blank check	One-shot blank check command	Checks the erase state of the entire memory.
Data write	High-speed write command	Writes data by the specification of the write address and the number of bytes to be written, and executes verify check.
	Continuous write command	Writes data from the address following the high-speed write command executed immediately before, and executes verify check.
★ System setting and control	Status read out command	Acquires the status of operations.
	Oscillating frequency setting command	Sets the oscillating frequency.
	Erasing time setting command	Sets the erasing time of one-shot erase.
	Writing time setting command	Sets the writing time of data write.
	Baud rate setting command	Sets the baud rate when using UART.
	Silicon signature command	Reads out the silicon signature information.
	Reset command	Escapes from each state.

The V854 sends back response commands to the commands issued from the dedicated flash writer. The following shows the response commands the V854 sends out.

Response Command Name	Function
ACK (acknowledge)	Acknowledges command/data, etc.
NAK (not acknowledge)	Acknowledges illegal command/data, etc.

14.6.5 Resources used

According to the flash memory programming mode setting, the resources used consist of the area from FFE000H to FFE7FFH of the internal RAM and all the registers. Area FFE800H to FFEFFFH of the internal RAM retains data as long as the power is on. The contents of the registers that are initialized by reset change to the default value.

[MEMO]

CHAPTER 15 DIFFERENCES BETWEEN VERSIONS

15.1 Differences between Versions with I²C Function and Versions without I²C Function

The product names of the versions with the I²C function are μ PD703008Y and 70F3008Y. They are identified by the letter “Y” in the product names.

Product Name		μ PD703008Y, 70F3008Y	μ PD703006, 703008, 70F3008
I ² C function	Function		
	I ² C function		Available
	Pin		Not available
	Interrupt		P33/SO1/SDA P35/SCK1/SCL
I ² C function	Register		INTIIC
	IIC0		Not available
	IICC		Not available
	IICS		Not available
I ² C function	IICCL		Not available (undefined)
	IIC		Not available (undefined)
	SAV		Not available (undefined)
			Not available (undefined)

15.2 Differences between On-chip Flash Memory Versions, On-chip Mask ROM Versions, and ROM-less Versions

The product names of the versions with the on-chip flash memory are μ PD70F3008 and 70F3008Y. They are identified by the letter “F” in the product names.

Part Number		μ PD703006	μ PD703008, 703008Y	μ PD70F3008, 70F3008Y
Parameter	On-chip ROM		None	Mask ROM
	Flash memory programming pin		None	Flash memory
Flash memory programming mode		None		Provided (V _{PP})
Flash memory programming mode		None		Provided (V _{PP} = 7.8 V, MODE0 to MODE2 = High-level)
Electrical specifications		Current consumption, etc. differ. (Refer to each product data sheet.)		
Others		Noise immunity and noise radiation differ for each product depending on the circuit size and mask layout.		

- ★
- Cautions**
1. There are differences in noise immunity and noise radiation between the flash memory version, mask ROM version, and ROM-less version. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the set using consumer samples (not engineering samples) of the mask ROM version.
 2. When replacing the flash memory version with the mask ROM version, be sure to write the same code into the internal ROM's reserved area.

[MEMO]

APPENDIX A REGISTER INDEX

(1/6)

Symbol	Name	Unit	Page
ADCR0	A/D conversion result register 0	ADC	299
ADCR1	A/D conversion result register 1	ADC	299
ADCR2	A/D conversion result register 2	ADC	299
ADCR3	A/D conversion result register 3	ADC	299
ADCR4	A/D conversion result register 4	ADC	299
ADCR5	A/D conversion result register 5	ADC	299
ADCR6	A/D conversion result register 6	ADC	299
ADCR7	A/D conversion result register 7	ADC	299
ADIC0	Interrupt control register	INTC	116
ADM0	A/D converter mode register 0	ADC	297
ADM1	A/D converter mode register 1	ADC	299
ASIM0	Asynchronous serial interface mode register 0	UART	209
ASIM1	Asynchronous serial interface mode register 1	UART	211
ASIS	Asynchronous serial interface status register 1	UART	212
BCC	Bus cycle control register	BCU	88
BPRM0	Baud rate generator prescaler mode register 0	BRG	292
BPRM1	Baud rate generator prescaler mode register 1	BRG	292
BPRM2	Baud rate generator prescaler mode register 2	BRG	292
BPRM3	Baud rate generator prescaler mode register 3	BRG	292
BRGC0	Baud rate generator compare register 0	BRG	291
BRGC1	Baud rate generator compare register 1	BRG	291
BRGC2	Baud rate generator compare register 2	BRG	291
BRGC3	Baud rate generator compare register 3	BRG	291
CC00	Capture/compare register 00	RPU	161
CC00L	Capture/compare register 00L	RPU	161
CC01	Capture/compare register 01	RPU	161
CC01L	Capture/compare register 01L	RPU	161
CC02	Capture/compare register 02	RPU	161
CC02L	Capture/compare register 02L	RPU	161
CC03	Capture/compare register 03	RPU	161
CC03L	Capture/compare register 03L	RPU	161
CC0IC0	Interrupt control register	INTC	116
CC0IC1	Interrupt control register	INTC	116
CC0IC2	Interrupt control register	INTC	116
CC0IC3	Interrupt control register	INTC	116
CC3	Capture/compare register 3	RPU	165
CKC	Clock control register	CG	137
CLOM	Clock output mode register	CG	154

Symbol	Name	Unit	Page
CM10	Compare register 10	RPU	163
CM10L	Compare register 10L	RPU	163
CM11	Compare register 11	RPU	163
CM11L	Compare register 11L	RPU	163
CM20	Compare register 20	RPU	164
CM21	Compare register 21	RPU	164
CM22	Compare register 22	RPU	164
CM23	Compare register 23	RPU	164
CM24	Compare register 24	RPU	164
CM1IC0	Interrupt control register	INTC	116
CM1IC1	Interrupt control register	INTC	116
CM2IC0	Interrupt control register	INTC	116
CM2IC1	Interrupt control register	INTC	116
CM2IC2	Interrupt control register	INTC	116
CM2IC3	Interrupt control register	INTC	116
CM2IC4	Interrupt control register	INTC	116
CC3IC0	Interrupt control register	INTC	116
CP10	Capture register 10	RPU	162
CP10L	Capture register 10L	RPU	162
CP11	Capture register 11	RPU	162
CP11L	Capture register 11L	RPU	162
CP12	Capture register 12	RPU	162
CP12L	Capture register 12L	RPU	162
CP13	Capture register 13	RPU	162
CP13L	Capture register 13L	RPU	162
CP3	Capture register 3	RPU	165
CSIC0	Interrupt control register	INTC	116
CSIC1	Interrupt control register	INTC	116
CSIC2	Interrupt control register	INTC	116
CSIC3	Interrupt control register	INTC	116
CSIM0	Clocked serial interface mode register 0	CSI	222
CSIM1	Clocked serial interface mode register 1	CSI	222
CSIM2	Clocked serial interface mode register 2	CSI	222
CSIM3	Clocked serial interface mode register 3	CSI	222
DWC	Data wait control register	BCU	86
ECR	Interrupt source register	CPU	52
EDVC0	Event divide control register 0	INTC	125
EDVC1	Event divide control register 1	INTC	125
EDVC2	Event divide control register 2	INTC	125
EDV0	Event divide counter 0	INTC	125

Symbol	Name	Unit	Page
EDV1	Event divide counter 1	INTC	125
EDV2	Event divide counter 2	INTC	125
EIPC	Interrupt status save register	CPU	52
EIPSW	Interrupt status save register	CPU	52
EVS	Event selection register	INTC	125
FEPC	NMI status save register	CPU	52
FEPSW	NMI status save register	CPU	52
IICC	IIC control register	I ² C	237
IICCL	IIC clock selection register	I ² C	241
IICS	IIC status register	I ² C	239
IIC	IIC shift register	I ² C	241
SVA	Slave address register	I ² C	242
IIIC0	Interrupt control register	INTC	116
INTM0	External interrupt mode register 0	INTC	106
INTM1	External interrupt mode register 1	INTC	121
INTM2	External interrupt mode register 2	INTC	121
INTM3	External interrupt mode register 3	INTC	121
INTM4	External interrupt mode register 4	INTC	121
INTM5	External interrupt mode register 5	INTC	121
INTM6	External interrupt mode register 6	INTC	121
INTM7	External interrupt mode register 7	INTC	123
ISPR	In-service priority register	INTC	118
MM	Memory expansion mode register	Port	68
OVIC0	Interrupt control register	INTC	116
OVIC1	Interrupt control register	INTC	116
P0	Port 0	Port	348
P1	Port 1	Port	350
P2	Port 2	Port	352
P3	Port 3	Port	354
P4	Port 4	Port	357
P5	Port 5	Port	359
P6	Port 6	Port	361
P7	Port 7	Port	363
P8	Port 8	Port	363
P9	Port 9	Port	364
P10	Port 10	Port	366
P11	Port 11	Port	368
P12	Port 12	Port	371
P13	Port 13	Port	373
P14	Port 14	Port	375

Symbol	Name	Unit	Page
P1IC0	Interrupt control register	INTC	116
P1IC1	Interrupt control register	INTC	116
P1IC2	Interrupt control register	INTC	116
P1IC3	Interrupt control register	INTC	116
P5IC0	Interrupt control register	INTC	116
P5IC1	Interrupt control register	INTC	116
P5IC2	Interrupt control register	INTC	116
P5IC3	Interrupt control register	INTC	116
PB	Port 13 buffer register	Port	322
PM0	Port 0 mode register	Port	349
PM1	Port 1 mode register	Port	351
PM2	Port 2 mode register	Port	353
PM3	Port 3 mode register	Port	355
PM4	Port 4 mode register	Port	358
PM5	Port 5 mode register	Port	360
PM6	Port 6 mode register	Port	362
PM9	Port 9 mode register	Port	365
PM10	Port 10 mode register	Port	367
PM11	Port 11 mode register	Port	369
PM12	Port 12 mode register	Port	371
PM13	Port 13 mode register	Port	374
PM14	Port 14 mode register	Port	375
PMC0	Port 0 mode control register	Port	349
PMC1	Port 1 mode control register	Port	351
PMC2	Port 2 mode control register	Port	353
PMC3	Port 3 mode control register	Port	356
PMC10	Port 10 mode control register	Port	367
PMC11	Port 11 mode control register	Port	370
PMC12	Port 12 mode control register	Port	372
PMC13	Port 13 mode control register	Port	374
PRCMD	Command register	CG	78
PSC	Power save control register	CG	142
PSW	Program status word	CPU	52, 106, 118, 128
PWM0	PWM modulo register 0 (12 bits)	PWM	329
PWM1	PWM modulo register 1 (12 bits)	PWM	329
PWM2	PWM modulo register 2	PWM	329
PWM3	PWM modulo register 3	PWM	329
PWMC0	PWM control register 0	PWM	327
PWMC1	PWM control register 1	PWM	327
PWMC2	PWM control register 2	PWM	327

Symbol	Name	Unit	Page
PWMC3	PWM control register 3	PWM	327
PWPR0	PWM prescaler register 0	PWM	328
PWPR1	PWM prescaler register 1	PWM	328
PWPR2	PWM prescaler register 2	PWM	328
PWPR3	PWM prescaler register 3	PWM	328
RTP	Output latch register	RPU	322
RXB	Receive buffer (9 bits)	UART	213
RXBL	Receive buffer L (lower 8 bits)	UART	213
SEIC0	Interrupt control register	INTC	116
SIO0	Serial I/O shift register 0	CSI	223
SIO1	Serial I/O shift register 1	CSI	223
SIO2	Serial I/O shift register 2	CSI	223
SIO3	Serial I/O shift register 3	CSI	223
SRIC0	Interrupt control register	INTC	116
STIC0	Interrupt control register	INTC	116
SVA	I ² C slave address register	I ² C	242
SYC	System control register	BCU	82
SYS	System status register	CG	79, 139
TM0	Timer 0	RPU	161
TM0L	Timer 0L	RPU	161
TM1	Timer 1	RPU	162
TM1L	Timer 1L	RPU	162
TM20	Timer 20	RPU	164
TM21	Timer 21	RPU	164
TM22	Timer 22	RPU	164
TM23	Timer 23	RPU	164
TM24	Timer 24	RPU	164
TM3	Timer 3	RPU	165
TMC00	Timer control register 00	RPU	166
TMC01	Timer control register 01	RPU	167
TMC02	Timer control register 02	RPU	168
TMC1	Timer control register 1	RPU	169
TMC20	Timer control register 20	RPU	170
TMC21	Timer control register 21	RPU	170
TMC22	Timer control register 22	RPU	170
TMC23	Timer control register 23	RPU	170
TMC24	Timer control register 24	RPU	170
TMC3	Timer control register 3	RPU	171
TOC0	Timer output control register 0	RPU	172
TOC1	Timer output control register 1	RPU	172

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Symbol	Name	Unit	Page
TOVS	Timer overflow status register	RPU	173
TXS	Transmit shift register (9 bits)	UART	214
TXSL	Transmit shift register L (lower 8 bits)	UART	214

APPENDIX B INSTRUCTION SET LIST

Legend

(1) Symbols used for operand description

Symbol	Description
reg1	General register (r0 to r31): Used as source register
reg2	General register (r0 to r31): Mainly used as destination register
immx	x-bit immediate
dispx	x-bit displacement
regID	System register number
bit#3	3-bit data for bit number specification
ep	Element pointer (r30)
cccc	4-bit data for condition code
vector	5-bit data for trap vector number (00H to 1FH)

(2) Symbols used for operation description

Symbol	Description
←	Assignment
GR[]	General register
SR[]	System register
zero-extend(n)	Zero-extends n to word length
sign-extend(n)	Sign-extends n to word length
load-memory(a,b)	Reads data of size b from address a
store-memory(a,b,c)	Writes data b of size c to address a
load-memory-bit(a,b)	Reads bit b of address a
store-memory-bit(a,b,c)	Writes c to bit b of address a
saturated(n)	Performs saturated processing of n (n is 2's complement). If n is $n \geq 7FFFFFFH$ as result of calculation, 7FFFFFFH. If n is $n \leq 80000000H$ as result of calculation, 80000000H.
result	Reflects result on flag
Byte	Byte (8 bits)
Halfword	Half-word (16 bits)
Word	Word (32 bits)
+	Add
−	Subtract
	Bit concatenation
x	Multiply
÷	Divide
AND	Logical product
OR	Logical sum

Symbol	Description
XOR	Exclusive logical sum
NOT	Logical negate
logically shift left by	Logical left shift
logically shift right by	Logical right shift
arithmetically shift right by	Arithmetic right shift

(3) Symbols used for execution clock description

Symbol	Description
i: issue	To execute another instruction immediately after instruction execution
r: repeat	To execute same instruction immediately after instruction execution
l: latency	To reference result of instruction execution by the next instruction

(4) Flag operation

Identifier	Description
(Blank)	Not affected
0	Cleared to 0
1	Set to 1
x	Set or cleared according to result
R	Previously saved value is restored

Condition code

Condition Name (cond)	Condition Code (cccc)	Conditional Expression	Description
V	0 0 0 0	OV = 1	Overflow
NV	1 0 0 0	OV = 0	No overflow
C/L	0 0 0 1	CY = 1	Carry Lower (Less than)
NC/NL	1 0 0 1	CY = 0	No carry No lower (Greater than or equal)
Z/E	0 0 1 0	Z = 1	Zero Equal
NZ/NE	1 0 1 0	Z = 0	Not zero Not equal
NH	0 0 1 1	(CY or Z) = 1	Not higher (Less than or equal)
H	1 0 1 1	(CY or Z) = 0	Higher (Greater than)
N	0 1 0 0	S = 1	Negative
P	1 1 0 0	S = 0	Positive
T	0 1 0 1	—	Always (unconditional)
SA	1 1 0 1	SAT = 1	Saturated
LT	0 1 1 0	(S xor OV) = 1	Less than signed
GE	1 1 1 0	(S xor OV) = 0	Greater than or equal signed
LE	0 1 1 1	((S xor OV) or Z) = 1	Less than or equal signed
GT	1 1 1 1	((S xor OV) or Z) = 0	Greater than signed

Instruction Set (alphabetical order) (1/4)

Mnemonic	Operand	Code	Operation	Execution Clock			Flag				
				i	r	l	CY	OV	S	Z	SAT
ADD	reg1, reg2	r r r r r 0 0 1 1 1 0 R R R R R	GR[reg2]←GR[reg2]+GR[reg1]	1	1	1	x	x	x	x	
	imm5, reg2	r r r r r 0 1 0 0 1 0 i i i i i	GR[reg2]←GR[reg2]+sign-extend(imm5)	1	1	1	x	x	x	x	
ADDI	imm16, reg1, reg2	r r r r r 1 1 0 0 0 0 R R R R R i i i i i i i i i i i i i i i i	GR[reg2]←GR[reg1]+sign-extend(imm16)	1	1	1	x	x	x	x	
AND	reg1, reg2	r r r r r 0 0 1 0 1 0 R R R R R	GR[reg2]←GR[reg2]AND GR[reg1]	1	1	1		0	x	x	
ANDI	imm16, reg1, reg2	r r r r r 1 1 0 1 1 0 R R R R R i i i i i i i i i i i i i i i i	GR[reg2]←GR[reg1]AND zero-extend(imm16)	1	1	1		0	0	x	
Bcond	disp9	d d d d d 1 0 1 1 d d d c c c c Note 1	if conditions are satisfied	3	3	3					
			When condition satisfied then PC←PC+sign-extned(disp9) When condition not satisfied	1	1	1					
CLR1	bit#3, disp16[reg1]	1 0 b b b 1 1 1 1 1 0 R R R R R d d d d d d d d d d d d d d d	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr, bit#3)) Store-memory-bit(adr, bit#3.0)	4	4	4				x	
CMP	reg1, reg2	r r r r r 0 0 1 1 1 1 R R R R R	result←GR[reg2]−GR[reg1]	1	1	1	x	x	x	x	
	imm5, reg2	r r r r r 0 1 0 0 1 1 i i i i i	result←GR[reg2]−sign-extend(imm5)	1	1	1	x	x	x	x	
DI		0 0 0 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 0 0 0 0 0	PSW.ID←1 (Maskable interrupt disabled)	1	1	1					
DIVH	reg1, reg2	r r r r r 0 0 0 0 1 0 R R R R R	GR [reg2]←GR [reg2]+GR [reg1] ^{Note 2} (signed division)	36	36	36		x	x	x	
EI		1 0 0 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 0 0 0 0 0	PSW.ID←0 (Maskable interrupt enabled)	1	1	1					
HALT		0 0 0 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0	Stops	1	1	1					
JARL	disp22, reg2	r r r r r 1 1 1 1 0 d 0 Note 3	GR[reg2]←PC+4 PC←PC+sign-extend(disp22)	3	3	3					
JMP	[reg1]	0 0 0 0 0 0 0 0 1 1 R R R R R	PC←GR[reg1]	3	3	3					
JR	disp22	0 0 0 0 0 1 1 1 1 0 d 0 Note 3	PC←PC+sign-extend(disp22)	3	3	3					
LD.B	disp16[reg1], reg2	r r r r r 1 1 1 0 0 0 R R R R R d d d d d d d d d d d d d d d	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←sign-extend(Load-memory(adr, Byte))	1	1	2					
LD.H	disp16[reg1], reg2	r r r r r 1 1 1 0 0 1 R R R R R d d d d d d d d d d d d d d 0 Note 4	adr←GR[reg1]+sign-extend(disp16) GR[reg2]sign-extend(Load-memory(adr, Halfword))	1	1	2					
LD.W	disp16[reg1], reg2	r r r r r 1 1 1 0 0 1 R R R R R d d d d d d d d d d d d d d 1 Note 4	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←Load-memory(adr, Word)	1	1	2					

- Notes**
1. d d d d d d d d is the higher 8 bits of disp9.
 2. Only the lower half-word is valid.
 3. d is the higher 21 bits of disp22.
 4. d d d d d d d d d d d d d d d d is the higher 15 bits of disp16.

Instruction Set (alphabetical order) (2/4)

Mnemonic	Operand	Code	Operation	Execution Clock			Flag				
				i	r	l	CY	OV	S	Z	SAT
LDSR	reg2, regID	r r r r r 1 1 1 1 1 1 R R R R R 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 Note 1	SR[regID]←GR[reg2]	1	1	3					
			regID = EIPC, FEPC								
			regID = EIPSW, FEPSW			1	x	x	x	x	x
MOV	reg1, reg2	r r r r r 0 0 0 0 0 0 R R R R R	GR[reg2]←GR[reg1]	1	1	1					
	imm5, reg2	r r r r r 0 1 0 0 0 0 i i i i i	GR[reg2]←sign-extend(imm5)	1	1	1					
MOVEA	imm16, reg1, reg2	r r r r r 1 1 0 0 0 1 R R R R R i i i i i i i i i i i i i i i i	GR[reg2]←GR[reg1]+sign-extend(imm16)	1	1	1					
MOVHI	imm16, reg1, reg2	r r r r r 1 1 0 0 1 0 R R R R R i i i i i i i i i i i i i i i i	GR[reg2]←GR[reg1]+(imm16 0 ¹⁶)	1	1	1					
MULH	reg1, reg2	r r r r r 0 0 0 1 1 1 R R R R R	GR[reg2]←GR[reg2] ^{Note 2} x GR[reg1] ^{Note 2} (Signed multiplication)	1	1	2					
	imm5, reg2	r r r r r 0 1 0 1 1 1 i i i i i	GR[reg2]←GR[reg2] ^{Note 2} x sign-extend(imm5) (Signed multiplication)	1	1	2					
MULHI	imm16, reg1, reg2	r r r r r 1 1 0 1 1 1 R R R R R i i i i i i i i i i i i i i i i	GR[reg2]←GR[reg1] ^{Note 2} x imm16 (Signed multiplication)	1	1	2					
NOP		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Uses 1 clock cycle without doing anything	1	1	1					
NOT	reg1, reg2	r r r r r 0 0 0 0 0 1 R R R R R	GR[reg2]←NOT(GR[reg1])	1	1	1	0	x	x		
NOT1	bit#3, disp16[reg1]	0 1 b b b 1 1 1 1 1 0 R R R R R d d d d d d d d d d d d d d d d	adr←GR[reg1]+sign-extend(disp16)	4	4	4				x	
			Z flag←Not(Load-memory-bit(ad, bit#3)) Store-memory-bit(ad, bit#3, Z flag)								
OR	reg1, reg2	r r r r r 0 0 1 0 0 0 R R R R R	GR[reg2]←GR[reg2]OR GR[reg1]	1	1	1	0	x	x		
ORI	imm16, reg1, reg2	r r r r r 1 1 0 1 0 0 R R R R R i i i i i i i i i i i i i i i i	GR[reg2]←GR[reg1]OR zero-extend(imm16)	1	1	1	0	x	x		
RETI		0 0 0 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 0 0	if PSW.EP=1 then PC ←EIPC PSW ←EIPSW else if PSW.NP=1 then PC ←FEPC PSW ←FEPSW else PC ←EIPC PSW ←EIPSW	4	4	4	R	R	R	R	R
SAR	reg1, reg2	r r r r r 1 1 1 1 1 1 R R R R R 0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 0	GR[reg2]←GR[reg2]arithmetically shift right by GR[reg1]	1	1	1	x	0	x	x	
	imm5, reg2	r r r r r 0 1 0 1 0 1 i i i i i	GR[reg2]←GR[reg2]arithmetically shift right by zero-extend(imm5)	1	1	1	x	0	x	x	

Notes 1. The op code of this instruction uses the field of reg1 though the source register is shown as reg2 in the above table. Therefore, the meaning of register specification for mnemonic description and op code is different from that of the other instructions.

rrrrr = regID specification

RRRRR = reg2 specification

2. Only the lower half-word data is valid.

Instruction Set (alphabetical order) (3/4)

Mnemonic	Operand	Code	Operation	Execution Clock			Flag				
				i	r	l	CY	OV	S	Z	SAT
SATADD	reg1, reg2	r r r r r 0 0 0 1 1 0 R R R R R	GR[reg2]←saturated(GR[reg2]+GR[reg1])	1	1	1	x	x	x	x	x
	imm5, reg2	r r r r r 0 1 0 0 0 1 i i i i i	GR[reg2]←saturated(GR[reg2]+sign-extend(imm5))	1	1	1	x	x	x	x	x
SATSUB	reg1, reg2	r r r r r 0 0 0 1 0 1 R R R R R	GR[reg2]←saturated(GR[reg2]−GR[reg1])	1	1	1	x	x	x	x	x
SATSUBI	imm16, reg1, reg2	r r r r r 1 1 0 0 1 1 R R R R R i i i i i i i i i i i i i i i i	GR[reg2]←saturated(GR[reg1]−sign-extend(imm16))	1	1	1	x	x	x	x	x
SATSUBR	reg1, reg2	r r r r r 0 0 0 1 0 0 R R R R R	GR[reg2]←saturated(GR[reg1]−GR[reg2])	1	1	1	x	x	x	x	x
SETF	cccc, reg2	r r r r r 1 1 1 1 1 1 0 c c c c 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	if conditions are satisfied then GR[reg2]←00000001H else GR[reg2]←00000000H	1	1	1					
SET1	bit#3, disp16[reg1]	0 0 b b b 1 1 1 1 1 0 R R R R R d d d d d d d d d d d d d d d d	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr, bit#3)) Store-memory-bit(adr, bit#3, 1)	4	4	4				x	
SHL	reg1, reg2	r r r r r 1 1 1 1 1 1 R R R R R 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0	GR[reg2]←GR[reg2] logically shift left by GR[reg1]	1	1	1	x	0	x	x	
	imm5, reg2	r r r r r 0 1 0 1 1 0 i i i i i	GR[reg2]←GR[reg1] logically shift left by zero-extend(imm5)	1	1	1	x	0	x	x	
SHR	reg1, reg2	r r r r r 1 1 1 1 1 1 R R R R R 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0	GR[reg2]←GR[reg2] logically shift right by GR[reg1]	1	1	1	x	0	x	x	
	imm5, reg2	r r r r r 0 1 0 1 0 0 i i i i i	GR[reg2]←GR[reg2] logically shift right by zero-extend(imm5)	1	1	1	x	0	x	x	
SLD.B	disp7[ep], reg2	r r r r r 0 1 1 0 d d d d d d d	adr←ep+zero-extend(disp7) GR[reg2]←sign-extend(Load-memory(adr, Byte))	1	1	2					
SLD.H	disp8[ep], reg2	r r r r r 1 0 0 0 d d d d d d d Note 1	adr←ep+zero-extend(disp8) GR[reg2]←sign-extend(Load-memory(adr, Halfword))	1	1	2					
SLD.W	disp8[ep], reg2	r r r r r 1 0 1 0 d d d d d d 0 Note 2	adr←ep+zero-extend(disp8) GR[reg2]←Load-memory(adr, Word)	1	1	2					
SST.B	reg2, disp7[ep]	r r r r r 0 1 1 1 d d d d d d d	adr←ep+zero-extend(disp7) Store-memory(adr, GR[reg2], Byte)	1	1	1					
SST.H	reg2, disp8[ep]	r r r r r 1 0 0 1 d d d d d d d Note 1	adr←ep+zero-extend(disp8) Store-memory(adr, GR[reg2], Halfword)	1	1	1					
SST.W	reg2, disp8[ep]	r r r r r 1 0 1 0 d d d d d d 1 Note 2	adr←ep+zero-extend(disp8) Store-memory(adr, GR[reg2], Word)	1	1	1					
ST.B	reg2, disp16[reg1]	r r r r r 1 1 1 0 1 0 R R R R R d d d d d d d d d d d d d d d d	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr, GR[reg2], Byte)	1	1	1					

- Notes**
1. dddddd is the higher 7 bits of disp8.
 2. dddddd is the higher 6 bits of disp8.

Instruction Set (alphabetical order) (4/4)

Mnemonic	Operand	Code	Operation	Execution Clock			Flag				
				i	r	l	CY	OV	S	Z	SAT
ST.H	reg2, disp16[reg1]	r r r r r 1 1 1 0 1 1 R R R R R d d d d d d d d d d d d d d 0 Note	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr, GR[reg2], Halfword)	1	1	1					
ST.W	reg2, disp16[reg1]	r r r r r 1 1 1 0 1 1 R R R R R d d d d d d d d d d d d d d 1 Note	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr, GR[reg2], Word)	1	1	1					
STSR	regID, reg2	r r r r r 1 1 1 1 1 1 R R R R R 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0	GR[reg2]←SR[regID]	1	1	1					
SUB	reg1, reg2	r r r r r 0 0 1 1 0 1 1 R R R R R	GR[reg2]←GR[reg2]−GR[reg1]	1	1	1	x	x	x	x	
SUBR	reg1, reg2	r r r r r 0 0 1 1 0 0 R R R R R	GR[reg2]←GR[reg1]−GR[reg2]	1	1	1	x	x	x	x	
TRAP	vector	0 0 0 0 0 1 1 1 1 1 1 i i i i i 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0	EIPC ←PC+4(Restored PC) EIPSW ←PSW ECR.EICC ←Interrupt code PSW.EP ←1 PSW.ID ←1 PC ←00000040H(vector = 00H to 0FH) 00000050H(vector = 10H to 1FH)	4	4	4					
TST	reg1, reg2	r r r r r 0 0 1 0 1 1 R R R R R	result←GR[reg2] AND GR[reg1]	1	1	1	0	x	x	x	
TST1	bit#3, disp16[reg1]	1 1 b b b 1 1 1 1 1 0 R R R R R d d d d d d d d d d d d d d d	adr←GR[reg1]+sign-extend(disp16) Z flag←Not(Load-memory-bit(adr, bit#3))	3	3	3				x	
XOR	reg1, reg2	r r r r r 0 0 1 0 0 1 R R R R R	GR[reg2]←GR[reg2] XOR GR[reg1]	1	1	1	0	x	x	x	
XORI	imm16, reg1, reg2	r r r r r 1 1 0 1 0 1 R R R R R i i i i i i i i i i i i i i i i	GR[reg2]←GR[reg1] XOR zero-extend(imm16)	1	1	1	0	x	x	x	

Note ddddddddddddddd is the higher 15 bits of disp16.

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