T-46-13-27

CATALYST SEMICONDUCTOR
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CAT28F010/28F010I

1 Megabit (128K x 8) CMOS FLASH MEMORY

Preliminary

DESCRIPTION

The CAT28F010/28F010I is a high speed 128K x 8-bit electrically erasable and reprogrammable Flash memory, ideally suited for applications requiring in-system or after-sale code updates. Electrical erasure of the full memory contents is achieved typically within 1 second.

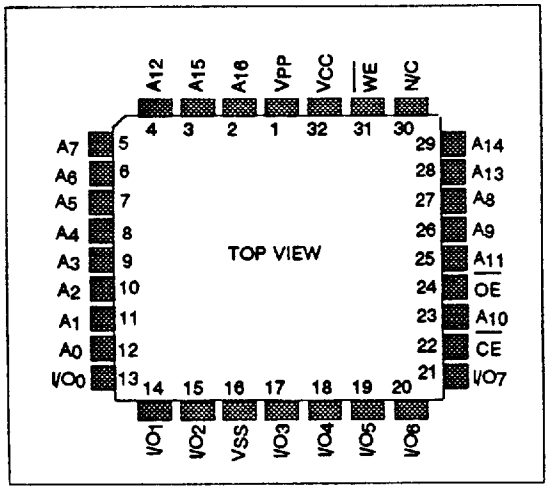
The CAT28F010/28F010I features *'Speed Programming'* capability, by which four bytes of the same data can be programmed simultaneously. This mode helps reduce the program (all bytes to 00H) time required prior to erasure.

It is pin and Read timing compatible with standard EPROM and EEPROM devices. Programming and Erase are performed through an operation and verify algorithm. The instructions are input via the I/O bus, using a two write cycle scheme. Address and Data are latched to free the I/O bus and address bus during the write operation. The CAT28F010/28F010I is packaged in a JEDEC-standard 32-pin plastic DIP and CERDIP or 32-pin PLCC package.

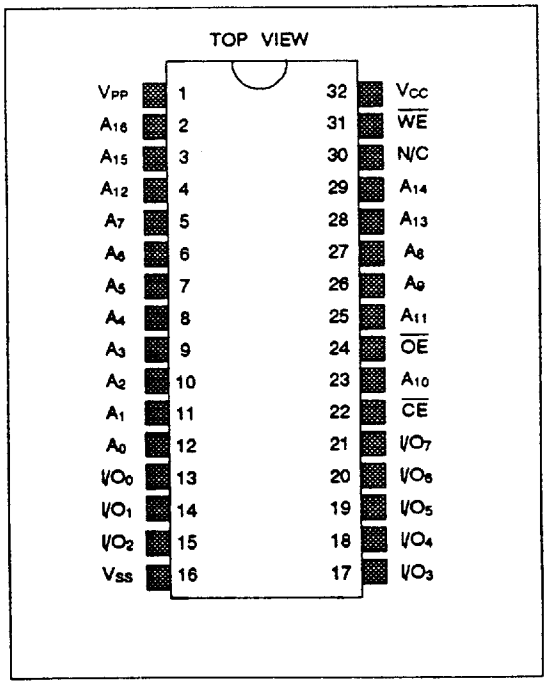
FEATURES

- Fast Access Time: 120/150/200 ns
- CMOS Low Power consumption:
  - Active: 30 mA max (CMOS/TTL levels)
  - Standby: 1 mA max (TTL levels)
  - Standby: 100 µA max (CMOS levels)
- High Speed Programming:
  - 10 µS per byte
  - 1 Sec Typ Chip Program
- 12.0V ± 5% Programming and Erase voltage
- Stop Timer for Program/Erase
- On-chip Address and Data Latches
- JEDEC Standard pinouts:
  - 32-pin DIP
  - 32-pin PLCC
- 10,000 Cycle Endurance
- 10 Year Data Retention
- Electronic Signature

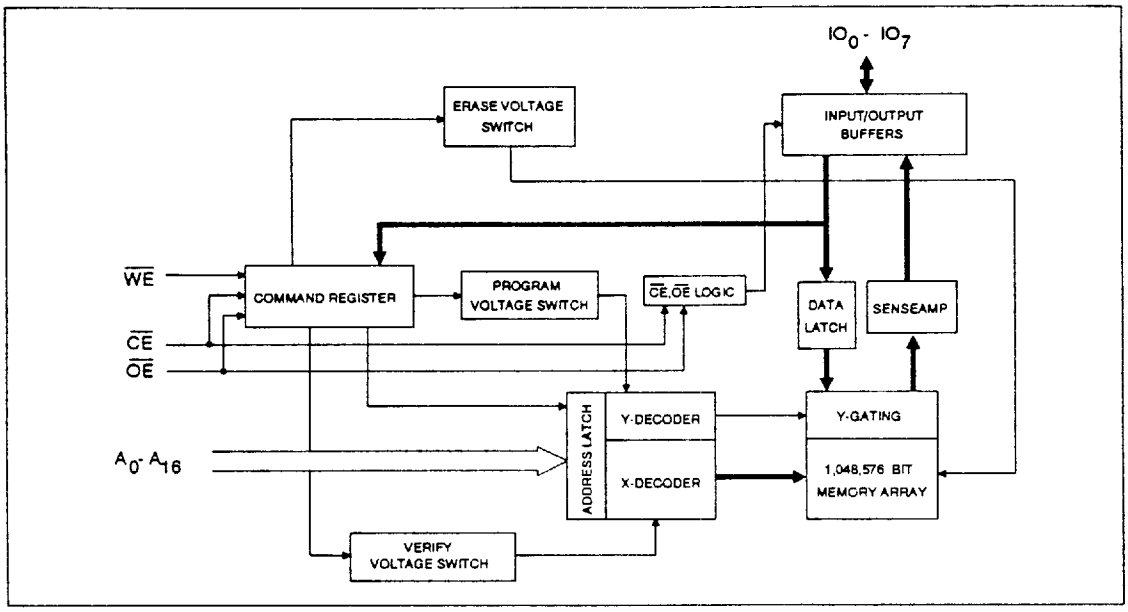
32 Pin PLCC



32 Pin DIP and CERDIP



BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Type	Name and Function
A_0 - A_{16}	Input	Address Inputs for memory addressing
I/O_0 - I/O_7	I/O	Data Input/Output
$\overline{CE}$	Input	Chip Enable
$\overline{OE}$	Input	Output Enable
$\overline{WE}$	Input	Write Enable
V_{CC}	-	Voltage Supply
V_{SS}	-	Ground
V_{PP}	-	Program/Erase Voltage Supply

CAPACITANCE: T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Conditions	Limits		Unit
			Min.	Max.	
C_{IN}[1]	Input Pin Capacitance	V_{IN} = 0.0 V	-	6.0	pF
C_{OUT}[1]	Output Pin Capacitance	V_{OUT} = 0.0 V	-	10.0	pF
C_{VPP}[1]	V_{PP} Supply Capacitance	V_{PP} = 0.0 V	-	25.0	pF

NOTE: (1) This parameter is tested initially and after a design or process change that affects the parameter.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-50°C to +95 °C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Pin A_9 with Respect to Ground	-2.0V to +13.5V(1)
V_{PP} with Respect to Ground during Erase/Program	-2.0V to +14.0V(1)
V_{CC} with Respect to Ground	-2.0V to +7.0V(1)
Package Power Dissipation Capability (T_A = 25°C)	1.0 W
Lead Soldering Temperature (10 secs)	300°C
Output Short Circuit Current	100 mA (2)

NOTES:
1. The minimum DC input voltage is -0.5V. During transitions inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20 ns.
2. Output shorted for no more than one second. No more than one output shorted at a time.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	I/O	NOTES
Read	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	D_{OUT}	
Output disable	V_{IL}	V_{IH}	V_{IH}	X	High-Z	
Standby	V_{IH}	X	X	V_{PPL}	High-Z	
Signature (MFG)	V_{IL}	V_{IL}	V_{IH}	X	31H	A_0 = V_{IL}, A_9 = 12V
Signature (Device)	V_{IL}	V_{IL}	V_{IH}	X	B4H	A_0 = V_{IH}, A_9 = 12V
Program/Erase	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	D_{IN}	See Command Table
Write Cycle	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	D_{IN}	During Write Cycle
Read Cycle	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	D_{OUT}	During Write Cycle

NOTE: Logic Levels: X = Logic 'Do not care' (V_{IH}, V_{IL}, V_{PPL}, V_{PPH})

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}(1)	Endurance	1K, 10K		Cycles/Byte	MIL-STD 883, Test Method 1033
T_{DR}(1)	Data Retention	10		years	MIL-STD 883, Test Method 1008
V_{ZAP}(1)	ESD Susceptability	2000		Volts	MIL-STD 883, Test Method 3015
I_{LTH}(1)(2)	Latch-Up	100		mA	JEDEC Standard 17

NOTES:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V_{CC}+1V.

WRITE COMMAND TABLE

Commands are written into the command register in one or two write cycles. The command register can be altered only when V_{PP} is high and the instruction byte is latched on the rising edge of WE. Write cycles also internally latch addresses and data required for programming and erase operations.

Mode \ Pins	First Bus Cycle			Second Bus Cycle			
	Operation	Address	D_{IN}	Operation	Address	D_{IN}	D_{OUT}
Set Read	Write	X	00H	Read	Any	-	D_{OUT}
Read Sig. (MFG)	Write	X	90H	Read	00	-	31H
Read Sig. (Device)	Write	X	90H	Read	01	-	B4H
Erase	Write	X	20H	Write	X	20H	-
Erase Verify	Write	X	A0H	Read	X	-	D_{OUT}
Program	Write	X	40H	Write	A_{IN}	D_{IN}	-
Program Verify	Write	X	C0H	Read	X	-	D_{OUT}
Speed Program	Write	X	E0H	Write	A_{IN}	D_{IN}	-
Speed Prog. Verify	Write	X	C0H	Read	X	-	D_{OUT}
				Read	Note 1	-	D_{OUT}
				Read	Note 1	-	D_{OUT}
				Read	Note 1	-	D_{OUT}
Reset	Write	X	FFH	Write	X	FFH	-

NOTE:

1. In Speed Program, the address latched is incremented to read all combinations of A_0 and A_1. For example, if the address latched is 13F4H, this location will be verified (Program Verify) when OE goes low. Then the address of the other three bytes (13F5H, 13F6H and 13F7H) must be specified to verify the data.

READ OPERATIONS

Read Mode

A Read operation is performed with both $\overline{CE}$ and $\overline{OE}$ low and with $\overline{WE}$ high. V_{PP} can be either high or low, however, if V_{PP} is high, the Set READ command has to be sent before reading data (see Write Operations). The data retrieved from the I/O pins reflects the contents of the memory location corresponding to the state of the 17 address pins. The respective timing waveforms for the read operation are shown in figure 1. Refer to the AC Read characteristics for specific timing parameters.

Signature Mode

The signature mode allows the user to identify the IC manufacturer and the type of device while the device resides in the target system. This mode can be activated in either of two ways; through the conventional method of applying a high voltage (12V) to address pin A_9 or by sending an instruction to the command register (see Write Operations).

The conventional mode is entered as a regular READ mode by driving the $\overline{CE}$ and $\overline{OE}$ pins low (with $\overline{WE}$ high), and applying the required high voltage on address pin A_9 while all other address lines are held at V_{IL}.

A Read cycle from address 0000H retrieves the binary code for the IC manufacturer on outputs I/O_0 to I/O_7:

CATALYST Code = 00110001 (31H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7.

28F010/28F010I Code = 1011 0100 (B4H)

Standby Mode

With $\overline{CE}$ at a logic-high level, the CAT28F010/28F010I is placed in a standby mode where most of the device circuitry is disabled, thereby substantially reducing power consumption. The outputs are placed in a high-impedance state.

WRITE OPERATIONS

The following operations are initiated by observing the sequence specified in the Write Command Table.

Read Mode

The device can be put into a standard READ mode by initiating a write cycle with 00H on the data bus. The subsequent read cycles will be performed similar to a standard EPROM or EEPROM Read.

Signature Mode

An alternative method for reading device signature (see Read Operations - Signature Mode), is initiated by writing the code 90H into the command register while keeping V_{PP} high. A read cycle from address 0000H with $\overline{CE}$ and $\overline{OE}$ low (and $\overline{WE}$ high) will output the device signature.

CATALYST Code = 00110001 (31H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_0 to I/O_7.

28F010/28F010I Code = 1011 0100 (B4H)

Erase Mode

During the first Write cycle, the command 20H is written into the command register. In order to commence the erase operation, the identical command of 20H has to be written again into the register. This two-step process ensures against accidental erasure of the memory contents. The final erase cycle will be stopped at the rising edge of $\overline{WE}$, at which time the Erase Verify command (A0H) is sent to the command register. During this cycle, the address to be verified is sent to the address bus and latched when $\overline{WE}$ goes high. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum erase timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Erase-Verify Mode

The Erase-verify operation is performed on every byte after each erase pulse to verify that the bits have been erased.

Programming Mode

The programming operation is initiated using the programming algorithm of figure 2. During the first write cycle, the command 40H is written into the command register. During the second write cycle, the address of the memory location to be programmed is latched on the falling edge of $\overline{WE}$, while the data is latched on the rising edge of WE. The program operation terminates with the next rising edge of $\overline{WE}$. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum program timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Program-Verify Mode

A Program-verify cycle is performed to ensure that all bits have been correctly programmed following each byte programming operation. The specific address is already latched from the write cycle just completed, and stays latched until the verify is completed. The Program-verify operation is initiated by writing C0H into the command register. An internal reference generates the necessary high voltages so that the user does not need to modify V_{CC}. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

Speed Programming

During the first write cycle, if the data E0H is sent instead of 40H, a 4 byte write operation will be performed. The next $\overline{WE}$ cycle programs the same data into four consecutive locations. The locations written to are specified by the latched address, and by all combinations of A_0 and A_1. The timings are similar to a standard programming operation.
This mode is particularly useful in reducing the erase algorithm time. When programming all bytes to 00H the speed programming mode reduces the time required by a factor of 4. Refer to figure 7 for the speed programming algorithm.

Speed Program Verify

To verify the four locations written, $\overline{OE}$ must be cycled 3 more times, while specifying the address as in a Read operation.

Abort/Reset

An Abort/Reset command is available to allow the user to safely abort an erase or program sequence. Two consecutive program cycles with FFH on the data bus will abort an erase or a program operation. The reset/abort operation can interrupt at any time in a program or erase operation and the device is reset to the Read Mode.

POWER UP/DOWN PROTECTION

The CAT28F010/28F010I offers protection against inadvertent programming during V_{PP} and V_{CC} power transitions. When powering up the device there is no power-on sequencing necessary. In other words, V_{PP} and V_{CC} may power up in any order. Additionally V_{PP} may be hardwired to V_{PPH} independent of the state of V_{CC} and any power up/down cycling. The internal command register of the CAT28F010 is reset to the Read Mode on power up.

POWER SUPPLY DECOUPLING

To reduce the effect of transient power supply voltage spikes, it is good practice to use a 0.1µF ceramic capacitor between V_{CC} and V_{SS} and V_{PP} and V_{SS}. These high-frequency capacitors should be placed as close as possible to the device for optimum decoupling.

DC CHARACTERISTICS

V_{CC} = 5V ± 10%, T_A = 0°C to +70°C (28F010), T_A = -40°C to +85°C (28F010I)

Symbol	Parameter	Limits Min	Limits Max	Unit	Conditions
I_{LI}	Input Leakage Current	-	± 1.0	µA	V_{IN} = V_{CC} or V_{SS}, V_{CC} = 5.5V, $\overline{OE}$ = V_{IH}
I_{LO}	Output Leakage Current	-	± 10	µA	V_{OUT} = V_{CC} or V_{SS}, V_{CC} = 5.5V, $\overline{OE}$ = V_{IH}
I_{SB1}	V_{CC} Standby Current CMOS	-	100	µA	$\overline{CE}$ = V_{CC} ± 0.5V, V_{CC} = 5.5V
I_{SB2}	V_{CC} Standby Current TTL	-	1.0	mA	$\overline{CE}$ = V_{IH}, V_{CC} = 5.5V
I_{CC1}	V_{CC} Active Read Current	-	30	mA	V_{CC} = 5.5V, $\overline{CE}$ = V_{IL}, I_{OUT} = 0mA, f = 6 MHz
I_{CC2}(1)	V_{CC} Programming Current	-	15	mA	V_{CC} = 5.5V, Programming in Progress
I_{CC3}(1)	V_{CC} Erase Current	-	15	mA	V_{CC} = 5.5V, Erasure in Progress
I_{CC4}(1)	V_{CC} Prog./Erase Verify Current	-	15	mA	V_{PP} =V_{PPH}, Program or Erase Verify in Progress
I_{PPS}	V_{PP} Standby Current	-	± 10	µA	V_{PP} = V_{PPL}
I_{PP1}	V_{PP} Read Current	-	200	µA	V_{PP} = V_{PPH}
I_{PP2}(1)	V_{PP} Programming Current	-	30	mA	V_{PP} = V_{PPH}, Programming in Progress
I_{PP3}(1)	V_{PP} Erase Current	-	30	mA	V_{CC} = 5.5V, Erasure in Progress
I_{PP4}(1)	V_{PP} Prog./Erase Verify Current	-	5.0	mA	V_{PP} = V_{PPH}, Program or Erase Verify in Progress
V_{IL}	Input Low Level TTL	-0.5	0.8	V	
V_{ILC}	Input Low Level CMOS	-0.5	0.8	V	
V_{OL}	Output Low Level	-	0.45	V	I_{OL} = 5.8mA, V_{CC} = 4.5V
V_{IH}	Input High Level TTL	2.0	V_{CC}+0.5	V	
V_{IHC}	Input High Level CMOS	0.7 V_{CC}	V_{CC}+0.5	V	
V_{OH}	Output High Level TTL	2.4	-	V	I_{OH} = -2.5mA,V_{CC} = 4.5V
V_{OH1}	Output High Level CMOS	0.85 V_{CC}	-	V	I_{OH} = -2.5mA,V_{CC} = 4.5V
V_{OH2}		V_{CC}-0.4			I_{OH} = -400µA,V_{CC} = 4.5V
V_{ID}	A_9 Signature Voltage	11.4	13.0	V	A_9 = V_{ID}
I_{ID}	A_9 Signature Current	-	200	µA	A_9 = V_{ID}
V_{LO}	V_{CC} Erase/Prog. Lockout Voltage	2.5	-	V	

NOTE:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

SUPPLY CHARACTERISTICS

Symbol	Parameter	Limits Min	Limits Max	Unit
V_{CC}	V_{CC} Supply Voltage	4.5	5.5	V
V_{PPL}	V_{PP} during Read Operations	0	6.5	V
V_{PPH}	V_{PP} during Read/Erase/Program	11.4	12.6	V

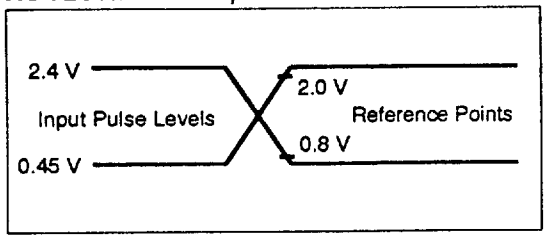
AC CHARACTERISTICS <READ Operation>

V_{CC} = 5V± 10%, T_A = 0°C to +70°C (28F010), T_A = -40°C to 85°C (28F010I)

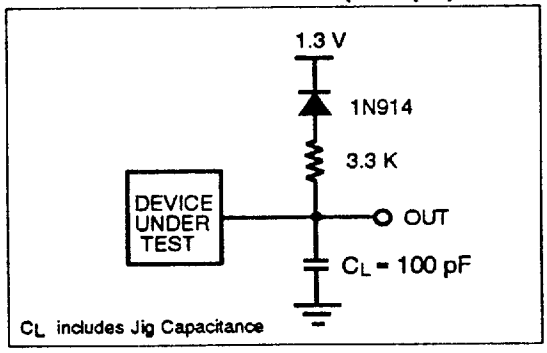
Symbol	Parameter	28F010/I-12 Min.	28F010/I-12 Max.	28F010/I-15 Min.	28F010/I-15 Max.	28F010/I-20 Min.	28F010/I-20 Max.	Unit
t_{RC}	Read Cycle Time	120	-	150	-	200	-	ns
t_{CE}	$\overline{CE}$ Access Time	-	120	-	150	-	200	ns
t_{ACC}	Address Access Time	-	120	-	150	-	200	ns
t_{OE}	$\overline{OE}$ Access Time	-	50	-	55	-	60	ns
t_{OH}	Output Hold from Addresss $\overline{OE}$/ $\overline{CE}$ change	0	-	0	-	0	-	ns
t_{OLZ}[5][6]	$\overline{OE}$ to Output in Low-Z	0	-	0	-	0	-	ns
t_{LZ}[5][6]	$\overline{CE}$ to Output in Low-Z	0	-	0	-	0	-	ns
t_{DF}[1][6]	$\overline{OE}$ High to Output High-Z	-	30	-	35	-	40	ns
t_{EHQZ}[1][6]	$\overline{CE}$ High to Output High-Z	-	55	-	55	-	55	ns
t_{WHGL}	Write Recovery Time before Read	6	-	6	-	6	-	µs

NOTES:
1. Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
2. Input Rise and Fall Times (10% to 90%) < 10 ns.
3. Input Pulse Levels = 0.45V and 2.4V.
4. Input and Output Timing Reference = 0.8V and 2.0V.
5. Low-Z is defined as the state where the external data may be driven by the output buffer but may not be valid.
6. This parameter is tested initially and after a design or process change that affects the parameter.

AC TESTING INPUT/OUTPUT WAVEFORM



AC TESTING LOAD CIRCUIT (example)



AC CHARACTERISTICS <PROGRAM/ERASE Operation>

V_{CC} = 5V± 10%, T_A = 0°C to +70°C (28F010), T_A = -40°C to +85°C (28F010I)

Symbol	Parameter	28F010/I-12		28F010/I-15		28F010/I-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	120	-	150	-	200	-	ns
t_{AS}	Address Setup Time	0	-	0	-	0	-	ns
t_{AH}	Address Hold Time	60	-	60	-	75	-	ns
t_{DS}	Data Setup Time	50	-	50	-	50	-	ns
t_{DH}	Data Hold Time	10	-	10	-	10	-	ns
t_{CS}	$\overline{CE}$ Setup Time	0	-	0	-	0	-	ns
t_{CH}	$\overline{CE}$ Hold Time	0	-	0	-	0	-	ns
t_{WP}	$\overline{WE}$ Pulse Width	60	-	60	-	60	-	ns
t_{WPH}	$\overline{WE}$ High Pulse Width	20	-	20	-	20	-	ns
t_{WHWH1}	Program Pulse Width	10	-	10	-	10	-	µs
t_{WHWH2}	Erase Pulse Width	9.5	-	9.5	-	9.5	-	ms
t_{WHGL}	Write Recovery Time Before Read	6	-	6	-	6	-	µs
t_{GHWL}	Read Recovery Time Before Write	0	-	0	-	0	-	µs
t_{VPEL}	V_{PP} Setup Time to $\overline{CE}$	100	-	100	-	100	-	ns

NOTES:
1. Input Rise and Fall Times (10% to 90%) < 10 ns.
2. Input Pulse Levels = 0.45V and 2.4V.
3. Input and Output Timing References = 0.8V and 2.0V.
4. Please refer to Supply characteristics for the value of V_{PPH} and V_{PPL}. The V_{PP} supply can be either hardwired or switched. If V_{PP} is switched, V_{PPL} can be ground, less than V_{CC} + 2.0V or a no connect with a resistor tied to ground.
5. Program and Erase operations are controled by internal stop timers.

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Notes	28F010/I-12			28F010/I-15			28F010/I-20			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Erase Time	1,2	-	1.0	10	-	1.0	10	-	1.0	30	sec
Chip Program Time	1,3	-	2	12.5	-	2	12.5	-	2	12.5	sec

Notes:
1. 'Typicals' are not guaranteed, but based on characterization data. Data taken at 25°C, 12.0V V_{PP}.
2. Minimum byte programming time (excluding system overhead) is 16 µs (10 µs program + 6 µs write recovery), while maximum is 400 µs/byte (16 µs x 25 loops). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
3. Excludes 00H Programming prior to Erasure.

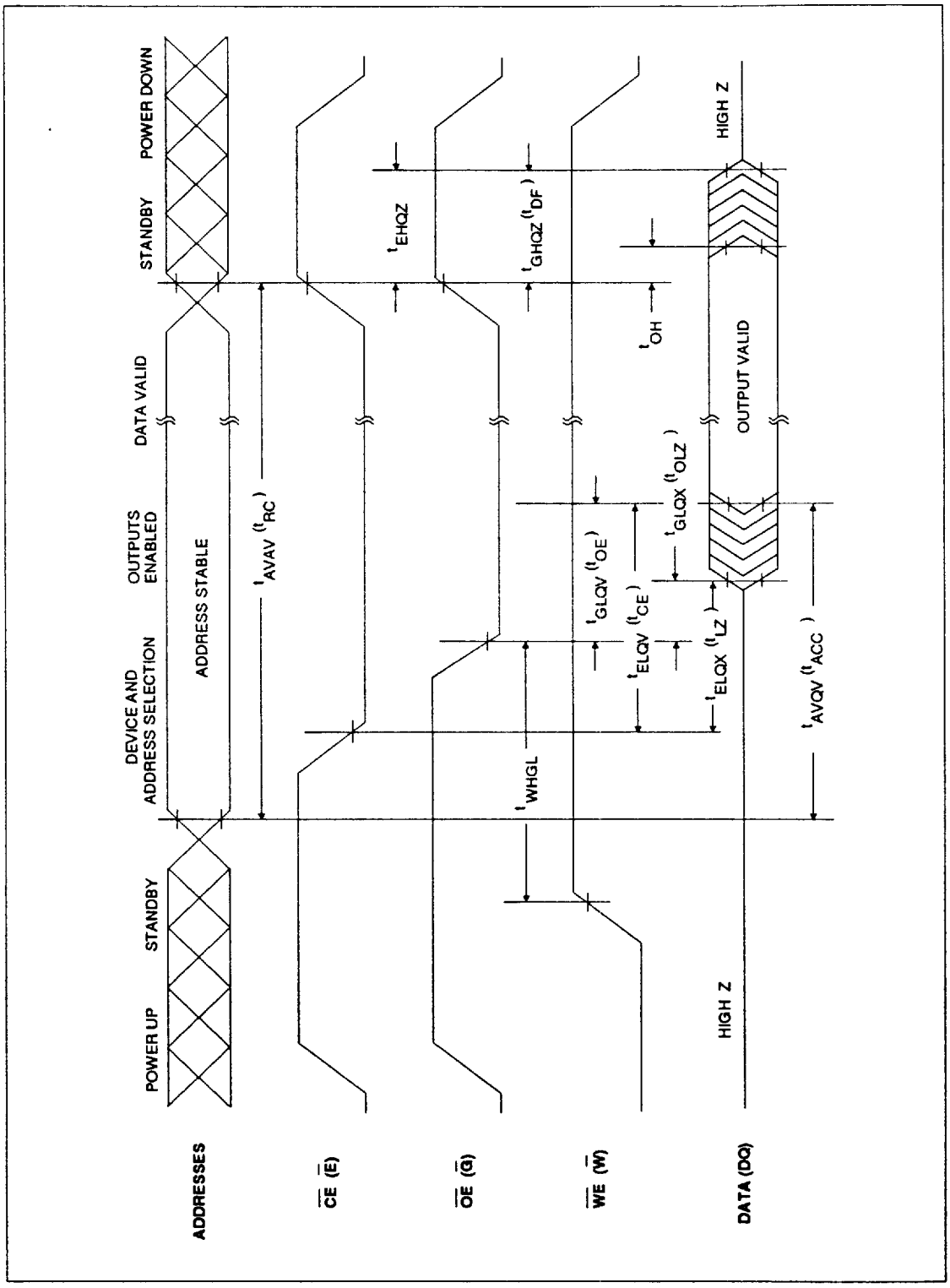
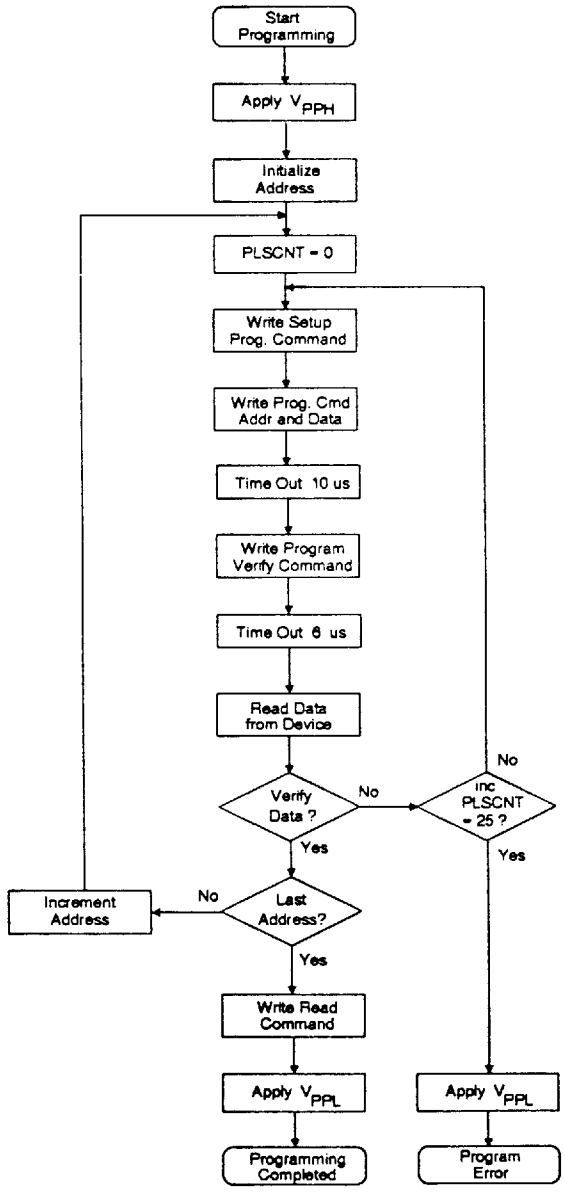


Figure 1. AC Timing <Read Operation>



Bus Operation	Command	Comments
Standby		V_{PP} ramps to V_{PPH} (or V_{PP} hardwired)
		Initialize Address
		Initialize pulse count PLSCNT = Pulse Count
1st Write Cycle	Write Setup	Data = 40H
2nd Write Cycle	Program	Valid Address and Data
		Wait
1st Write Cycle	Program Verify	Data = C0H
		Wait
Read		Read Byte to verify Programming
Standby		Compare Data Output to Data Expected
1st Write Cycle	Read	Data = 00H Sets the Register for Read Operation
Standby		V_{PP} ramps to V_{PPL} (or V_{PP} hardwired)

NOTE: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

Figure 2. Programming Algorithm

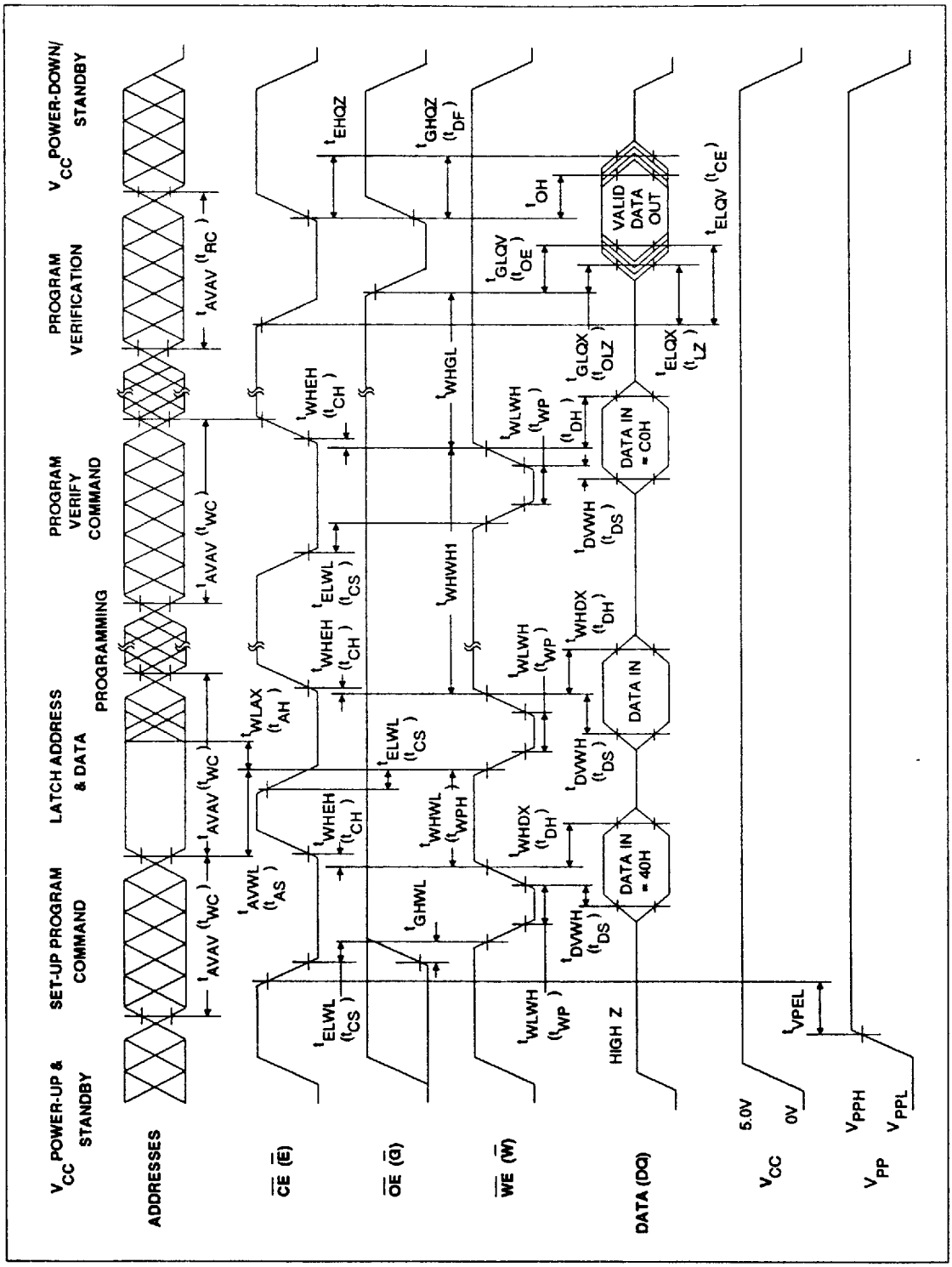


Figure 3. AC Timing <Programming Operation>

Alternate $\overline{CE}$-Controlled Writes

Symbol	Parameter	28F010/I-12 Min.	28F010/I-12 Max.	28F010/I-15 Min.	28F010/I-15 Max.	28F010/I-20 Min.	28F010/I-20 Max.	Unit
t_{AVAV}	Write Cycle Time	120	-	150	-	200	-	ns
t_{AVEL}	Address Setup Time	0	-	0	-	0	-	ns
t_{ELAX}	Address Hold Time	80	-	80	-	95	-	ns
t_{DVEH}	Data Setup Time	50	-	50	-	50	-	ns
t_{EHDX}	Data Hold Time	10	-	10	-	10	-	ns
t_{EHGL}	Write Recovery Time before Read	6	-	6	-	6	-	µs
t_{GHEL}	Read Recovery Time before Write	0	-	0	-	0	-	µs
t_{WLEL}	$\overline{WE}$ Set-up Time before $\overline{CE}$	0	-	0	-	0	-	ns
t_{EHWH}	Write Enable Hold Time	0	-	0	-	0	-	ns
t_{ELEH}	Write Pulse Width	70	-	70	-	80	-	ns
t_{EHEL}	Write Pulse Width High	20	-	20	-	20	-	ns
t_{VPEL}	V_{PP} Set-up Time to $\overline{CE}$ low	1.0	-	1.0	-	1.0	-	µs

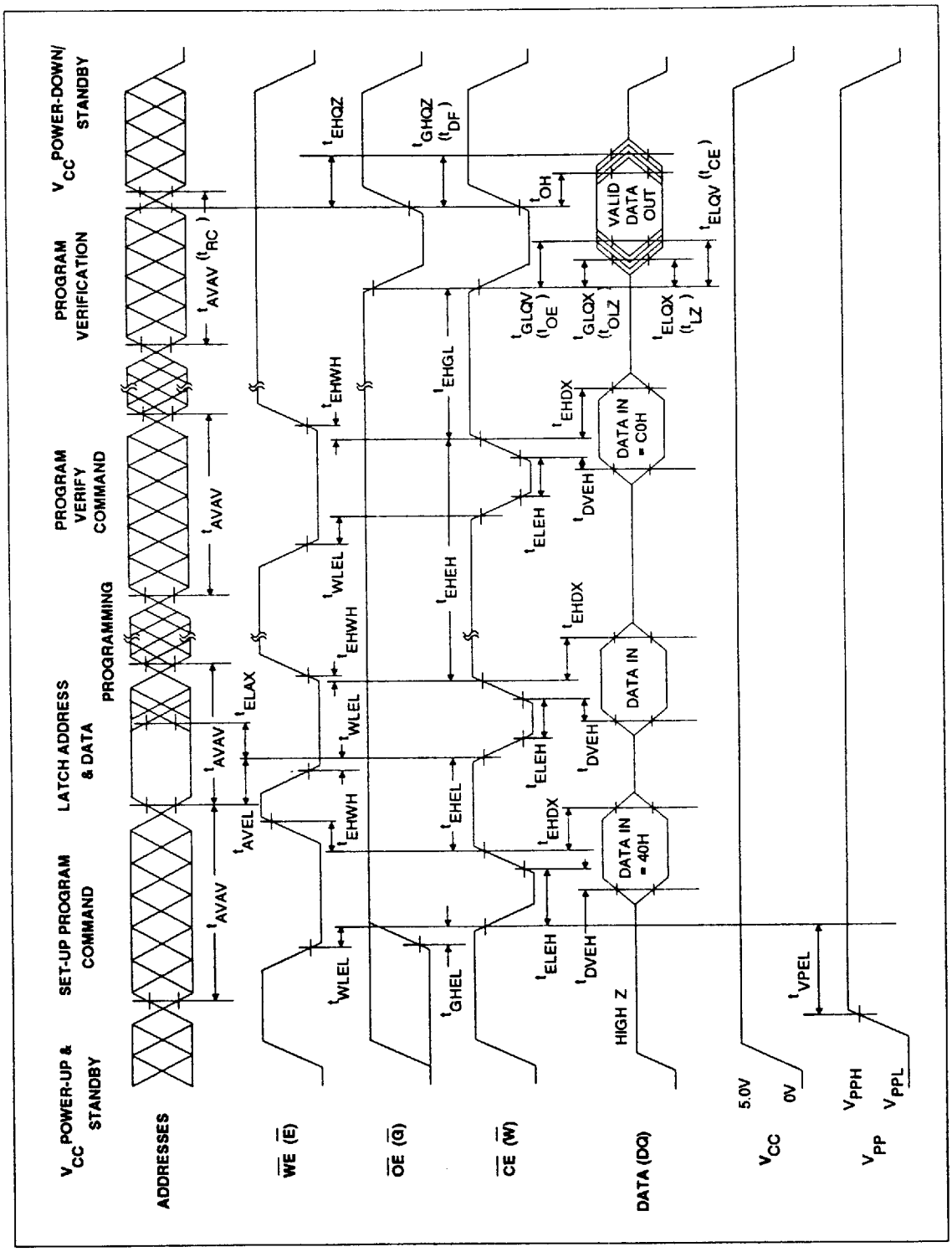
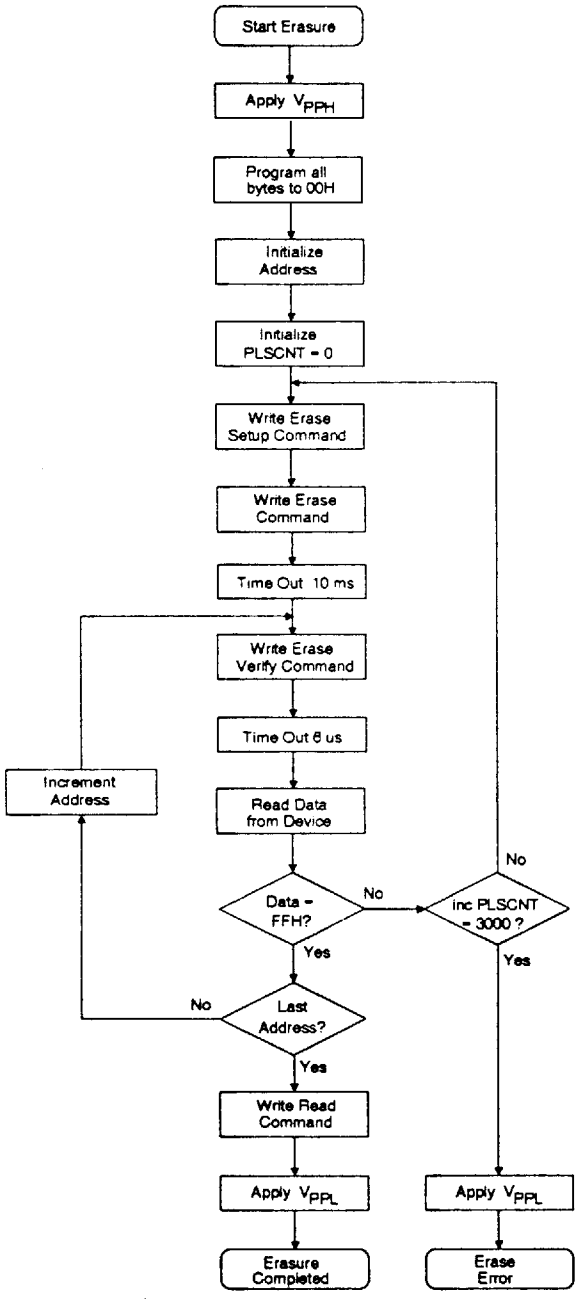


Fig. 4. Alternate AC Timing <Prog. Operation>



Bus Operation	Command	Comments
		V_{PP} ramps to V_{PPH} (or V_{PP} hardwired)
Standby		All Bytes Shall be programmed to 00 before an erase operation
		Initialize Address
		PLSCNT = Pulse Count
Write	Erase	Actual Erase needs 10 ms pulse , Data = 20H
Write	Erase	Data = 20H
		Wait
Write	Erase Verify	Address = Byte to verify Data=20H; Stops Erase Operation
		Wait
Read		Read Byte to verify erasure
Standby		Compare Output to FF Increment pulse count
Write	Read	Data = 00H, Resets the Register for Read Operations
Standby		V_{PP} ramps to V_{PPL} (or V_{PP} hardwired)

NOTE: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

Figure 5. Chip Erase Algorithm

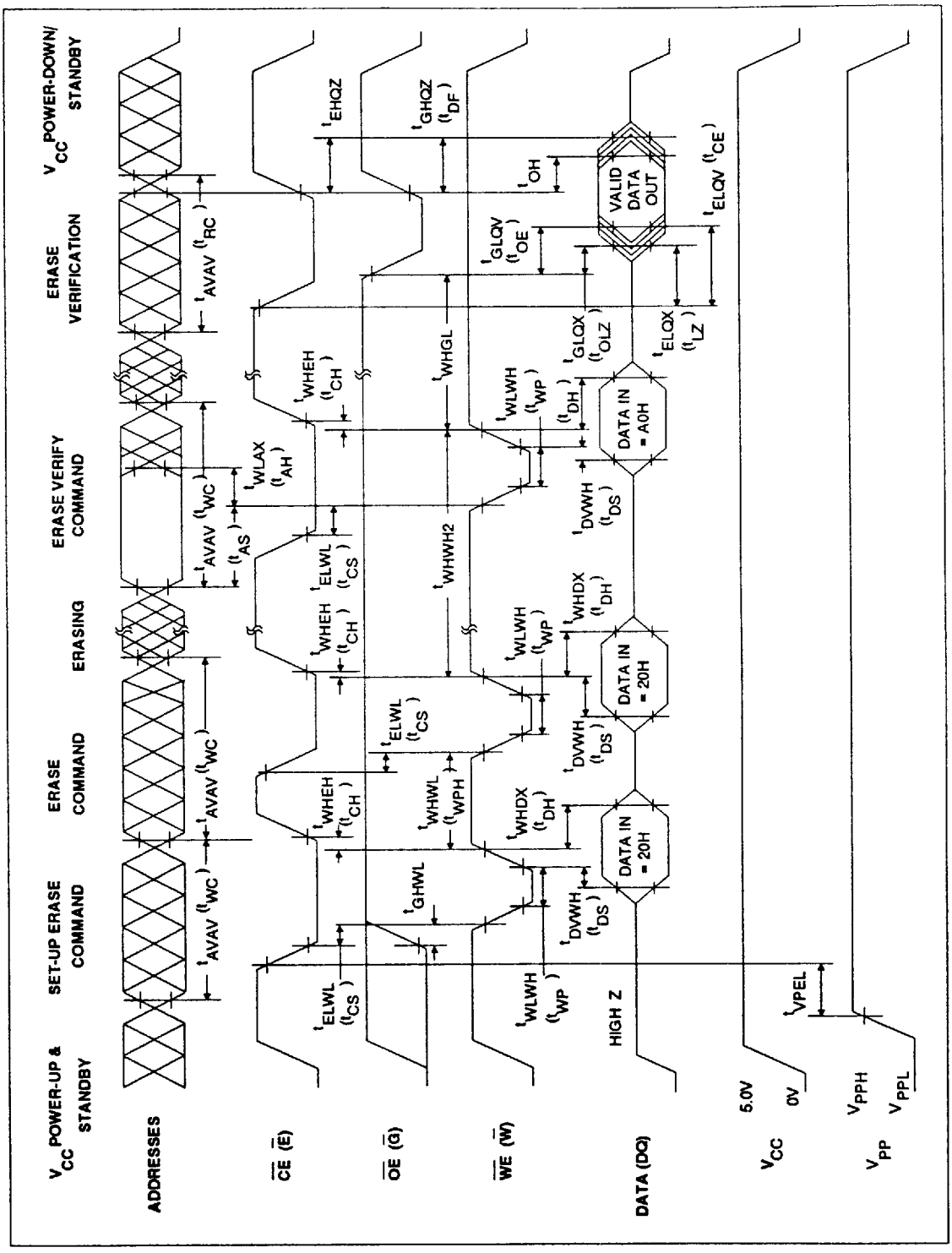
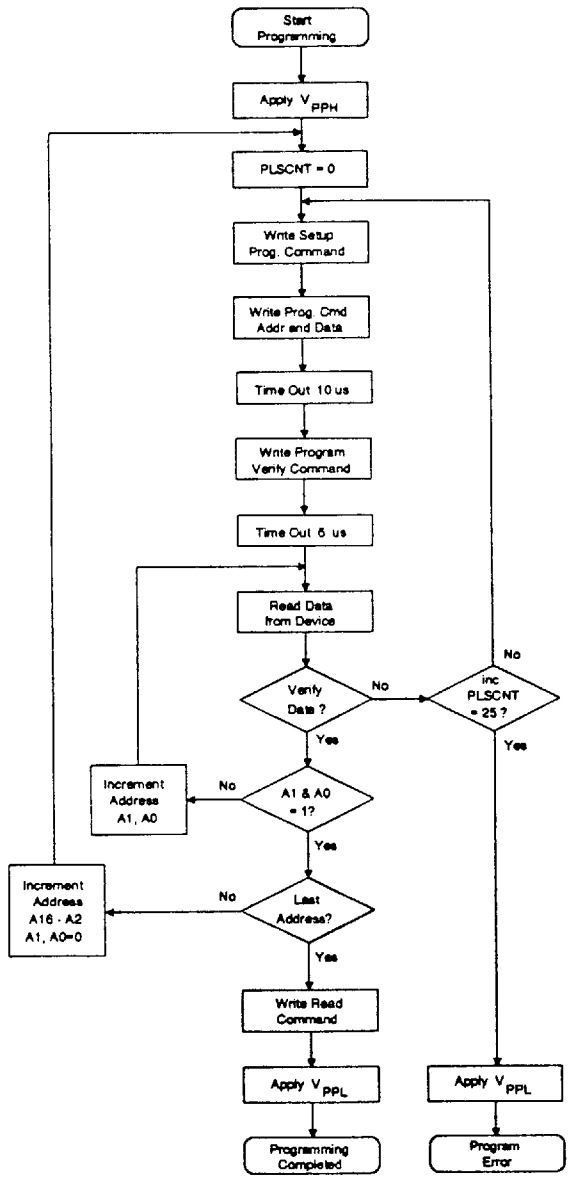


Figure 6. AC Timing <Erase Operation>



Bus Operation	Command	Comments
Standby		V_{PP} ramps to V_{PPH} (or V_{PP} hardwired)
		Initialize pulse count PLSCNT = Pulse Count
1st Write Cycle	Write Setup	Data = E0H
2nd Write Cycle	Program	Valid Address and Data A2 to A16, A0 or A1 = 0
		Wait
1st Write Cycle	Program Verify	Data = C0H
		Wait
Read		Read Byte to verify Programming
Standby		Compare 4 Data Bytes to Data Expected
		Increment Address (A0,A1)
		Increment Address (A2 to A16) Set A1 = 0, A0 = 0
1st Write Cycle	Read	Data = 00H Sets the Register for Read Operation
Standby		V_{PP} ramps to V_{PPL} (or V_{PP} hardwired)

NOTE: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

Figure 7. Speed Programming Algorithm

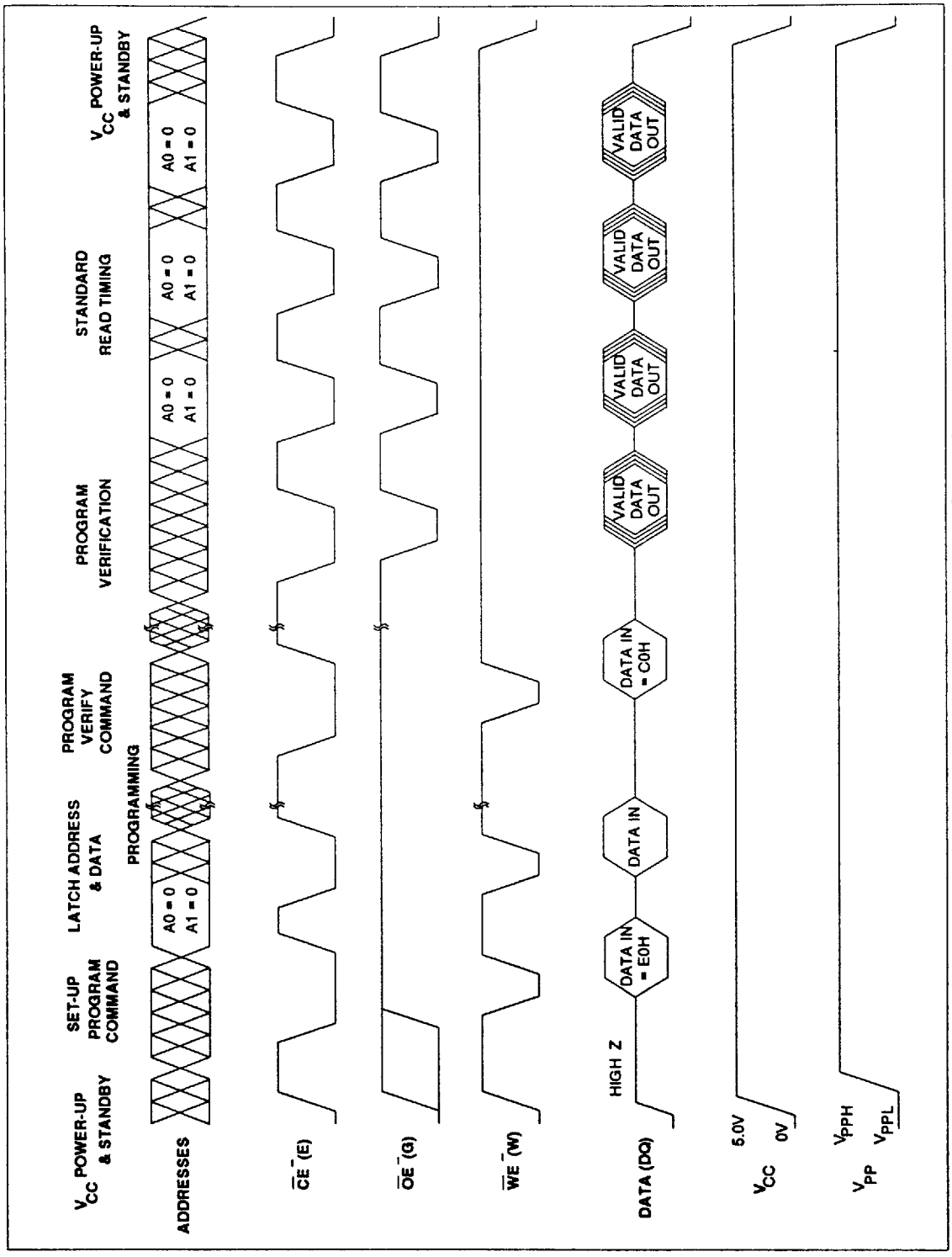


Fig.8 AC Timing <Speed Prog. Operation>

ORDERING INFORMATION

Part Number	Organization	Endurance Cycles	Access Time	Temp. Range	Package
CAT28F010-12	128K x 8	1000	120 ns	†	P,N,D
CAT28F010-15	128K x 8	1000	150 ns	†	P,N,D
CAT28F010-20	128K x 8	1000	200 ns	†	P,N,D
CAT28F010I-12	128K x 8	1000	120 ns	I	P,N,D
CAT28F010I-15	128K x 8	1000	150 ns	I	P,N,D
CAT28F010I-20	128K x 8	1000	200 ns	I	P,N,D
CAT28F010H-12	128K x 8	10,000	120 ns	†	P,N,D
CAT28F010H-15	128K x 8	10,000	150 ns	†	P,N,D
CAT28F010H-20	128K x 8	10,000	200 ns	†	P,N,D
CAT28F010HI-12	128K x 8	10,000	120 ns	I	P,N,D
CAT28F010HI-15	128K x 8	10,000	150 ns	I	P,N,D
CAT28F010HI-20	128K x 8	10,000	200 ns	I	P,N,D

Key:
† = Commercial (0°C to +70°C)
I = Industrial (-40°C to +85°C)
P = 32 Pin Plastic DIP
N = 32 Pin PLCC
D = 32 Pin CERDIP
H = 10,000 cycle endurance

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