Features

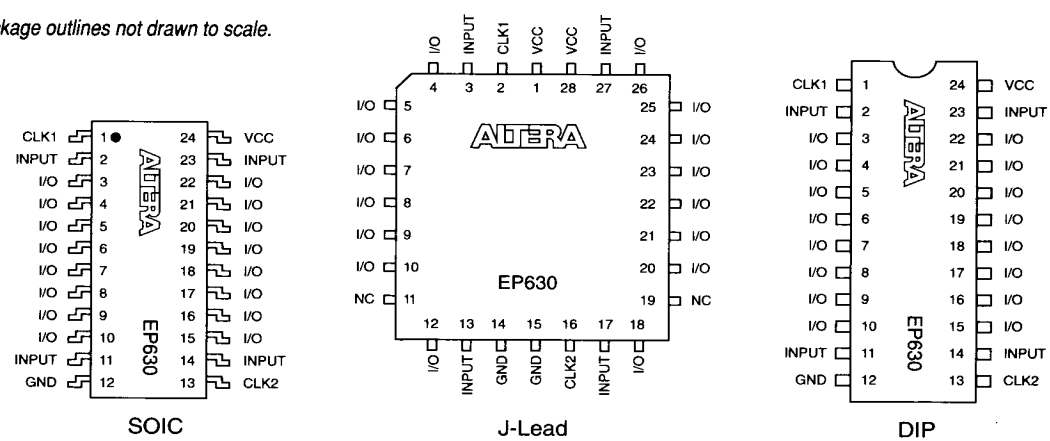
- High-performance 16-macrocell EPLD
  - Combinatorial speeds with t_{PD} = 15 ns
  - Counter frequencies up to 83 MHz
  - Pipelined data rates up to 83 MHz
- Pin-, function-, and JEDEC-File-compatible with Altera's EP610, EP610A, and EP610T EPLDs
- 100% generically testable to provide 100% programming yield
- Available in one-time-programmable (OTP) plastic chip carrier packages
  - 24-pin, 300-mil dual in-line package (PDIP)
  - 24-pin, 300-mil small-outline integrated circuit (SOIC)
  - 28-pin J-lead chip carrier (PLCC)
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

General Description

Altera's EP630 Erasable Programmable Logic Device (EPLD) is a fast, low-power version of the EP610 device. The EP630 EPLD can implement a 16-bit counter at up to 83 MHz and typically consumes 5 mA when operating at 1 MHz. The EP630 EPLD is available in OTP plastic 24-pin, 300-mil DIP; 24-pin, 300-mil SOIC; and 28-pin J-lead chip carrier packages. It is available with maximum t_{PD} values of 15 ns and 20 ns. See Figure 12.

Figure 12. EP630 Package Pin-Out Diagrams

Package outlines not drawn to scale.



Absolute Maximum Ratings Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	14.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–175	175	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time	*See Note (2)*		40	ns
t_F	Input fall time	*See Note (2)*		40	ns

DC Operating Conditions *See Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (non-turbo standby)	$V_I = V_{CC}$ or GND, No load, *See Note (5)*		20	150	µA
I_{CC2}	V_{CC} supply current (non-turbo mode)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (6)*		5	10	mA
I_{CC3}	V_{CC} supply current (turbo mode)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (6)*		45	90	mA

Capacitance *See Note (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *See Note (4)*

			EP630-15		EP630-20		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	*See Note (8)*	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20	20	ns
t_{PD2}	I/O input to non-registered output			17		22	20	ns
t_{PZX}	Input to output enable			15		20	20	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (9)*		15		20	20	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		15		20	20	ns
t_{IO}	I/O input pad and buffer delay			2		2	0	ns

Global Clock Mode			EP630-15		EP630-20		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	*See Note (8)*	Unit
f_{MAX}	Maximum frequency	*See Note (10)*	83.3		62.5		0	MHz
t_{SU}	Input setup time		9		11		20	ns
t_{H}	Input hold time		0		0		0	ns
t_{CH}	Clock high time		6		8		0	ns
t_{CL}	Clock low time		6		8		0	ns
t_{CO1}	Clock to output delay			11		13	0	ns
t_{CNT}	Minimum clock period			12		16	0	ns
f_{CNT}	Internal maximum frequency	*See Note (6)*	83.3		62.5		0	MHz

Array Clock Mode			EP630-15		EP630-20		Non-Turbo Adder	
Symbol	Parameter	Conditions	Min	Max	Min	Max	*See Note (8)*	Unit
f_{MAX}	Maximum frequency	*See Note (10)*	71.4		55.5		0	MHz
t_{ASU}	Input setup time		6		8		20	ns
t_{AH}	Input hold time		6		8		0	ns
t_{ACH}	Clock high time		7		9		0	ns
t_{ACL}	Clock low time		7		9		0	ns
t_{ACO1}	Clock to output delay			15		20	20	ns
t_{ACNT}	Minimum clock period			14		18	0	ns
f_{ACNT}	Internal maximum frequency	*See Note (6)*	71.4		55.5		0	MHz

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) For all clocks: t_R and t_F = 20 ns.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
(5) When in non-turbo mode, an EPLD will automatically enter standby mode if logic transitions do not occur (approximately 100 ns after the last transition).
(6) Measured with a device programmed as a 16-bit counter.
(7) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only.
(8) See "Turbo Bit" earlier in this data sheet.
(9) Sample-tested only for an output change of 500 mV.
(10) The f_{MAX} values represent the highest frequency for pipelined data.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EP630-15, EP630-20
Industrial	(–40° C to 85° C)	EP630-20
Military	(–55° C to 125° C)	Consult factory

Figure 13 shows the output drive characteristics for EP630 I/O pins and typical supply current versus frequency for the EP630 EPLD.

Figure 13. EP630 Output Drive Characteristics and I_{CC} vs. Frequency