DATA SHEET

TDA5149G

12 V Voice Coil Motor (VCM) driver and spindle motor pre-driver combination chip

Product specification
File under Integrated Circuits, IC11

1996 May 06

Philips Semiconductors

PHILIPS

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TDA5149G

FEATURES

General features

- Single-chip voice coil motor driver and spindle motor pre-driver
- Internal voltage reference generator
- Programming of timing parameters via the serial bus
- Control of sleep, brake and disable modes for both the VCM and spindle via the serial bus
- Temperature monitor circuit
- General purpose uncommitted operational amplifier.

Voice coil motor driver

- On-board full-bridge power DMOS driver with low R_{DSon}
- Class AB linear amplifier with no dead zone
- Adjustable gain and bandwidth
- Retract circuit operating at power-down.

Spindle motor pre-driver

- Designed to drive external N-channel power MOSFETs for brushless, sensorless DC motors
- Internal or external commutation control
- Digital commutation timing
- Average motor supply current control with Pulse Width Modulation (PWM)
- Soft switching under PWM control
- Spindle brake after park at power-down.

APPLICATIONS

- 12 V high-performance hard disk drives.

GENERAL DESCRIPTION

The TDA5149G is a combination of a voice coil motor driver and a spindle motor pre-driver, capable of operating 12 V high-performance hard disk drives.

The device integrates a spindle pre-driver that drives three external N-channel power MOSFETs in order to drive a three-phase brushless, sensorless DC motor in full wave mode. In the normal mode, commutations are generated from the internal Back EMF (BEMF) sensing circuitry. Commutations, however, can also be generated from an external source, thereby providing the possibility of driving the motor in the stepper-motor mode.

The VCM driver is a linear transconductance amplifier capable of handling currents up to 1.65 A. It allows external adjustment of the gain and compensation. The TDA5149G also contains two drivers for a latch that secures the heads in the event of power-down.

To control functions such as park, brake, sleep or disable and to program the different timing parameters, the TDA5149G is provided with a three-wire serial port. A high precision voltage monitor is also included, for both 5 and 12 V power supplies. Finally, the IC contains a temperature monitor circuit and an uncommitted operational amplifier connected to V_{DD}, which can be used freely within the application. The device is contained in a LQFP64 package with 4 pins connected to the lead frame for improved heat dissipation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	general supply voltage (pin 54)		10.8	12.0	13.2	V
V_{DDD}	digital supply voltage (pin 55)		4.5	5.0	5.5	V
V_{DDA1}	analog supply voltage (pin 27)		4.5	5.0	5.5	V
I_{oVCM}	voice coil motor output current		–	–	1.65	A
R_{DSon}	VCM power DMOS total on-resistance (including leads and bond wires)	T_j = 25 °C	–	–	0.65	Ω
		T_j = 125 °C	–	–	1.1	Ω

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5149G	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

BLOCK DIAGRAMS

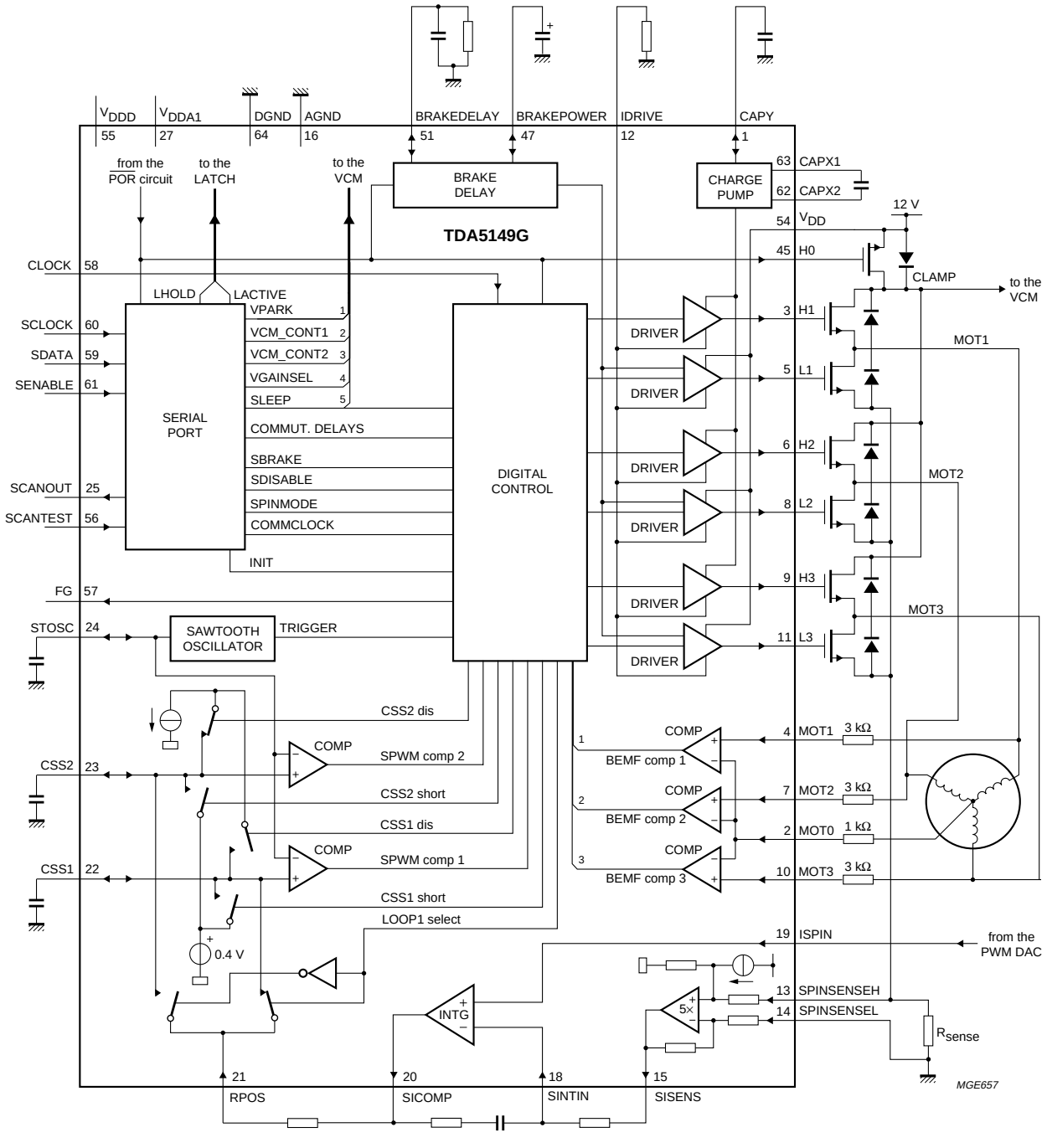


Fig.1 Block diagram of the spindle part.

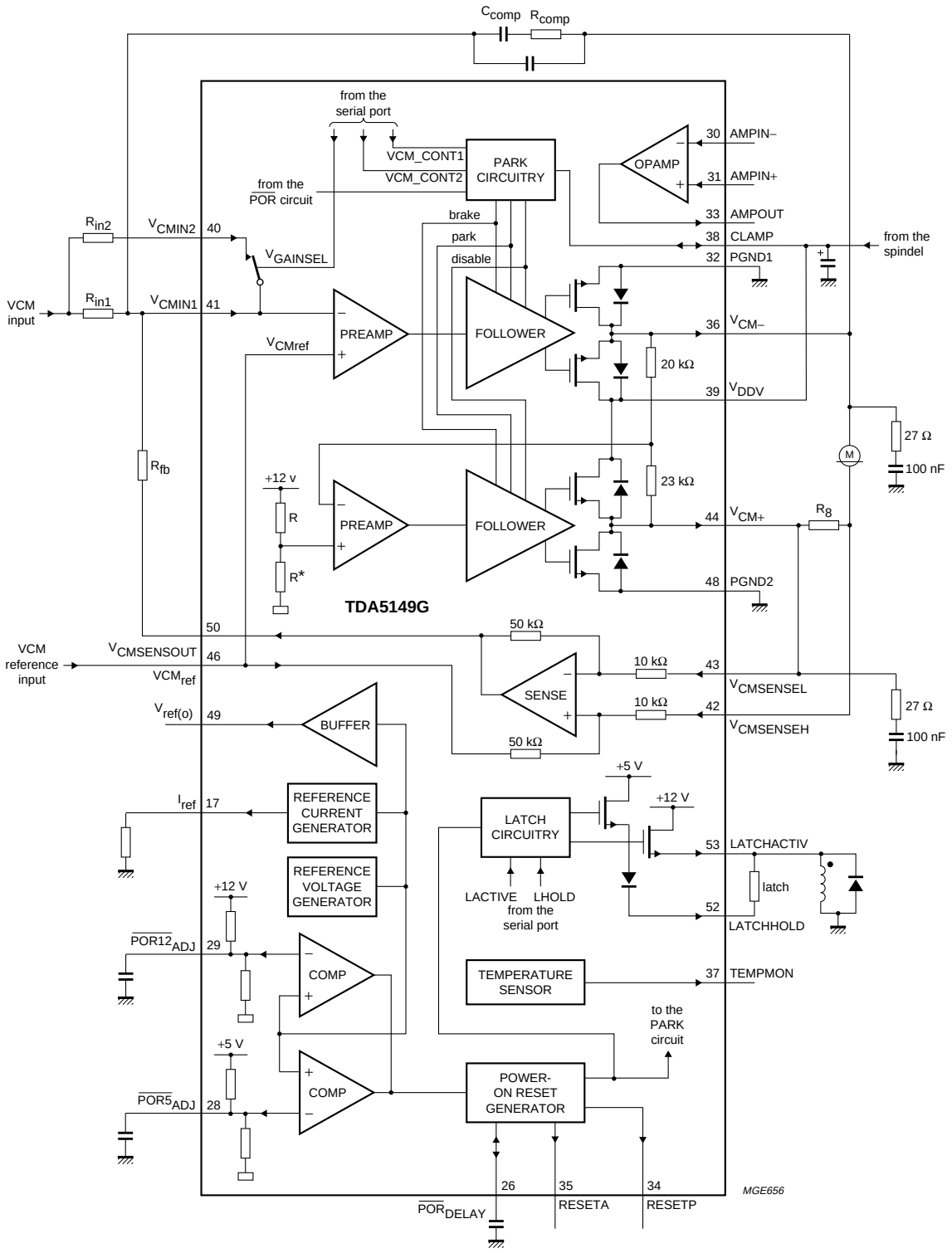


Fig.2 Block diagram of the VCM and RESET circuits.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
CAPY	1	I/O	charge pump capacitor
MOT0	2	I	motor centre tap input
H1	3	O	driver output to gate of upper power FET 1
MOT1	4	I	back EMF comparator input 1
L1	5	O	driver output to gate of lower power FET 1
H2	6	O	driver output to gate of upper power FET 2
MOT2	7	I	back EMF comparator input 2
L2	8	O	driver output to gate of lower power FET 2
H3	9	O	driver output to gate of upper power FET 3
MOT3	10	I	back EMF comparator input 3
L3	11	O	driver output to gate of lower power FET 3
IDRIVE	12	I	adjustment for output stage drive current
SPINSENSEH	13	I	positive spindle sense amplifier input
SPINSENSEL	14	I	negative spindle sense amplifier input
SISENS	15	O	spindle sense amplifier output
AGND	16	–	general analog ground; note 1
I_{ref}	17	O	reference current generator output
SINTIN	18	I	negative integrator input
ISPIN	19	I	positive integrator input, average current adjustment
SICOMP	20	O	integrator output
RPOS	21	I	duty cycle modulator input
CSS1	22	I/O	soft switching capacitor 1
CSS2	23	I/O	soft switching capacitor 2
STOSC	24	I/O	sawtooth oscillator capacitor
SCANOUT	25	O	test output
$\overline{POR}_{DELAY}$	26	I/O	power-on reset delay capacitor (active LOW)
V_{DDA1}	27	–	analog supply voltage 1 (+5 V)
$\overline{POR5}_{ADJ}$	28	O	adjustment of $\overline{POR}$ threshold (for +5 V)
$\overline{POR12}_{ADJ}$	29	O	adjustment of $\overline{POR}$ threshold (for +12 V)
AMPIN–	30	I	negative input of the uncommitted operational amplifier
AMPIN+	31	I	positive input of the uncommitted operational amplifier
PGND1	32	–	power ground 1 for VCM DMOS; note 1
AMPOUT	33	O	uncommitted operational amplifier output
RESETP	34	O	power-on reset digital output with passive pull-up resistor
RESETA	35	O	power-on reset digital output with active pull-up resistor
V_{CM-}	36	O	negative output voltage of the VCM power stage
TEMPMON	37	O	temperature monitor output
CLAMP	38	I/O	clamp capacitor used for head retraction
V_{DDV}	39	–	power supply for VCM DMOS driver (+12 V)
V_{CMIN2}	40	I	switchable VCM control input voltage

SYMBOL	PIN	I/O	DESCRIPTION
V_{CMIN1}	41	I	VCM control input voltage
$V_{CMSENSEH}$	42	I	positive VCM sense amplifier input voltage
$V_{CMSENSEL}$	43	I	negative VCM sense amplifier input voltage
V_{CM+}	44	O	positive output voltage of the VCM power stage
H0	45	O	gate control of the isolating power FET
VCM_{ref}	46	I	reference voltage input for the VCM
BRAKEPOWER	47	I/O	reservoir capacitor for the brake/park circuitry
PGND2	48	–	power ground 2 for VCM DMOS; note 1
$V_{ref(o)}$	49	O	reference voltage generator output
$V_{CMSENSOUT}$	50	O	VCM sense amplifier output voltage
BRAKEDELAY	51	I/O	powerless brake delay adjustment
LATCHHOLD	52	O	latch hold output
LATCHACTIV	53	O	latch activate output
V_{DD}	54	–	general supply voltage (+12 V)
V_{DDD}	55	–	digital supply voltage (+5 V)
SCANTEST	56	I	test mode input
FG	57	O	commutation frequency generator output
CLOCK	58	I	clock for digital timing input
SDATA	59	I	serial port data input
SCLOCK	60	I	serial port clock input
SENABLE	61	I	serial port enable input
CAPX2	62	I/O	charge pump capacitor input/output
CAPX1	63	I/O	charge pump capacitor input/output
DGND	64	–	digital ground; note 1

Note

1. The 4 ground pins are tied to the lead frame for better heat dissipation.

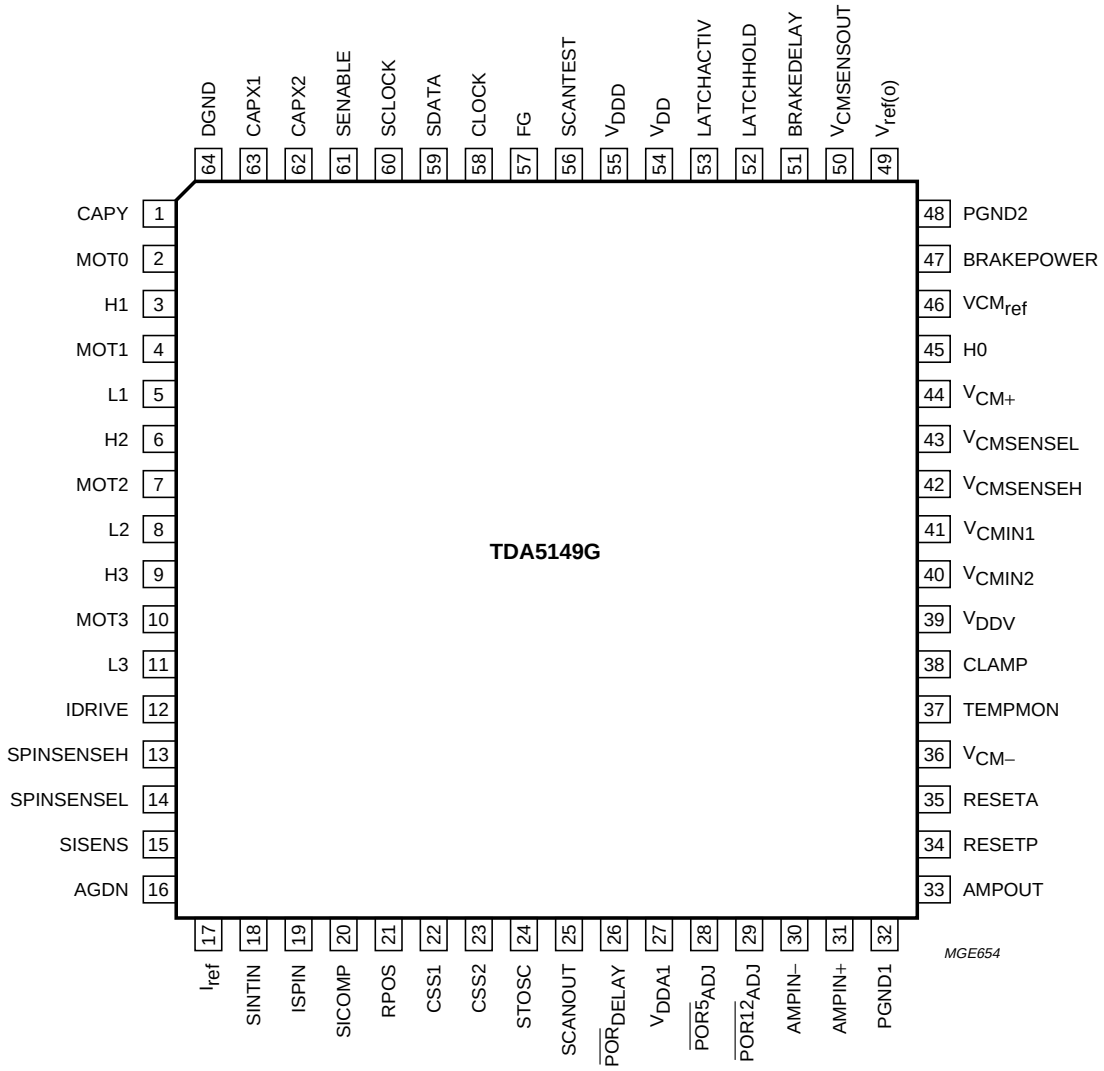


Fig.3 Pin configuration.

FUNCTIONAL DESCRIPTION

Spindle

The spindle section contains both the low and high side pre-drivers for a three phase DC brushless motor. The digital commutation control, using the timing information provided via the serial port, is responsible for the proper switch-on and switch-off of the external power FETs. It is also responsible for selecting the correct BEMF comparator.

For optimum power efficiency, a continuous PWM method is used to control the average current from the power supply to the motor coils. This PWM mode, by controlling the average power supply current, produces a lower torque ripple and thus lower audible noise. In order to reduce further acoustic noise the TDA5149G is provided with a soft switching circuit to turn-on and turn-off linearly the switching current under PWM control. The switching transition time is controlled by the digital commutation circuit and is fixed to 50% of the time between two zero-crossings, i.e. 30° of the electrical revolution.

Soft switching is achieved by activating, during commutation, a free-running duty-cycle modulator controlled by a linearly decreasing voltage across a capacitor. This will reduce the current smoothly in the off-going leg to zero. In conjunction with this additional PWM open loop, the average current control regulates the sum of the current in the off-going and on-going leg.

This method requires two PWM control loops; one to control the average current (main loop) and one to control the current in the off-going leg. The swapping of the two loops is realized with a pair of analog switches that are sequentially switched by the digital commutation circuitry.

The PWM control also causes PWM pulses on the back EMF. These pulses disturb correct sensing of the back EMF for the zero-crossing detection. Consequently, edge-triggered latches are inserted behind the back EMF comparators, thus ensuring reliable back EMF sensing.

In the SPINMODE, programmable via the serial bus, the user can feed their own commutation pulses to the pre-drivers and control the motor in the stepper-motor mode. The commutation pulses are applied to the TDA5149G via the serial bus by setting the COMMCLK bit successively to logic 1 and logic 0.

The different control modes of the TDA5149G can be commanded via the serial bus. These modes are as follows:

- Sleep mode: all analog circuits, except the power supply monitor, are switched off to reduce the power consumption of both the 12 and 5 V supplies.
- Disable mode: the output voltage of all pre-drivers is LOW thus the external power MOSFETs are not conducting.
- Brake mode: all low side pre-drivers are turned on (output voltage HIGH) thus switching on the low-side power MOSFETs. In this way the back EMF voltage of the motor is short-circuited to ground.

Voice coil motor

The VCM is a linear, symmetrical, class AB, H-bridge type power amplifier with all power devices on-chip. The driver is a transconductance amplifier that controls the output currents up to 1.65 A. The driver is constructed in a master-slave configuration with the zero current level internally adjusted in such a way that it corresponds to the middle of the output swing. Moreover, the gain of the slave has been made greater than 1 in order to ensure full saturation of the driver output VCM+.

The gain of the closed loop is programmable, using the $V_{GAINSEL}$ bit. This bit can be programmed via the serial bus. A sense resistor (R_S) allows the measurement of the VCM current. The voltage across this resistor is connected to an accurate sense amplifier with a typical gain of 5. The output of the sense amplifier ($V_{CMSENSOUT}$) is fed back to the input of the VCM amplifier. Because of the symmetry of the circuit, the compensation network can be connected between the VCM1 input and the VCM– output.

Control modes such as VCM-BRAKE, VCM-DISABLE and VCM-PARK can be controlled via the serial bus.

Latch drivers

The TDA5149G provides the possibility of driving an external latch to secure the VCM heads. There are two modes; the activate mode (LACTIVE) and the hold mode (LHOLD). The hold mode is used to preserve power. Both modes are controlled via the serial bus. The drivers are switched off during the SLEEP mode or in the event of a power-down.

Power-on/power-off reset

The power-on reset circuitry monitors the analog, digital and general supplies. The voltage thresholds have been set internally for both supplies, i.e. 4.4 V for V_{DDA} and V_{DDD}, and 10.5 V for V_{DD}. External adjustment and filtering, to suppress supply spikes, has been made possible through the pins $\overline{POR5}_{ADJ}$ and $\overline{POR12}_{ADJ}$.

When either of the supplies falls below their threshold levels, the reset circuit provides two active LOW output signals. The RESETA signal is a full CMOS output and the RESETP signal has an active pull-down MOS transistor with a passive pull-up resistance of 10 kΩ. The latter can be used for emulation purposes. Both signals remain LOW until the supply voltages are again above the threshold level, delayed by a time constant period that is determined by the value of the capacitor connected to pin $\overline{POR}_{DELAY}$.

A park sequence is initiated on a reset fault. This includes disabling the actuator latch drivers and starting a delayed spindle brake operation by switching on the low side pre-drivers simultaneously. This brake delay is determined by an external RC combination connected to BRAKEDELAY. Actuator PARK and spindle BRAKE can also be controlled via the serial port.

At power-up, the two reset output signals (RESETA and RESETP) will remain LOW as long as either supply voltage is below the specified threshold plus the hysteresis voltage. Once the supply voltages are above their specific trip levels, the two reset signals become HIGH after the power-on reset delay ($\overline{POR}_{DELAY}$). This delay time is determined by the value of the capacitor connected to the $\overline{POR}_{DELAY}$ pin.

Powerless park/brake

As with the normal retract procedure, an actuator park sequence is initiated whenever a power-down situation occurs. The power-on/power-off reset circuit generates the two active LOW reset signals and also activates the VCM park circuit. The VCM park circuit provides a voltage, retrieved from the rectified back EMF voltage of the running-out spindle, of 1.2 V (typ.) to the VCM pin. The voltage at pin VCM+ is 0 V. This voltage is supplied by the capacitor C_{CLAMP} that is connected to the CLAMP pin. This capacitor smooths the rectified back EMF and stores the electrical energy generated by the motor.

To ensure that the stored energy in the clamp capacitor is only used for the park operation, the CLAMP input must be isolated from the power supply. This can be achieved by using a Schottky diode or a reverse connected N-channel power FET (see Fig.1). The TDA5149G provides an output H0 to control this power FET.

At power-down the brake delay circuit is also enabled. The brake delay circuit is supplied by the energy stored in the capacitor (charged during normal operation from V_{DD}) that is connected to the BRAKEPOWER pin. Both the BRAKEDELAY and BRAKEPOWER pins are then isolated from the 12 V supply voltage. When the voltage on the BRAKEDELAY pin reaches a value of 1.6 V (typ.), the low-side external power FETs are turned on to brake the spindle motor. The BRAKEPOWER capacitor then supplies the current to keep the power FETs conducting. This means that the voltage on this capacitor decreases with time.

Serial port

The serial port is used to modify the various operational modes of the TDA5149G and to adjust the timing parameters to ensure the proper commutation sequence of the spindle motor. It is a synchronous, slave only, three-wire communication port with data (SDATA), clock (SCLOCK) and enable (SENABLE) inputs.

The serial port requires the data to be sent in bytes, the LSB (data 0) to be sent first and the MSB (address 2) last. The three most significant bits (MSBs) determine the register address, the remaining five bits represent the data, which means up to 8 registers can be independently addressed.

When SENABLE is LOW, the serial port is disabled and the IC is not affected by any change both on SDATA and SCLOCK. When SENABLE is HIGH the data is written serially to the shift register on the rising edge of SCLOCK. When SENABLE goes LOW the shifting sequence is stopped and the last 8 bits that are clocked in are latched into the appropriate control register. Therefore, the transmission of two consecutive bytes requires that SENABLE is LOW for at least a duration of ‘t’ (see Chapter “Characteristics”).

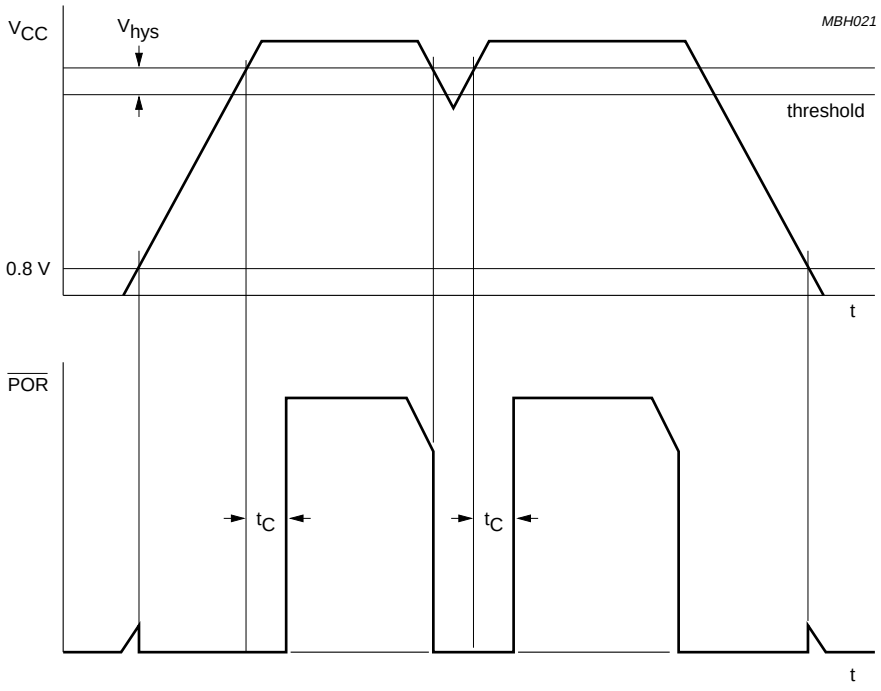


Fig.4 Power-on/power-off reset timing.

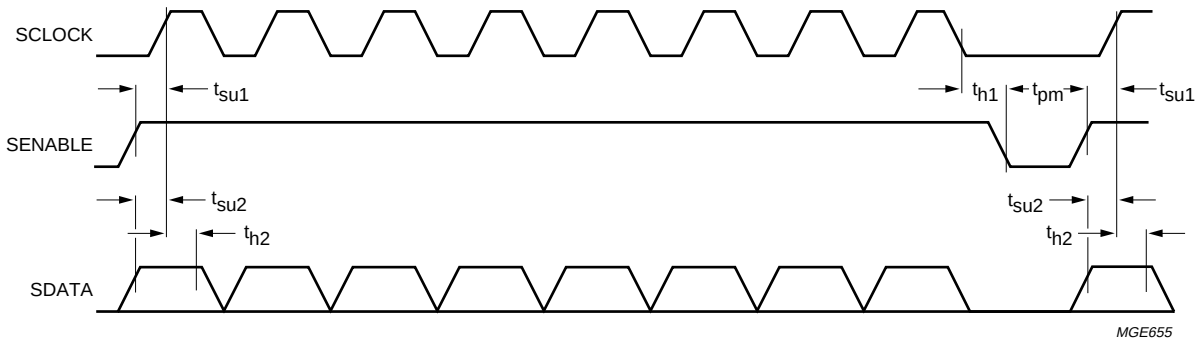


Fig.5 Serial port signal timing

Table 1 Serial port registers

REGISTER ADDRESSED	DATA4	DATA3	DATA2	DATA1	DATA0
Reg # 0	INIT	COMMCLCK	SPINMODE	SDISABLE	SBRAKE
Reg # 1	not used	HARD_SW	LHOLD	LACTIVATE	SLEEP
Reg # 2	not used	not used	VGAINSEL	VCM_CTRL_1	VCM_CTRL_0
Reg # 3	not used	not used	PRESCALER_2	PRESCALER_1	PRESCALER_0
Reg # 4	STARTUP_4	STARTUP_3	STARTUP_2	STARTUP_1	STARTUP_0
Reg # 5	WATCHDOG_4	WATCHDOG_3	WATCHDOG_2	WATCHDOG_1	WATCHDOG_0
Reg # 6	not used	not used	COMDELIM_2	COMDELIM_1	COMDELIM_0
Reg # 7	BLANK_4	BLANK_3	BLANK_2	BLANK_1	BLANK_0

Table 2 REG # 0: address 000; DATA = | INIT | COMMCLK | SPINMODE | SDISABLE | SBRAKE |

DATA BIT	RESET STATE	DESCRIPTION
INIT	1	initializes the three bits commutation shift register in state 1 (see Table 13)
COMMCLK	0	commutation clock in stepper mode (one commutation every LOW-to-HIGH transition)
SPINMODE	0	stepper/BEMF detection mode selection. SPINMODE = 1 means stepper motor mode in hard-switching configuration
SDISABLE	1	logic 1 sets the pre-drivers outputs LOW so that the spindle motor coils are in the high-impedance state
SBRAKE	0	logic 1 sets the lower pre-driver outputs HIGH and the upper pre-driver outputs LOW so that the spindle motor coils are shorted to ground

Table 3 REG # 1: address 001; | not used | HARD_SW | LHOLD | LACTIVE | SLEEP |

DATA BIT	RESET STATE	DESCRIPTION
HARD_SW	0	logic 1 disables the soft switching circuitry, which means PWM is applied on the lower FETs only.This mode is also forced in stepper motor mode.
LHOLD	0	logic 1 turns on the hold current supplied by V_{DDD} through the latch. It is ignored if LACTIVE = 1
LACTIVE	0	logic 1 turns on the activate current supplied by V_{DD} through the latch
SLEEP	0	logic 1 disables spindle, VCM and latch driver outputs. The whole analog circuitry is turned off except the reference bandgap and the voltage monitors. The uncommitted operational amplifier is also cut off.

Table 4 REG # 2: address 010; | not used | not used | VGAINSEL | VCM_CTRL_1 | VCM_CTRL_0 |

DATA BIT	RESET STATE	DESCRIPTION
VGAINSEL	1	logic 1 turns on the switch between V_{CMIN1} and V_{CMIN2}, resulting in a higher gain for the transconductance of the VCM closed loop
VCM_CTRL_1	1	see Table 5
VCM_CTRL_0	1	see Table 5

Table 5 Operating conditions for VCM_CTRL_1 and VCM_CTRL_0

VCM_CTRL_1	VCM_CTRL_0	MODE
0	0	VCM operating
0	1	VCM brake
1	0	VCM park
1	1	VCM disable

Table 6 REG # 3: address 011; | not used | not used | PRESCALER_REG [2 to 0]

DATA BIT	RESET STATE	DESCRIPTION(1)
PRESCALER_2	0	sets the division factor that is applied to the external clock (pin 58) in order to obtain the appropriate internal clock frequency for the proper determination of the commutation delays. The prescaling factors can be obtained as shown in Table 7
PRESCALER_1	1	
PRESCALER_0	0	

Note

1. CLOCK (pin 58) must be valid before the end of the $\overline{\text{POR}}$ delay.

Table 7 Prescaler factors

PRESCALER_REG	FREQUENCY (MHz)(1)
0 0 0	1
0 0 1	2
0 1 0	4
0 1 1	8
1 0 0	16
1 0 1	32
1 1 0	64
1 1 1	128

Note

1. Internal clock frequency is equal to external clock frequency divided by prescaler ratio.

Table 8 REG # 4: address 100; | STARTUP_REG[4 to 0] |

DATA BIT	RESET STATE	DESCRIPTION
STARTUP_4	0	The start-up timer instigates the spin-up in the absence of the back EMF zero crossings. If the rotational speed is high enough, the commutations are sequenced regardless of the start-up counter. But if no BEMF zero crossing occurs, which is the case if the motor is stationary or rotating very slowly, the start-up timer reaches its terminal count given by the STARTUP_REG, thereby causing the next commutation. If t_{IC} is the period of the internal clock then; STARTUP delay = $[(\{0 \text{ to } 31\} \times 32) + 2) \times 511) + 2] \times t_{IC}$
STARTUP_3	0	
STARTUP_2	0	
STARTUP_1	0	
STARTUP_0	0	

Table 9 REG # 4: address 101; | WATCHDOG_REG[4 to 0] |

DATA BIT	RESET STATE	DESCRIPTION
WATCHDOG_4	0	The watchdog timer checks for correct back EMF polarity, which indicates correct rotation of the motor WATCHDOG delay = $[(\{0 \text{ to } 31\} \times 64) + 1] \times t_{IC}$
WATCHDOG_3	0	
WATCHDOG_2	0	
WATCHDOG_1	0	
WATCHDOG_0	0	

Table 10 REG # 6: address 110; | not used | not used | COMDELIM_REG[2 to 0] |

DATA BIT	RESET STATE	DESCRIPTION
COMDELIM_2	0	Defines the maximum commutation delay limit by setting the saturation value of the zero crossing counter. t_{IC} represents the period of the internal clock. Table 11 shows the delays which can be obtained.
COMDELIM_1	0	
COMDELIM_0	0	

Table 11 Commutation delay limit

COMDELIM_REG	COUNTER SATURATION VALUE	MAXIMUM COMMUTATION DELAY
111	2047	$t_{IC} \times 1023$
110; note 1	1535	$t_{IC} \times 767$
101	1023	$t_{IC} \times 511$
100; note 1	767	$t_{IC} \times 383$
011	511	$t_{IC} \times 255$
010; note 1	383	$t_{IC} \times 191$
001	255	$t_{IC} \times 127$
000; note 1	191	$t_{IC} \times 95$

Note

1. Even COMDELIM _REG values must be avoided.

Table 12 REG # 7: address 111; | BLANK_REG[4 to 0] |

DATA BIT	RESET STATE	DESCRIPTION
BLANK_4	0	In the hard switching mode, the blank delay inhibits the back EMF comparator outputs just at the moment the MOT outputs are commutating, until they have been stabilized again. To avoid false zero-crossing detection, the blank delay operates in the same way at the end of the fly-back pulse (hard-switching mode), or at the end of the soft-switching interval (soft-switching mode). BLANK delay = $[(\{0 \text{ to } 31\} \times 4) + 1] \times t_{IC}$
BLANK_3	0	
BLANK_2	0	
BLANK_1	0	
BLANK_0	0	

Table 13 Configuration of the six commutation states in hard-switching mode

STATE	SHIFT REGISTER	H1[1]	H2[1]	H3[1]	L1[2]	L2[2]	L3[2]
1[3]	111	ON	–	–	–	PWM	–
2	011	ON	–	–	–	–	PWM
3	001	–	ON	–	–	–	PWM
4	000	–	ON	–	PWM	–	–
5	100	–	–	ON	PWM	–	–
6	110	–	–	ON	–	PWM	–

Note

1. H1, H2 and H3 are the upper power FETs connected to MOT1, MOT2 and MOT3 respectively.
2. L1, L2 and L3 are the lower power FETs connected to MOT1, MOT2 and MOT3 respectively.
3. INIT = 1 means ‘state 1’ situation with PWM stuck in OFF on L2.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	general supply voltage	indefinite time period	–0.3	+13.5	V
			–0.3	+15	V
V_{DDD}	digital supply voltage	indefinite time period	–0.3	+6.0	V
			–0.3	+7.0	V
V_{DDA}	analog supply voltage	indefinite time period	–0.3	+6.0	V
			–0.3	+7.0	V
V_{DDV}	supply for VCM DMOS driver	indefinite time period	–0.3	+13.5	V
			–0.3	+15	V
V_{CM+}	output voltage of the VCM power stage		–0.7	+15	V
V_{CM-}	output voltage of the VCM power stage		–0.7	+15	V
I_{CM+}	output current of the VCM power stage	current peak <0.5 s	–	2.5	A
ICM–	output current of the VCM power stage	current peak <0.5 s	–	2.5	A
V_{MOT}	BEMF comparator input voltage (pins 4, 7 and 10)		–0.7	–	V
V_n	input voltages on other pins		–0.3	–	V
T_{stg}	IC storage temperature		–55	+125	°C
$T_{j(max)}$	maximum junction temperature		–	150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

ESD according to MIL STD 883C - method 3015 (HBM 1500 Ω, 100 pF) 3 pulses positive and 3 pulses negative on each pin versus ground - Class 1: 0 to 1999 V.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER(1)	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	54	K/W

Note

1. This is obtained in a standard PCB: standard PCB size: 100 mm × 75 mm × 1.6 mm; material = glass epoxy FR4, single copper layer. With dedicated PCB tailored to heat dissipation, the thermal resistance could be as low as 40 K/W.

OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Temperature						
T_{amb}	operating ambient temperature		–5	–	+70	°C
Supplies: pins 27, 55, 54 and 39						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DD}	general supply voltage		10.8	12.0	13.2	V
I_{DDA}	analog supply current	normal mode	–	5.5	7.5	mA
V_{DDV}	supply voltage for VCM DMOS driver		10.8	12.0	13.2	V
VCM reference voltage: pin 46 (VCM_{ref})						
VCM_{ref}	reference voltage input level		1.9	–	4.0	V
Charge pump: pin 1 (CAPY)						
C_{CAPX}	charge pump capacitor	between CAPX1 and CAPX2	6.8	10	13	nF
C_{CAPY}	charge pump capacitor	between CAPY and ground	16	22	30	nF
CLAMP: pin 38						
C_{CLAMP}	clamp capacitance	between CLAMP and ground	–	47	–	µF
BRAKEPOWER: pin 47						
C_{BP}	brakepower capacitance	note 1	–	47	–	µF
Sense resistors						
R_{SSENS}	spindle sense resistor		0.15	–	–	Ω
R_{VSENS}	VCM sense resistor		0.15	–	–	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Spindle pre-drivers: pin 12 (IDRIVE)						
R_{IDRIVE}	resistance for pre-driver current adjustment		32	–	470	kΩ
Reference current: pin 17 (I_{ref})						
R_{Iref}	resistance for reference current adjustment		47	–	470	kΩ
Sawtooth oscillator: pin 24 (STOSC)						
C_{SO}	sawtooth oscillator capacitance	note 2	150	–	700	pF
Power-on reset: pin 26 ($\overline{POR}_{DELAY}$)						
$C_{\overline{PORDELAY}}$	$\overline{POR}_{DELAY}$ capacitance	note 3	–	100	–	nF
Digital inputs for the serial port: pins 58 to 61 (CLOCK, SDATA, SCLOCK and SENABLE)						
V_{IH}	HIGH level input voltage		2.4	–	–	V
V_{IL}	LOW level input voltage		–	–	0.8	V

Notes

1. To guarantee a powerless brake duration of at least 10 s. A low leakage capacitor must be used (<0.1 μA).
2. For a frequency range of 25 to 100 kHz. $C_{STOSC} = 0.775 (I_{ref}/f_{PWM})$.
3. For a RESETA/RESETP pulse duration of approximately 100 ms.

CHARACTERISTICS

V_{DD} = 12 V; $V_{DDA} = V_{DDD}$ = 5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies: pins 27, 55 and 54						
I_{DDA}	analog supply current	normal mode	–	5.5	7.5	mA
		sleep mode	–	1.6	2.0	mA
I_{DDD}	digital supply current	normal mode	–	5.5	7.5	mA
		sleep mode	–	1.6	2.0	mA
I_{DD}	general supply current	normal mode	–	12	17	mA
		sleep mode	–	2.9	4.0	mA
VOLTAGE REFERENCE: PIN 49 ($V_{ref(o)}$)						
$V_{ref(o)}$	reference voltage generator output	$I_{ref(o)}$ = ±1 mA	2.47	2.57	2.67	V
CURRENT REFERENCE: PIN 17 ($I_{ref(o)}$)						
$I_{ref(o)}$	reference current generator output	R_{ref} = 120 kΩ; note 1	20.6	21.4	22.2	μA
TEMPERATURE MONITOR: PIN 37 (TEMPMON)						
V_{OLT}	output voltage at LOW temperature	T_j = 25 °C	2.15	2.17	2.19	V
V_{OHT}	output voltage at HIGH temperature	T_j = 150 °C; note 2	3.03	3.055	3.08	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VCM REFERENCE: PIN 46 (VCM_{ref})						
I_i	input current	V_{VCMref} = 2 V; note 3	–250	–	+60	µA
Spindle: pre-drivers						
CHARGE PUMP: PIN 1 (CAPY)						
V_{CP}	charge pump DC voltage	I_{CAPY} < 1 mA	18.5	19.3	19.8	V
$V_{ripple(p-p)}$	voltage ripple (peak-to-peak value)	I_{CAPY} = 1 mA	–	–	0.8	V
BACK EMF COMPARATORS: PINS 2, 4, 7 AND 10 (MOT0, MOT1, MOT2 AND MOT3)						
V_{iCM}	common mode input voltage	note 4	–0.7	–	V_{DD} + 0.7	V
I_{bias}	input bias current	MOT0	–10	–	0	µA
V_{SWhys}	switching level for hysteresis	for negative transition with respect to MOT0	–13	–	–7	mV
		for positive transition with respect to MOT0	7	–	13	mV
ΔV_{CSW}	variation in comparator switching levels for one IC		–4.2	–	+4.2	mV
$V_{i(hys)}$	input voltage hysteresis		–	0.5	–	mV
SPINDLE LOWER PRE-DRIVERS: PINS 5, 8 AND 11 (L1, L2 AND L3)						
V_{OH}	HIGH level output voltage	I_{OH} = –0.5 mA	7.2	8.0	8.8	V
I_{source}	output source current	R_{IDRIVE} = 120 kΩ; note 5	–0.9	–0.7	–0.5	mA
I_{sink}	output sink current		1.2	1.6	2.0	mA
SR	slew rate	R_{IDRIVE} = 120 kΩ; note 6	–	10	–	V/µs
SPINDLE UPPER PRE-DRIVERS: PINS 3, 6 AND 9 (H1, H2 AND H3)						
V_{OH}	HIGH level output voltage	I_{OH} = –0.5 mA	18.0	18.8	19.6	V
I_{source}	output source current	R_{IDRIVE} = 120 kΩ; note 7	–1.3	–1.0	–0.7	mA
I_{sink}	output sink current		1.3	1.75	2.2	mA
SR	slew rate	R_{IDRIVE} = 120 kΩ; note 6	–	10	–	V/µs
H0: PIN 45						
V_o	output voltage	normal condition	18.3	18.8	20	V
OUTPUT CURRENT ADJUSTMENT: PIN 12 (IDRIVE)						
I_{refSP}	spindle pre-driver reference current	R_{IDRIVE} = 120 kΩ; note 7	20.6	21.4	22.2	µA
Spindle: PWM						
SPINDLE SENSE AMPLIFIER: PINS 13 AND 14 (SPINSENSEH AND SPINSENSEL)						
ΔV_i	differential input voltage		0	–	1.84	V
I_{sense+}	positive input sense current		–60	–51	–42	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SISENS: PIN 15						
ΔV_o	output voltage shift		1.38	1.43	1.48	V
V_o	output voltage level		1.37	–	V_{DD} – 1.2	V
G_S	spindle sense amplifier gain		4.85	5.0	5.15	V/V
f_{UG}	unity gain bandwidth		1	–	–	MHz
SPINDLE CURRENT LOOP FILTER AMPLIFIER: PINS 18 AND 19 (SINTIN AND ISPIN)						
V_{iCM}	common mode input voltage		1.3	–	3.2	V
$V_{i(os)}$	input offset voltage		–3.0	–	+3.0	mV
I_i	input current		–1	–	0	µA
SICOMP: PIN 20						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	–	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = –0.6 mA	3.5	–	–	V
SR	slew rate		0.5	0.9	1.5	V/µs
f_{UG}	unity gain bandwidth		1	–	–	MHz
SPINDLE PWM COMPARATORS: PINS 22 AND 23 (CSS1 AND CSS2)						
V_{dc}	discharge clamp voltage	$I_{CSS1,2}$ = 0.5 mA	–	–	0.45	V
$I_{sink(d)}$	sink current	for normal CSS1 and CSS2 discharge; R_{Iref} = 120 kΩ	20.2	21.0	21.8	µA
$I_{sink(s)}$	sink current	for CSS1 and CSS2 short	1	–	–	mA
ANALOG SWITCHES: PIN 21 (RPOS)						
R_{Son}	switch-on resistance		150	250	400	Ω
R_{Soff}	switch-off resistance		10	–	–	MΩ
SAWTOOTH OSCILLATOR: PIN 24 (STOSC)						
V_{SUL}	voltage swing upper limit		2.9	3.0	3.1	V
V_{SLL}	voltage swing lower limit	static test	0.53	0.55	0.57	V
I_{source}	source current	note 8	–44.4	–42.8	–41.2	µA
I_{sink}	sink current	note 9	500	800	1100	µA
Voice coil motor driver						
VCM PREAMPLIFIERS: PINS 41 AND 40 (V_{CMIN1} AND V_{CMIN2})						
I_i	input current		–10	–	+10	µA
$V_{i(os)}$	input offset voltage		–6	–	+6	mV
f_{UG}	unity gain bandwidth		–	3	–	MHz
G_{RSon}	gain switch-on resistance	VGAINSEL = 1	–	–	60	Ω
G_{RSoff}	gain switch-off resistance	VGAINSEL = 0	10	–	–	MΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VCM DRIVER AMPLIFIERS: PINS 44 AND 36 (V_{CM+} AND V_{CM-})						
t_{COD}	cross-over switch time		–	2	5	µs
G_{vSD}	slave driver voltage gain		1.12	1.15	1.18	V/V
V_{OD}	output drop voltage including bond wires and leads	I_o = 1 A; T_j = 25 °C	–	–	0.65	V
		I_o = 0.2 A	–	–	0.45	V
		I_o = 1 A; T_j = 150 °C	–	–	1.1	V
t_{RFS}	recovery time from saturation		–	–	100	µs
SR	output slew rate		1.4	2.0	–	V/µs
f_{UG}	unity gain bandwidth		1.5	3	–	MHz
V_{park}	park voltage	over full temperature range	0.9	1.2	1.4	V
VCM SENSE AMPLIFIER: PINS 43 AND 42 ($V_{CMSENSEL}$ AND $V_{CMSENSEH}$)						
V_I	input voltage range		–0.7	–	V_{DD} + 0.7	V
I_I	input current	common mode from 0 to 12 V	–60	–	+250	µA
$V_{CMSENSOUT}$: PIN 50						
V_{OSL}	LOW level output saturation voltage	I_{OL} = 0.4 mA		–	0.5	V
V_{OSH}	HIGH level output saturation voltage	I_{OH} = –0.4 mA	V_{DD} – 1.5	–	–	V
G_s	sense amplifier gain		4.85	5.0	5.15	V/V
f_{UG}	unity gain bandwidth		–	1	–	MHz
$V_{o(os)}$	output offset voltage	$V_{CMSENSEH}$ = 6 V; $V_{CMSENSEL}$ = 6 V	–23	–	+23	mV
G_{CM}	common mode gain		–	–	–50	dB
Latch drivers						
LATCHACTIV: PIN 53						
I_{source}	output source current	over full temperature range	–0.5	–	–	A
R_{DSon}	FET switch-on resistance	T_j = 25 °C; I_{source} = –0.5 A	–	–	1.2	Ω
$\Delta R_{DSon}/T$	FET switch-on resistance temperature variation		–	6.4	–	mΩ/°C
LATCHHOLD: PIN 52						
I_{source}	output source current		–0.1	–	–	A
V_{DO}	diode drop voltage	T_j = 25 °C, I_D = 1 mA	–	750	775	mV
ΔV_{DO}	diode drop voltage temperature variation		–	–2	–	mV/°C
R_{on}	total on-resistance	T_j = 25 °C	–	8	12	Ω
ΔR_{on}	total on-resistance temperature variation		–	40	–	mΩ/°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Uncommitted operational amplifier						
AMPIN– AND AMPIN+: PINS 30 AND 31						
$V_{i(os)}$	input offset voltage		–3.5	–	+3.5	mV
$I_{i(bias)}$	input bias current		–1	–	0	µA
V_{CM}	common mode voltage		0	–	V_{DD} – 1.6	V
AMPOUT: PIN 33						
G_{OL}	open loop gain		–	67	–	dB
f_{co}	cross-over frequency	C_L = 10 pF	–	1.5	–	MHz
PSRR	power supply rejection ratio		60	–	–	dB
V_{OH}	HIGH level output voltage	I_{OH} = –0.5 mA	V_{DDD} + 0.3	–	–	V
V_{OL}	LOW level output voltage	I_{OL} = 0.5 mA	–	–	0.3	V
SR	slew rate		–	1.0	–	V/µS
Brake delay						
BRAKEPOWER: PIN 47						
V_{NM}	normal mode voltage		V_{DD} – 0.85	–	–	V
I_{sink}	input sink current	prior to automatic brake; $V_{BRAKEPOWER}$ = 9 V	–	35	50	µA
		while braking; over full temperature range; $V_{BRAKEPOWER}$ = 6.5 V	–	0.6	2	µA
V_{BV}	brakepower voltage for proper brake operation		5.0	–	–	V
V_D	drop voltage between brake power and L1, L2 and L3	$V_{BRAKEPOWER}$ = 6.5 V	–	–	0.8	V
BRAKEDELAY: PIN 51						
V_{NM}	normal mode voltage		V_{DD} – 0.85	–	–	V
V_{trip}	trip level voltage for automatic brake	over full temperature range; note 10	1.4	1.7	2.0	V
I_{LI}	leakage current	over full temperature range	–200	–	+200	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power-on/power-off reset						
UNDER THRESHOLD COMPARATORS: PINS 29 AND 28 ($\overline{POR12}_{ADJ}$ AND $\overline{POR5}_{ADJ}$)						
$V_{\overline{PORTH5}}$	5 V threshold voltage for power-on/power-off detection		4.30	4.37	4.50	V
V_{DDDhys}	hysteresis on V_{DDD} comparator		30	55	80	mV
$V_{\overline{PORTH12}}$	12 V threshold voltage for power-on/power-off detection		10.25	10.4	10.75	V
V_{DDhys}	hysteresis on V_{DD} comparator		60	95	130	mV
$R_{\overline{POR5}low}$	$\overline{POR5}_{ADJ}$ lower resistance	T_j = 25 °C	25340	28800	32260	Ω
$\Delta R_{\overline{POR5}low}$	$\overline{POR5}_{ADJ}$ lower resistance temperature variation		–	66	–	Ω/°C
$R_{Rup/Rlo}$	$\overline{POR5}_{ADJ}$ resistance ratio	over full temperature range	0.715	0.725	0.735	–
$R_{\overline{POR12}low}$	$\overline{POR12}_{ADJ}$ lower resistance	T_j = 25 °C	10560	12000	13440	Ω
$\Delta R_{\overline{POR12}low}$	$\overline{POR12}_{ADJ}$ lower resistance temperature variation		–	27	–	Ω/°C
$R_{Rup/Rlo}$	$\overline{POR12}_{ADJ}$ resistance ratio	over full temperature range	3.07	3.11	3.15	–
POWER-ON/POWER-OFF DELAY GENERATOR: PIN 26 ($\overline{POR}_{DELAY}$)						
I_{source}	source current		–2.4	–2.2	–1.8	μA
V_{HT}	RESET output threshold voltage	note 11	2.51	2.57	2.63	V
V_{LT}	LOW threshold voltage		–	–	0.4	V
RESETP: PIN 34						
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	–	–	0.4	V
R_{pu}	pull up resistor	over full temperature range	6	10	14	kΩ
RESETA: PIN 35						
V_{OH}	HIGH level output voltage	I_{OH} = –1.5 mA	V_{DDD} – 0.7	–	–	V
V_{OL}	LOW level output voltage	I_{OL} = 3 mA		–	0.4	V
Digital control						
CLOCK: PIN 58						
f_{clk}	clock frequency		–	–	12	MHz
δ	duty factor		40	50	60	%
FG: PIN 57						
V_{OH}	HIGH level output voltage	I_{OH} = –0.15 mA	V_{DDD} – 0.7	–	–	V
V_{OL}	LOW level output voltage	I_{OL} = 0.10 mA	–	–	0.4	V

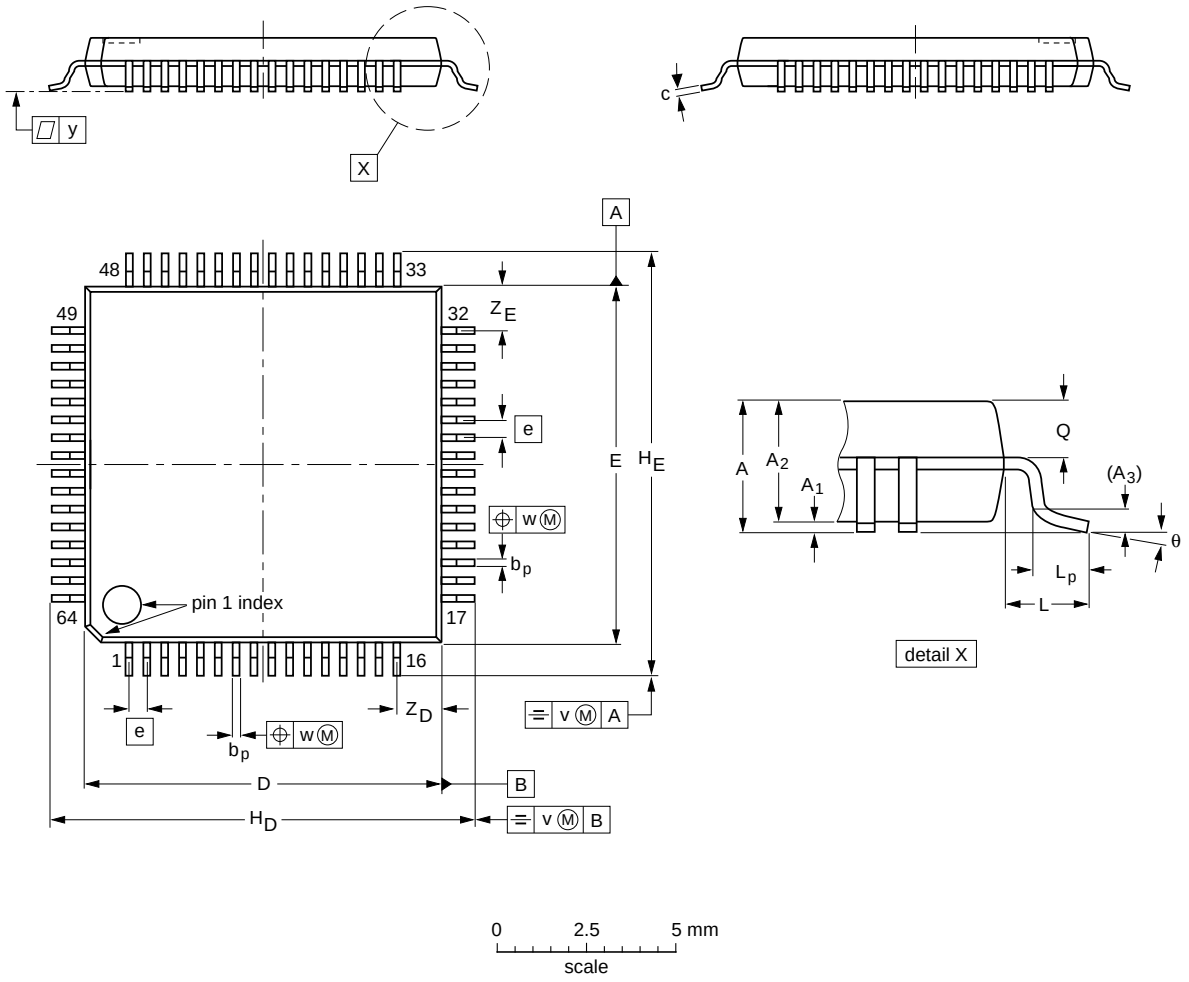
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial port						
SENABLE: PIN 61						
t_{su}	set-up time	with respect to the rising edge	46	–	–	ns
t_h	hold time		19	–	–	ns
t_{pm}	time between 2 serial port commands	t_{IC} = internal clock cycle; note 12	$2t_{IC}$	–	–	µs
SDATA: PIN 59						
t_{su}	set-up time	with respect to the rising edge	22	–	–	ns
t_h	hold time		20	–	–	ns
SCLOCK: PIN 60						
f_{SCL}	clock frequency		–	–	10	MHz
δ	duty factor		30	50	70	%

Notes

1. $I_{ref} = \frac{V_{ref(o)}}{R_{Iref}}$
2. Corresponds to an averaged variation of 7 mV/°C.
3. Including the $V_{CMSENSE}$ amplifier input current.
4. Extended voltages are allowed if series resistors are used (see Fig.1).
5. The gain between the pre-driver output current and the IDRIVE current is typically; lower source = 35, upper source = 50, lower sink = 75 and upper sink = 80.
6. Typical value for external FET such as PHN210.
7. $II_{SPREF} = \frac{V_{ref(o)}}{R_{IDRIVE}}$
8. $II_{source} = 2 \times \frac{V_{ref(o)}}{R_{Iref}}$
9. Valid if the STOSC capacitance is in the nominal range of 150 to 700 pF.
10. $t_{BRAKEDELAY} \approx 2RC$.
11. $t_{\overline{PORDELAY}} \approx C_{\overline{PORDELAY}}$, with $C_{\overline{PORDELAY}}$ in µF.
12. Master clock (pin 58) must be running (1 cycle = T_{ec}) – $t_{IC} = T_{ec}$x (prescaler ratio).

PACKAGE OUTLINE

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT314-2						~~94-01-07~~ 95-12-19

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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NOTES

NOTES

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Printed in The Netherlands

397021/1200/01/pp28 Date of release: 1996 May 06
Document order number: 9397 750 00823

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