

Features

- 32768 x 8 bit static CMOS RAM
- 35 and 55 ns Access Time
- Common data inputs and data outputs
- Three-state outputs
- Typ. operating supply current
 - 35 ns: 45 mA
 - 55 ns: 30 mA
- Standby current < 40 μ A at 125 $^{\circ}$ C
- TTL/CMOS-compatible
- Power supply voltage 2.5 - 3.6 V
- Operating temperature range
 - 40 $^{\circ}$ C to 85 $^{\circ}$ C
 - 40 $^{\circ}$ C to 125 $^{\circ}$ C
- QS 9000 Quality Standard
- ESD protection > 2000 V (MIL STD 883C M3015.7)
- Latch-up immunity >100 mA
- Package: SOP28 (300/330 mil)

Description

The UL62H256A is a static RAM manufactured using a CMOS process technology with the following operating modes:

- Read
- Write
- Standby
- Data Retention

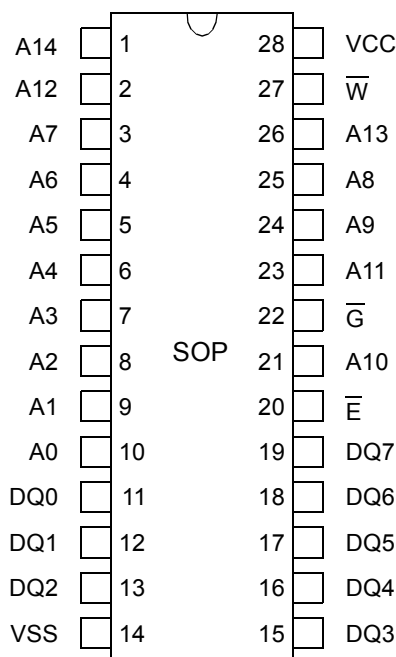
The memory array is based on a 6-Transistor cell.

The circuit is activated by the falling edge of \overline{E} . The address and control inputs open simultaneously. According to the information of \overline{W} and \overline{G} , the data inputs, or outputs, are active. In a Read cycle, the data outputs are activated by the falling edge of \overline{G} , afterwards the data word will be available at the outputs DQ0-DQ7. After the address change, the data outputs

go High-Z until the new information is available. The data outputs have no preferred state. The Read cycle is finished by the falling edge of \overline{W} , or by the rising edge of \overline{E} , respectively.

Data retention is guaranteed down to 2 V. With the exception of \overline{E} , all inputs consist of NOR gates, so that no pull-up/pull-down resistors are required.

Pin Configuration



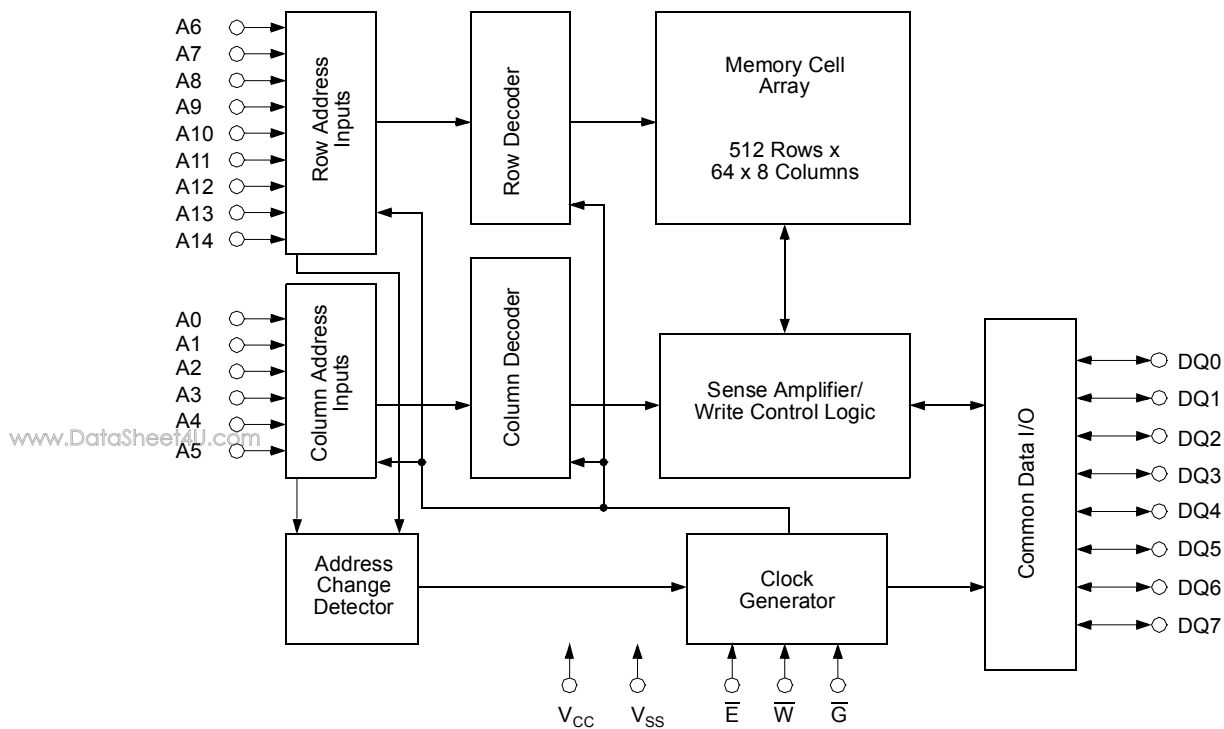
Top View

Pin Description

Signal Name	Signal Description
A0 - A14	Address Inputs
DQ0 - DQ7	Data In/Out
\overline{E}	Chip Enable
\overline{G}	Output Enable
\overline{W}	Write Enable
VCC	Power Supply Voltage
VSS	Ground

UL62H256A

Block Diagram



Truth Table

Operating Mode	\bar{E}	\bar{W}	\bar{G}	DQ0 - DQ7
Standby/not selected	H	*	*	High-Z
Internal Read	L	H	H	High-Z
Read	L	H	L	Data Outputs Low-Z
Write	L	L	*	Data Inputs High-Z

* H or L

Characteristics

All voltages are referenced to $V_{SS} = 0\text{ V}$ (ground).

All characteristics are valid in the power supply voltage range and in the operating temperature range specified.

Dynamic measurements are based on a rise and fall time of $\leq 5\text{ ns}$, measured between 10 % and 90 % of V_I , as well as input levels of $V_{IL} = 0.2\text{ V}$ and $V_{IH} = 2.8\text{ V}$. The timing reference level of all input and output signals is 1.5 V, with the exception of the t_{dis} -times and t_{en} -times, in which cases transition is measured $\pm 200\text{ mV}$ from steady-state voltage.

Absolute Maximum Ratings ^a	Symbol	Min.	Max.	Unit
Power Supply Voltage	V_{CC}	-0.3	4.6	V
Input Voltage	V_I	-0.5	$V_{CC} + 0.5$ ^b	V
Output Voltage	V_O	-0.5	$V_{CC} + 0.5$ ^b	V
Power Dissipation	P_D	-	1	W
Operating Temperature	T_a	-40 -40	85 125	°C
Storage Temperature	T_{stg}	-65	150	°C
Output Short-Circuit Current at $V_{CC} = 3.3\text{ V}$ and $V_O = 0\text{ V}$ ^c	$ I_{OS} $		100	mA

^a Stresses greater than those listed under „Absolute Maximum Ratings“ may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

^b Maximum voltage is 4.6 V

^c Not more than 1 output should be shorted at the same time. Duration of the short circuit should not exceed 30 s.

Recommended Operating Conditions	Symbol	Conditions	Min.	Max.	Unit
Power Supply Voltage	V_{CC}		2.5	3.6	V
Input Low Voltage ^d	V_{IL}		-0.3	0.5	V
Input High Voltage	V_{IH}		2.0	$V_{CC} + 0.3$	V

^d -2 V at Pulse Width 30 ns

UL62H256A

Electrical Characteristics	Symbol	Conditions	Min.	Max.	Unit
Supply Current - Operating Mode	$I_{CC(OP)}$	$V_{CC} = 3.6\text{ V}$ $V_{IL} = 0.5\text{ V}$ $V_{IH} = 2.0\text{ V}$ $t_{cW} = 35\text{ ns}$ $t_{cW} = 55\text{ ns}$		90 70	mA mA
Supply Current - Standby Mode (CMOS level)	$I_{CC(SB)}$	$V_{CC} = 3.6\text{ V}$ $V_{\bar{E}} = V_{CC} - 0.2\text{ V}$ K-Type A-Type		10 40	μA μA
Supply Current - Standby Mode (TTL level)	$I_{CC(SB)1}$	$V_{CC} = 3.6\text{ V}$ $V_{\bar{E}} = 2.0\text{ V}$ K-Type A-Type		10 20	mA mA
Output High Voltage	V_{OH}	$V_{CC} = 2.5\text{ V}$ $I_{OH} = -1.0\text{ mA}$	2.2		V
Output Low Voltage	V_{OL}	$V_{CC} = 2.5\text{ V}$ $I_{OL} = 2.1\text{ mA}$		0.4	V
Input High Leakage Current	I_{IH}	$V_{CC} = 3.6\text{ V}$ $V_{IH} = 3.6\text{ V}$		2	μA
Input Low Leakage Current	I_{IL}	$V_{CC} = 3.6\text{ V}$ $V_{IL} = 0\text{ V}$	-2		μA
Output High Current	I_{OH}	$V_{CC} = 2.5\text{ V}$ $V_{OH} = 2.2\text{ V}$		-1.0	mA
Output Low Current	I_{OL}	$V_{CC} = 2.5\text{ V}$ $V_{OL} = 0.4\text{ V}$	2.1		mA
Output Leakage Current High at Three-State Outputs	I_{OHZ}	$V_{CC} = 3.6\text{ V}$ $V_{OH} = 3.6\text{ V}$		2	μA
Low at Three-State Outputs	I_{OLZ}	$V_{CC} = 3.6\text{ V}$ $V_{OL} = 0\text{ V}$	-2		μA

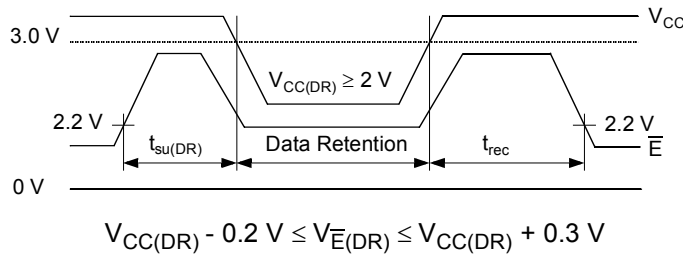
Switching Characteristics Read Cycle	Symbol		35		55		Unit
	Alt.	IEC	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	t_{cR}	35		55		ns
Address Access Time to Data Valid	t_{AA}	$t_{a(A)}$		35		55	ns
Chip Enable Access Time to Data Valid	t_{ACE}	$t_{a(E)}$		35		55	ns
\overline{G} LOW to Data Valid	t_{OE}	$t_{a(G)}$		15		25	ns
\overline{E} HIGH to Output in High-Z	t_{HZCE}	$t_{dis(E)}$		12		15	ns
\overline{G} HIGH to Output in High-Z	t_{HZOE}	$t_{dis(G)}$		12		15	ns
\overline{E} LOW to Output in Low-Z	t_{LZCE}	$t_{en(E)}$	3		3		ns
\overline{G} LOW to Output in Low-Z	t_{LZOE}	$t_{en(G)}$	0		0		ns
Output Hold Time from Address Change	t_{OH}	$t_{v(A)}$	3		3		ns
\overline{E} LOW to Power-Up Time	t_{PU}		0		0		ns
\overline{E} HIGH to Power-Down Time	t_{PD}			35		55	ns

Switching Characteristics Write Cycle	Symbol		35		55		Unit
	Alt.	IEC	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	t_{cW}	35		55		ns
Write Pulse Width	t_{WP}	$t_{w(W)}$	20		35		ns
Write Setup Time	t_{WP}	$t_{su(W)}$	20		35		ns
Address Setup Time	t_{AS}	$t_{su(A)}$	0		0		ns
Address Valid to End of Write	t_{AW}	$t_{su(A-WH)}$	25		40		ns
Chip Enable Setup Time	t_{CW}	$t_{su(E)}$	25		40		ns
Pulse Width Chip Enable to End of Write	t_{CW}	$t_{w(E)}$	25		40		ns
Data Setup Time	t_{DS}	$t_{su(D)}$	15		25		ns
Data Hold Time	t_{DH}	$t_{h(D)}$	0		0		ns
Address Hold from End of Write	t_{AH}	$t_{h(A)}$	0		0		ns
\overline{W} LOW to Output in High-Z	t_{HZWE}	$t_{dis(W)}$		15		20	ns
\overline{G} HIGH to Output in High-Z	t_{HZOE}	$t_{dis(G)}$		12		15	ns
\overline{W} HIGH to Output in Low-Z	t_{LZWE}	$t_{en(W)}$	0		0		ns
\overline{G} LOW to Output in Low-Z	t_{LZOE}	$t_{en(G)}$	0		0		ns

UL62H256A

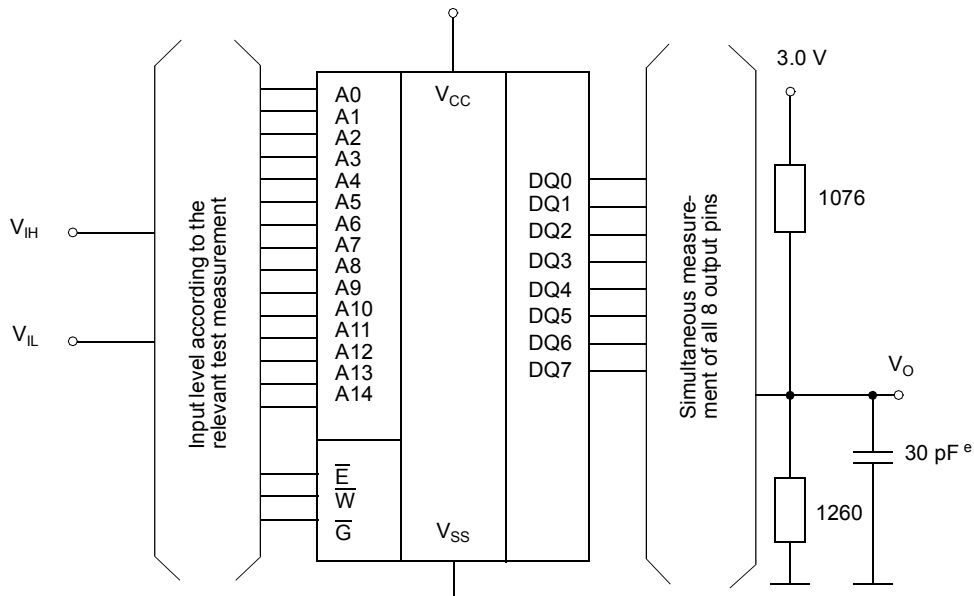
Data Retention Mode

\bar{E} - controlled



Data Retention Characteristics	Symbol		Conditions	Min.	Typ.	Max.	Unit
	Alt.	IEC					
Data Retention Supply Voltage		$V_{CC(DR)}$		2			V
Data Retention Supply Current		$I_{CC(DR)}$	$V_{CC(DR)} = 2\text{V}$ $V_{\bar{E}} = V_{CC(DR)} - 0.2\text{V}$ K-Type A-Type			5 20	μA μA
Data Retention Setup Time	t_{CDR}	$t_{SU(DR)}$	See Data Retention Waveforms (above)	0			ns
Operating Recovery Time	t_R	t_{REC}		t_{CR}			ns

Test Configuration for Functional Check



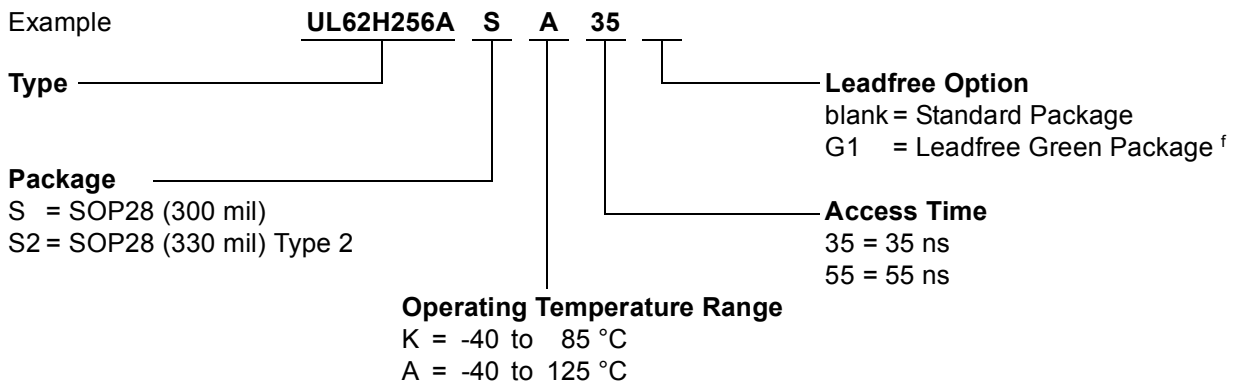
^e In measurement of $t_{dis(E)}$, $t_{dis(W)}$, $t_{en(E)}$, $t_{en(W)}$, $t_{en(G)}$ the capacitance is 5 pF.

Capacitance	Conditions	Symbol	Min.	Max.	Unit
Input Capacitance	$V_{CC} = 3.3\text{ V}$ $V_I = V_{SS}$	C_i		7	pF
Output Capacitance	$f = 1\text{ MHz}$ $T_a = 25\text{ }^\circ\text{C}$	C_o		7	pF

All pins not under test must be connected with ground by capacitors.

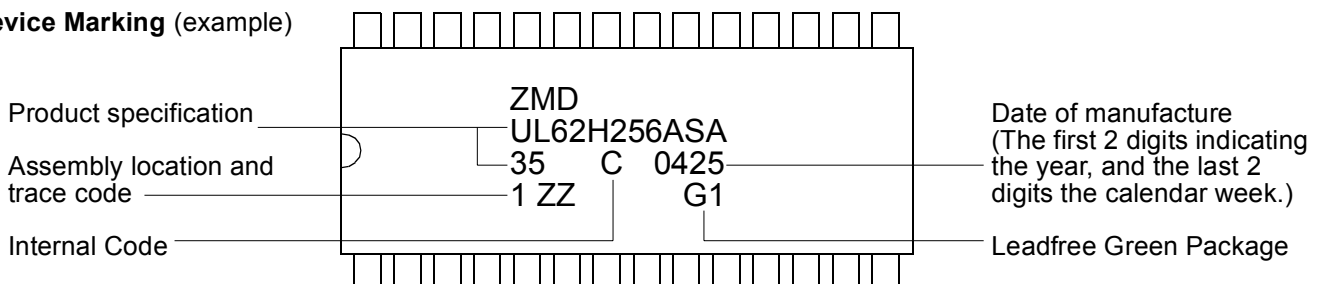
www.DataSheet4U.com

Ordering Code



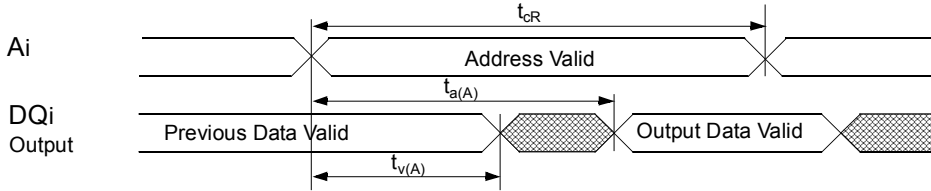
^f on special request

Device Marking (example)



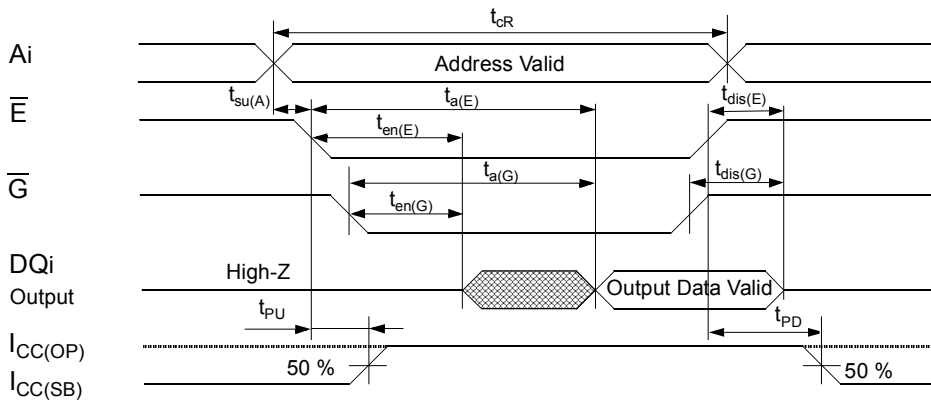
UL62H256A

Read Cycle 1: A_i -controlled (during Read Cycle : $\bar{E} = \bar{G} = V_{IL}, \bar{W} = V_{IH}$)

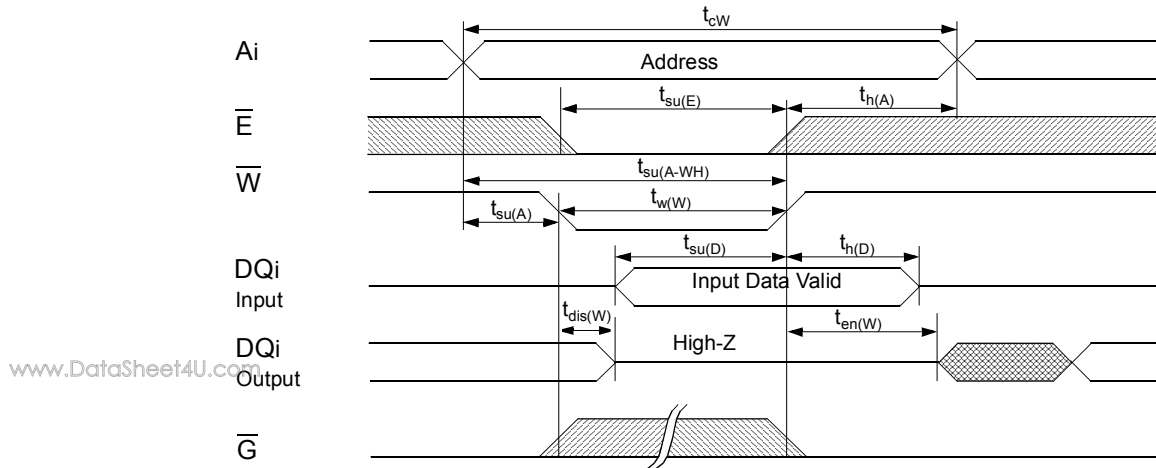


www.DataSheet4U.com

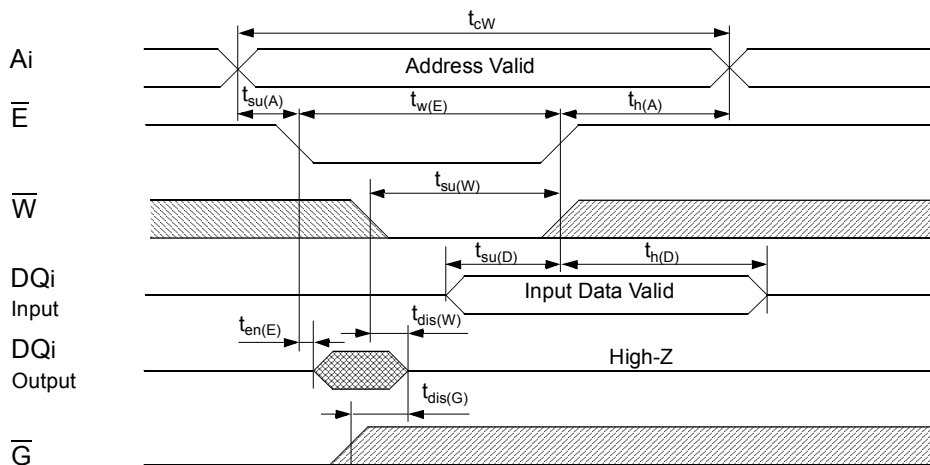
Read Cycle 2: \bar{G} -, \bar{E} -controlled (during Read Cycle: $\bar{W} = V_{IH}$)



Write Cycle1: \overline{W} -controlled



Write Cycle 2: \overline{E} -controlled



undefined  L- to H-level  H- to L-level 

The information describes the type of component and shall not be considered as assured characteristics. Terms of delivery and rights to change design reserved.

LIFE SUPPORT POLICY

ZMD products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the ZMD product could create a situation where personal injury or death may occur. Components used in life-support devices or systems must be expressly authorized by ZMD for such purpose.

LIMITED WARRANTY

The information in this document has been carefully checked and is believed to be reliable. However Zentrum Mikroelektronik Dresden AG (ZMD) makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon it. The information in this document describes the type of component and shall not be considered as assured characteristics.

ZMD does not guarantee that the use of any information contained herein will not infringe upon the patent, trademark, copyright, mask work right or other rights of third parties, and no patent or licence is implied hereby. This document does not in any way extent ZMD's warranty on any product beyond that set forth in its standard terms and conditions of sale.

ZMD reserves terms of delivery and reserves the right to make changes in the products or specifications, or both, presented in this publication at any time and without notice.