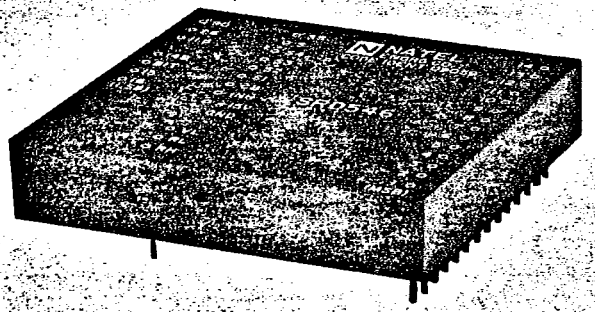
NATEL SRD546

Synchro/Resolver-to-Digital Converter Many Pin-Programmable Features

Features

- **16 bit resolution**
- **1 arc-minute accuracy**
- **Built-In-Test**
- **Continuous tracking even during data transfer**
  (inhibit does not interrupt tracking)
- **Pin-programmable for all standard voltages**
- **Internal reference synthesizer**
  (for improved dynamic accuracy)
- **Automatic gain compensation**
  (allows 2:1 signal variation)
- **Pin-programmable for synchro or resolver inputs**
- **Pin-programmable for 14-bit output**
- **2880°/sec tracking rate in 14-bit mode**
- **TTL and CMOS compatible**
- **Signal and reference transformer isolation**



- **MIL-STD 883B processing available**
- **Priced at $695/USA price**
  (SRD546-1S)

Applications

Testing Digital to Synchro/Resolver converters
Servo systems
Ordnance control
Navigation and collision avoidance systems
Machine tool control systems

Description

Model SRD546 is packaged in a small module, offering flexibility with many programmable features and is primarily designed to provide a low-cost alternative for testing digital-to-synchro/resolver converters. The 546 is pin-programmable for both synchro and resolver inputs, pin-programmable for 11.8, 26 or 90 V-rms line-to-line signal voltages and operates from a reference voltage of 10 to 130 V-rms. Both signal and reference inputs are transformer isolated and provide high common mode rejection. The digital output is compatible with both TTL and CMOS and is programmable for CMOS output levels up to main-supply (+15 V). In addition the converter offers a high accuracy of 1 arc minute.

Model 546 is a Type II tracking converter with zero velocity lag error. A programming pin is available to increase the velocity tracking of the converter to 8 rps (2880°/sec) by operating it in the 14-bit mode. An internal reference synthesizer permits improved dynamic accuracy by reducing the effects of "speed voltages," at high rotational speeds. The accuracy of the converter is maintained with signal-to-reference phase shifts up to ±45 degrees.

A built-in-test (BIT) feature provides a logic one when the tracking error exceeds ±1°. An AGC (automatic-gain-compensation) circuit is incorporated in the converter design allowing signal voltage variations of ±30% without any degradation in accuracy or change in converter hysteresis.

The output interface of the converter is facilitated by providing a Converter Busy signal. In addition the converter can be inhibited on command by using the INH input for static or dynamic read out.

Requiring only a single +15 V-dc main power supply for its operation, the converter maintains both static and dynamic accuracy over a wide range of power supply variations. The digital output voltage levels can be controlled independently by a logic voltage input V_L. The logic supply voltage V_L can range from 3.0 V-dc to the main power supply voltage. At 5 V-dc logic supply, the output is TTL compatible and can drive 4 standard TTL loads.

Although pin compatible converters are available, Natel's Model SRD546 offers superior dynamic performance, while maintaining its high accuracy over wide (±30%) variations of input signal levels. An additional feature available in the SRD546 is a holding register which allows the user to inhibit the output without interrupting the converter loop.

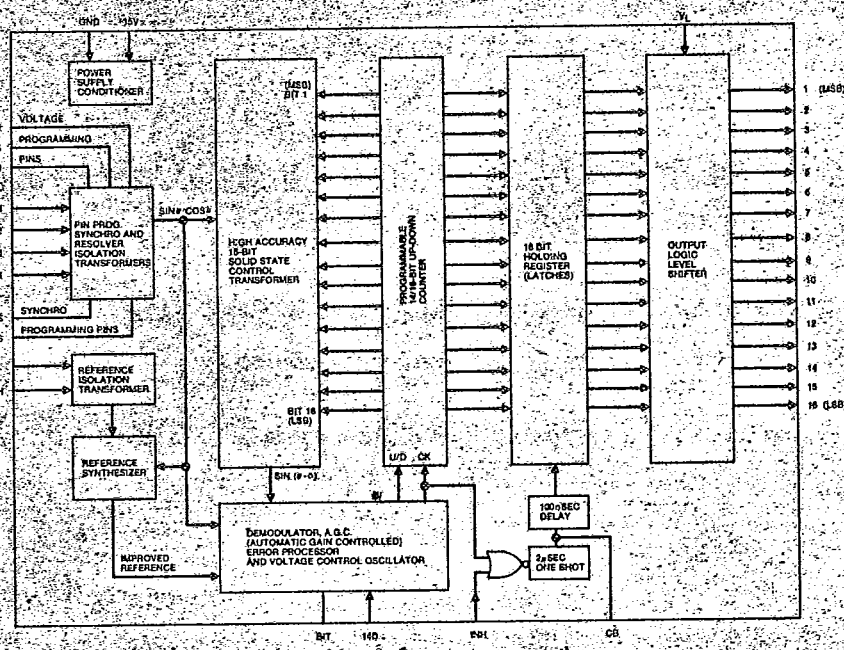


FIGURE 1 SRD546 Block Diagram

Theory of Operation

The operation of the Model SRD546 is illustrated in the functional block diagram of figure 1. The SRD546 is a high gain Type II tracking converter exhibiting zero error for a constant velocity input. The basic conversion process consists of continuously comparing the digital output angle (ϕ) and the Synchro (or Resolver) input angle (θ). An up-down counter, containing the feed-back angle, is changed (increased or decreased) until the feed-back angle equals the input angle. Once synchronized, the output angle tracks the input angle continuously and the data is always fresh and always available (except during transitions). The input signal conditioner accepts either a Synchro or Resolver input and converts it into low level signals $\sin\theta$ and $\cos\theta$. The feed-back loop consisting of an error processor, voltage-controlled oscillator and a 16-bit up-down counter produces a 16-bit digital angle (ϕ). The input and feed-back signals are combined in a solid state control transformer to obtain an error voltage, (e) according to the following trigonometic identity:

$$\text{"e"} = \sin(\theta-\phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

When the error voltage goes to null, $\sin(\theta-\phi)$ is zero, which makes the angle θ equal to the angle ϕ. Thus, the digital output represents the input shaft angle. The error voltage is an ac signal proportional to the instantaneous error between the input angle and the feed-back angle. This error voltage is synchronously demodulated with the "synthesized reference" signal. The demodulated output is a dc signal proportional to the tracking error ($\theta-\phi$). The dc error is integrated to produce a voltage proportional to the converter's tracking velocity. The velocity signal is the control input to a voltage-controlled oscillator. The VCO output changes the up-down counter, which contains the feed back angle, ϕ. The up-down counter functions as the second integrator in the tracking loop. The output of the counter is supplied to a holding register followed by logic level shifters for output interface compatibility.

Built-in-Test (BIT)

A BIT signal provides an over-velocity or fault indication output signal. The error voltage of the converter is monitored continuously, and when the tracking error exceeds 1 degree (over-velocity or failure), a logic "1" signal is generated to indicate invalid data. Under normal operation the BIT output is at logic "0". Possible conditions that will cause the BIT output to show fault indication are:

- Power-turn-on --- BIT output will return to logic "0" when converter synchronizes to correct input angle ±1°.
- Step-input --- Instantaneous input changes greater than ±1° until the converter synchronizes.
- Synchro malfunction --- one or more open stator lines or a missing reference input.
- Converter malfunction --- any converter failure which prevents synchronization to the input angle.

From above discussion it is apparent that the BIT output not only serves to self-test the converter but also provides and indication of the operation of the synchro transmission system as well.

Input Signal Programming

Model SRD546 offers user flexibility of either the synchro or resolver input and, in addition, offers voltage-level programming for both synchro and resolver inputs. For synchro inputs pin S is connected to pin SS, and input signal is connected to pins S1, S2, S3 (leave S4 unconnected). For resolver inputs, pins S and SS are left unconnected and input signal is connected to pins S1, S2, S3, S4. For input signal voltage level programming, the connections are shown in the table below.

VOLTAGE LEVEL	PIN 11.8	PIN 26	PIN 90
11.8 V-rms L-L	N.C.	GND	GND
26 V-rms L-L	GND	N.C.	GND
90 V-rms L-L	GND	GND	N.C.

Automatic Gain Compensation

An AGC circuit incorporated withing the SRD546 allows the converter to maintain its high accuracy over a wider range (2 to 1) of signal amplitudes than previously possible for synchro-to-digital converters. The hysteresis of the converter is kept constant over this range.

In theory, the accuracy of an S/D or R/D converter is not affected by signal amplitude variations because the conversion process is ratiometric and therefore not dependent on the magnitude of the input. In practice, however, the necessity of providing hysteresis to prevent hunting or jitter in the least significant bit (LSB) introduces a controlled inaccuracy in the converter. In most analog-to-digital converters ≥0.5LSB hysteresis is introduced. In synchro-to-digital converters this has to be increased to approximately 0.9LSB as the error voltage is a non-linear function [e=K sin $(\theta-\phi)$] of the input shaft angle. Previous converters derived this hysteresis level as a fixed threshold at nominal input signal amplitude. Thus the conversion accuracy would vary directly with synchro input signal amplitude . . . becoming degraded for the lower amplitudes and creating excessive jitter for higher amplitudes.

The SRD546 monitors the input signals continuously and effectively modifies the gain of the error voltage as a function of input signal amplitude.

Reference Synthesizer

To maintain the highest accuracy under both static and dynamic conditions, the SRD546 utilizes a monolithic "reference synthesizer" to correct for a phase difference between the signal and reference inputs of up to ±45°.

Conventional tracking synchro/resolver-to-digital converters use a phase sensitive demodulator to detect the phase and amplitude of the error voltage, sin $(\theta-\phi)$. A phase sensitive demodulation rejects any resultant quadrature signal (signal 90° out of phase) only if the synchro input and its reference are exactly in phase. A quadrature signal results from dynamic synchro operation that is referred to as the "speed voltage," and is proportional to the shaft rotational speed. Although most converter specifications discuss dynamic lag error, and ignore the error due to "speed voltages," this error is very real. For a 400 Hz synchro with a 10° phase shift rotating at 8 rps (2880°/sec), the dynamic error due to speed voltage would be 0.2 degree or 12 arc-minutes!

Natel's Model 546 greatly reduces the effects of this error by creating a synthetic reference. The sine and cosine voltages from the signal conditioner are combined to obtain an in-phase internal reference. Together with the external reference voltage (to determine phase) this synthesized reference is used for demodulating the error voltage.

Resolution Programming

To allow speed-vs-resolution tradeoff, the SRD546 can be programmed for either 14-bit or 16-bit resolution. This programming function is accomplished by control 14B. An open pin at 14B makes the converter operate in the 14-bit mode (bits 15 and 16 are forced to logic "low"). A logic "low" or ground at pin 14B allows the converter to operate in the 16-bit mode. The loop gain of the converter is automatically compensated in both 14-bit and 16-bit modes, providing stable operation in both modes.

Although resolution is reduced in the 14-bit mode, the tracking speed and the acceleration constant are increased by a factor of 4.

Improving Settling Time (Without Loss of Resolution)

Connecting the BIT output to 14B provides an interesting method for reducing settling time while maintaining 16-bit resolution during tracking. At power turn-on or for a large step input, the BIT output would be at logic "high," forcing the converter to operate in the 14-bit mode (x4 tracking rate). As soon as the output is synchronized to within ±1° of the input angle, the converter automatically reverts to 16-bit mode.

This technique, also, can be used in applications where input speeds are variable and the converter must not lose synchronization at high-speed shaft rotations.

Output Data Transfer

Output data transfer from the SRD546 is shown in figure 2. The data is continuously available at the output pins, but it may be changing at any specific time. In order not to transfer data during transition times, the inhibit function should be used. There are two methods available for transferring data. One method is to monitor the CB output and transfer data at the trailing edge of the CB pulse. The preferred method is on command signal. Set the INH input to logic "high" for not less than 400ns. When the INH goes "low", a 1.5μs busy pulse is generated. The 16-bits of output data may then be transferred on the trailing edge of CB output.

Note that applying inhibit to the converter will latch the data in the 16-bit holding register (and will prevent it from being updated) . . . but will not interfere with the continuous operation of the conversion process.

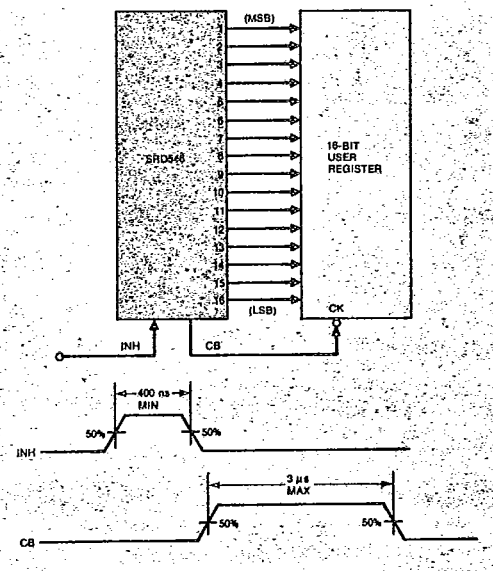


FIGURE 2 Circuit Configuration for Output Data Transfer

Specifications

PARAMETER	VALUE	REMARKS
Digital Output Resolution	16-bits (0.33 arc-minute)	Pin-progammable for 14-bits for higher tracking speed
Accuracy	± 2.5 arc-minutes ± 1.0 arc-minute	14-bit mode 16-bit mode
Reference Input		Transformer Isolated
Voltage	10 to 130 V-rms	
Frequency	360 to 1000 Hz	
Input Impedance	500 kΩ	
Breakdown Voltage	500 V minimum to ground	
Common Mode Range	± 300 V peak maximum	dc plus recurrent ac peak
Synchro/Resolver Inputs		Transformer Isolated
Input Voltages (Line-to-Line) (pin-programmable)	11.8 V-rms ± 30% 26 V-rms ± 30% 90 V-rms ± 30%	Accuracy of the converter is maintained with ± 30% variation in signal voltages
Input Impedance	500 kΩ	
Breakdown Voltage	500 V minimum to ground	
Common Mode Range	± 300 V peak maximum	dc plus recurrent ac peak
Common Mode Rejection Ratio	70 dB minimum	dc to 1000 Hz
Harmonic Distortion	10% maximum	Without degradation in accuracy specification
Digital Inputs		
14B	GND Open	16-bit resolution 14-bit resolution
11.8, 26, 90	See table on page 2	Input L-L voltage programming pins
Inhibit Control (INH) Logic "0" Logic "1"	 -0.3 V-dc to 0.2 V_L 0.5 V_L to 1.0 V_L	30 kΩ minimum pull-up resistor to V_L Digital output follows analog input signals Output data latched in holding register
Digital Outputs		
Logic type	TTL/CMOS Compatible	Depends on logic voltage (V_L)
Drive Capability		
(Bits 1-16, CB, BIT)	4 Standard TTL loads (6.4 mA sink current)	For 5 V-dc logic voltage
Data bits (1-16)	Natural Binary Angle	Positive logic
CB	Logic "0" Logic "1" (1.5 μsec pulse for every LSB change)	Output angle not changing Output angle changing (Leading edge initiates output change)
BIT	Logic "0" Logic "1"	Digital output tracking analog input Fault indication (Tracking error ≥± 1° typical)
Dynamic Characteristics		Typical values unless otherwise specified
Maximum Tracking Rate (Error < ¼ LSB)	±8 rps (2880° per sec) minimum ± 2 rps (720° per sec) minimum	14-bit mode 16-bit mode
Maximum Acceleration	160,000°/sec² 40,000°/sec²	14-bit mode 16-bit mode
Acceleration for 1 LSB error	2,600°/sec² 160°/sec²	14-bit mode (1 LSB=0.022 degree) 16-bit mode (1 LSB=0.0055 degree)
Setting time to 1 LSB (for 179° step change)	100 msec 300 msec	14-bit mode (1 LSB=0.022 degree) 16-bit mode (1 LSB=0.0055 degree)
Setting time to 1 LSB (Small signal step < 1.4°)	10 msec 40 msec	14-bit mode (1 LSB=0.022 degree) 16-bit mode (1 LSB=0.0055 degree)

PARAMETER	VALUE	REMARKS
Reference synthesizer		
Phase-shift between Input signals and Input reference	± 45° Guaranteed ± 60° Typical	Without any degradation of converter accuracy
Power Supplies		Internal decoupling capacitors provided
Main Supply (+ 15 V) Voltage Current	11 V-dc to 17 V-dc 50 mA maximum, 30 mA typical	Typically +15 V-dc
Logic Voltage (V_L) Voltage Current	3.0 V-dc to Main Supply 1 mA maximum	5 V-dc for TTL compatible output (plus digital load at logic "high")
Physical Characteristics		Encapsulated module
Size Weight	3.48 x 3.12 x 0.82 inch (88.5 x 79.4 x 20.8 mm) 9 oz (255g) max	

Absolute Maximum Ratings

Signal Inputs ..... 200 V-rms L-L
Reference Input ..... 200 V-rms
Main Supply Voltage ..... +20 V-dc
Logic Supply Voltage (V_L) ..... +20 V-dc
Digital Inputs ..... -0.3 V-dc to V_L
Storage Temperature ..... -55°C to +125°C

Binary/Angular Resolution Table

BINARY BITS (N)	DEGREES/BIT	MINUTES/BIT	SECONDS/BIT	RADIANS OR MILLIRADIANS	ANGULAR MILS	RESOLUTION (2^N)
1	180.0	10800.0	648000.0	3.1415927	3200.0	2
2	90.0	5400.0	324000.0	1.5707963	1600.0	4
3	45.0	2700.0	162000.0	0.7853982	800.0	8
4	22.5	1350.0	81000.0	0.3926991	400.0	16
5	11.25	675.0	40500.0	0.1963495	200.0	32
6	5.625	337.5	20250.0	0.0981748	100.0	64
7	2.8125	168.75	10125.0	0.0490874	50.0	128
8	1.40625	84.375	5062.5	0.0245437	25.0	256
9	0.703125	42.1875	2531.25	12.27184 millirad.	12.5	512
10	0.3515625	21.09375	1265.625	6.13592	6.25	1024
11	0.1757813	10.546875	632.8125	3.06796	3.125	2048
12	0.0878906	5.273438	316.40625	1.53398	1.5625	4096
13	0.0439453	2.636719	158.20313	0.76699	0.78125	8192
14	0.0219727	1.318359	79.10156	0.38350	0.390625	16384
15	0.0109863	0.659180	39.55078	0.19175	0.1953125	32768
16	0.0054932	0.329590	19.77539	0.09587	0.0976563	65536
17	0.0027466	0.164795	9.88770	0.04794	0.0488281	131072
18	0.0013733	0.082397	4.94385	0.02397	0.0244141	262144
19	0.0006866	0.041199	2.47192	0.01198	0.0122070	524288
20	0.0003433	0.020599	1.23596	0.00598	0.0061035	1048576
21	0.0001717	0.010300	0.61798	0.00300	0.0030518	2097152
22	0.0000858	0.005150	0.30899	0.00150	0.0015259	4194304
23	0.0000429	0.002575	0.15450	0.00075	0.0007629	8388608
24	0.0000215	0.001287	0.07725	0.00037	0.0003815	16777216

1 RADIAN = 57.29578 DEGREES
1 ANGULAR MIL = 0.05625 DEGREE
1 ANGULAR MIL = 3.375 ARC-MINUTES
1 DEGREE = 0.01745 RADIAN
1 DEGREE = 17.45329 MILLIRADIAN
1 DEGREE = 17.77778 ANGULAR MILS

Pin Designations

+15 V	Main Power Supply Voltage (11 V-dc to 17 V-dc)
V_L	Logic Voltage 5 V-dc (For TTL compatible output) 3.0 V-dc to Main power supply voltage (For CMOS compatible output)
GND	Power Supply Ground Digital Ground
1-16	Parallel Output Data Bits - 1 is MSB = 180 degrees 16 is LSB = 0.0055 degree
S1, S2, S3, S4	Input Analog Signals Leave S4 unconnected for synchro-input
S, SS	Synchro Programming-pins - Synchro Input - connect S to SS Resolver Input - Leave S and SS unconnected
11.8, 26, 90	Input Voltage Programming-pins - For 11.8 V-rms input GND pins 26 and 90 (Leave Pin 11.8 unconnected) For 26 V-rms input GND pins 11.8 and 90 (Leave Pin 26 unconnected) For 90 V-rms input GND pins 11.8 and 26 (Leave Pin 90 unconnected)
RH, RL	Reference Voltage Input (10 to 130 V-rms)
INH	INH Function - A logic "high" freezes the digital angular output. Internal loop keeps tracking the analog input. For continuous output updating this pin must be connected to GND.

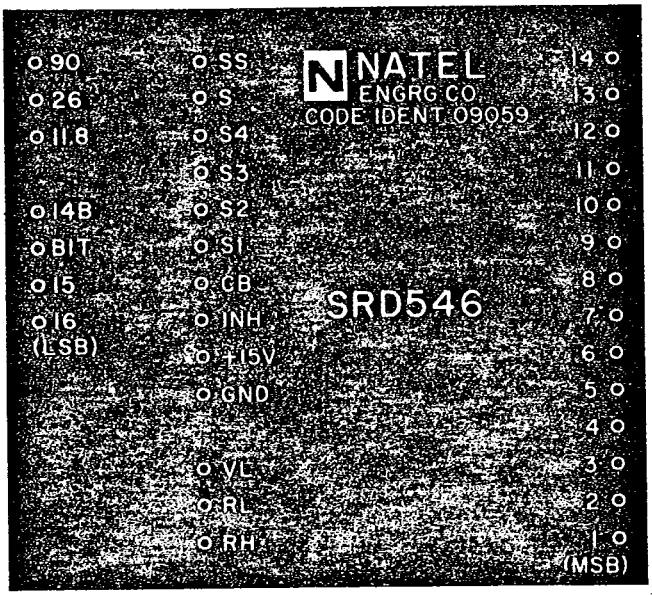


FIGURE 3 SRD546 Pin Assignments

CB	Converter Busy - A 1.5μs pulse which occurs during updating of the holding register. Output data can be transferred at the trailing edge of the CB pulse. When converter output is not changing CB is at logic "low."
BIT	Built-In-Test - A Logic "high" output indicates that output is not tracking the input analog signal within ±1°.
14B	Output Resolution Control - Allows 4 times tracking speed in 14 bit-mode. Logic "low" or ground = 16-bit output. Open or unconnected = 14-bit output; (Bits 15 and 16 will be at Logic "low")

Synchro/Resolver Connections and Phasing

The connections for synchro and resolver inputs are shown in figure 4. The input signals are transformer isolated. The isolation transformers can be pin-programmed to accept either synchro or resolver inputs. In addition the transformers can accept 11.8, 16 or 90 V-rms line-to-line input signal voltages by appropriate pin-programming (see input signal programming on page 2). Besides voltage programming, the isolation transformers perform two other functions. For both synchro and resolver format inputs, they serve as a precision attenuator reducing the amplitude of high level ac input signals to levels that can be processed by the converter. For a synchro input, the isolation transformers are connected as a Scott-T, which allows them to convert three-wire synchro information into resolver format (sin θ and cos θ) for further processing.

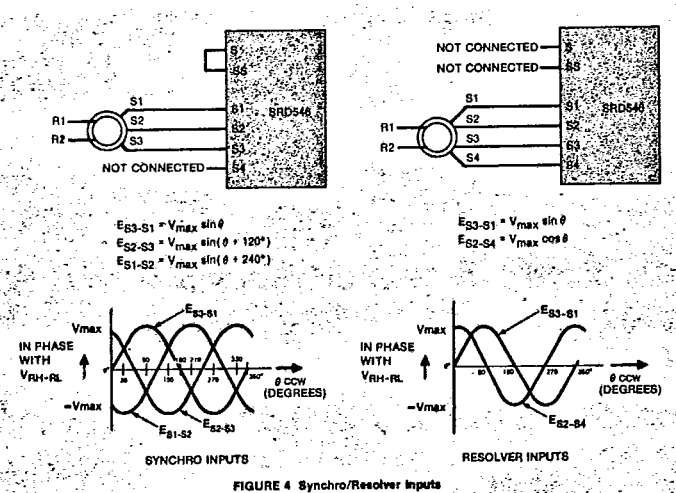


FIGURE 4 Synchro/Resolver Inputs

Dynamic Performance

The SRD546 design incorporates the proven Type II tracking design (KV=∞) and has been configured to provide superior dynamic performance independent of power supply voltage over the range of 11 V-dc to 17 V-dc.

The converter will track the input angles up to specified tracking rates (see specifications, pages 4 and 5) with no lag error. The acceleration constant (K_A) for the converter is 160,000°/sec². Both small and large signal response for the SRD546 are shown in figure 7.

The ***Large Signal*** transient response is dependent solely on the maximum velocity (ωmax) and the maximum acceleration (αmax) of which the converter is capable. The large signal parameters are defined in figure 5. The synchronizing time (t_{SYNC}) for large signals can be partitioned into three distinct intervals, Acceleration time (t_{ACC}) Slew time (t_{SLEW}) and Overshoot time (t_{OS}).

Acceleration time is the time interval from application of the step-input to the point at which the converter reaches its maximum velocity.

Slew time is the time interval from the point at which maximum velocity is obtained to the point at which the output angle is first equal to the input angle.

Overshoot time is the time interval from the point at which the converter output angle first equals the input angle (and applies constant acceleration in the opposite direction) to the point at which the output angle again reaches the input angle.

At the end of overshoot time, the small signal response becomes dominant and the converter will settle to the final value according to its small signal transient response function.

The ***Small Signal*** settling time (t_S) is specified for step inputs of less than 1.4 degrees. For small signal steps, the settling time is a function of the transient response of the converter. The transfer functions in both 14-bit and 16-bit modes are shown in figure 6.

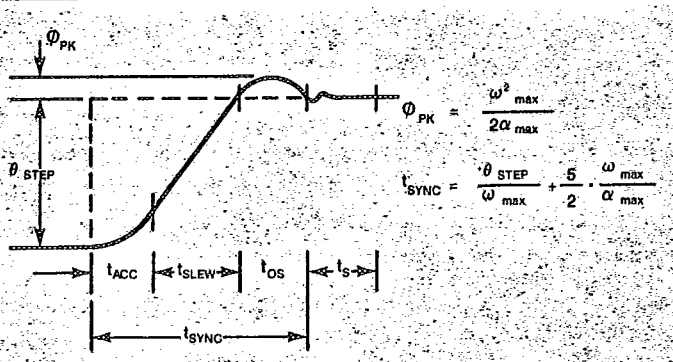


FIGURE 5 Large Signal (≥1.4°) Response Parameters

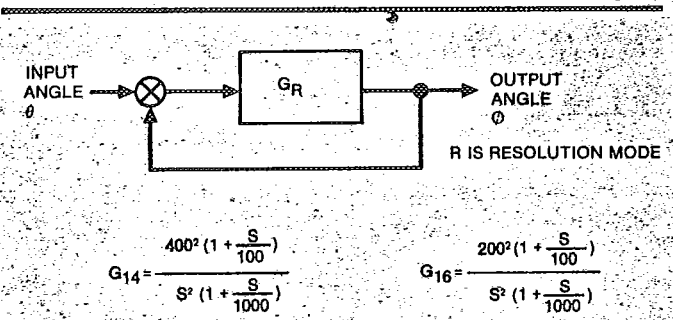


FIGURE 6 Transfer Functions for SRD546

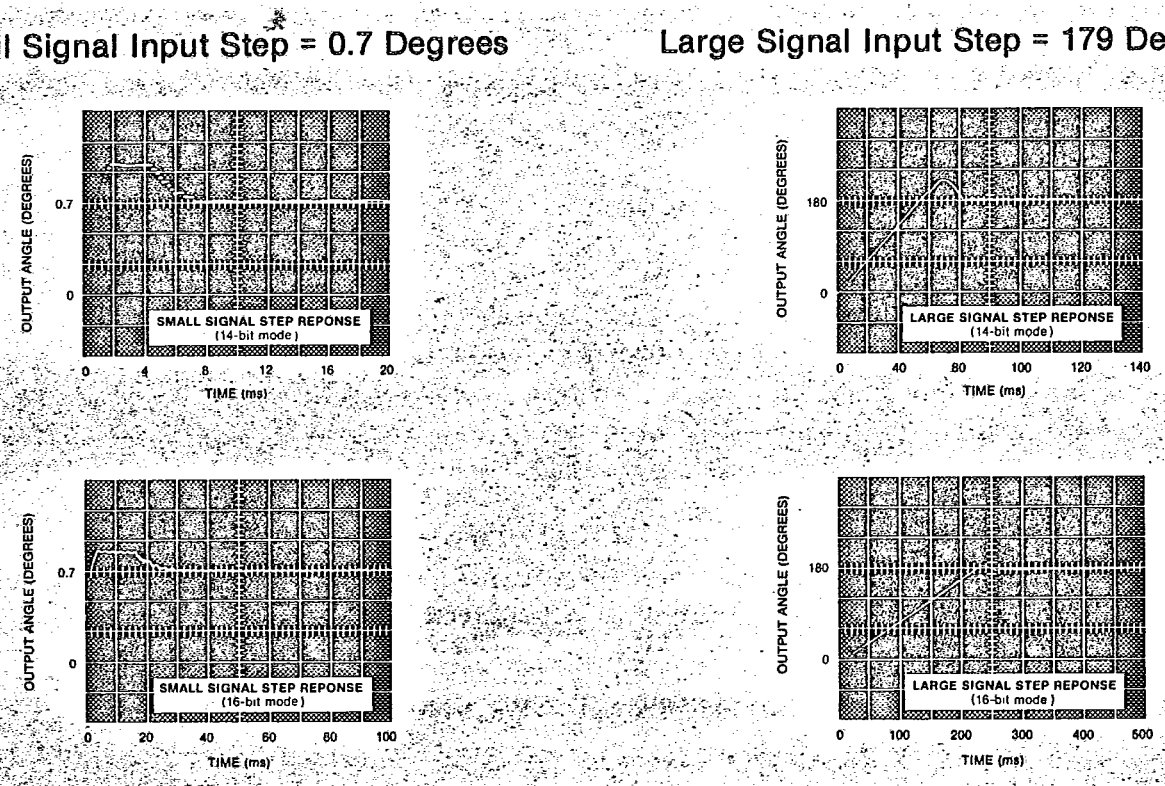
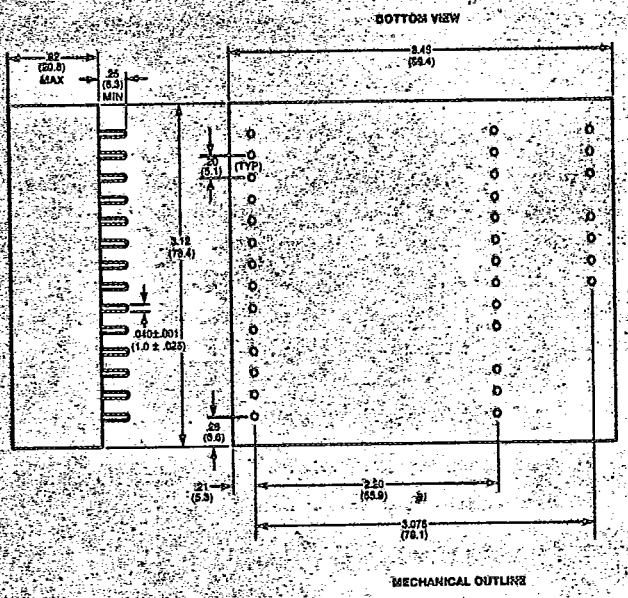


FIGURE 7 Dynamic Characteristics



MECHANICAL OUTLINE

Ordering Information

SRD546 - T M

Temperature Range	MIL-Specifications
1 = 0°C to +70°C	S = Standard
2 = -25°C to +85°C	B = MIL-STD-883B
3 = -55°C to +105°C	C = MIL-STD-883C

A wide range of other SYNCHRO CONVERSION products and application assistance is available from Natel. Application Notes can be requested when available . . . and Natel's applications engineers are at your disposal for specific problems.

Other Synchro Conversion products available from Natel

36-PIN DDIP HYBRIDS

- 16-bit microprocessor-compatible Digital-to-Synchro/Resolver converter, with double buffered inputs and 1 arc-minute accuracy (HDSR2006).
- 14-bit digital-to-synchro/resolver converter that is pin-compatible with existing designs with transformation and angular accuracy improvement of a factor of 2 to 4 (HDSR2504)
- 16-bit microprocessor-compatible Synchro/Resolver-to-Digital converter, with 3-state outputs, operating from a single +5-V power supply (HSRD1006).

DISCRETE MODULES AND SYSTEMS

- Two-speed logic combiner with 20-bit, 3-state output, in a 1.3 x 2.6 x .35 inch size (TSL1X36)
- 14 and 16-bit Digital to Synchro/Resolver converters, with internal power amplifiers (5012, 5112, 5116)
- High power Synchro/Resolver Drivers
- 10 to 20-bit single-speed Synchro-to-Digital converters.

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