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A TDK Group Company

SSI 32R525R/525RM
2 and 4-Channel Thin Film Read/Write Device

February 1993

DESCRIPTION

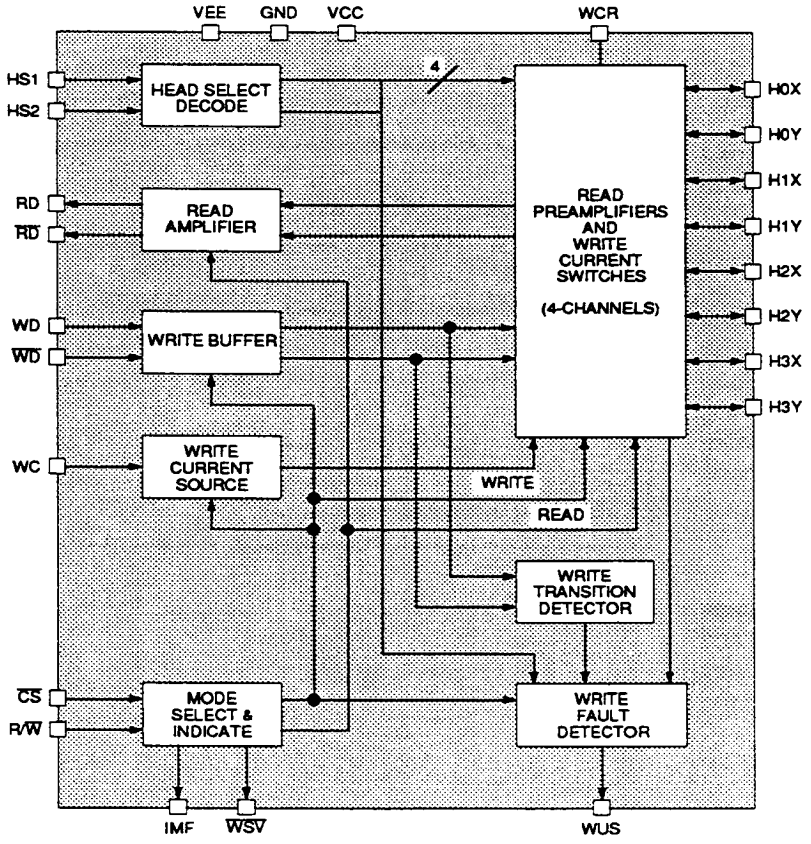
The SSI 32R525R/525RM is an integrated read/write circuit designed for use with non-center tapped thin film heads in disk drive systems. Each chip controls four heads and has three modes of operation: read, write, and idle. The circuit contains four channels of read amplifiers and write drivers and also has an internal write current source. The 32R525RM provides the same device as the 32R525R in a mirror pinout.

A current monitor (IMF) output is provided that allows a multichip enable fault to be detected. An enabled chip's output will produce one unit of current. An open collector output, write select verify (WSV), will go low if the write current source transistor is forward biased. The circuit operates on +5 volt, and -5 volt power and is available in 20-lead and 24-lead SOL packages.

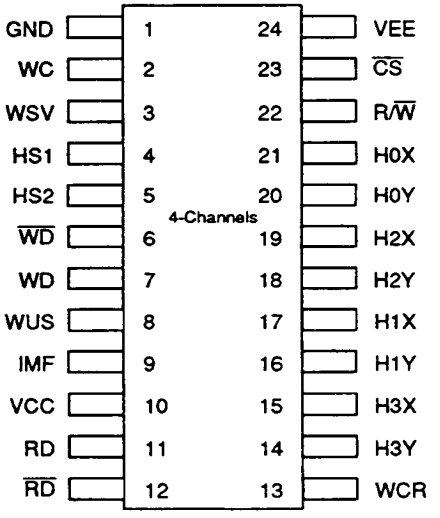
FEATURES

- **High performance**
  - **Read Mode Gain = 125 V/V nominal**
  - **Input Noise = 0.8 nV/$\sqrt{Hz}$ max**
  - **Input Capacitance = 35 pF max**
  - **Write Current Range = 25 mA to 40 mA**
  - **Write Current Rise Time = 10 nsec max**
  - **Head Voltage Swing = 3.8 Vpp min**
- **Write unsafe detection**
- **-5V, +5V power supplies**

BLOCK DIAGRAM



PIN DIAGRAM



24-Lead SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

WRITE MODE

In Write Mode (R/$\overline{W}$ and $\overline{CS}$ low) the circuit functions as a differential current switch. The Head Select Inputs (HS1 and HS2) determine the selected head. The write current magnitude is adjusted by an external resistor Rex from WC to Vcc.

$$Iw = \frac{80}{Rex} Adc$$

WRITE MODE FAULT DETECT CIRCUIT

Several circuits are dedicated to detecting fault conditions associated with the write mode. A logical high (off) level will be present at the Write Unsafe (WUS) terminal if any of the following write fault conditions are present:

- Open head circuit
- Head shorted to ground
- No write current
- Write current transition frequency too low
- Head select input(s) open circuit
- Write mode not logically selected

The Write Unsafe output is open-collector and is usually terminated by an external resistor connected to Vcc.

READ MODE

In Read Mode, (R/$\overline{W}$ high and $\overline{CS}$ low), the circuit functions as a low noise differential amplifier. The read amplifier input terminals are determined by the Head Select inputs. The read amplifier outputs (RD, $\overline{RD}$) are open collector, requiring external load resistors connected to Vcc. The amplifier gain polarity is non–inverting between HX, Y inputs and RD outputs.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RD and $\overline{RD}$ outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wired OR'ed.

MODE SELECTION AND INDICATION CIRCUIT

Logical control inputs which select mode and head channel are TTL compatible. Their functions are described in Tables 1 and 2.

Selection of the write mode is indicated by a low (on) state of the Write Select Verify ($\overline{WSV}$) terminal. The open collector output is usually terminated by an external resistor connected to Vcc.

The selection of either the write or read mode is indicated by the flow of a unit of current into the Current Monitor (IMF) terminal. By summing the currents from multiple circuits, the user can determine that one, and only one, circuit is active.

The mode select inputs have internal pull up circuits so that if an input is open it will rise to the upper logic level.

Table 1: Head Select Table

Head Selected	HS2	HS1
0	0	0
1	0	1
2	1	0
3	1	1

Table 2: Mode Select Table

Mode Select			Indicating & Fault Outputs		
$\overline{CS}$	R/$\overline{W}$	Selected Mode	IMF	WSV	WUS
1	X	Idle	off	off	off
0	1	Read	on	off	off
0	0	Write	on	on	on*

*Provided that no fault is detected.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
CONTROL INPUT PINS		
$\overline{CS}$	I	Chip Select input. A logical low level enables the circuit for a read or write operation. Has internal pull up.
R/$\overline{W}$	I	Read/Write select. A logical low level enables the Write mode (when $\overline{CS}$ is low). Has internal pull up.
HS1,HS2	I	Head Select inputs. Logical combinations (Table 1) select one of four heads.
HEAD TERMINAL PINS		
H0X - H3X H0Y - H3Y	I/O	Connection to read/write magnetic head terminals.
DATA INPUT/OUTPUT PINS		
WD, $\overline{WD}$	I	Differential Write Data inputs used to write data patterns on the disk.
RD, $\overline{RD}$	I	Differential Read Data pattern output amplified playback from the disk. These outputs are normally terminated in 100Ω resistors to Vcc.
EXTERNAL COMPONENT CONNECTION PINS		
WC	I	Resistor connected to Vcc to provide desired value of write current.
CURRENT MONITOR PINS		
$\overline{WSV}$	O	Write Select Verify is an open collector output with the on state indicating that the circuit has been selected for a write operation. It is normally terminated to +Vcc through a resistor.
WUS	O	Write Unsafe is an open collector output with the off state indicating that conditions are not proper for a write operation.
IMF	O	High impedance output sinks a unit of monitor current when the chip is enabled.
POWER, GROUND PINS		
Vcc	I	Positive power supply voltage for circuit functions.
VEE	I	Negative power supply voltage.
GND	I/O	Power supply common.
WCR	–	Write Current Connection to power supply common.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.75 ≤ VCC ≤ 5.20, -5.50 ≤ VEE ≤ -4.75V, 0° ≤ T (junction) ≤ 125°C.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Positive Supply Voltage, Vcc	6 VDC
Negative Supply Voltage, VEE	-6 VDC
Operating Junction Temperature	-20 to +130°C
Storage Temperature	-65 to +150°C
Lead Temperature (Soldering, 10 sec)	260°C
Input Voltages	
Head Select (HS)	-0.4 to Vcc + 0.3V
Chip Enable ($\overline{CS}$)	-0.4 to Vcc+ 0.3V
Read Select (R/$\overline{W}$)	-0.4V to Vcc + 0.3V
Write Data (WD, $\overline{WD}$)	-VEE to 0.3V
Head Inputs (Read Mode)	-0.6 to 0.4V
Outputs	
Read Data (RD, $\overline{RD}$)	Vcc - 2.5 to Vcc + 0.3V
Write Unsafe (WUS)	-0.4V to Vcc + 0.3 and 20 mA V
Write Select Verify (WSV)	-0.4V to Vcc + 0.3 and 20 mA V
Current Monitor (IMF)	-0.4 to Vcc + 0.3V
Current Reference (WC)	-1.0 mA to 5.0 mA
Head Outputs (Write Mode)	-100 mA to 1.0 mA

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Power Dissipation	Idle Mode			100	mW
	Read Mode			350	mW
	Write Mode, Iw = 40 mA			500	mW
Positive Supply Current (ICC)	Idle Mode			10	mA
	Read Mode			25	mA
	Write Mode			12	mA
Negative Supply Current (IEE)	Idle Mode			-8	mA
	Read Mode			-45	mA
	Write Mode			-40 - Iw	mA

DC CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
High Level Input Voltage (VIH) ($\overline{CS}$, R/$\overline{W}$, HS1, HS2)		2.0			V
Low Level Input Voltage (VIL) ($\overline{CS}$, R/$\overline{W}$, HS1, HS2)				0.8	V
High Level Input Current (IIH) ($\overline{CS}$, R/$\overline{W}$)	(VIH=2.7V)			20	µA
Low Level Input Current (IIL) ($\overline{CS}$, R/$\overline{W}$)	(VIL=0.4V)			-400	µA
High Level Input Current (IIH) (HS1, HS2)	(VIH=2.7V)			250	µA
Low Level Input Current (IIL) (HS1, HS2)	(VIL=0.4V)			250	µA
High Level Input Voltage (VIH) (WD, $\overline{WD}$)		-1.0		.6	V
Low Level Input Voltage (VIL) (WD, $\overline{WD}$)		-2.0		-1.5	V
High Level Input Current (IIH) (WD, $\overline{WD}$)	(VIH=-0.6V, VIL=-2.0V)			150	µA
Low Level Input Current (IIL) (WD, $\overline{WD}$)	(VIL=-2.0V, VIH=-1.0V)	-20			µA
Output Off Leakage Curr. (IOFF) (WUS,- WSV)	(VOFF=5.0V)			100	µA
Low Level Output Voltage (VOL) (WUS, -WSV)	(IOL=8.0 mA)			0.4	V
Output Leakage Current (IOFF) (IMF)	(VOFF=5.0V)			20	µA
Output on Current (ION) (IMF)	(VON=0.5V to 5.0V)	2.4		3.5	mA
Data Input Voltage Range		-2.0		0.6	V
Data Input Current (per side)	Chip Enabled			150	µA
Data Input Capacitance	per side to GND			10	pF

ELECTRICAL SPECIFICATIONS (Continued)

READ MODE

Tests performed with 100Ω load resistors from RD and $\overline{RD}$ through series isolation diodes to VCC.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Voltage Gain	Vin = 1m Vpp, f = 300 kHz	100	125	150	V/V
Voltage Bandwidth (-3dB)	Zs < 5z, Vin = 1m Vpp f midband = 300 kHz	55		100	MHz
Input Noise Voltage	Zs = 0Ω , Vin = 0V, Power Bandwidth = 30 MHz			0.8	$nV\sqrt{Hz}$
Differential Input Capacitance	Vin = 0V, f = 5 MHz			35	pF
Differential Input Resistance	Vin = 0V, f = 5 MHz	500		1800	Ω
Input Bias Current (per side)	Vin = 0V			0.17	mA
Dynamic Range	DC input voltage where AC gain falls to 90% of the gain with 0.5m Vpp input signal	-3.0		3.0	mV
Common Mode Rejection Ratio	Vin = 100m Vpp, 0V DC 1 MHz ≤ f ≤10 MHz	50			dB
	f = 20 MHz	46			dB
Power Supply Rejection Ratio	VCC or VEE = 100m Vpp 1 MHz ≤ f ≤ 10 MHz	65			dB
	f = 20 MHz	40			dB
Channel Separation	The three unselected channels are driven with Vin = 20m Vpp 1 MHz ≤ f ≤ 10 MHz	46			dB
	f = 20 MHz	40			dB
Output Offset Voltage		-360		360	mV
Output Leakage Current	Idle Mode			0.01	mA
Output Common Mode Voltage		VCC -0.75		VCC -0.45	V
Single Ended Output Resistance		10			KΩ
Single Ended Output Capacitance				10	pF

WRITE MODE

Current Tolerance	Current set to nominal value by Rex = 1.6K to 3.6 kΩ, Tj = 50°C	-8		+8	%
Differential Head voltage swing	Iw = 40 mA	3.8			Vpp

WRITE MODE (continued)

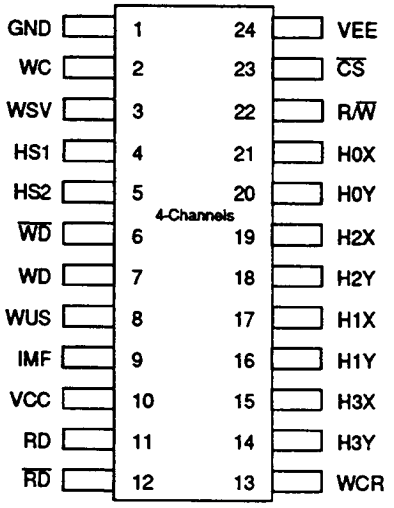
PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Current Range (Iw)	Rwc = 3600Ω to 1600Ω	25		45	mA
Differential Output Resistance, Rd		1700		2600	Ω
Differential Output Capacitance				10	pF
WD, $\overline{WD}$ Transition Frequency	WUS = low	1.0			MHz

SWITCHING CHARACTERISTICS

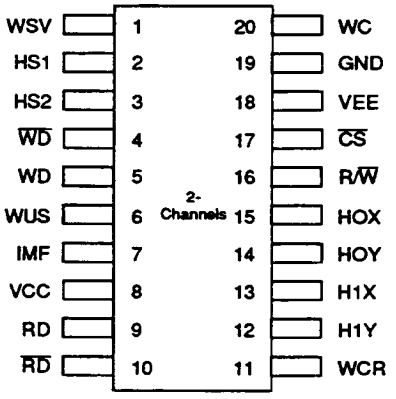
Idle to Read/Write Transition Time				0.5	µs
Read/Write to Idle Transition Time				0.5	µs
Read to Write Transition Time	VL$\overline{CS}$ = 0.8V, Delay to 90% of Iw			0.5	µs
Write to Read Transition Time	VL$\overline{CS}$ = 0.8V, Delay to 90% of 20 MHz Read Signal envelope, Iw decay to 10%			0.5	µs
Head Select Switching Delay	Read or Write Mode			0.5	µs
Head Current Transition Time 10% to 90%	Iw = 40 mA, Lh = 0.15 µH, Rh = 20Ω			12	ns
Head Current Overshoot	Iw = 40 mA, Lh = 0.15 µH, Rh = 20Ω, relative to total current change			50	%
Head Current Switching Time Asymmetry	Lh = 0, Rh = 0, WD / $\overline{WD}$ transitions 2 ns, switching time asymmetry 0.2 ns			1.5	ns
WSV Transition Time	Delay from 50% of write select swing to 90% of final WSV voltage, Load = 2 kΩ // 20 pF			0.25	µs
Unsafe to Safe Delay After Write Data Begins (WUS)	f(data) = 5 MHz			0.5	µs
Safe to Unsafe Delay, (WUS)	Head open or shorted to GND, no write current, head select input open			0.5	µs
Safe to Unsafe Delay, (WUS)	Non-switching write data	0.5		2.0	µs
IMF Switching Time	Delay from 50% of $\overline{CS}$ to 90% of final IMF current			0.25	µs

SSI 32R525R/525RM
2 and 4-Channel Thin Film Read/Write Device

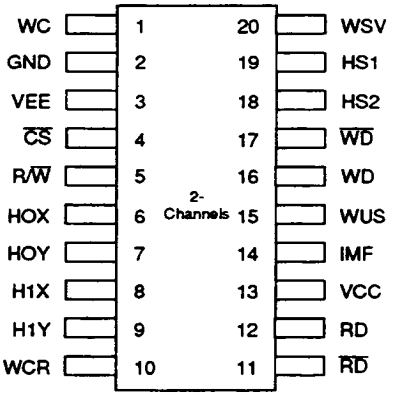
PACKAGE PIN DESIGNATIONS
(Top View)



32R525R-4 Channel
24-Lead SOL



32R525R
20-Lead SOL



32R525RM
20-Lead SOL

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32R525R		
20-Lead SOL	32R525R-2CL	32R525R-2CL
24-Lead SOL	32R525R-4CL	32R525R-4CL
SSI 32R525RM		
20-Lead SOL	32R525RM-2CL	32R525RM-2CL

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