Features

- **Gain Control in 20-dB Steps**
- **Very Low I/Q Amplitude and Phase Errors**
- **High Input P1dB**
- **Small and Optimized Package for High Reliability and Performance**

Applications

- **Infrastructure Digital Communication Systems**
- **GSM/Cellular Transceivers**
- **ISM Band Transceivers**

Benefits

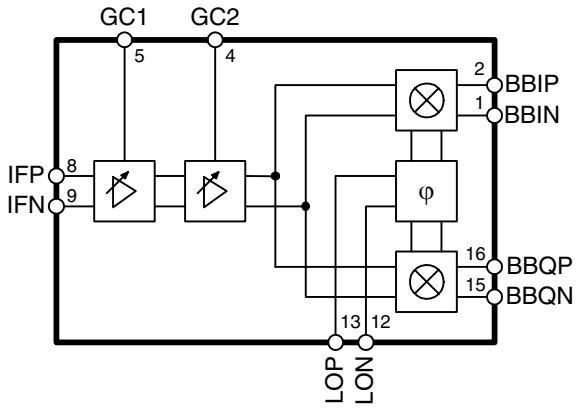
- **Fully Integrated Device with Reduced External Component Count**

Electrostatic sensitive device.
Observe precautions for handling.

Description

The ATR0797 is a multi-purpose demodulator RFIC. The silicon monolithic integrated circuit is designed with Atmel's advanced SiGe technology. This demodulator is capable of both quadrature demodulation or direct IF output. Features include switchable gain control on a frequency range from 65 MHz to 300 MHz. The device performs a very low amplitude as well as phase error and allows high input P1dB. The ATR0797 targets a variety of system applications for communications including 3G wireless.

Figure 1. Block Diagram



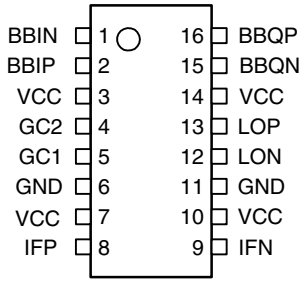
65 - 300 MHz SiGe IF Receiver/ Demodulator

ATR0797

Rev. 4665B–SIGE–10/03

Pin Configuration

Figure 2. Pinning



Pin Description

Pin	Symbol	Function
1	BBIN	Baseband I-axis negative output, self biasing
2	BBIP	Baseband I-axis positive output, self biasing
3	VCC	5 V power supply
4	GC2	Gain control input, stage 2, 5 V CMOS levels
5	GC1	Gain control input, stage 1, 5 V CMOS levels
6	GND	Ground
7	VCC	5 V power supply
8	IFP	IF positive input, self biasing, AC-coupled
9	IFN	IF negative input, self biasing, AC-coupled
10	VCC	5 V power supply
11	GND	Ground
12	LON	Local oscillator, negative input, self biasing, AC-coupled
13	LOP	Local oscillator, positive input, self biasing, AC-coupled
14	VCC	5 V power supply
15	BBQN	Baseband Q-axis negative output, self biasing
16	BBQP	Baseband Q-axis positive output, self biasing

Product Description

Atmel's ATR0797 is a variable gain I-Q demodulator designed for use in receiver IF sections, that are typically existing in superheterodyne RF architectures.

The ATR0797 has two gain stages that are independent of each other. These gain stages are broadband differential amplifiers each with a digital control pin to set the gain. Since the amplifiers have approximately the same gain, setting GC1 high and GC2 low results in approximately the same gain as setting GC1 low and GC2 high. Former setting offers better noise figures.

The IF input is a differential input that has internal bias circuitry to set the common mode voltage. The use of blocking capacitors to facilitate AC coupling is highly recommended to avoid changing the common mode voltage. Either input may be driven single ended if the other input is connected to ground through an AC short such as a 1000 pF capacitor. This typically results in slightly lower input P1dB.

The two matched mixers are configured with the quadrature LO generator to provide in-phase and quadrature baseband outputs.

The LO and IF ports offer a differential 50 Ω impedance. The passives at these ports (parallel L-R network) and the package itself adds inductance that tends to degrade return loss.

The ATR0797 features immunity from changes in LO power. The gain features change by less than 0.6 dB over a 6 dB range of LO power. Also note the excellent I/Q balance, which typically falls within 0.1 dB and 1 degree from 65 MHz to 300 MHz, and varies less than 0.05 dB and 0.5 degree over temperature (-40°C to +85°C).

The frequency response of the IF and LO ports is dominated by the L-R network on the input. When de-embedded, the gain and P1dB response is within 0.5 dB from 65 MHz to 300 MHz.

The figures in the datasheet illustrate a typical ATR0797's performance with respect to temperature. Note that these numbers include the effect of the R-L network in the IF port.

Evaluation board design and equipment constraints:

Please take into account that the evaluation board uses baluns on the I/Q outputs, and these baluns limit the low frequency response of the device. For true baseband operation, the baluns should be removed, and the differential signals used directly.

The 27 pF capacitor on the evaluation board is appropriate for lower frequencies.

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All voltages are referred to GND.

Parameters	Symbol	Value	Unit
Supply voltage	V_{CC}	5.5	V
LO input	LOP, LON	10	dBm
IF input	IFN, IFP	10	V
Operating temperature	T_{OP}	-40 to +85	°C
Storage temperature	T_{stg}	-65 to +150	°C

Note: The device may not survive all maximums applied simultaneously.

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	35	K/W

Electrical Characteristics

Test conditions: V_{CC} = 5 V, T_{amb} = 25°C, LO input: 0 dBm at 200 MHz
IF input: at 200.1 MHz, GC1 = 0, GC2 = 0; 0 dBm
IF input: at 200.1 MHz, GC1 = 1, GC2 = 0; -20 dBm
IF input: at 200.1 MHz, GC1 = 1, GC2 = 1; -40 dBm

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type[1]
1	**IF Input (I/Q Mixing to Baseband)**								
1.1	Frequency range		8, 9	f	65	120 - 220	300	MHz	B
1.2	IF input return loss	50 Ω nominal differential input[2]	8,9	RL		20		dB	D
1.3	IF input common mode voltage	Internally gernerated		V_{CH}		2		V	
1.4	Gain	Gain set = high; GC1 = GC2 = 1	8, 9	G	28	31	33	dB	A
1.5	Input P1dB		8, 9	P1dB	-26	-24		dBm	C
1.6	DSB Noise figure		8, 9	NF		11		dB	D
1.7	Gain	Gain set = medium; GC1 = 1; GC2 = 0 or GC1 = 0; GC2 = 1	8, 9	G	9	12	14	dB	A
1.8	Input P1dB		8, 9	P1dB	-8	-6		dBm	C
1.9	DSB Noise figure		8, 9	NF		14.5		dB	D
1.10	Gain	Gain set = low; GC1 = GC2 = 0	8, 9	G	-9	-6.5	-4	dB	A
1.11	Input P1dB		8, 9	P1dB	12	14		dBm	C
1.12	DSB Noise figure		8, 9	NF		31		dB	D

Notes:
1. Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter
2. The parasitic inductance of the package, the board, and L5, L6 must be matched out at the center frequency with a series capacitor to achieve 20 dB of port match.
3. The parasitic inducfance of the package must be matched out to reach 20 dB port match above 100 MHz.

Electrical Characteristics (Continued)

Test conditions: V_{CC} = 5 V, T_{amb} = 25°C, LO input: 0 dBm at 200 MHz
IF input: at 200.1 MHz, GC1 = 0, GC2 = 0; 0 dBm
IF input: at 200.1 MHz, GC1 = 1, GC2 = 0; -20 dBm
IF input: at 200.1 MHz, GC1 = 1, GC2 = 1; -40 dBm

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type(1)
2	**I/Q Output**								
2.1	I/Q output frequency range		1, 2, 15, 16	$f_{I/Q}$	DC		500	MHz	D
2.2	I/Q output amplitude error		1, 2, 15, 16		-0.2		+0.2	dB	A
2.3	I/Q phase error		1, 2, 15, 16		-2		+2	deg	A
2.4	I/Q output common mode voltage		1, 2, 15, 16			2.5		V	A
2.5	I/Q output differential offset voltage		1, 2, 15, 16	V_{offset}	-100		+100	mV	A
2.6	I/Q output return loss	50 Ω nominal differential output(3)	1, 2, 15, 16	$RL_{I/Q}$		20		dB	D
3	**LO input**								
3.1	LO input level		12, 13	P_{LO}	-3	0	+3	dBm	D
3.2	Return loss		12, 13	RL_{LO}		20		dB	D
3.3	LO frequency range		12, 13	RL_{LO}	65		300	MHz	D
4	**Miscellaneous**								
4.1	Supply voltage		3, 7, 10, 14	V_{CC}	4.75	5	5.25	V	A
4.2	Supply current		3, 7, 10, 14	I_{CC}		195		mA	A
4.3	GC1, GC2 logic level low		4, 5	V_{IL}	0		$0.3 \times V_{CC}$	V	D
4.4	GC1, GC2 logic level high		4, 5	V_{IH}	$0.7 \times V_{CC}$		V_{CC}	V	D
4.5	GC1, GC2 input impedance		4, 5	Z	40			kΩ	D

Notes:
1. Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter
2. The parasitic inductance of the package, the board, and L5, L6 must be matched out at the center frequency with a series capacitor to achieve 20 dB of port match.
3. The parasitic inducfance of the package must be matched out to reach 20 dB port match above 100 MHz.

Figure 3. Gain versus Temperature

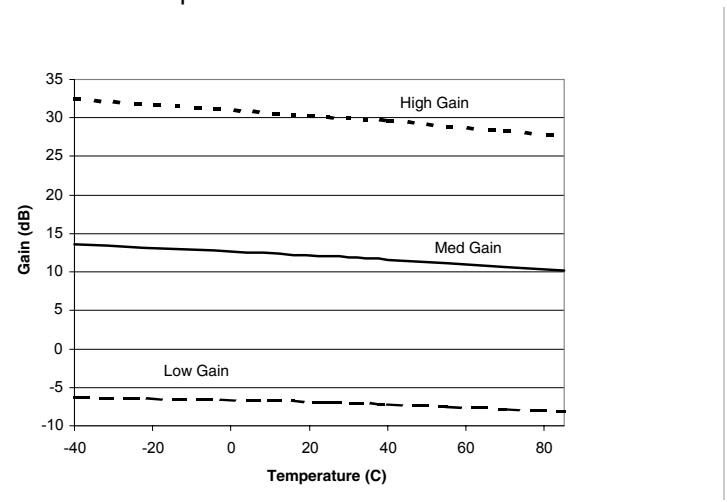


Figure 4. Noise Figure versus Temperature

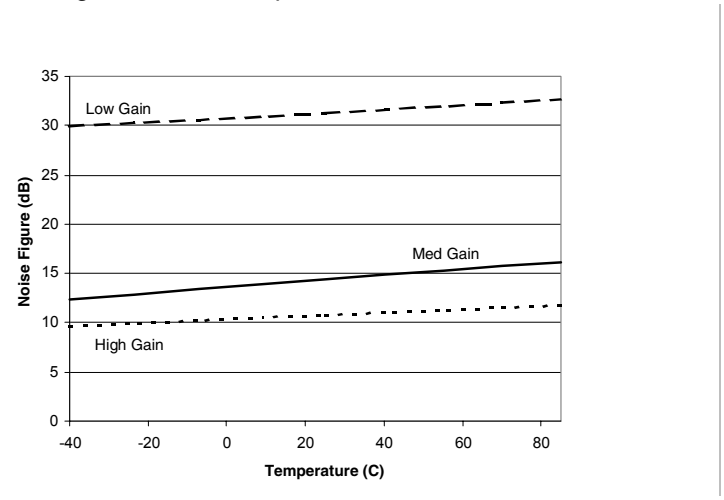


Figure 5. Amplitude Difference versus LO Frequency

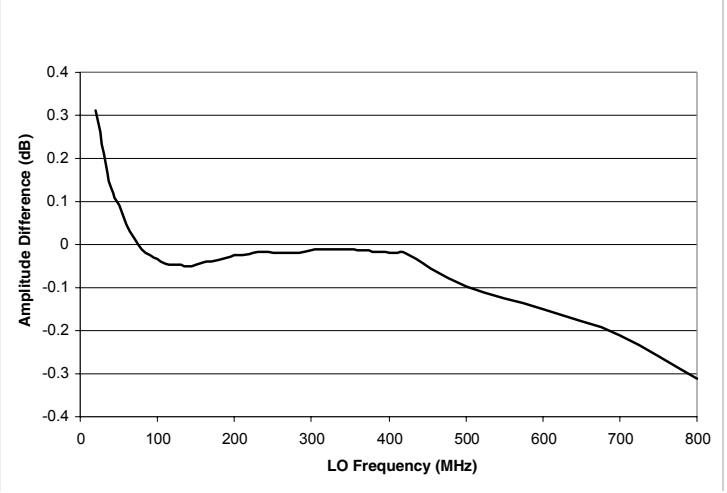


Figure 6. Output P1dB versus Temperature

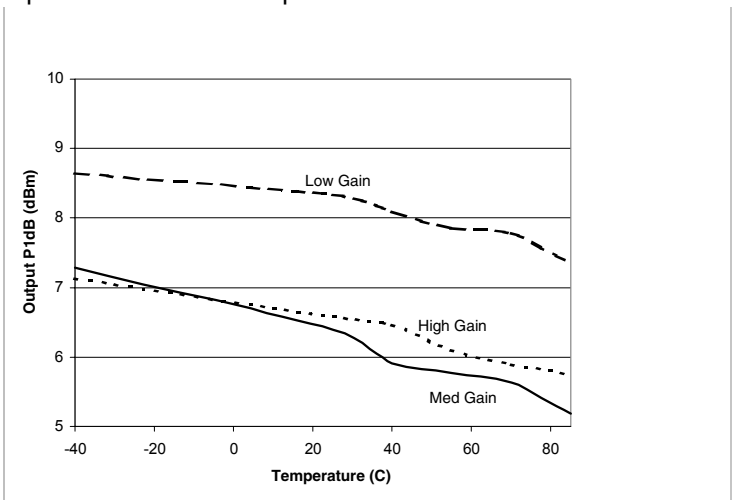


Figure 7. Output P1dB versus LO Power

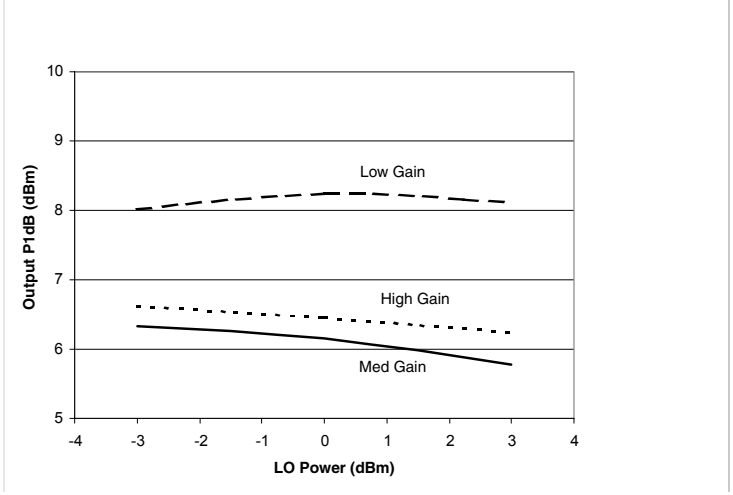


Figure 8. Phase Difference versus LO Frequency

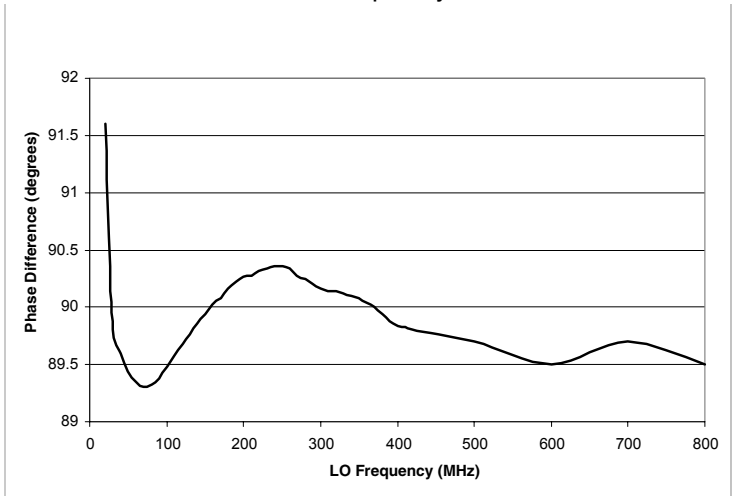


Figure 9. Demo Test Board Schematic

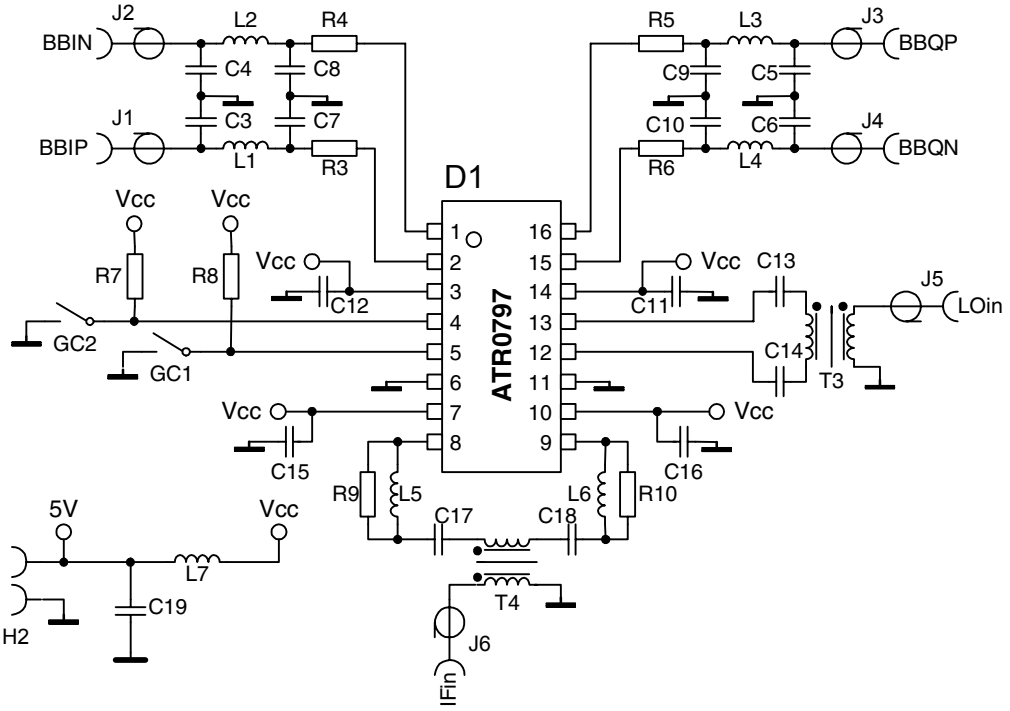


Table 1. Bill of Materials

Component	Reference	Vendor	Part Number	Value	Size/Package
IF Demodulator	D1	Atmel	ATR0797		TSSOP16
SMA end launch connector	J1, J2, J3, J4, J5, J6	Johnson Components™	742-0711-841		
Transformer	T3, T4	Mini-Circuits®	TC1-1		
Supply bypass capacitor	C19			1 µF	1206
Resistor	R7, R8			1 kΩ	0402
Capacitor	C11, C12, C16			22 pF	0402
Inductor	L1, L2, L3, L4, L7	Würth Elektronik®	74476401	1 µH	1210
Capacitor	C13, C14, C17, C18			68 pF	0402
Resistor	R3, R4, R5, R6			0 Ω	0402
Capacitor	C3, C4, C5, C6, C7, C8, C9, C10			820 pF	0402
Resistor	R9, R10			51 Ω	0402
Inductor	L5, L6			10 nH	0402
Capacitor	C15			100 pF	0402

Figure 10. Demo Test Board (Fully Asembled PCB)

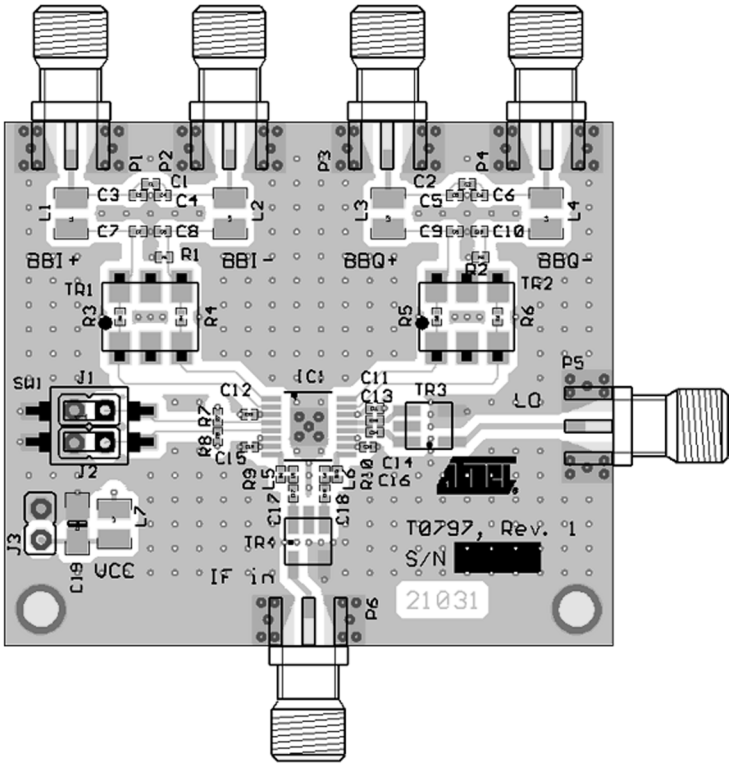
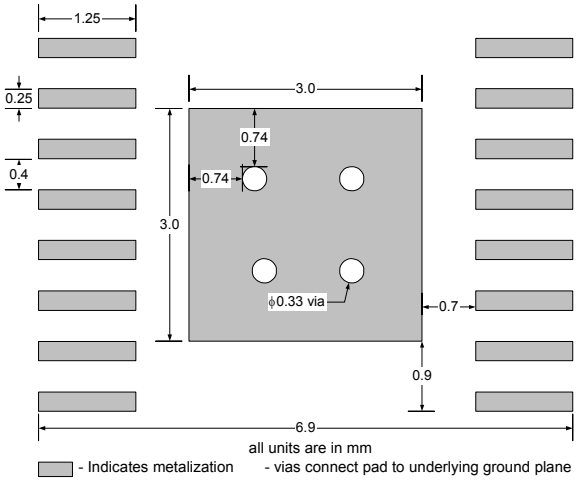


Figure 11. Recommended Package Footprint



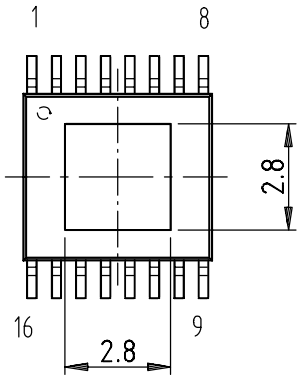
Remark: Heatslug must be soldered to GND.
In order to avoid soldering problems, plugging of the vias under the heatslug is recommended. Only ground signal traces are allowed directly under the package.

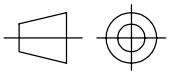
Ordering Information

Extended Type Number	Package	Remarks
ATR0797	TSSOP16	–

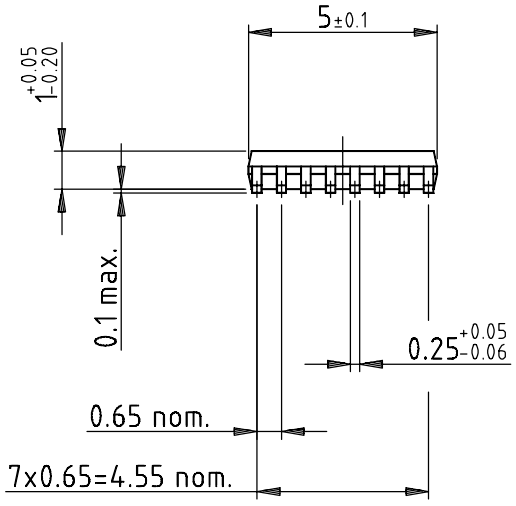
Package Information

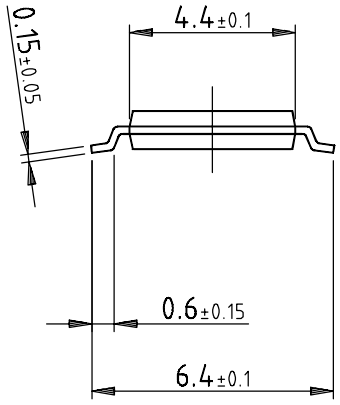
Package: SSOP16
(acc. JEDEC SMALL OUTLINE No. MO-153)
Dimensions in mm





technical drawings
according to DIN
specifications





Drawing-No.: 6.543-5079.01-4
Issue: 1; 10.07.01

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

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