Different Termination Schemes

In this application note we will talk about the different ECL / PECL output termination schemes and AC coupling of the ECL / PECL inputs and outputs.

Any signal path on a printed circuit board may be considered as a form of transmission line. If the line propagation delay is short with respect to the rise time of the signal then the reflections are masked out and are not seen as an overshoot or ringing; thus when the edge speed increases with faster forms of logic, the line lengths should be shorter in order to retain signal integrity.

When high-speed signals are transmitted over long lines, terminations should be used to minimize reflections and signal distortion. These reflections cause ringing on the signal line, which, if severe, will affect system noise immunity. The reflections appear as overshoot and undershoot on the output waveform.

In ECL systems, every output must be terminated matching the characteristic impedance of the transmission lines. Some of the most popular values of the transmission line impedance are 50 to 75Ω for multilayer etched boards, 100Ω for multi-wire boards, and 100 to 120Ω for wire-wrap boards. Standard prepackaged termination resistors are available with values of 50, 68, 75 and 100Ω.

In this application note, we will discuss four types terminations mentioned below:

1. Parallel Termination
2. Thevenin equivalent parallel termination
3. Series Termination
4. “Y” Termination

Parallel Termination

In this method, the ECL / PECL outputs are terminated with a termination resistor, R_P, to a termination supply voltage of VTT = Vcc-2.0V. The value of Rp must be equal to the impedance of the transmission line, Zo. See Figure 1. If there is a mismatch, line reflections will be present with an increase in both noise and propagation delay. The placement of the termination resistors is important and they should be placed as close to their destination as possible. In this parallel terminated lines, the line termination supplies the output pull-down resistors; consequently, no pull-down resistors are required at the outputs of the driving gate. The advantage of using this method is that the average power consumption is reduced but on the flip side, it requires an additional power supply. Average current consumption and power dissipation may be of interest when using this termination scheme, Table 1 shows average current and power dissipation for different transmission lines.

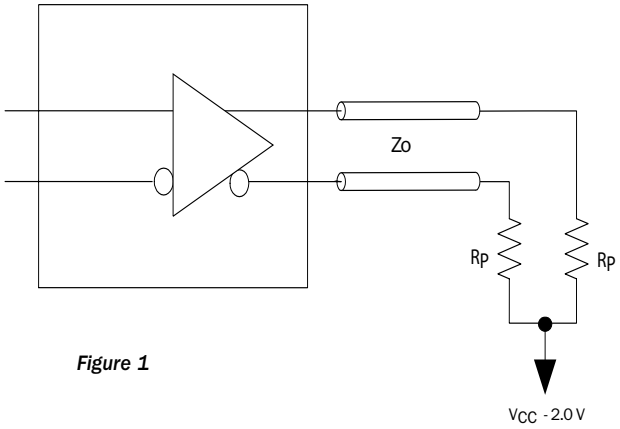

Figure 1

			PDavg (mW)	
Zo	Rp	Iavg (mA)	IC Output	Rp
50	50	14	14	13
75	75	9.3	9.5	9.1
100	100	7.3	7.3	7.1
150	150	5	4.9	5

Table 1

Thevenin Equivalent Parallel Termination

This method does not require an additional power supply. Basically it requires one pull-up resistor between the output and VCC and a pull-down resistor between the output and Vee. The values of these two resistors, R_{P1}& R_{P2}, will change depending on the supply voltage range of the device. The scheme is very easy to implement and it is cost effective compared to parallel termination scheme; however, the power consumption on the external resistors are a little higher. The placement of these termination resistors must be very close to its destination for optimum performance. Equations 1 and 2, will allow us to calculate the values of these termination resistors based on the value of transmission line impedance. Refer to figure 2 for the schematic and table 3 for R_{P1}& R_{P2} values for different supply voltage range and transmission line impedance. Table 2 depicts average current consumption and power dissipation for different transmission line impedance values using Thevenin equivalent parallel termination scheme.

$$R_{P1} = \frac{V_{EE} * R_T}{V_{EE} - V_{TT}} \quad (1) \qquad R_{P2} = \frac{V_{EE} * R_T}{V_{TT}} \quad (2)$$

Conditions:

- $R_T = Z_o$, impedance of the transmision line
- $V_{TT} = V_{CC}$ - 2.0V
- V_{EE} = - 3.0V to - 5.5V, V_{CC} = 0V or
- V_{CC} = +3.0V to + 5.5V, V_{EE} = 0V

Zo(Ω)	R_{P1} = 1.8*Zo(Ω)	R_{P2} = 2.25*Zo(Ω)	Iavg (mA)	PD on R_{P1} and R_{P2}(mW)
50	90	113	28.2	109
75	135	169	18.8	72.7
100	180	225	14.1	54.5
150	270	338	9.4	36.3

Table 2

Note:
Numbers in Table 2 assumes VCC = 4.5V.

Zo (Ω)	Supply Voltage +3.3V or -3.3V		Supply Voltage +5.0V or -5.0V	
	R_{P1}	R_{P2}	R_{P1}	R_{P2}
50	127	83	83	125
75	190	124	125	188
100	254	165	167	250
150	380	248	250	375

Table 3

Thevenin Equivalent Termination Scheme

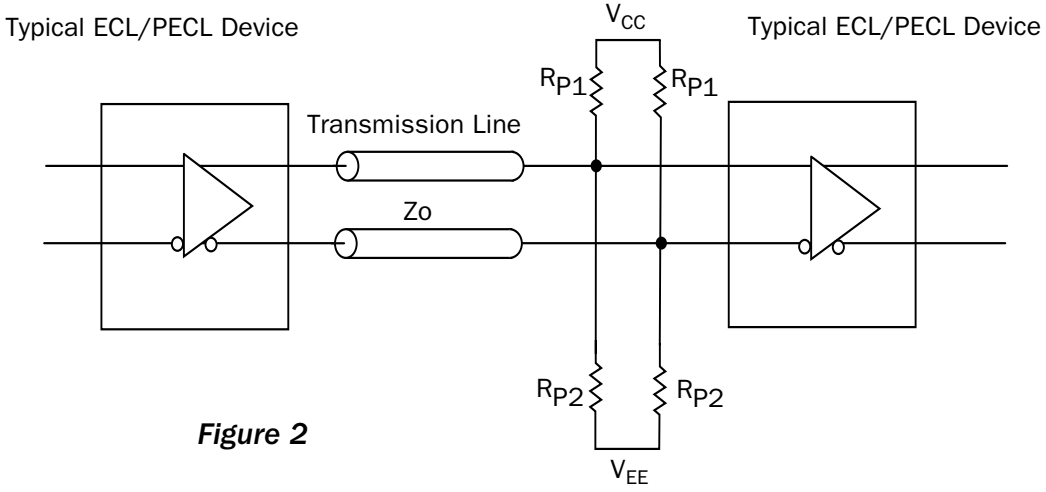

Figure 2

Series Termination

Using series damping or series termination technique may control overshoot and ringing on longer transmission lines. Series damping is accomplished by inserting a small resistor Rs in series with the output of the gate as shown in figure 3. In this case the value of R_T is such that it can drive 5-15mA of current. It is mandatory that R_S added to the output impedance must be equal to Zo. Signal transmitted from point A is reflectedat point B. But due to the presence of R_S (R_S+R_{OUT}=Zo), this signal is not seen at B. The advantage of this method is that the power does not increase as much as in the parallel termination method even when multiple lines are connected to A. Series Termination scheme does not require an extra power supply for termination. It is cost effective, easy to implement, absorbs any reflections returning to source, and is ideal for Back-plane designs, or any designs with impedance discontinuities.

The driven inputs must be near the end of the line to avoid receiving a 2-step signal. Table 4 depicts average current consumption and power dissipation for different transmission line impedance values using series termination scheme.

Zo (Ω)	R_P (Ω)	Iavg (mA)	Pdavg (mW)	
			IC Output	R_T (Ω)
50	269	9.8	12.9	25.8
75	399	7.9	8.6	16.8
100	530	4.9	6.5	12.7
150	791	3.2	4.2	8.1

Table 4

Some recommended values for R_T at different supply voltages are:

- R_T = 150 Ω for Vcc = 3.3V
- R_T = 270 Ω for Vcc = 5.0V

Rs = 43Ω for Zo = 50Ω and Vcc = 3.0V to 5.5V

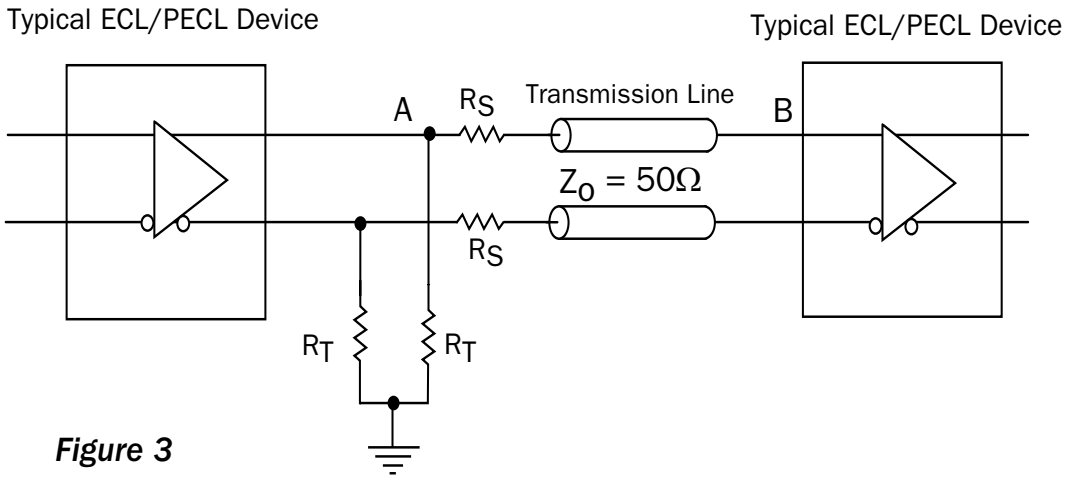

Figure 3

"Y" Scheme Termination

Another alternative would be the "Y" scheme termination as shown in figures 4 and 5. The advantage of using "Y" scheme termination is that it does not require an extra power supply for termination, it is cost effective and easy to implement. This scheme is applicable only to sources with differential outputs.

"Y" Termination Scheme for 5.0 V Power Supply

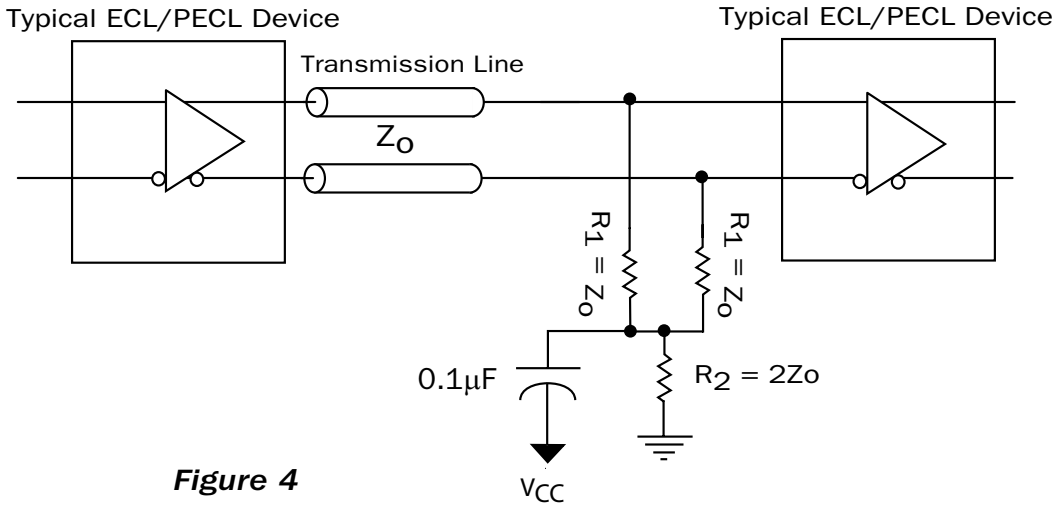

Figure 4

"Y" Termination Scheme for 3.3 V Power Supply

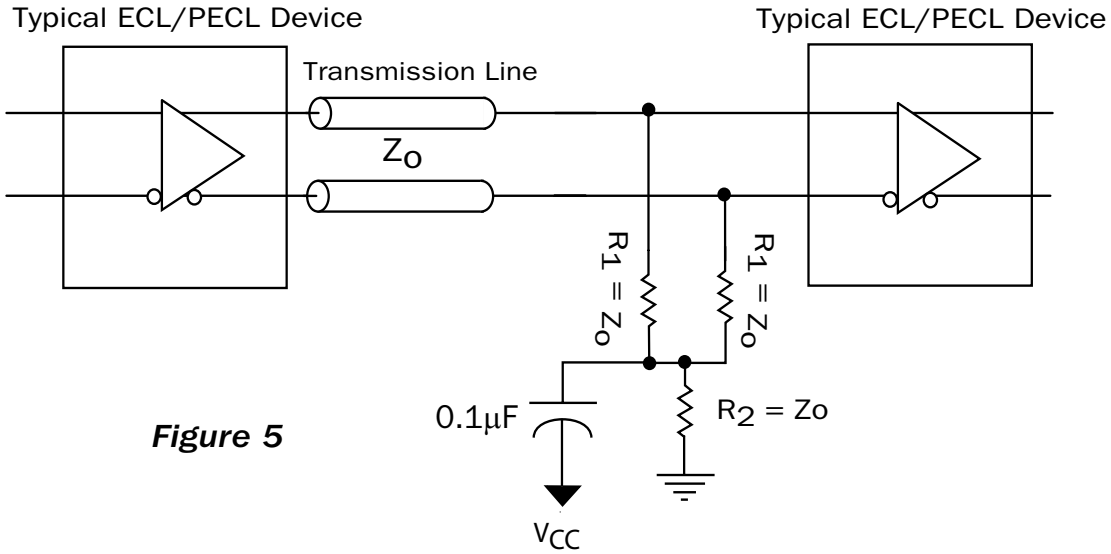

Figure 5

Capacitive Coupling Method

Some design applications require the ECL or PECL signals to be AC coupled due to nonstandard ECL signal levels coming from a source. In addition, capacitive coupling is a preferred way of interfacing either a signal from a 3.3V system to a 5.0V device or even interfacing ECL signals with PECL devices. Examples below show some of the suggested solutions for the AC coupled ECL or PECL type signals. When the destination device does not provide a VBB output pin for proper biasing when its inputs are AC coupled, the following scheme shown in figure 6 can be used.

- Values of R1 and R2 are determined based on the supply voltage range.
- $R_{Pulldown}$ =150Ω for V_{CC} = 3.0V and 270Ω for V_{CC} = 5.0V
- R1 = 68.5Ω for V_{CC} = 5.0V and 85Ω for V_{CC} = 3.3V
- R2 = 185Ω for V_{CC} = 5.0V and 122Ω for V_{CC} = 3.3V

When the destination device does provide a VBB output for proper biasing of its inputs in capacitive coupling mode, the solution in figure 7 should be used for proper signal interface.

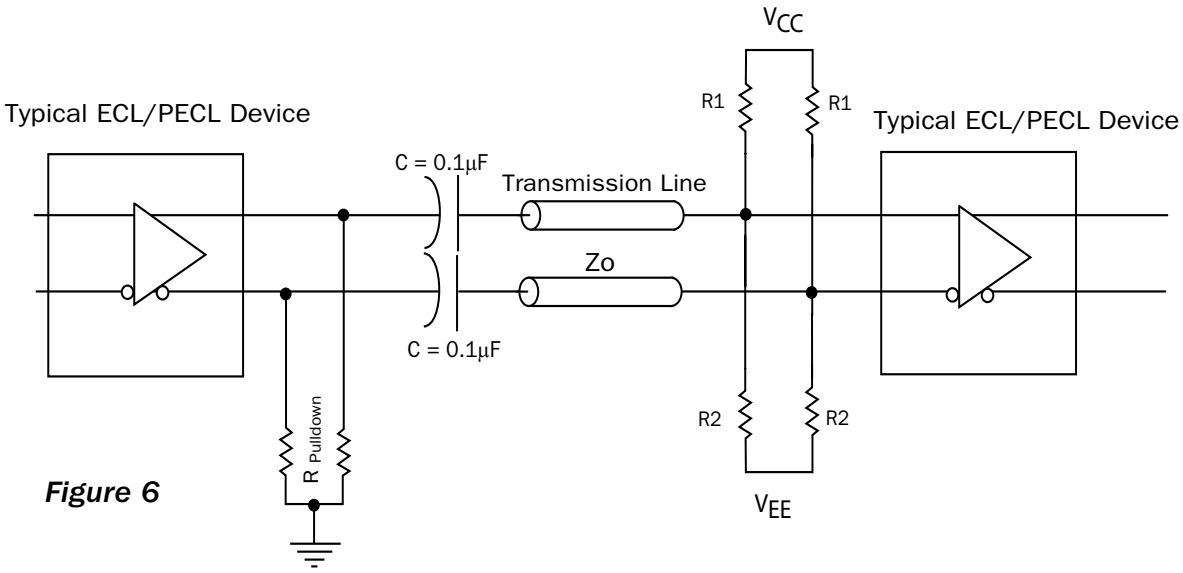

Figure 6

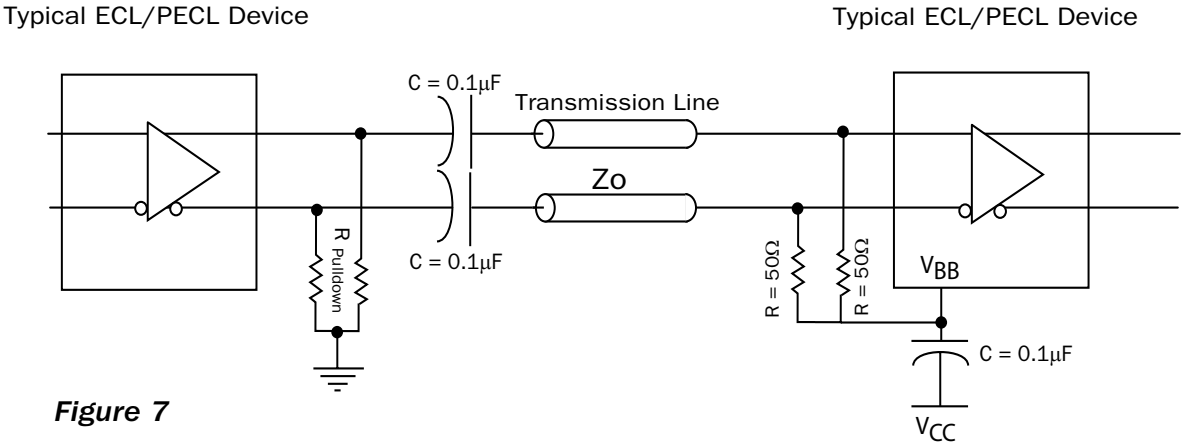

Figure 7

Pseudo Random Data in AC Coupled Environment

In applications where serial data does not have continuous transition from High to Low for a long period of time, the inputs of the receiver may reach the same potential level or null-state; in turn, this would make the system unstable. To prevent this problem, a high value resistor should be connected between the input of the receiver (usually the true input) and V_{CC}. Refer to figure 8 for further illustration.

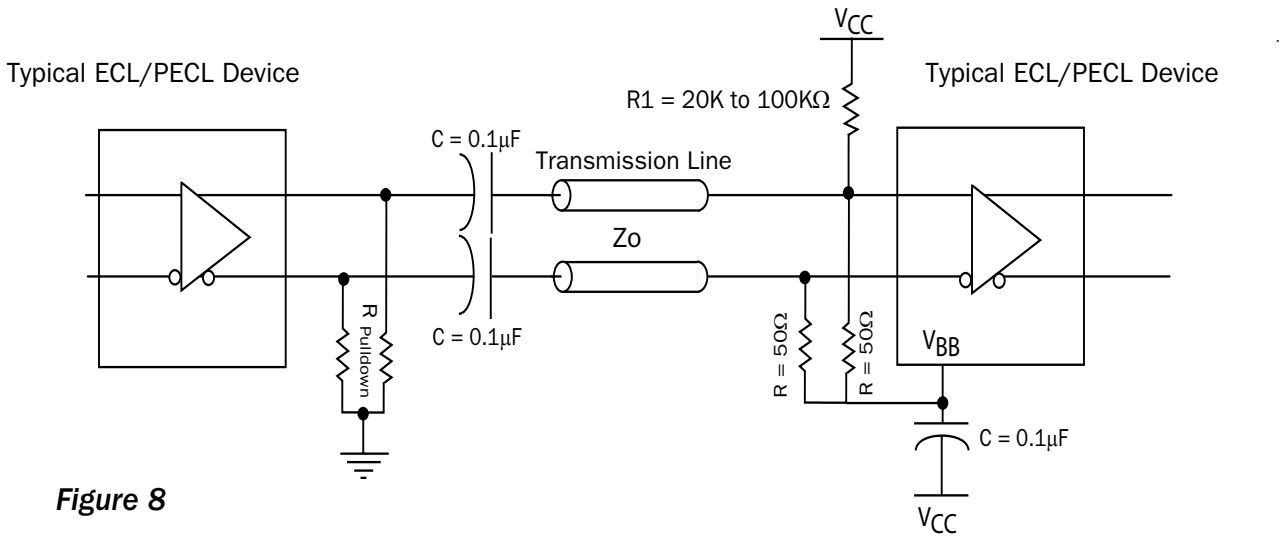

Figure 8

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