12-Bit, 500 kHz, Low-Power
Sampling A/D Converter

DATEL
INNOVATION and EXCELLENCE

FEATURES

· **12-Bit resolution**
· **Internal Sample/Hold**
· **500 kHz minimum throughput**
· **Functionally complete**
· **Small 24-pin DIP**
· **Low-power, 1.4 Watts**
· **Three-state output buffers**
· **No missing codes**
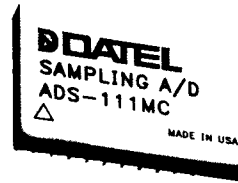
GENERAL DESCRIPTION

DATEL's ADS-111 is a 12-bit, functionally complete, sampling A/D converter that is packaged in a space-saving 24-pin DIP. A minimum throughput rate of 500 kHz is achieved while only dissipating 1.4 Watts.

Manufactured using thick-film and thin-film hybrid technology, a proprietary chip and unique laser trimming schemes, the ADS-111's exclusive performance is based upon a digitally-corrected subranging architecture.

DATEL
SAMPLING A/D
ADS-111MC
MADE IN USA

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	13	±5V
2	BIT 11 OUT	14	DIGITAL GROUND
3	BIT 10 OUT	15	EOC
4	BIT 9 OUT	16	START CONVERT
5	BIT 8 OUT	17	ENABLE (1-12)
6	BIT 7 OUT	18	COMP BIN
7	BIT 6 OUT	19	ANALOG INPUT
8	BIT 5 OUT	20	BIPOLAR
9	BIT 4 OUT	21	+10V REF
10	BIT 3 OUT	22	+15V
11	BIT 2 OUT	23	ANALOG GROUND
12	BIT 1 OUT (MSB)	24	-15V
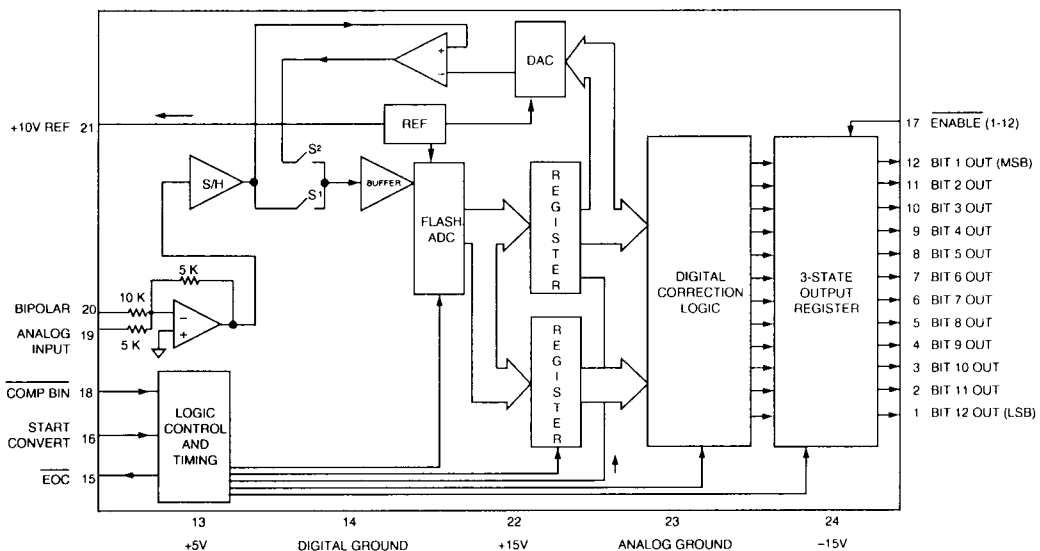
Figure 1. ADS-111 Simplified Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 22)	0 to +18	Volts dc
–15V Supply (Pin 24)	0 to –18	Volts dc
+5V Supply (Pin 13)	–0.5 to +7.0	Volts dc
Digital Inputs		
(Pins 16, 17, 18)	–0.3 to V_{DD} + 0.3	Volts dc
Analog Input (Pin 19)	–15 to +15	Volts dc
Lead Temp.(10 Sec.)	300 max	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
ADS-111	—	±5	—	Volts dc
(See Table 4 also)	—	0 to +10	—	Volts dc
Input Impedance	5.0	15.0	—	M Ohms
Input Capacitance	—	3	5	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	—	—	Volts dc
Logic "0"	—	—	0.5	Volts dc
Logic Loading "1"	—	—	5.0	µA
Logic Loading "0"	—	—	–600	µA
A/D PERFORMANCE				
Integral Non–Linearity				
+25 °C	—	±1/2	±3/4	LSB
0 °C to +70 °C	—	±1/2	±3/4	LSB
–55 C to +125 °C	—	—	±2	LSB
Differential Non–Linearity				
+25 °C	—	±1/2	±3/4	LSB
0 °C to +70 °C	—	±1/2	±3/4	LSB
–55 C to +125 °C	—	—	±1	LSB
Full Scale Absolute Accuracy				
+25 °C	—	±5	±10	LSB
0 °C to +70 °C	—	±6	±18	LSB
–55 C to +125 °C	—	±10	±32	LSB
Unipolar Zero Error,				
+25 °C (Tech Note 1)	—	±3	±5	LSB
Unipolar Zero Tempco	—	±15	±30	ppm/ °C
Bipolar Zero Error,				
+25 °C (Tech Note 1)	—	±3	±5	LSB
Bipolar Zero Tempco	—	±5	±8	ppm/ °C
Bipolar Offset Error,				
+25 °C (Tech Note 1)	—	±4	±8	LSB
Bipolar Offset Tempco	—	±20	±40	ppm/ °C
Gain Error, +25 °C	—	±4	±8	LSB
(See Tech Note 1)				
Gain Tempco	—	±20	±40	ppm/ °C
No Missing Codes (12 Bits)	Over the Operating Temp. Range.			

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels				
Logic "1"	2.4	—	—	Volts dc
Logic "0"	—	—	0.4	Volts dc
Logic Loading "1"	—	—	–160	µA
Logic Loading "0"	—	—	6.4	mA
Internal Reference				
Voltage, +25 °C	+9.98	+10.0	+10.02	Volts dc
Drift.	—	±5	±30	ppm/ °C
External Current	—	—	1.5	mA
Resolution	12 Bits			
Output Coding				
(Pin 18 Hi)	Straight binary/offset binary			
(Pin 18 Low)	Complementary binary			
	Complementary offset binary			
DYNAMIC PERFORMANCE				
Conversion Rate				
+25 °C	500	600	—	kHz
0 °C to +70 °C	500	600	—	kHz
–55 C to +125 °C	500	—	—	kHz
Total Harmonic Distortion				
DC to 60 kHz at Vin ≤5V p–p	—	–70	–65	dB
DC to 40 kHz at Vin = 10V p–p	—	–70	–65	dB
Slew Rate	—	90	—	V/µSec.
Aperture Delay Time	—	20	—	nSec.
Aperture Uncertainty	—	±100	—	pSec.
S/H Acquisition Time to 0.01% (10V step)				
+25 °C	—	—	715	nSec.
0 °C to +70 °C	—	—	765	nSec.
–55 °C to +125 °C	—	—	900	nSec.
(Sinusoidal Input)	—	—	465	nSec.
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
–15V dc Supply	–14.25	–15.0	–15.75	Volts dc
+5V dc Supply	+4.75	+5.0	+5.25	Volts dc
Power Supply Current				
+15V dc Supply	—	+38	+55	mA
–15V dc Supply	—	–38	–50	mA
+5V dc Supply*	—	+75	+95	mA
Power Dissipation	—	1.4	2.05	Watts
Power Supply Rejection	—	—	0.01	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range, Case				
–MC	0	—	+70	°C
–MM	–55	—	+125	°C
Storage Temperature Range	–65	—	+150	°C
Package Type	24–pin DIP			
Weight	0.42 ounces (12 grams), Max.			

* +5V power usage at 1 TTL logic loading per data output bit.

TECHNICAL NOTES

1. Applications which are unaffected by endpoint errors or re-move them through software will use the typical connections shown in Figure 3. Remove system errors or adjust the small initial errors of the ADS-111 to zero using the optional external circuitry shown in Figure 1. The external adjust-ment circuit has no affect on the throughput rate.

2. Always connect the analog and digital grounds to a ground plane beneath the converter for best performance. The ana-log and digital grounds are not connected internally.

3. Bypass the analog and digital supplies and the +10V reference (pin 21) to ground with a 4.7 μF, 25V tantalum electrolytic capacitor in parallel with a 0.1 μF ceramic capacitor. Bypass the +10V reference (pin 21) to analog ground (pin 23).

4. Obtain straight binary/offset binary output coding by tying COMP BIN (pin 18) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie COMP BIN (pin 18) to ground. This signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. To obtain three-state outputs, connect ENABLE (pin 17) to a logic "0" (low). Otherwise, connect pin 17 to a logic "1" (high).

6. Do not change the status of COMP BIN (pin 18) while EOC (pin 15) is high.

Table 1. Input Range Selection

INPUT RANGE	INPUT PIN	TIE TOGETHER
±5V dc	Pin 19	Pin 20 to Pin 21
0 to+10V dc	Pin 19	Pin 20 to Ground

Table 2. Zero and Gain Adjust

FSR	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V dc	+1.22mV dc	+9.9963V dc
±5V dc	+1.22mVdc	+4.9963V dc

Table 3. Input Ranges (using external calibration)

INPUT RANGE	R1	R2	UNIT
0 to +10V, ±5V	2	2	k Ohms
0 to +5V, ±2.5V	2	6	k Ohms
0 to +2.5V, ±1.25V	2	14	k Ohms
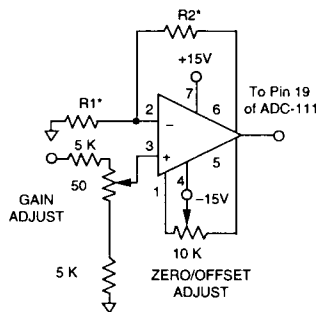
Figure 4. Optional Calibration Circuit

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3, Figure 4, and Table 1 for the appropriate full-scale range (FSR). Apply a pulse of 200 nanoseconds minimum to the START CONVERT input (pin 16) at a rate of 250 kHz. This rate reduces flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments
Apply a precision voltage reference source between the amplifier's analog input and ground. Adjust the output of the reference source per Table 3. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the pin 18 tied high (straight binary) or between 1111 1111 1111 and 1111 1111 1110 with pin 18 tied low (complementary binary).

For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with pin 18 tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with pin 18 tied low (complementary offset binary).

3. Full-Scale Adjustment
Set the output of the voltage reference used in step 2 to the value shown in Table 3. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for (pin 18) tied high or between 0000 0000 0001 and 0000 0000 0000 for (pin 18) tied low.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 4.
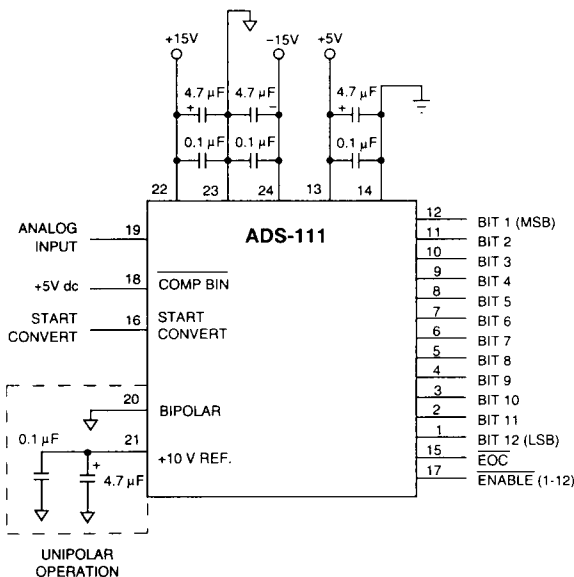

Figure 3. Typical ADS-111 Connection Diagram

Table 4. Output Coding for Bipolar Operation

INPUT RANGE 0 to +10V dc	UNIPOLAR SCALE	STRAIGHT BIN. OUTPUT CODING MSB LSB	COMP. BINARY OUTPUT CODING MSB LSB	BIPOLAR SCALE	INPUT RANGE ±5V dc
+9.9976V	+FS −1 LSB	1111 1111 1111	0000 0000 0000	+FS −1 LSB	+4.9976V
+8.7500V	7/8 FS	1110 0000 0000	0001 1111 1111	+3/4 FS	+3.7500V
+7.5000V	3/4 FS	1100 0000 0000	0011 1111 1111	+1/2 FS	+2.5000V
+5.0000V	1/2 FS	1000 0000 0000	0111 1111 1111	0	0.0000V
+2.5000V	1/4 FS	0100 0000 0000	1011 1111 1111	−1/2 FS	-2.5000V
+1.2500V	1/8 FS	0010 0000 0000	1101 1111 1111	+3/4 FS	-3.7500V
+0.0024V	1 LSB	0000 0000 0001	1111 1111 1110	−FS + 1 LSB	-4.9976V
0.0000V	0	0000 0000 0000	1111 1111 1111	−FS	-5.0000V
		OFF. BINARY	COMP. OFF. BIN.		

TIMING

Figure 2 shows the relationship between the various input signals. The timing shown applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design
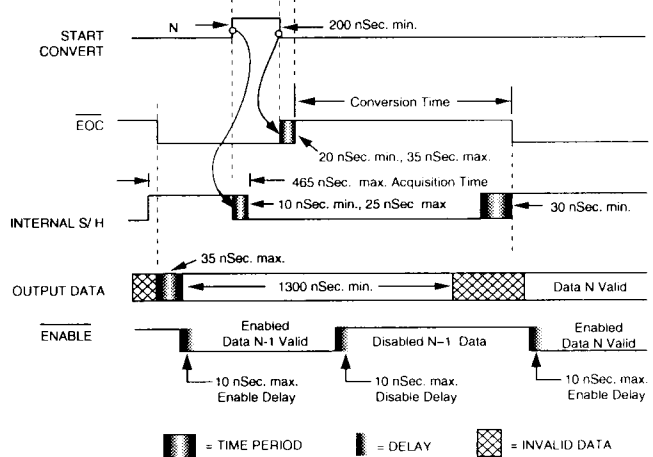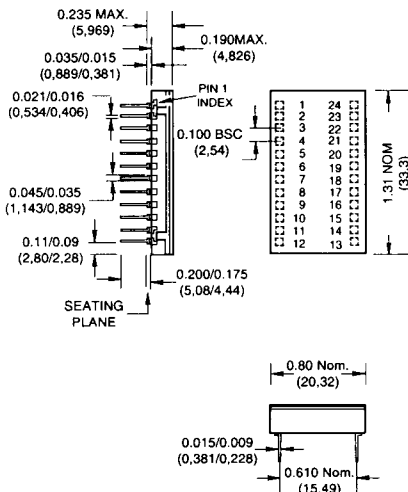

Figure 2. ADS-111 Timing Diagram

MECHANICAL DIMENSIONS
INCHES (mm)

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE
ADS-111MC	0 °C to +70 °C
ADS-111MM	-55 °C to +125 °C

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required.

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