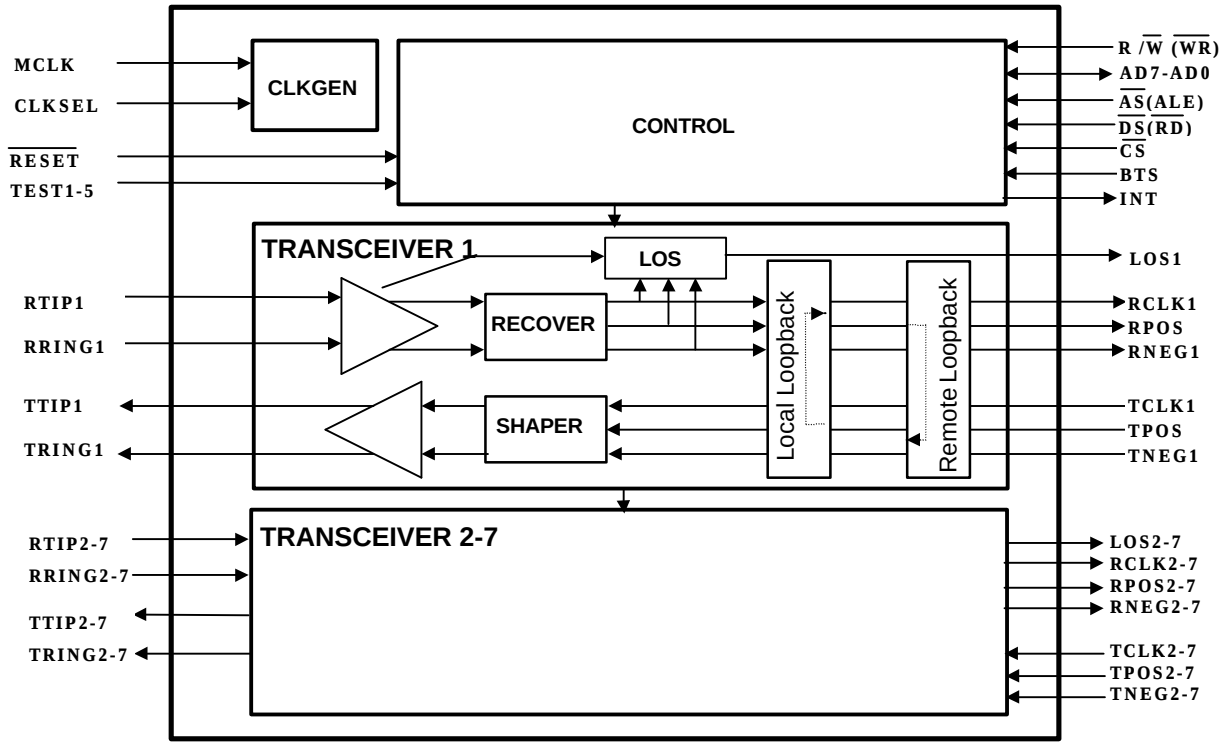
AK2546

7 channel T1 Transceiver

FEATURE

- 7ch short haul T1 transceiver
- Jitter Tolerance: Compliant with GR-499 Category I, II
- Transmitter Pulse Shape: Compliant with GR-499
- Loss of Signal Detection
- Selectable Signal Polarity
- Local/Remote Loopback
- Parallel Microprocessor Interface
- Single 3.3V±5% Operation
- Low Power Consumption (105mW/ch: Typ)
- Pin-to-pin compatible with AK2548 (7 channel E1 transceiver)
- Small Plastic Package 144pin LQFP

BLOCK DIAGRAM

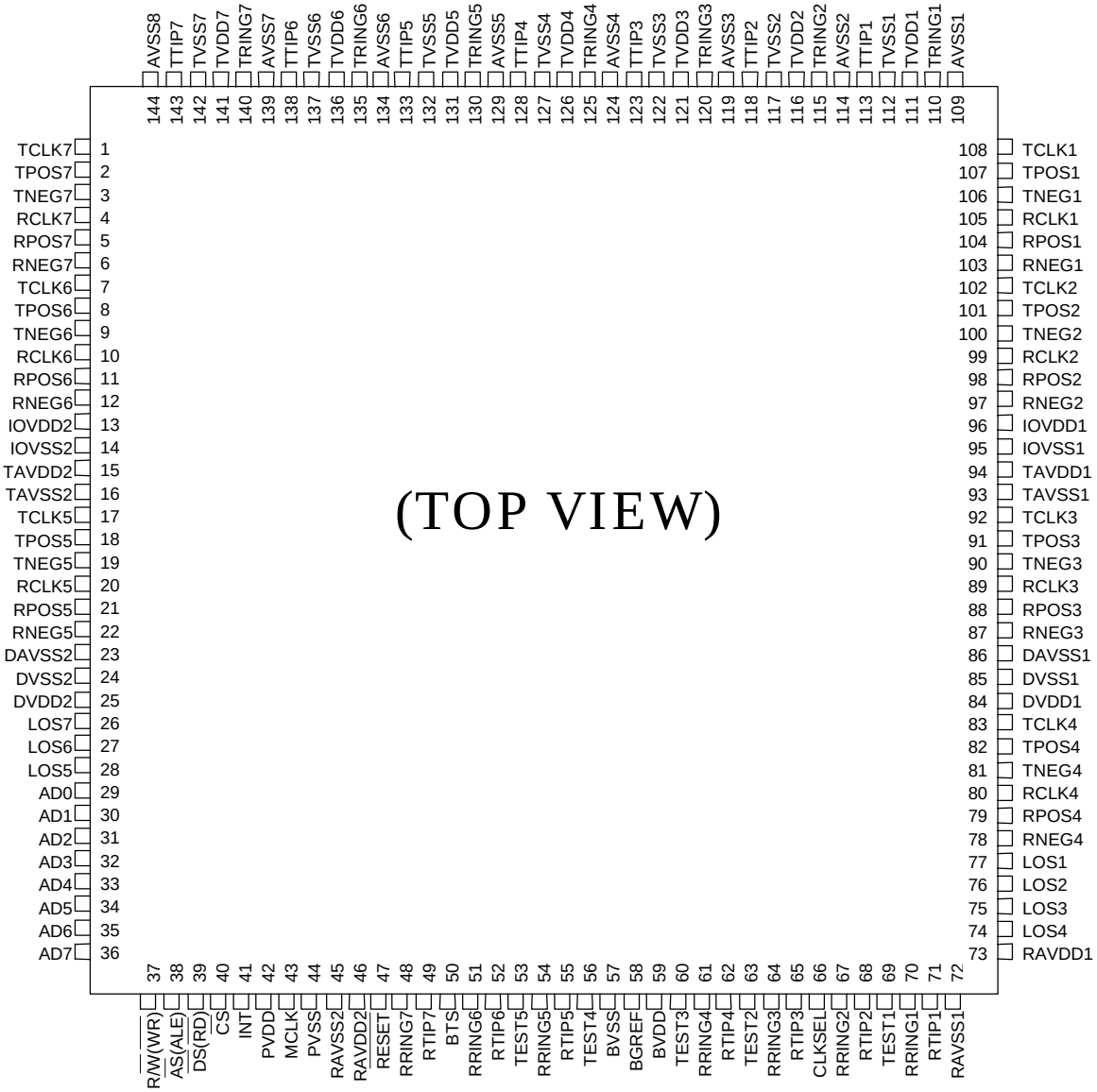


7 Channel T1 Transceiver Block Diagram

GENERAL DESCRIPTION

The AK2546 is the 7 channel short haul T1 transceiver for a SONET MUX, M13 MUX, etc.
It includes seven independent transmitters, clock and data recovery, LOS detector, control circuit in one LQFP-144 package which saves space, power consumption and the board design time. Internally generated transmit pulse provides the appropriate pulse shape for line length ranging from 0 to 655 feet from a DSX-1 cross connect.

PIN ASSIGNMENTS



PIN CONDITION

Pin No.	Pin Name	I/O	Pin Type	AC Load	DC Load	Comments
1	TCLK7	I	CMOS			
2	TPOS7	I	CMOS			
3	TNEG7	I	CMOS			
4	RCLK7	O	CMOS	≤15pF		
5	RPOS7	O	CMOS	≤15pF		
6	RNEG7	O	CMOS	≤15pF		
7	TCLK6	I	CMOS			
8	TPOS6	I	CMOS			
9	TNEG6	I	CMOS			
10	RCLK6	O	CMOS	≤15pF		
11	RPOS6	O	CMOS	≤15pF		
12	RNEG6	O	CMOS	≤15pF		
13	IOVDD2	I	Power			
14	IOVSS2	I	Power			
15	TAVDD2	I	Power			
16	TAVSS2	I	Power			
17	TCLK5	I	CMOS			
18	TPOS5	I	CMOS			
19	TNEG5	I	CMOS			
20	RCLK5	O	CMOS	≤15pF		
21	RPOS5	O	CMOS	≤15pF		
22	RNEG5	O	CMOS	≤15pF		
23	DAVSS2	I	Power			
24	DVSS2	I	Power			
25	DVDD2	I	Power			
26	LOS7	O	CMOS	≤15pF		
27	LOS6	O	CMOS	≤15pF		
28	LOS5	O	CMOS	≤15pF		
29	AD0	I/O	CMOS	≤50pF		
30	AD1	I/O	CMOS	≤50pF		
31	AD2	I/O	CMOS	≤50pF		
32	AD3	I/O	CMOS	≤50pF		
33	AD4	I/O	CMOS	≤50pF		
34	AD5	I/O	CMOS	≤50pF		
35	AD6	I/O	CMOS	≤50pF		
36	AD7	I/O	CMOS	≤50pF		

Pin No.	Pin Name	I/O	Pin Type	AC Load	DC Load	Comments
37	R/$\overline{W}$($\overline{WR}$)	I	CMOS			
38	$\overline{AS}$(ALE)	I	CMOS			
39	$\overline{DS}$($\overline{RD}$)	I	CMOS			
40	$\overline{CS}$	I	CMOS			
41	INT	O	Open drain			PMOS Open drain
42	PVDD	I	Power			
43	MCLK	I	CMOS			
44	PVSS	I	Power			
45	RAVSS2	I	Power			
46	RAVDD2	I	Power			
47	$\overline{RESET}$	I	CMOS			
48	RRING7	I	Analog			
49	RTIP7	I	Analog			
50	BTS	I	CMOS			
51	RRING6	I	Analog			
52	RTIP6	I	Analog			
53	TEST5	I	CMOS			Note1)
54	RRING5	I	Analog			
55	RTIP5	I	Analog			
56	TEST4	I	CMOS			Note1)
57	BVSS	I	Power			
58	BGREF	O	Analog		12kΩ	±1% accuracy
59	BVDD	I	Power			
60	TEST3	I	CMOS			Note1)
61	RRING4	I	Analog			
62	RTIP4	I	Analog			
63	TEST2	I	CMOS			Note2)
64	RRING3	I	Analog			
65	RTIP3	I	Analog			
66	CLKSEL	I	CMOS			
67	RRING2	I	Analog			
68	RTIP2	I	Analog			
69	TEST1	I	CMOS			Note1)
70	RRING1	I	Analog			
71	RTIP1	I	Analog			
72	RAVSS1	I	Power			

Pin No.	Pin Name	I/O	Pin Type	AC Load	DC Load	Comments
73	RAVDD1	I	Power			
74	LOS4	O	CMOS	≤15pF		
75	LOS3	O	CMOS	≤15pF		
76	LOS2	O	CMOS	≤15pF		
77	LOS1	O	CMOS	≤15pF		
78	RNEG4	O	CMOS	≤15pF		
79	RPOS4	O	CMOS	≤15pF		
80	RCLK4	O	CMOS	≤15pF		
81	TNEG4	I	CMOS			
82	TPOS4	I	CMOS			
83	TCLK4	I	CMOS			
84	DVDD1	I	Power			
85	DVSS1	I	Power			
86	DAVSS1	I	Power			
87	RNEG3	O	CMOS	≤15pF		
88	RPOS3	O	CMOS	≤15pF		
89	RCLK3	O	CMOS	≤15pF		
90	TNEG3	I	CMOS			
91	TPOS3	I	CMOS			
92	TCLK3	I	CMOS			
93	TAVSS1	I	Power			
94	TAVDD1	I	Power			
95	IOVSS1	I	Power			
96	IOVDD1	I	Power			
97	RNEG2	O	CMOS	≤15pF		
98	RPOS2	O	CMOS	≤15pF		
99	RCLK2	O	CMOS	≤15pF		
100	TNEG2	I	CMOS			
101	TPOS2	I	CMOS			
102	TCLK2	I	CMOS			
103	RNEG1	O	CMOS	≤15pF		
104	RPOS1	O	CMOS	≤15pF		
105	RCLK1	O	CMOS	≤15pF		
106	TNEG1	I	CMOS			
107	TPOS1	I	CMOS			
108	TCLK1	I	CMOS			

Pin No.	Pin Name	I/O	Pin Type	AC Load	DC Load	Comments
109	AVSS1	I	Power			
110	TRING1	O	Analog			driver output
111	TVDD1	I	Power			
112	TVSS1	I	Power			
113	TTIP1	O	Analog			driver output
114	AVSS2	I	Power			
115	TRING2	O	Analog			driver output
116	TVDD2	I	Power			
117	TVSS2	I	Power			
118	TTIP2	O	Analog			driver output
119	AVSS3	I	Power			
120	TRING3	O	Analog			driver output
121	TVDD3	I	Power			
122	TVSS3	I	Power			
123	TTIP3	O	Analog			driver output
124	AVSS4	I	Power			
125	TRING4	O	Analog			driver output
126	TVDD4	I	Power			
127	TVSS4	I	Power			
128	TTIP4	O	Analog			driver output
129	AVSS5	I	Power			
130	TRING5	O	Analog			driver output
131	TVDD5	I	Power			
132	TVSS5	I	Power			
133	TTIP5	O	Analog			driver output
134	AVSS6	I	Power			
135	TRING6	O	Analog			driver output
136	TVDD6	I	Power			
137	TVSS6	I	Power			
138	TTIP6	O	Analog			driver output
139	AVSS7	I	Power			
140	TRING7	O	Analog			driver output
141	TVDD7	I	Power			
142	TVSS7	I	Power			
143	TTIP7	O	Analog			driver output
144	AVSS8	I	Power			

Note1) Should be connected to VSS externally.

Note2) Should be connected to VDD externally

PIN DESCRIPTIONS

Pin Name	I/O	Function	Comment
T1 Transceiver			
TTIP1-7 TRING1-7	O O	Transmit Tip/Ring Output Bipolar output over transmit transformer	
TPOS1-7 TNEG1-7	I I	Transmit Positive/Negative Data Input Input on the falling edge of TCLK	
TCLK1-7	I	Transmit Clock Input	
RTIP1-7 RRING1-7	I I	Receive Tip/Ring Input Bipolar Input over receive transformer	
RPOS1-7 RNEG1-7	O O	Receive Positive/Negative Data Output Output on the falling edge of RCLK	
RCLK1-7	O	Receive Clock Output recovered from receive data input	
LOS1-7	O	Loss of signal output Output “high” when detect loss of signal LOSx output is not masked by MLOSx register.	
TVDD1-7		Positive Power Supply for the Transmit Driver	
TVSS1-7		Negative Power Supply for the Transmit Driver	
AVSS1-8		Analog ground	
Common Block			
MCLK	I	1.544MHz or 24.704MHz External Reference Clock Input	
$\overline{\text{AS}}$(ALE)	I	Address Select(Address Latch Enable) Input	
INT	O	Interrupt Output(PMOS open drain, should be tied to GND through a resistor), Active High, INT output goes “high” when the alarm is reported to any one of LOSx, LOTCx or LOMC registers. This pin can be masked by MLOSx, MLOTCx or MLOMC registers.	
$\overline{\text{DS}}$($\overline{\text{RD}}$)	I	Data Strobe(Read Enable) Input	
R/$\overline{\text{W}}$ ($\overline{\text{WR}}$)	I	Read/Write(Write Enable) Input	
$\overline{\text{CS}}$	I	Chip Select Input	
BTS	I	Bus Type Select Input BTS=“H” : Motorola Mode BTS=“L” : Intel Mode	
AD0-AD7	I/O	Address/Data Input/Output Used for read/write internal registers.	
CLKSEL	I	MCLK Select Input CLKSEL=“H”:1.544MHz CLKSEL=“L”:24.704MHz	
$\overline{\text{RESET}}$	I	Reset Input Active “Low” input pulse over 200ns initializes the internal circuit and forces RPOSx/RNEGx output “low” and LOSx output “high”.	

Pin Name	I/O	Function	Comment
Common block			
TEST1,3-5	I	Factory Use. Should be connected to VSS externally.	
TEST2	I	Factory Use. Should be connected to VDD externally.	
TAVDD1,2		Positive Power Supply for the analog circuitry in the transmitters	
TAVSS1,2		Negative Power Supply for the analog circuitry in the transmitters	
RAVDD1,2		Positive Power Supply for the digital circuitry in the transmitters	
RAVSS1,2		Negative Power Supply for the digital circuitry in the transmitters	
DVDD1,2		Positive Power Supply for Digital	
DVSS1,2		Negative Power Supply for Digital	
DAVSS1,2		Ground for Digital	
IOVDD1,2		Positive Power Supply for I/O	
IOVSS1,2		Negative Power Supply for I/O	
BVDD		Positive Power Supply for Reference Circuit	
BVSS		Negative Power Supply for Reference Circuit	
PVDD		Positive Power Supply for PLL	
PVSS		Negative Power Supply for PLL	
BGREF		Bandgap Reference Output. 12k ±1% external register should be connected across this pin and VSS.	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Typ	Max	Units	Condition
DC Supply	VDD	-0.3		6.5	V	
Input Voltage	VIN1	-0.3		VDD+0.3	V	Apply to except for RTIPx, RRINGx
	VIN2	-3		VDD+0.3	V	Apply to RTIPx, RRINGx
Input Current	IIN			10	mA	
Storage Temperature	Tstg	-55		130	°C	

Note) All voltages with respect to ground. :

All negative voltage pins = 0V. VDD apply to all positive voltage pins.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	min	typ	max	Units	Condition
DC Supply	VDD	3.135	3.3	3.465	V	3.3V±5%
Ambient Operating Temperature	Ta	-40	25	+85	°C	

Note) All voltages with respect to ground. :

All negative voltage pins = 0V. VDD apply to all positive voltage pins.

ELECTORICAL CHARACTERISTICS

DC CHARACTERISTICS

Parameter	Symbol	min	typ	max	Units	Condition
Power Consumption(/ch)	PD		105	260	mW	Note1
Digital High-Level Output Voltage	VOH	0.9VDD			V	IOH=-40µA
Digital Low-Level Output Voltage	VOL			0.4	V	IOL=500µA
Digital High-Level Input Voltage	VIH	0.7VDD			V	
Digital Low-Level Input Voltage	VIL			0.3VDD	V	
Input Leak Current	Ii			10	µA	
Output Current	IOL	1.0			mA	INT pin

Note1: typ : 50% mark, Room temp., VDD 3.3V, line length 399feet, Load 100Ω

max: 100% mark, Temp./VDD in all range, line length 655feet, Load 100Ω

Not include any other load (ex. External pull up register) except lines.

RECEIVER

Receiver characteristics are guaranteed on the conditions as shown below.

VDD=3.3V±5%, VSS, GND=0V, Ta=-40~85°C,

MCLK frequency: 1.544MHz±100ppm, 24.704MHz±100ppm,

Bipolar input frequency: 1.544MHz±130ppm(reference input level: $3V_{0p}$±20%)

Parameter	Symbol	Min	Typ	Max	Units	Condition
Sensitivity		-6			dB	Note1
Loss of Signal Threshold		0.35	0.5	0.7	V	Note2
Allowable Consecutive Zero before LOS		170	175	180	bits	
S/X tolerance				12	dB	Note3
Generated Jitter			30		nspp	Note4
Low pulse density immunity		1/16			Mark	
Jitter Tolerance	GR-499 Category I,II					

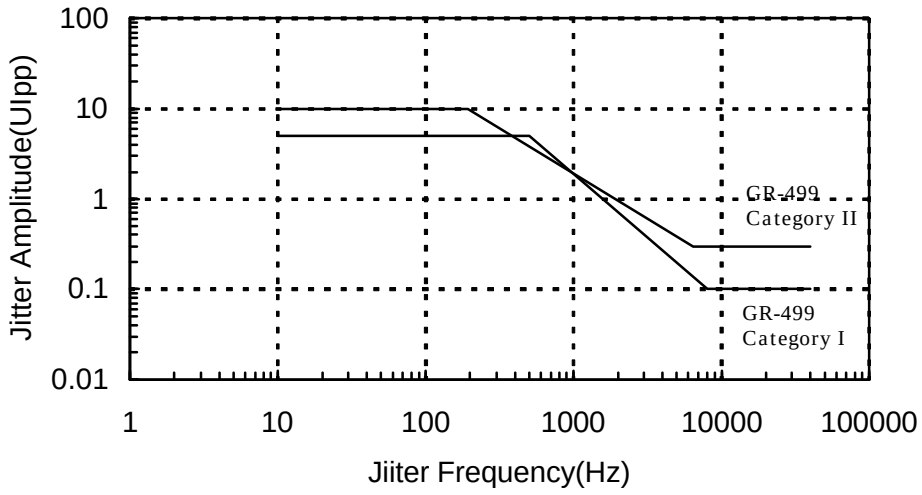
Note1: Relative value to the reference level. Compare at 772kHz with All Mark Pattern.

Note2: Level at the chip side of transformer. Loss of signal is logical AND between an analog loss of Signal monitors input level and a digital loss of signal check recovered data stream.

Note3: PN20 and AMI 1/8 Mark pattern input. Noise frequency is 770kHz.

Note4: PN20 pattern input.

JITTER TOLERANCE



TRANSMITTER

Transmitter characteristics are guaranteed on the conditions as shown below.

VDD=3.3V±5%, VSS, GND=0V,Ta=-40~85°C,

MCLK frequency: 1.544MHz±100ppm, 24.704MHz±100ppm

Parameter		Symbol	Min	Typ	Max	Units	Condition
Output Pulse Shape							GR-499,Note1
Output Pulse Amplitude			2.5	3.0	3.5	V_{0p}	Note1, Note2
Output Pulse Imbalance					0.4	dB	
Output Jitter	10Hz-8kHz				0.02	UIpp	
	10Hz-40kHz				0.025		
	8kHz-40kHz				0.025		
	Broad Band				0.05		
Power Levels@772kHz			12.6	15	17.9	dBm	Note3
Power Levels @1.544MHz					-29	dB	Note3, Note4

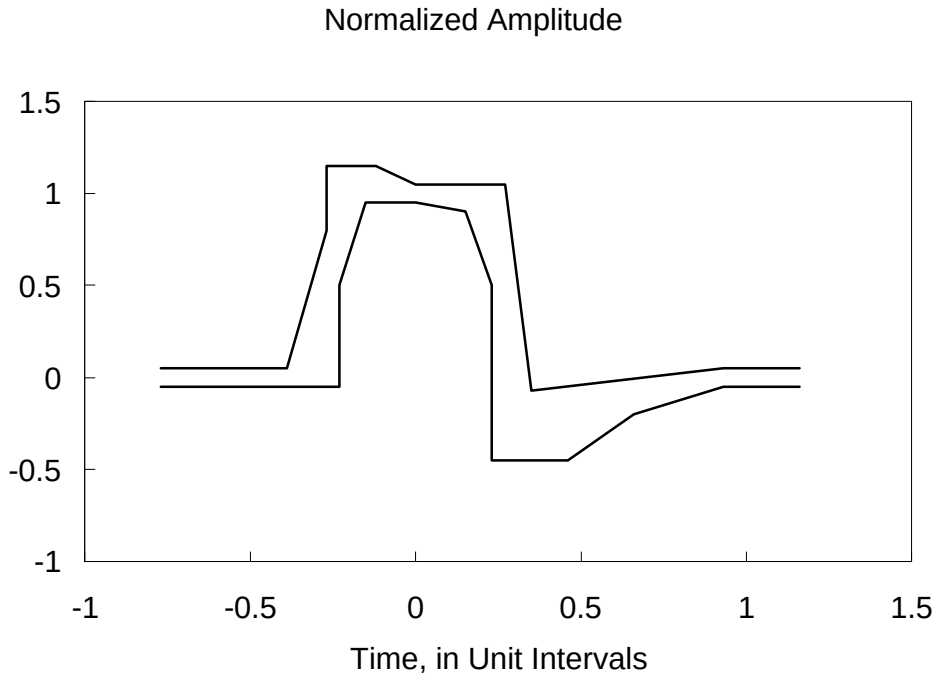
Note1: Measured at the DSX terminated with 100Ω.

Note2: Amplitude at the pulse center to normalize to unity.
Turns Ratio and DCR are recommended value.

Note3: Measured in a 2kHz band width around the specified frequency. Transmit all mark pattern.

Note4: Compare to the power at 772kHz

ISOLATED PULSE MASK (GR-499)



AC CHARACTERISTICS (Clock/Data)

Parameter		Symbol	Min	Typ	Max	Units	Condition
Clock Frequency	MCLK	Fci	1.543846 24.70153	1.544000 24.70400	1.544154 24.70647	MHz	±100ppm
Clock Pulse Width	MCLK TCLK	t_{pwhi} t_{pwli}		324		ns	Refer to Fig.2
Clock Pulse Width	RCLK	t_{pwho} t_{pwlo}		324		ns	Refer to Fig.1
Duty Cycle	RCLK TCLK			50		%	Note1
Setup/Hold Time	RCLK RPOS RNEG	t_{su1} t_{h1}	150			ns	Refer to Fig.1
Setup/Hold Time	TCLK TPOS TNEG	t_{su2} t_{h2}	50			ns	Refer to Fig.2
Rise Time	RCLK RPOS RNEG	t_r			100	ns	Refer to Fig.3 Note2
Fall Time	TCLK TPOS TNEG	t_f			40	ns	Refer to Fig.3 Note2

Note1) Duty Cycle:$(t_{pwho}/(t_{pwho}+t_{pwlo}))\times 100\%$

Note2) Drive 15pF Load Capacitance

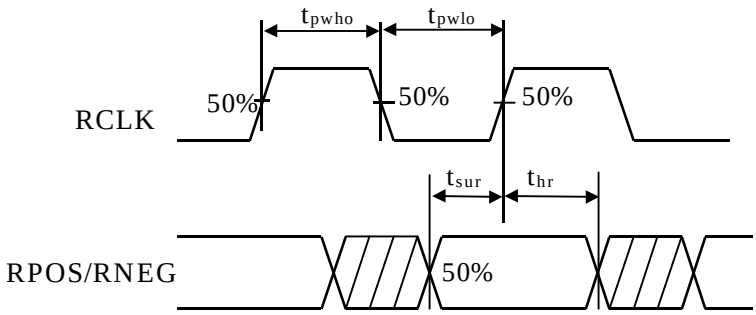


Fig.1 Receiver Timing

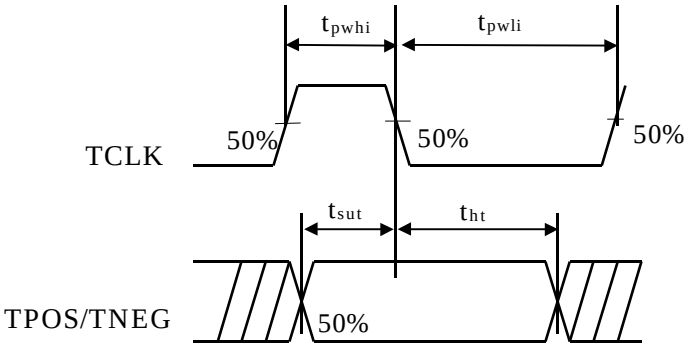


Fig.2 Transmitter Timing

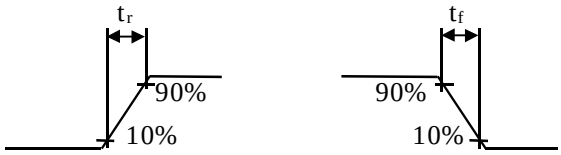


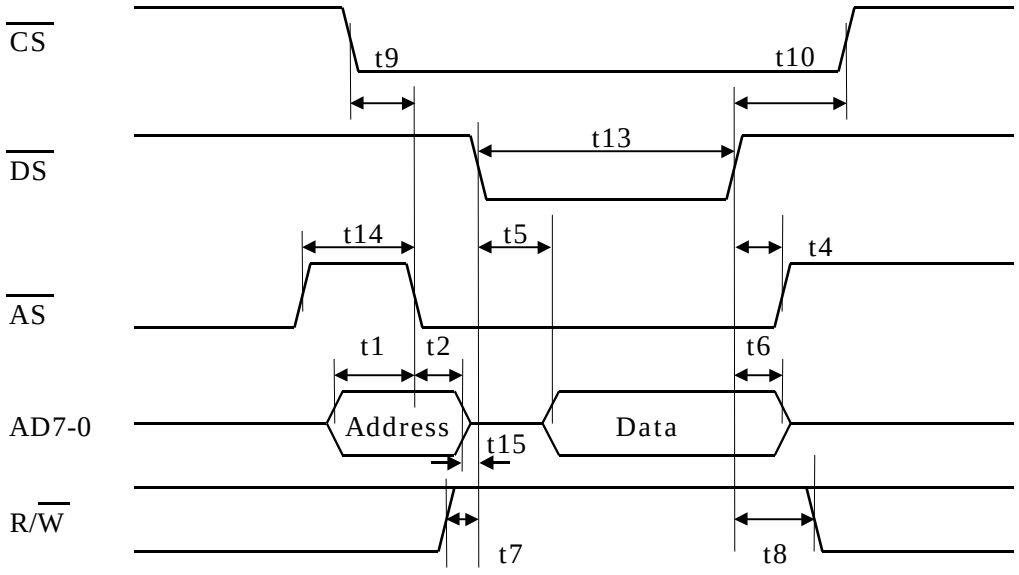
Fig.3 Rise and Fall Times
(RCLK, RPOS, RNEG, TCLK, TPOS, TNEG)

AC CHARACTERISTICS (Parallel Port)

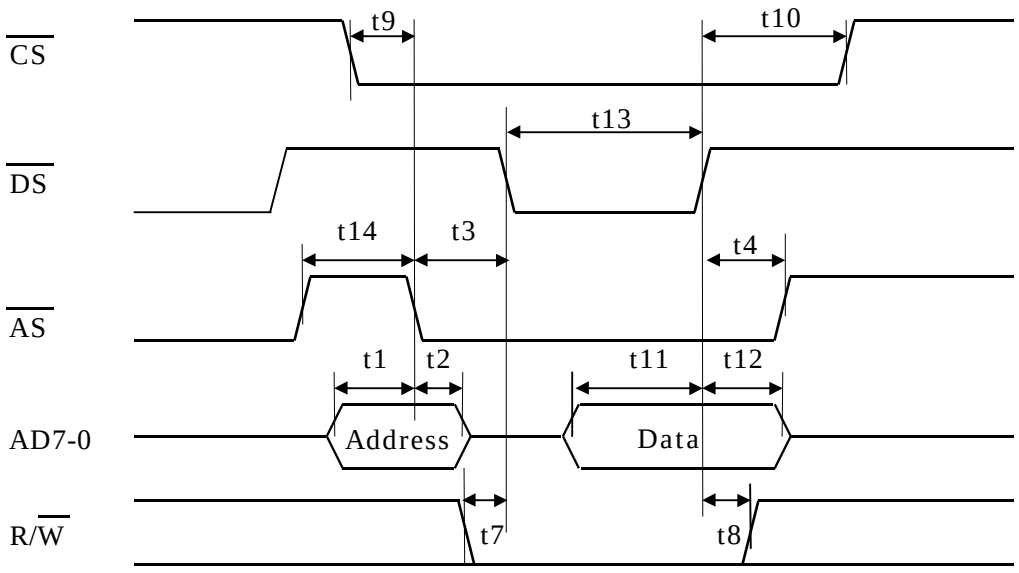
Parameter	Symbol	Min	Typ	Max	Units	Condition
Read/Write Cycle	tcyc	250			ns	
Motorola Mode						
Address Setup Time	t1	10	—	—	ns	
Address Hold Time	t2	10	—	—	ns	
$\overline{AS}$ to $\overline{DS}$ Delay Time	t3	20	—	—	ns	
$\overline{DS}$ to $\overline{AS}$ Delay Time	t4	20	—	—	ns	
Read Data Delay Time	t5	—	—	40	ns	
Read Data Hold Time	t6	—	—	20	ns	
R/$\overline{W}$ Setup Time	t7	10	—	—	ns	
R/$\overline{W}$ Hold Time	t8	10	—	—	ns	
$\overline{CS}$ Setup Time	t9	10	—	—	ns	
$\overline{CS}$ Hold Time	t10	15	—	—	ns	
Write Data Setup Time	t11	40	—	—	ns	
Write Data Hold Time	t12	20	—	—	ns	
$\overline{DS}$ Pulse Width	t13	100	—	—	ns	
$\overline{AS}$ Pulse Width	t14	20	—	—	ns	
Address Invalid to $\overline{DS}$ Delay Time	t15	0	—	—	ns	
Intel Mode						
Address Setup Time	t21	10	—	—	ns	
Address Hold Time	t22	10	—	—	ns	
ALE to $\overline{WR}$ Delay Time	t23	20	—	—	ns	
$\overline{WR}$ to ALE Delay Time	t24	20	—	—	ns	
$\overline{RD}$ to ALE Delay Time	t25	20	—	—	ns	
Read Data Delay Time	t26	—	—	40	ns	
Read Data Hold Time	t27	—	—	20	ns	
$\overline{CS}$ Setup Time	t28	10	—	—	ns	
$\overline{CS}$ Hold Time	t29	15	—	—	ns	
Write Data Setup Time	t30	40	—	—	ns	
Write Data Hold Time	t31	20	—	—	ns	
$\overline{RD}$ Pulse Width	t32	100	—	—	ns	
$\overline{WR}$ Pulse Width	t33	100	—	—	ns	
ALE Pulse Width	t34	20	—	—	ns	
Address Invalid to $\overline{RD}$ Delay Time	t35	0	—	—	ns	

Notes) CL= 50pF on AD0-AD7. All of the timing is specified at 50%VDD.

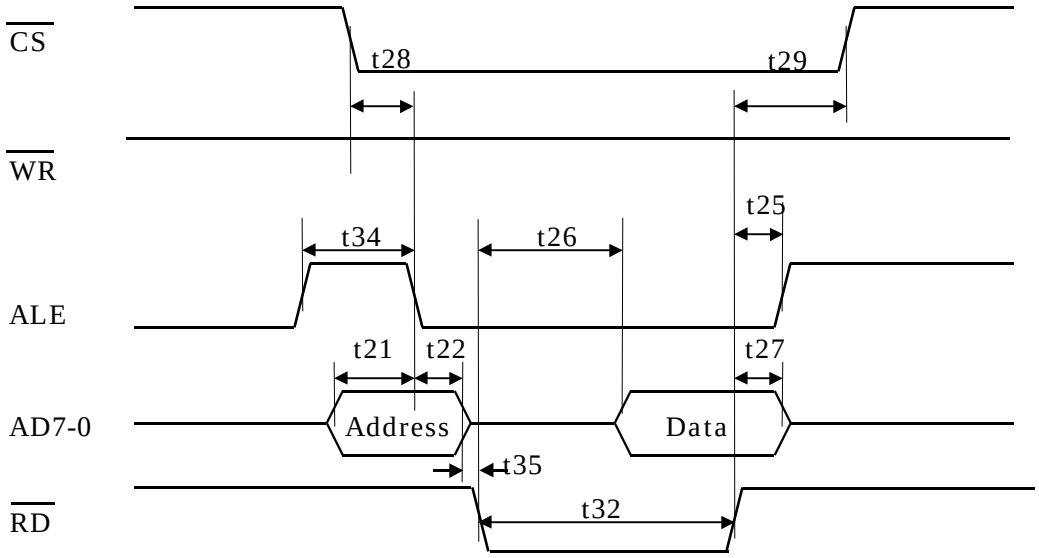
Motorola Mode(READ)



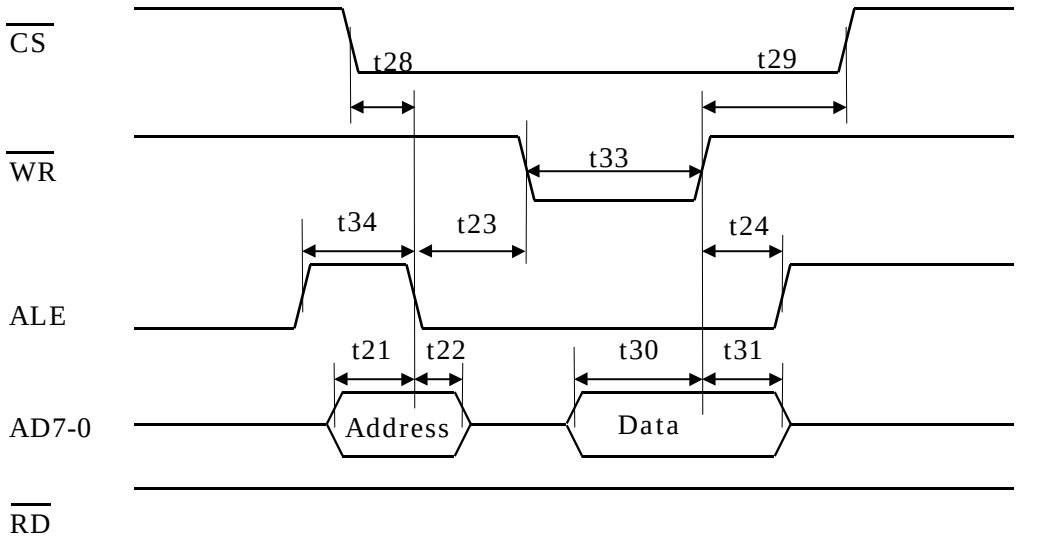
Motorola Mode(WRITE)



Intel Mode(READ)



Intel Mode(WRITE)



REGISTER DESCRIPTION

REGISTER MAP

*A7-A4="0"

Address				Function							
A3	A2	A1	A0	Bit7 <AD7>	Bit6 <AD6>	Bit5 <AD5>	Bit4 <AD4>	Bit3 <AD3>	Bit2 <AD2>	Bit1 <AD1>	Bit0 <AD0>
Status Register (READ ONLY)											
0	0	0	0	LOS7 (1)	LOS6 (1)	LOS5 (1)	LOS4 (1)	LOS3 (1)	LOS2 (1)	LOS1 (1)	0
0	0	0	1	LOTC7 (1)	LOTC6 (1)	LOTC5 (1)	LOTC4 (1)	LOTC3 (1)	LOTC2 (1)	LOTC1 (1)	LOMC (1)
Mask Control Register (WRITE/READ)											
0	0	1	0	MLOS7 (1)	MLOS6 (1)	MLOS5 (1)	MLOS4 (1)	MLOS3 (1)	MLOS2 (1)	MLOS1 (1)	RDEN (0)
0	0	1	1	MLOTC7 (1)	MLOTC6 (1)	MLOTC5 (1)	MLOTC4 (1)	MLOTC3 (1)	MLOTC2 (1)	MLOTC1 (1)	MLOMC (1)
Channel Control Register (WRITE/READ)											
0	1	1	0	LENG31 (0)	LENG21 (0)	LENG11 (0)	RLOOP1 (0)	LLOOP1 (0)	POLN1 (1)	MSK1 (1)	PD1 (1)
0	1	1	1	LENG32 (0)	LENG22 (0)	LENG12 (0)	RLOOP2 (0)	LLOOP2 (0)	POLN2 (1)	MSK2 (1)	PD2 (1)
1	0	0	0	LENG33 (0)	LENG23 (0)	LENG13 (0)	RLOOP3 (0)	LLOOP3 (0)	POLN3 (1)	MSK3 (1)	PD3 (1)
1	0	0	1	LENG34 (0)	LENG24 (0)	LENG14 (0)	RLOOP4 (0)	LLOOP4 (0)	POLN4 (1)	MSK4 (1)	PD4 (1)
1	0	1	0	LENG35 (0)	LENG25 (0)	LENG15 (0)	RLOOP5 (0)	LLOOP5 (0)	POLN5 (1)	MSK5 (1)	PD5 (1)
1	0	1	1	LENG36 (0)	LENG26 (0)	LENG16 (0)	RLOOP6 (0)	LLOOP6 (0)	POLN6 (1)	MSK6 (1)	PD6 (1)
1	1	0	0	LENG37 (0)	LENG27 (0)	LENG17 (0)	RLOOP7 (0)	LLOOP7 (0)	POLN7 (1)	MSK7 (1)	PD7 (1)

*Other address is reserved.

* Initial value is in ( ).

*"<>" show I/O pin name. Address A0-A3 should be input via AD0-AD3 pins.

STATUS REGISTER

Symbol	Description
LOSx (x=1 to 7)	Loss of signal alarm for channel x. Read only register. When the loss of signal is detected, LOSx is set High.
LOTCx (x=1 to 7)	Loss of TCLK alarm for channel x. Read only register. When the loss of TCLKx is detected, LOTCx is set High.
LOMC	Loss of MCLK alarm. Read only register. When the loss of MCLK is detected, LOMC is set High.

MASK CONTROL

Symbol	Description
MLOSx (x=1 to 7)	Mask loss of signal alarm for channel x. MLOSx is active-high to prevent LOSx from setting INT output “high”. It is possible to read LOSx register regardless of the status of MLOSx. Initial value is “high”.
MLOTCx (x=1 to 7)	Mask loss of TCLK alarm for channel x. MLOTCx is active-high to prevent LOTCx from setting INT output “high”. It is possible to read LOTCx register regardless of the status of MLOTCx. Initial value is “high”.
MLOMC	Mask loss of MCLK alarm. MLOMC is active-high to prevent LOMC from setting INT output “high”. It is possible to read LOMC register regardless of the status of MLOMC. Initial value is “high”. When the loss of MCLK is detected, LOSx register and LOSx pins are set “high” at the same time. Therefore all MLOSx register must be set “high” to prevent loss of MCLK from setting INT output. In this case, LOMC can be read.

CHANNEL CONTROL REGISTER

Symbol	Description
LENGyx	The generated transmit pulse in channel x provides the appropriate pulse shape for line length from a DSX-1 cross connect through the setting of this register as shown below in Table 1.
RLOOPx/ LLOOPx	Loopback mode of channel x is activated through the setting of these registers as shown below in Table 2.
POLNx	This register as shown in Table 3 controls TIPx/RINGx output polarity. Initial value is “high”.
PDx	PDx is active-high to set the corresponding transceiver in power down mode. The impedance between TTIP and TRING is set to 30kΩ(typ). LOSx goes “high” in power down mode. Initial value is “high”.
MSKx	MSKx is active-high to prevent LOSx or LOTCx from setting INT output “high”. Initial value is “high”.
RDEN	RDEN is active-high to prevent RCLK, RPOS, and RNEG output from forcing to “low” or “high” by the detection of Loss of signal. Initial value is “low”.

Table 1. Pulse Shape Control

LENG3x	LENG2x	LENG1x	Line Length
0	0	0	0-133feet (Initial Value)
0	0	1	133-266feet
0	1	0	266-399feet
0	1	1	399-533feet
1	0	0	533-655feet

Table 2. Loopback mode Select

RLOOPx	LLOOPx	Function
0	0	Normal (Initial value)
0	1	Local Loop back
1	0	Remote Loop back
1	1	Inhibited

Table 3. TIPx/RINGx Polarity Control

POLNx	POSx/NEGx	TIPx/RINGx
1	0	space
	1	mark
0	0	mark
	1	space

OUTPUT CONTROL

*: don't care

LOS: LOSx output and LOSx register

Reset, Loss of MCLK, Power down

$\overline{\text{RESET}}$	MCLK	PD	Loopback		POLN	RDEN	TCLK	Receive signal	TTIP TRING	RCLK	RPOS RNEG	LOS
			Local	Remote								
0	*	*	*	*	*	*	*	*	0(Note 1)	0	0	1
1	loss	*	*	*	1	*	*	*	0	0	0	1
1	loss	*	*	*	0	*	*	*	0	0	1	1
1	clocked	1	*	*	1	*	*	*	0(Note 1)	0	0	1
1	clocked	1	*	*	0	*	*	*	0(Note 1)	0	1	1

Normal Operation($\overline{\text{RESET}}$=1, MCLK: Clocked, PD=0)

Loopback		POLN	RDEN	TCLK	Receive signal	TTIP TRING	RCLK	RPOS RNEG	LOS
Local	Remote								
0	0	1	*	clocked	in	TPOS TNEG	RCLK	RTIP RRING	0
0	0	1	0	clocked	loss	TPOS TNEG	0	0	1
0	0	1	*	loss	in	0	RCLK	RTIP RRING	0
0	0	1	0	loss	loss	0	0	0	1
0	0	1	1	clocked	loss	TPOS TNEG	RCLK	RTIP RRING	1
0	0	1	1	loss	loss	0	RCLK	RTIP RRING	1
0	0	0	*	clocked	in	$\overline{\text{TPOS}}$ TNEG	RCLK	$\overline{\text{RTIP}}$ RRING	0
0	0	0	0	clocked	loss	$\overline{\text{TPOS}}$ TNEG	0	1	1
0	0	0	*	loss	in	0	RCLK	$\overline{\text{RTIP}}$ RRING	0
0	0	0	0	loss	loss	0	0	1	1
0	0	0	1	clocked	loss	$\overline{\text{TPOS}}$ TNEG	RCLK	$\overline{\text{RTIP}}$ RRING	1
0	0	0	1	loss	loss	0	RCLK	$\overline{\text{RTIP}}$ RRING	1

Remote Loopback($\overline{\text{RESET}}$=1, MCLK: Clocked, PD=0)

Loopback		POLN	RDEN	TCLK	Receive	TTIP	RCLK	RPOS	LOS
Local	Remote				signal	TRING		RNEG	
0	1	1	*	*	in	RTIP RRING	RCLK	RTIP RRING	0
0	1	1	0	*	loss	RTIP RRING	0	0	1
0	1	1	1	*	loss	RTIP RRING	RCLK	RTIP RRING	1
0	1	0	*	*	in	RTIP RRING	RCLK	$\overline{\text{RTIP}}$ $\overline{\text{RRING}}$	0
0	1	0	0	*	loss	RTIIP RRING	0	1	1
0	1	0	1	*	loss	RTIP RRING	RCLK	$\overline{\text{RTIP}}$ $\overline{\text{RRING}}$	1

Local Loopback($\overline{\text{RESET}}$=1, MCLK: Clocked, PD=0)

Loopback		POLN	RDEN	TCLK	Receive	TTIP	RCLK	RPOS	LOS
Local	Remote				signal	TRING		RNEG	
1	0	1	*	clocked	in	TPOS TNEG	TCLK (Note 2)	TPOS TNEG	0
1	0	1	*	clocked	loss	TPOS TNEG	TCLK (Note 2)	TPOS TNEG	1
1	0	1	*	loss	in	0	0	0	0
1	0	1	*	loss	loss	0	0	0	1
1	0	0	*	clocked	in	TPOS TNEG	TCLK (Note 2)	TPOS TNEG	0
1	0	0	*	clocked	loss	TPOS TNEG	TCLK (Note 2)	TPOS TNEG	1
1	0	0	*	loss	in	0	0	1	0
1	0	0	*	loss	loss	0	0	1	1

Note 1) The impedance between TTIP and TRING is 30kΩ(typ).

Note 2) The phase of the TCLK satisfies receive output timing.

THEORY OF OPERATION

Loss of signal

Loss of signal in channel x is reported by setting LOSx register “high”.
The receiver will indicate loss of signal upon receiving 175 consecutive zeros or detecting input level being below the threshold (ALOS).
LOSx returns to “low” when the received signal returns to 12.5% ones density and not including 100 consecutive zeros. (GR-820)

When Loss of Signal is detected in channel x, LOSx register is set “high” and LOSx pin becomes “high”. When LOSx is set “high”, interrupt will be issued on INT pin if MLOSx is “low”. LOSx pin becomes high regardless of MLOSx status. MLOSx is active-high and masks LOSx interrupt. LOSx registers and LOSx pins represent the current status of received signal regardless of the MLOSx status.

Loss of TCLK

Loss of TCLKx is reported by setting LOTCx “high”. When LOTCx is set “high”, INT output becomes “high” if MLOTCx is “low”. MLOTCx is active-high and masks LOTCx interrupt. LOTCx represents the current status of TCLKx and can be read regardless of MLOTCx status. When Loss of TCLKx is detected, TTIPx/TRINGx will be forced to “0”.

Loss of MCLK

Loss of MCLK is reported by setting LOMC “high”. When LOMC is set “high”, INT output becomes “high” if MLOMC is “low”. MLOMC is active-high and masks LOMC interrupt. LOMC represents the current status of MCLK and can be read regardless of MLOMC status. When the loss of MCLK is detected, LOSx register and LOSx pin goes “high” at the same time. Therefore all MLOSx register must be set to “high” to prevent loss of MCLK from setting INT output

INT output

INT output becomes “high” when the alarm is reported to any one of LOSx, LOTCx or LOMC registers. This pin can be masked by MLOSx, MLOTCx or MLOMC registers.

Local Loopback

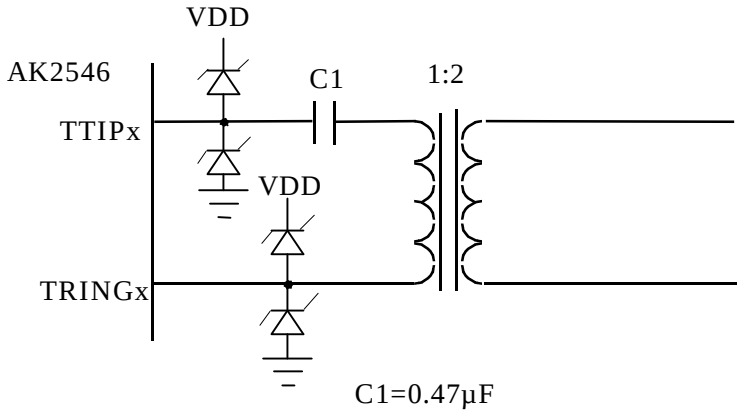
In Local Loopback mode, TPOSx, TNEGx, TCLKx signals are looped back to RPOSx, RNEGx, RCLKx output. RTIPx, RRINGx inputs are ignored but loss of signal detection is active.
The transmitter in channel x outputs TTIPx, TRINGx normally.

Remote Loopback

In Remote Loopback mode, RTIPx/RRINGx signals are looped back to TTIPx/TRINGx output.
The receiver in channel x output RPOSx, RNEGx, RCLKx normally and detect loss of signal.
TPOSx, TNEGx, TCLKx inputs are ignored.

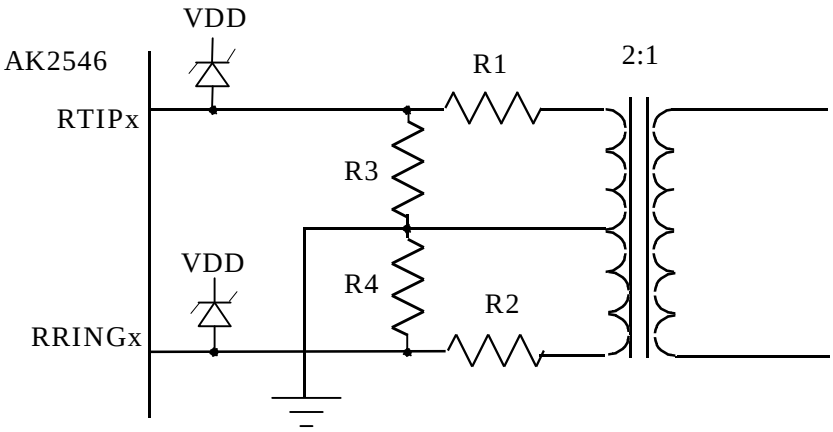
RECOMMENDED EXTERNAL CIRCUIT

Transmit Circuit



C1=0.47µF

Received Circuit



R1=R2=68Ω

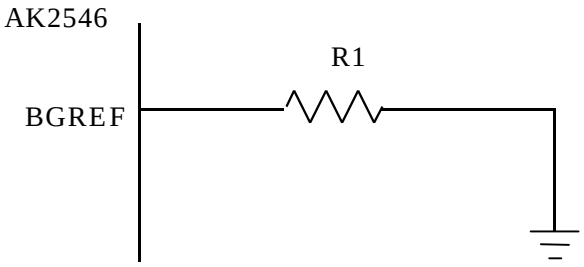
R3=R4=130Ω

Recommended Transformer Specification

	Turns Ratio (Typ)	Primary Inductance (Min)	Leakage Inductance (Max)	Interwinding Capacitance (Max)	DCR (Max)	
					pri	sec
Tx	1:2	720µH	0.3µH	30pF	0.6Ω	1.2Ω
Rx	1:2	720µH	0.3µH	30pF	0.6Ω	1.2Ω

Reference current circuit

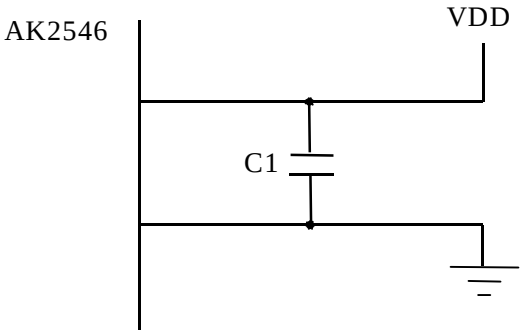
To determine input reference current, connect 12kΩ±1% resistor.



R1=12kΩ±1%

Power Supply

To attenuate the power supply noise, connect capacitors between VDD and VSS respectively. The value of the capacitance AK2546 need depend on the condition of the power supply line. Please decide the value of the capacitance after your evaluation.



Pin name	C1
RAVDD1-RAVSS1, RAVDD2-RAVSS2, BVDD-BVSS, TAVDD1-TAVSS1, TAVDD2-TAVSS2	1µF
TVDD1-TVSS1, TVDD2-TVSS2, TVDD3-TVSS3, TVDD4-TVSS4, TVDD5-TVSS5, TVDD6-TVSS6, TVDD7-TVSS7, IOVDD1-IOVSS1, IOVDD2-IOVSS2, DVDD1-DVSS1, DVDD2-DVSS2, PVDD-PVSS	0.01µF

Recommended conditions for PCB board

For the performance of noise and heat, the board design must be taken care.

Recommended conditions for PCB board is shown below.

Recommended conditions:

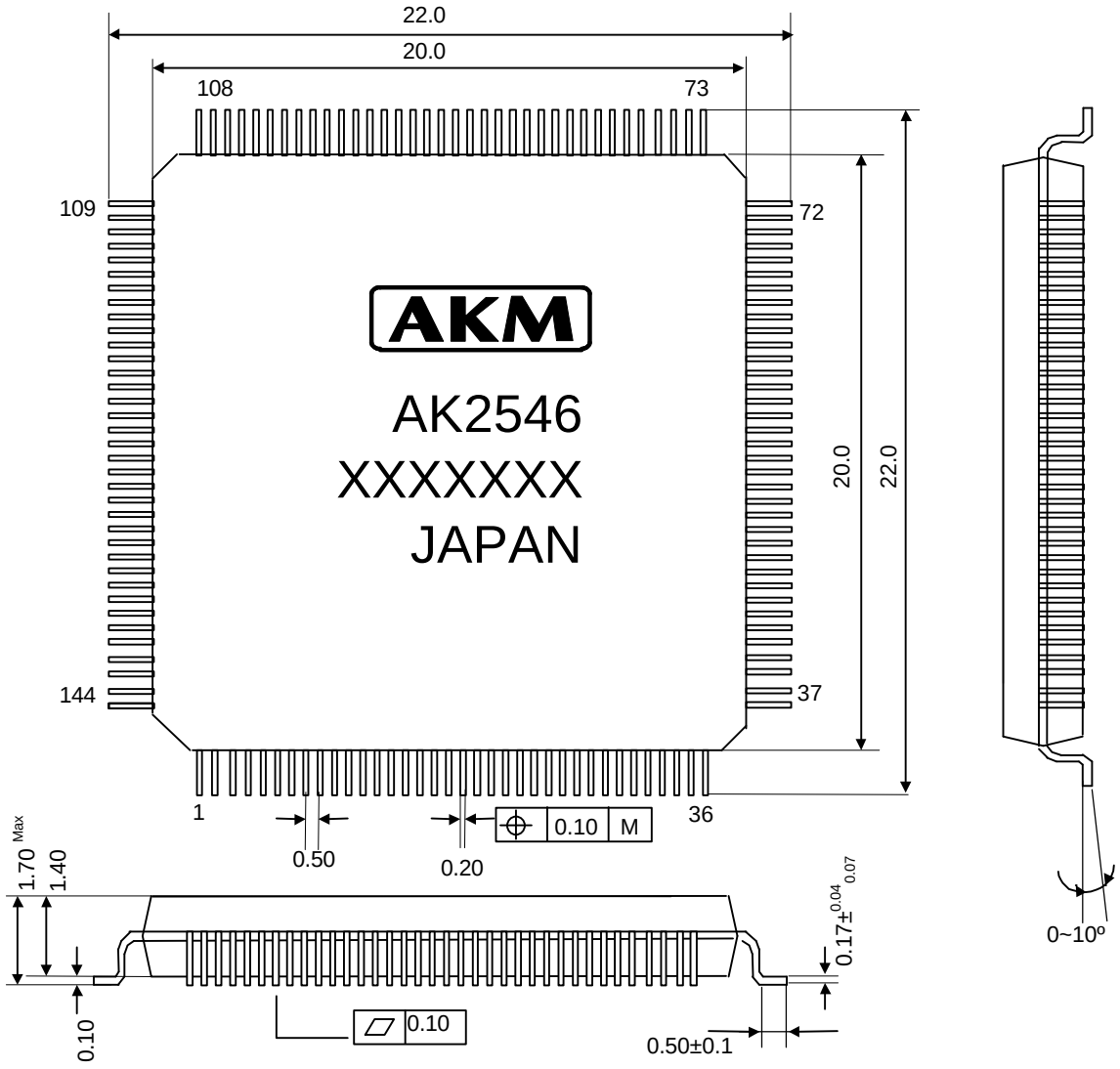
Multilayerboard with more than two VDD or GND layer

Please design the rest of pattern for GND

PACKAGE

144pin LQFP

OUTPUT DIMENSIONS



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