Prototyping with STPC Consumer-S for STPC Elite production

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1. Overview.

This document describes how to design for the STPC Elite in a way that it can be prototyped by the STPC Consumer-S. The purpose is to start a STPC Elite design prior to silicon availability.

All information is extracted from the STPC Consumer-S and STPC Elite datasheets.

2. Differences between the two devices.

2.1 Functional difference.

The STPC Elite can be described as a graphics-less and video-less version of the STPC Consumer-S. As a result, the list of functionnal differences between the 2 devices is relatively simple.

Improved features:
- The STPC Elite supports 64-Mbit and 128-Mbit SDRAM devices.

New features:
- JTAG.
- 16 General Purpose I/Os.
- 24MHz DEV_CLK is now a General Purpose programmable Clock (ball H24).

Removed features:
- All graphics and video related features.

The STPC Elite is manufactured in 0.25µm technology with all the corresponding advantages: speed, power consumption.

2.2   Pinout differences.

TABLE 1. Pinout differences

Ball	STPC Consumer-S	STPC Elite	Comment
G3	NC	TCLK	JTAG
N1	NC	TMS	JTAG
W1	NC	TDI	JTAG
AC2	NC	TDO	JTAG
G26	NC	Hi-Z / PA[22]	ISA / Local Bus
A20	NC	Hi-Z / PA[23]	ISA / Local Bus
AE5	HSYNC	GPIO[0]	
AC5	VSYNC	GPIO[1]	
AD5	VIN[0]	GPIO[2]	
AF5	VIN[2]	GPIO[3]	
AE6	VIN[3]	GPIO[4]	
AC7	VIN[4]	GPIO[5]	
AD6	VIN[5]	GPIO[6]	
AF6	VIN[6]	GPIO[7]	
AE7	VIN[7]	GPIO[8]	
AF7	VIN[1]	GPIO[9]	
AD7	COMP	GPIO[10]	
AD8	BLUE	GPIO[11]	
AE9	GREEN	GPIO[12]	
AF9	RED	GPIO[13]	
AE10	RSET	GPIO[14]	
AD9	VDD_DAC2	GPIO[15]	
AF10	VSS_DAC2	NC	
E26	VSS_DLL	NC	
D18	VDD5	NC	5V Power Supply for PCI pads
A16	VDD5	NC	5V Power Supply for PCI pads
B11	VDD5	NC	5V Power Supply for PCI pads
B9	VDD5	NC	5V Power Supply for PCI pads
AF8	VDD_DAC1	NC	
AC9	VSS_DAC1	NC	
AC10	VREF_DAC	NC	
AD10	RED_TV	NC	
AC12	ODD_EVEN#	NC	
AD12	VDDA_TV	NC	

Ball	STPC Consumer-S	STPC Elite	Comment
AE12	BLUE_TV	NC	
AF12	VREF1_TV	NC	
AE13	VCS	NC	
AF13	VSSA_TV	NC	
AC14	VREF2_TV	NC	
AD11	DCLK	NC	
AE11	IREF1_TV	NC	
AF11	GREEN_TV	NC	
AE14	IREF2_TV	NC	
AF14	CVBS	NC	
AE15	VCLK	NC	
E25	VSS_DLL	2.5V	VSS_DLL is connected to GND
G24	3.3V	2.5V	VDD_CPUCLK_PLL
F26	3.3V	2.5V	VDD_HCLK_PLL
F25	3.3V	2.5V	VDD_DEVCLK_PLL
AC17	3.3V	2.5V	VDD_MCLKI_PLL
AC15	3.3V	2.5V	VDD_MCLKO_PLL
AD13	3.3V	NC	VDD_DCLK_PLL
D11	3.3V	2.5V	Core Power Supply
L23	3.3V	2.5V	Core Power Supply
T4	3.3V	2.5V	Core Power Supply
AC6	3.3V	2.5V	Core Power Supply

The Not Connected pins (NC) are not bonded to the die and can be left routed to the signal for the other configuration.

The PA signals of the local bus are in Tri-State when the STPC is in ISA bus mode.

2.3   Strap Option differences.

Basically, the strap option differences can be divided in three categories: The new ones, the ones with a different definition, and the ones with a potentially different configuration.

TABLE 2. New strap options

Signals	Elite	Comment
MD[3:2]	HCLK PLL Speed	Extends MD[26:24] to improve HCLK speed selection
MD[4]	PCI_CLKO divisor	Extends MD[17] to improve PCI_CLKO speed selection
MD[5]	HCLK synchro	Pull-Up if HCLK = MCLK, Pull-Down otherwise
MD[6]	PCI_CLK PLL speed	Pull-Down if PCI_CLK < 32MHz, otherwise Pull-Up
MD[7]	PCI_CLK PLL speed	Pull-Down
MD[13:10]	PCI_CLK deskew	Value not finalized yet

TABLE 3. Reallocated strap options

Signals	Elite	Consumer-S	Comment
MD[20]	CPU CLK multiplier	DCLK direction	Pull-Up in both cases

TABLE 4. Strap options with potentially different configuration

Signals	Elite	Comment
MD[26:24]	HCLK PLL Speed	Value changed due to MD[3:2] extending HCLK speed selection
MD[30:27]	HCLK Delay	Value not finalized yet
MD[35:31]	HCLK Skew	Value not finalized yet
MD[43:41]	CPU DLL TIC Value	Value not finalized yet
MD[46:45]	HCLK mode	Value not finalized yet (Pull Up by default)

3.   Solution.

3.1   2.5V Power Pins.

In the STPC Elite a certain number of balls are powered with 2.5V supply and not 3.3V. These must be connected to a 2.5V supply which can be located on the same plane as the 3.3V supply.

The VSS_DLL ball (E25) needs to be connected to ground (Consumer-S) or to the 2.5V power plane (Elite) using a null resistor, a solder drop, or any equivalent method.

3.2   Not Connected balls.

All the balls which are Not Connected in STPC Consumer-S or STPC Elite configuration can be left routed. The target being to use the STPC Elite for the final board, all the graphics/video signals of the STPC Consumer-S are either not connected (outputs and analog inputs), either connected to Ground (power supplies).

The result is summarized in the following table:

TABLE 5. Untouched signals

Ball	Signal	Comment
G3	TCLK	JTAG
N1	TMS	JTAG
W1	TDI	JTAG
AC2	TDO	JTAG
G26	Hi-Z / PA[22]	ISA / Local Bus
A20	Hi-Z / PA[23]	ISA / Local Bus
AF10	VSS_DAC2	GND
E26	VSS_DLL	GND
D18, A16, B11, B9	VDD5	5V Power Supply for PCI pads
AF8	VDD_DAC1	GND
AC9	VSS_DAC1	GND
AD12	VDDA_TV	GND
AF13	VSSA_TV	GND
AD13	VDD_DCLK_PLL	GND

3.3   GPIO signals.

The only features of the STPC Elite which can not be tested with the STPC Consumer-S are the 16 General Purpose I/O Signals. These GPIOs need to be carrefully connected on board due to their functionnality in the case of the STPC Consumer-S:
- GPIO[1:0] correspond to TTL outputs.
- GPIO[9:2] correspond to TTL inputs.
- GPIO[14:10] correspond to analog signals.
- GPIO[15] corresponds to a power supply.

When the STPC Consumer-S is mounted, the TTL inputs can be left routed according to the STPC Elite configuration, the TTL outputs could be left connected but their behaviour must not create conflicts, and all the other signals must be connected as described in the table.

TABLE 6. New functions.

STPC Elite	Connection	Connecting the STPC Consumer-S	
GPIO[0]	Design dependent	HSYNC	
GPIO[1]	Design dependent	VSYNC	
GPIO[2]	Design dependent	VIN[0]	Pull-Up or Pull-Down
GPIO[3]	Design dependent	VIN[2]	Pull-Up or Pull-Down
GPIO[4]	Design dependent	VIN[3]	Pull-Up or Pull-Down
GPIO[5]	Design dependent	VIN[4]	Pull-Up or Pull-Down
GPIO[6]	Design dependent	VIN[5]	Pull-Up or Pull-Down
GPIO[7]	Design dependent	VIN[6]	Pull-Up or Pull-Down
GPIO[8]	Design dependent	VIN[7]	Pull-Up or Pull-Down
GPIO[9]	Design dependent	VIN[1]	Pull-Up or Pull-Down
GPIO[10]	Design dependent	COMP	Leave unconnected
GPIO[11]	Design dependent	BLUE	Leave unconnected
GPIO[12]	Design dependent	GREEN	Leave unconnected
GPIO[13]	Design dependent	RED	Leave unconnected
GPIO[14]	Design dependent	RSET	Leave unconnected
GPIO[15]	Design dependent	VDD_DAC2	GND

3.4   Strap options.

The new strap options can be implemented for the STPC Consumer-S, this does not affect the behaviour of the device.

The strap options with different value should remain easy to modify. This can be achieved by adding a dummy resistor in the schematics and doing the final choice during the assembly of the board.

4. Technical Support

STMicroelectronics is on the Internet with a worldwide web (WWW) site on which product presentation, technical literature as well as product support information can be found.

A dedicated STPC section is available providing up to date hardware documentation and software tools.

The Web address is:

WWW : *http://www.st.com/stpc*

5. Update History for Application Note AN XXXX

This is the first issue.

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