Per Pin Parametric Measurement Unit/Source Measure Unit

AD5520

FEATURES

Force/Measure Functions
- Force Voltage/Current, Measure Current/Voltage
- Force Current/Voltage, Measure Current/Voltage

Force/Measure Voltage Range ±11 V

4 Programmable Force/Measure Current Ranges
- ±4 μA, ±40 μA, ±400 μA, ±4 mA

Extended Current Ranges
- ±40 mA and ±160 mA with External Driver

Clamp Circuitry and Window Comparators On Board

Guard Amplifier

64-Lead LQFP Package

APPLICATIONS

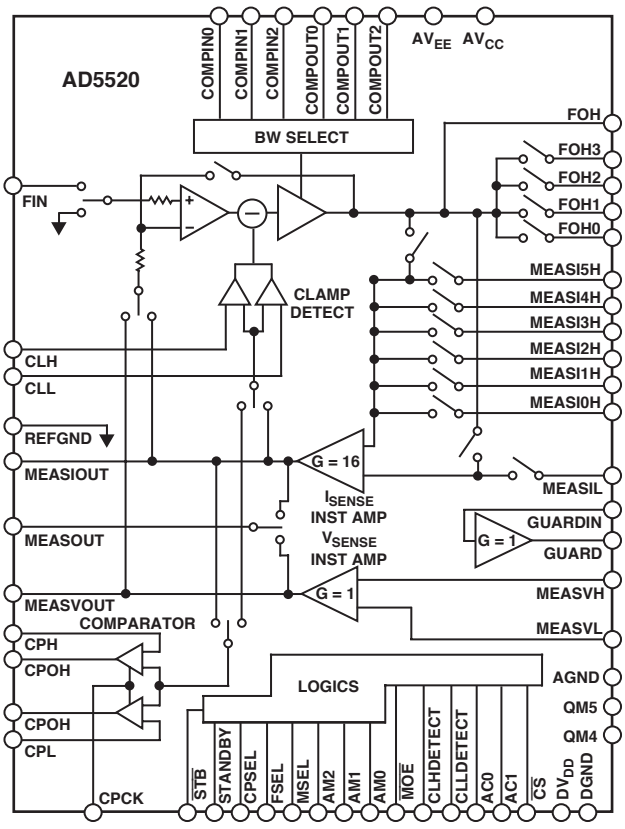
Automatic Test Equipment
- Per Pin PMU, Shared Pin PMU, Device Power Supply

Instrumentation
- Source Measure, Parametric Measurement, Precision Measurement

GENERAL DESCRIPTION

The AD5520 is a single channel per pin parametric measurement unit (PPMU) for use in semiconductor automatic test equipment. The part is also suited for use as a source measurement unit for instrumentation applications. It contains programmable modes to force a pin voltage and measure the corresponding current or force a current and measure the voltage. The AD5520 can force/measure over a ±11 V range or currents up to ±4 mA with its on-board force amplifier. An external amplifier is required for wider current ranges. The device provides a force sense capability to ensure accuracy at the tester pin. A guard output is also available to drive the shield of a force/sense pair. The AD5520 is available in a 64-lead LQFP package.

FUNCTIONAL BLOCK DIAGRAM



REV. A

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AD5520—SPECIFICATIONS

(AV_{CC} = +15 V ± 5%, AV_{EE} = –15 V ± 5%, DV_{DD} = 5 V ± 10%, AGND = 0 V, REFGND = 0 V, DGND = 0 V. All specifications 0°C to 70°C, unless otherwise noted.)

Parameter	Min	Typ[1]	Max	Unit	Test Conditions/Comments
VOLTAGE FORCE MODE					
Force Control Output Voltage Range	±11			V	R_{LOAD} = 10 kΩ, C_{LOAD} = 50 pF
FOH Output Impedance		70		Ω	
FOH0		2.5		kΩ	
FOH1		3		kΩ	
FOH2		500		Ω	
FOH3		60		Ω	
Input Offset Error		±1	±5	mV	
Gain Error			1	%	
Clamp Voltage Error[2]			±1	% FS	of FIN
CURRENT MEASURE/FORCE					Set with external sense resistors
FOH0		±4		µA	MODE0, R_S = 125 kΩ
FOH1		±40		µA	MODE1, R_S = 12.5 kΩ
FOH2		±400		µA	MODE2, R_S = 12.5 kΩ
FOH3		±4		mA	MODE3, R_S = 125 Ω
CURRENT MEASURE MODE					
High Sense Input Range, $V_{MEASIxH}$			±11	V	
Linearity[3]			±0.01	% FSR	+11 V > V_{FOL} > –11 V
Input Bias Current		±1	±3	nA	
Input Bias Current Drift[1]		50		pA/°C	
Output Offset Error			±100	mV	MODE0
			±100	mV	MODE1
			±100	mV	MODE2
			±100	mV	MODE3
Gain Error		±0.1	±0.35	%	Gain of 16
Gain Error Temperature Coefficient[4]		30		µV/°C	
MEASIOUT Output Load Current		±4		mA	
CMRR		95		dB	@ DC
CURRENT FORCE MODE					
Input Offset Error			±10	mV	With MODE0, MODE1, MODE2, MODE3
Gain Error			1	%	
Clamp Current Error[2]			±1	% FS	of FIN
VOLTAGE MEASURE MODE					
Differential Input Range	±11			V	
Low Sense Input Voltage Range	±100			mV	MEASVL
Linearity[3]			+0.005	% FSR	+11 V > V_{MEASVH} to V_{MEASVL} > –11 V
Input Offset Error		±5	±10	mV	FIN = 0 V, Measured @ MEASVOUT
Input Offset Error Temperature Coefficient[1]		±15		mV/°C	
Gain Error		±0.03	±0.15	%	Gain of 1
Gain Error Temperature Coefficient[4]		2		mV/°C	
Input Bias Current		±1	±3	nA	
Input Bias Current Drift[4]		50		pA/°C	
MEASVOUT Output Load Current		±4		mA	
CMRR[4]		73		dB	@ DC
AMPLIFIER SETTLING TIME[4, 5]					
V_{SENSE} Amp		20		µs	To 0.2%
I_{SENSE} Amp		12		µs	To 0.2%
LOOP SETTLING[4, 5]					Settling to within 0.024% of 8 V step
COMPIN2 = 100 pF		450	600	µs	MODE0
		285	390	µs	MODE1
		170	240	µs	MODE2, MODE3
COMPIN1 = 1000 pF		2	2.5	ms	MODE0
		1.8	2.4	ms	MODE1, MODE2, MODE3
COMPIN0 = 3000 pF		5.75	8.7	ms	MODE0, MODE1, MODE2, MODE3

Parameter	Min	Typ[1]	Max	Unit	Test Conditions/Comments
SLEW RATE[4, 5]		50		mV/µs	COMPIN2 = 100 pF
		4.3		mV/µs	COMPIN1 = 1000 pF
		1.28		mV/µs	COMPIN0 = 3000 pF
COMPARATOR					
CPH, CPL Input Range	±11			V	$V_{CPH} > V_{CPL}$
Input Offset			±7	mV	
GUARD DRIVER					
Output Voltage	±11			V	
Output Impedance		130		Ω	Capacitive Load Only
Output Offset Voltage		400		mV	
Load Current[4]		±4		mA	
Output Settling Time[4]		0.5	2	µs	100 pF Capacitive Load
ANALOG REFERENCE INPUTS					
Force Control Input Range	±11			V	
Force Control Input Impedance		1		MΩ	
Clamp Control Input Range	±11			V	$V_{CLH} > V_{CLL}$
Clamp Control Input Impedance		1		MΩ	
Comparator Threshold Input Range	±11			V	
Comparator Threshold Input Impedance		1		MΩ	
Input Capacitance[4]		3		pF	
ANALOG MEASUREMENT OUTPUTS					
Voltage Measure Output Impedance		2		Ω	
Current Measure Output Impedance		3		Ω	
Multiplexed Sense Output Impedance		1		kΩ	
Input Capacitance					
MEASIxH, MEASVH, FOHx		8		pF	
LOGIC INPUTS					
Input Current			±1	µA	All digital inputs together
Input Low Voltage, V_{INL}			0.8	V	
Input High Voltage, V_{IHL}	2.0			V	
Input Capacitance[4]		3		pF	
LOGIC OUTPUTS					
Output Low Voltage, V_{OL}[4]			0.4	V	I_{SINK} = 2 mA
Output High Voltage, V_{OH}[4]	2.4			V	I_{SOURCE} = 2 mA
POWER REQUIREMENTS					
AV_{CC}	+14.25	+15	+15.75	V	For specific performance[6]
AV_{EE}	–14.25	–15	+15.75	V	
Power Supply Rejection Ratio, PSRR[1]					
FOH		–25		dB	100 kHz
		–16		dB	500 kHz
		–15		dB	1 MHz
MEASOUT		–55		dB	100 kHz
		–10		dB	500 kHz
DC PSR		90		dB	
DV_{DD}		5		V	
I_{AVCC}			12	mA	
I_{AVEE}			12	mA	
I_{DVDD}			0.5	mA	Digital inputs at supply rails

NOTES
[1]Typical values are at 25°C and nominal supply, unless otherwise noted.
[2]Full-scale = 11 V.
[3]Full-scale range = 22 V.
[4]Guaranteed by design and characterization but not subject to production test.
[5]Force control amplifier dominates slew rate and settling time.
[6]Operational with ±12 V supplies, force/measure range is reduced to ±8.5 V.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2]

(AV_{CC} = +15 V ± 5%, AV_{EE} = –15 V ± 5%, AGND = 0 V, REFGND = 0 V, DGND = 0 V. All specifications 0°C to 70°C, unless otherwise noted.)

Parameter	DV_{DD} 5 V ± 10%	DV_{DD} 3.3 V	Unit	Conditions/Comments
t_1	0	0	ns min	$\overline{CS}$ Falling Edge to $\overline{STB}$ Falling Edge Setup Time
t_2	30	200	ns min	$\overline{STB}$ Pulse Width
t_3	40	70	ns min	$\overline{STB}$ Rising Edge to $\overline{CS}$ Rising Edge Setup Time
t_4	0	40	ns min	Data Setup Time
t_5	550	560	ns min	$\overline{CS}$ Falling Edge to CPCK Rising Edge Setup Time
t_6	320	320	ns min	CPCK Pulse Width
t_7	450	500	ns min	CPCK to $\overline{STB}$ Falling Edge Setup Time
t_8	150	800	ns min	$\overline{STB}$ Rising Edge to QMx, CLxDETECT Valid
t_9	100	440	ns min	$\overline{STB}$ Rising Edge to CPOH, CPOL Valid
t_{10}	240	240	µs min	Comparator Setup Time, MODE2, MODE3 settling
t_{11}	150	500	ns min	Comparator Hold Time
t_{12}	100	440	ns min	Comparator Output Delay Time
t_{13}	320	320	ns min	Comparator Strobe Pulse Width

NOTES
[1]See Figure 1.
[2]All input signals are specified with tr = tf = 1 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.

Specifications subject to change without notice.

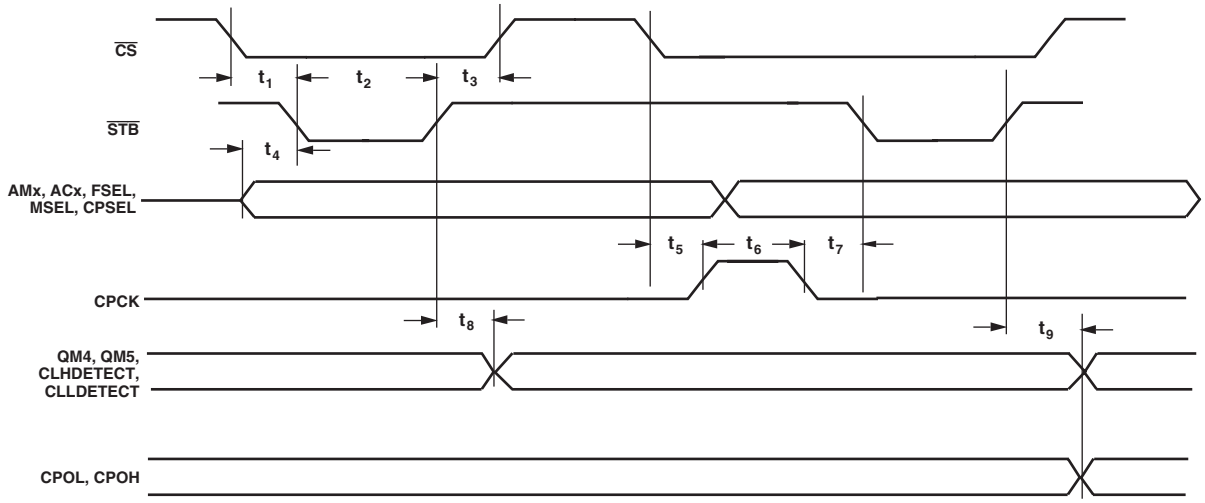


Figure 1. Timing Diagram

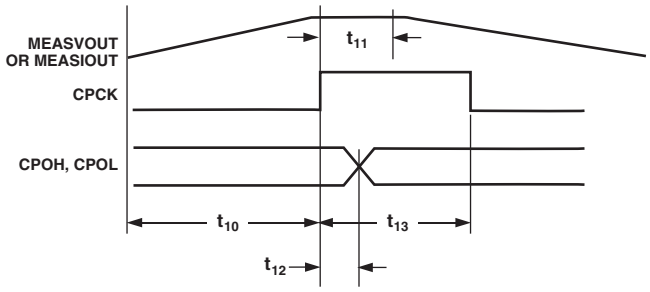


Figure 2. Comparator Timing

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C, unless otherwise noted.)

AV_{CC} to AV_{EE} . . . . . 34 V
AV_{CC} to AGND . . . . . –0.3 V, +17 V
AV_{EE} to AGND . . . . . +0.3 V, –17 V
DV_{DD} . . . . . –0.3 V to +6 V
Digital Inputs to DGND . . . . . –0.3 V to DV_{DD} + 0.3 V
Analog Inputs to AGND . . . . . AV_{CC} + 0.3 V to AV_{EE} – 0.3 V
C_{LH} to C_{LL} . . . . . –0.3 V to +34 V
C_{PH} to C_{PL} . . . . . –0.3 V to +34 V
REFGND, DGND . . . . . AV_{CC} + 0.3 V to AV_{EE} – 0.3 V

Operating Temperature Range
Commercial (J Version) . . . . . 0°C to 70°C
Storage Temperature Range . . . . . –65°C to +150°C
Maximum Junction Temperature, (T_J max) . . . . . 150°C
Package Power Dissipation . . . . . (T_J max – T_A)/θ_{JA}
Thermal Impedance θ_{JA} . . . . . 47.8°C/W
Lead Temperature (Soldering 10 sec) . . . . . 300°C
IR Reflow, Peak Temperature . . . . . 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

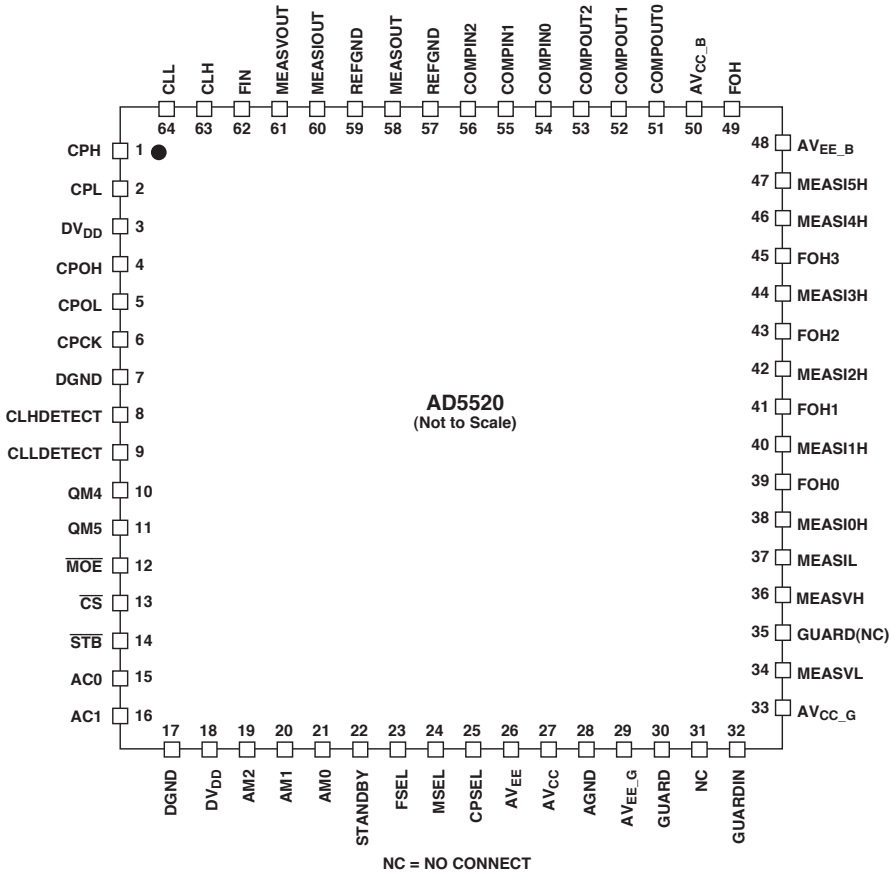
Model	Temperature Range	Package Description	Package Option
AD5520JST	0°C to 70°C	64-Lead LQFP	ST-64-2
AD5520JST-REEL	0°C to 70°C	64-Lead LQFP	ST-64-2
EVAL-AD5520EB		Evaluation Board and Software	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5520 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

64-Lead LQFP



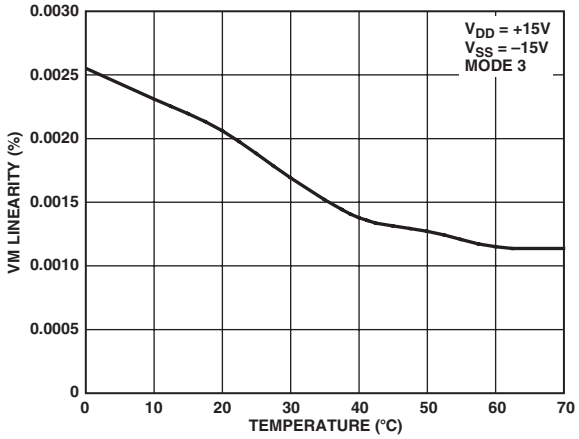
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	CPH	Upper Comparator Threshold Voltage Input, CPH > CPL.
2	CPL	Lower Comparator Threshold Voltage Input, CPL < CPH.
3, 18	DV_{DD}	Digital Supply Voltage.
4	CPOH	Logic Output. When high, indicates MEASVOUT or MEASIOUT > CPH.
5	CPOL	Logic Output. When high, indicates MEASVOUT or MEASIOUT < CPL.
6	CPCK	Logic Input. Used to initiate comparator sampling and update CPOH and CPOL.
7, 17	DGND	Digital Ground.
8	CLHDETECT	Logic Output. When high, indicates upper clamp active. For details, see the Clamp Function section.
9	CLLDETECT	Logic Output. When high, indicates lower clamp active. For details, see the Clamp Function section.
10	QM4	Logic Output. When high, indicates current range Mode 4 is enabled. May be used to drive external relay or switch. For details, see the High Current Ranges section.
11	QM5	Logic Output. When high, indicates current range Mode 5 is enabled. May be used to drive external relay or switch. For details, see the High Current Ranges section.
12	$\overline{MOE}$	Active Low MEASOUT Enable.
13	$\overline{CS}$	Active Low Logic Input. The device is selected when this pin is low. For details, see the Interface section.
14	$\overline{STB}$	Active Low Logic Input. Used in conjunction with CPCK and $\overline{CS}$ to configure the device for different configurations. Rising edge of $\overline{STB}$ triggers sequence inputs. For details, see the Interface section.
15	AC0	Logic Input. Used in conjunction with AC1 to select one of three external compensation capacitors. For details, see the Force Control Amplifier section.
16	AC1	Logic Input. Used in conjunction with AC0 to select one of three external compensation capacitors. For details, see the Force Control Amplifier section.

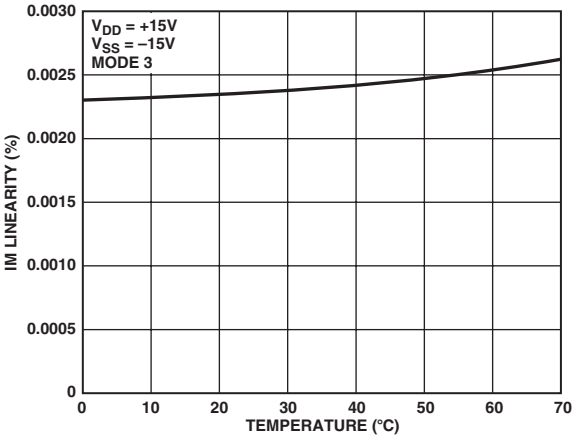
PIN FUNCTION DESCRIPTIONS (continued)

Pin No.	Mnemonic	Description
19	AM2	Logic Input. Used in conjunction with AM1 and AM0 to select one of six current ranges or to enable standby mode. For details, see the Current Ranges section.
20	AM1	Logic Input. Used in conjunction with AM2 and AM0 to select one of six current ranges or to enable standby mode. For details, see the Current Ranges section.
21	AM0	Logic Input. Used in conjunction with AM2 and AM1 to select one of six current ranges or to enable standby mode. For details, see the Current Ranges section.
22	STANDBY	Logic Input. When high, device is in standby mode of operation. For details, see the Standby Mode section.
23	FSEL	Logic Input. Force mode select. Used to select between current or voltage force operation. For details, see the Force Voltage or Force Current section.
24	MSEL	Logic Input. Measure mode select. Used to connect MEASOUT to either MEASIOUT when high or MEASVOUT when low.
25	CPSEL	Logic Input. Comparator select. Used to compare CPL, CPH to MEASVOUT when low, or to MEASIOUT when high. For details, see the Comparator Function and Strobing section.
26	AV_{EE}	Most Negative Supply Voltage.
27	AV_{CC}	Most Positive Supply Voltage.
28	AGND	MEASx Input Ground.
29	AV_{EE_G}	Most Negative Supply Voltage.
30	GUARD	Guard Output.
31	NC	No Connect.
32	GUARDIN	Guard Input.
33	AV_{CC_G}	Most Positive Supply Voltage.
34	MEASVL	DUT Voltage Sense Inputs (Low Sense).
35	GUARD(NC)	No Connect.
36	MEASVH	DUT Voltage Sense Inputs (High Sense).
37	MEASIL	DUT Current Sense Inputs (Low Sense).
38	MEASI0H	DUT Current Sense Inputs (High Sense).
39	FOH0	Force Control Voltage Output.
40	MEASI1H	DUT Current Sense Inputs (High Sense).
41	FOH1	Force Control Voltage Output.
42	MEASI2H	DUT Current Sense Inputs (High Sense).
43	FOH2	Force Control Voltage Output.
44	MEASI3H	DUT Current Sense Inputs (High Sense).
45	FOH3	Force Control Voltage Output.
46	MEASI4H	DUT Current Sense Inputs (High Sense).
47	MEASI5H	DUT Current Sense Inputs (High Sense).
48	AV_{EE_B}	Most Negative Supply Voltage.
49	FOH	External Force Driver Control Voltage Output.
50	AV_{CC_B}	Most Positive Supply Voltage.
51	COMPOUT0	Compensation Capacitor 0 Output.
52	COMPOUT1	Compensation Capacitor 1 Output.
53	COMPOUT2	Compensation Capacitor 2 Output.
54	COMPIN0	Compensation Capacitor 0 Input.
55	COMPIN1	Compensation Capacitor 1 Input.
56	COMPIN2	Compensation Capacitor 2 Input.
57, 59	REFGND	Analog Input/Output Reference Ground.
58	MEASOUT	Multiplexed DUT Voltage/Current Sense Output. For details, see the Measured Parameter section.
60	MEASIOUT	DUT Current Sense Output.
61	MEASVOUT	DUT Voltage Sense Output.
62	FIN	Force Control Voltage Input.
63	CLH	Upper Clamp Voltage Input CLH > CLL.
64	CLL	Lower Clamp Voltage CLL < CLH.

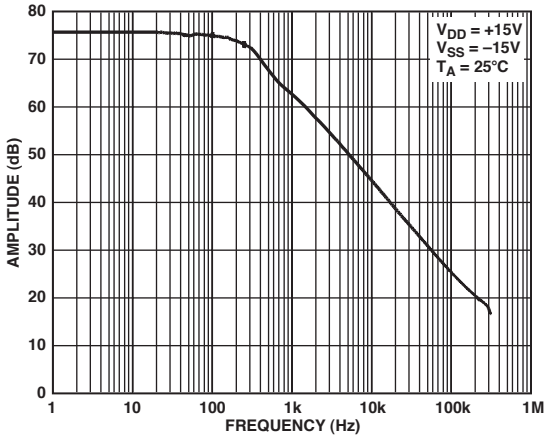
AD5520–Typical Performance Characteristics



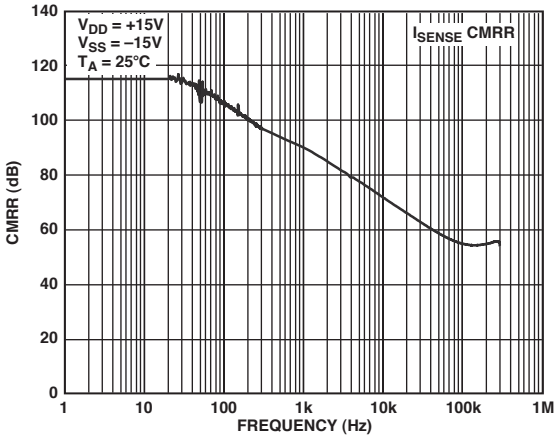
TPC 1. Voltage Sense Amplifier Linearity vs. Temperature



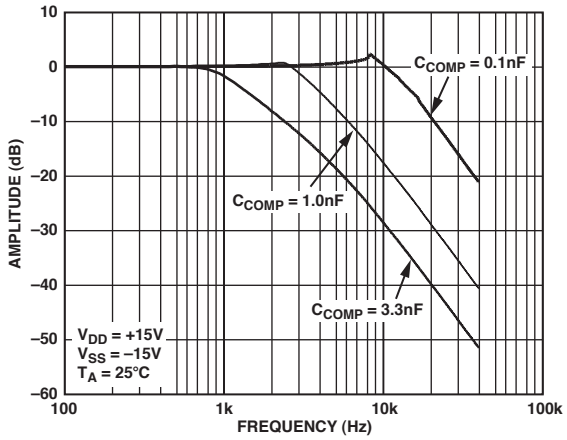
TPC 4. Current Sense Linearity vs. Temperature



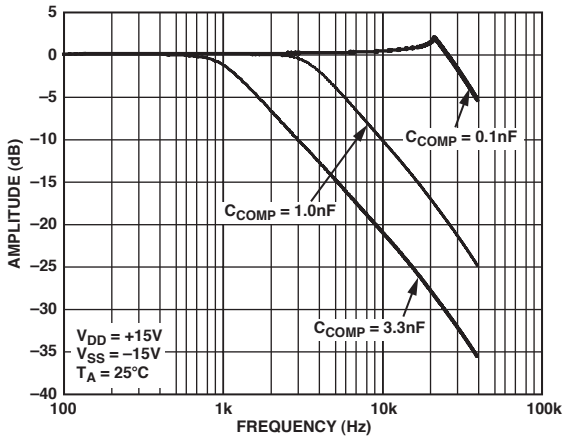
TPC 2. Voltage Sense Amplifier CMRR vs. Frequency



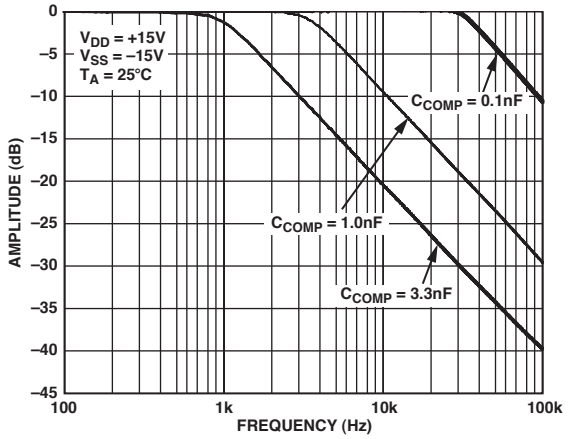
TPC 5. Current Sense Amplifier CMRR vs. Frequency



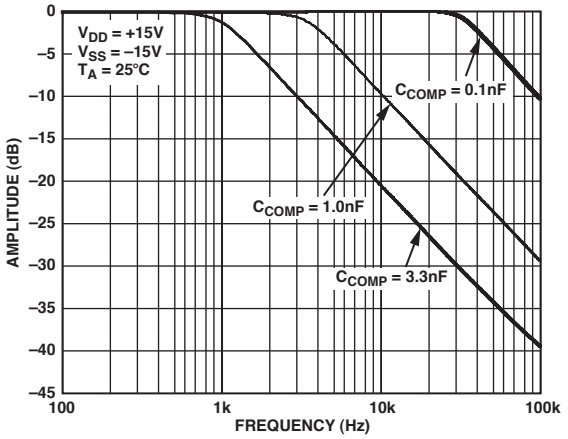
TPC 3. Force Amplifier Bandwidth–MODE 0 (4 μA)



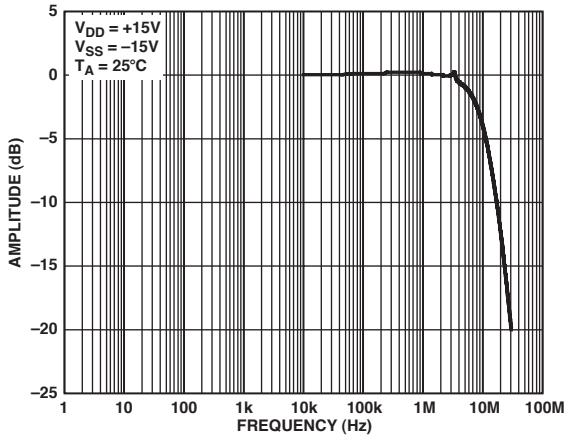
TPC 6. Force Amplifier Bandwidth–MODE 1 (40 μA)



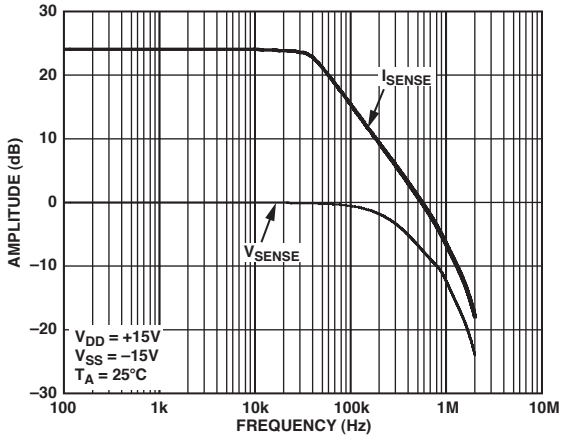
TPC 7. Force Amplifier Bandwidth–MODE 2 (400 μA)



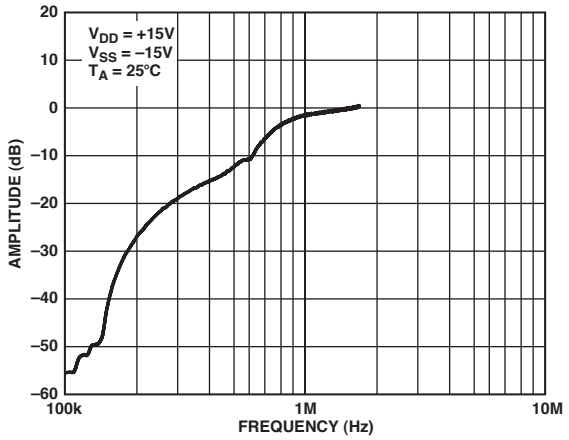
TPC 10. Force Amplifier Bandwidth–MODE 3 (4 mA)



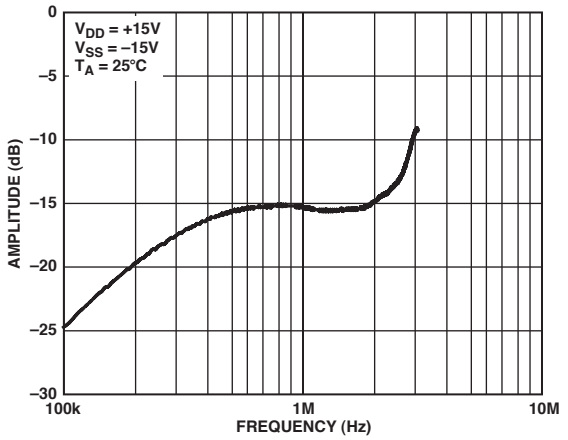
TPC 8. Guard Amplifier Bandwidth



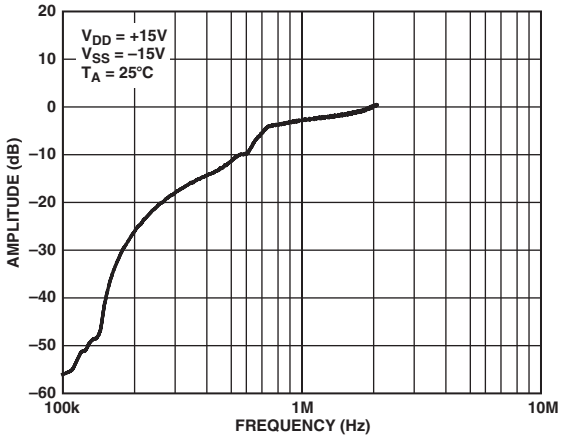
TPC 11. Voltage Sense and Current Sense Amplifier Bandwidths



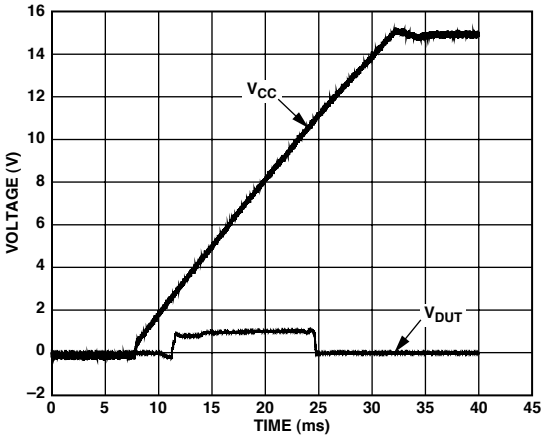
TPC 9. Current Sense Amplifier AC PSRR



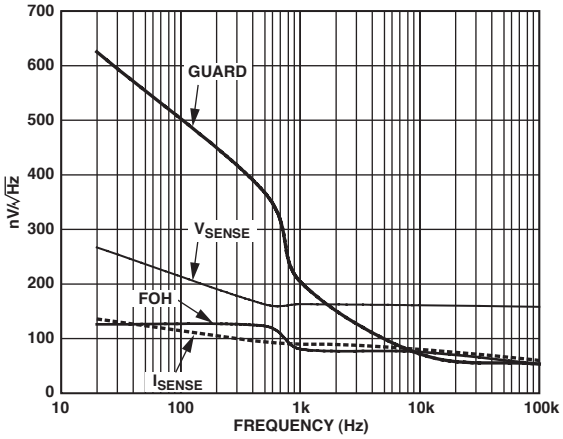
TPC 12. Force Amplifier AC PSRR–MODE 3, C_{COMP} = 100 pF



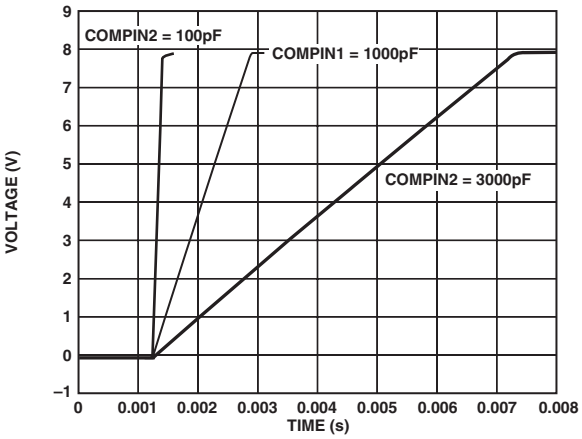
TPC 13. Voltage Sense Amplifier AC PSRR



TPC 15. Power Up



TPC 14. Noise Spectral Density



TPC 16. Settling Time, Mode 2

THEORY OF OPERATION

The AD5520 is a single channel per pin parametric measurement unit (PPMU) for use in semiconductor automatic test equipment. It contains programmable modes to force a pin voltage and measure the corresponding current (FVMI), force current measure voltage (FIMV), force current measure current (FIMI), and force voltage measure voltage (FVMV). The PPMU can force or measure a voltage from –11 V to +11 V. It can force or measure a current over four ranges: 4 μA, 40 μA, 400 μA, and 4 mA. The addition of an external driver allows two extended ranges.

The device provides a force sense capability to ensure accuracy at the tester pin. A guard output is also available to drive the shield of a force/sense pair.

The AD5520 has an on-board window comparator that provides two bits of useful information, DUT too low or too high. Also provided on the chip is clamp circuitry that will flag via CLHDETECT and CLLDETECT if the voltage applied to FIN or across the DUT has exceeded the voltage applied to CLL and CLH.

On chip is clamp circuitry that clamps the output of the force amplifier if the voltage at MEASIOUT and MEASVOUT exceeds CLL and CLH.

INTERFACE

The AD5520 PPMU is controlled via a number of digital inputs, which are discussed in detail in the following sections. All inputs are TTL compatible. $\overline{CS}$ is used to select the device while $\overline{STB}$ (active low input) latches data available on the other digital inputs and updates any required digital outputs. The rising edge of $\overline{STB}$ triggers sequence inputs. The remaining digital inputs control the function of the PMU—which measure mode it is in, which compensation capacitor is used, and the selected current range.

Standby Mode

The AD5520 may be placed into standby mode via the standby logic input. In this mode, the force amplifier is disconnected from the force input (FIN), the switch in series with the force output pins, FOHx, is opened, and the current measure amplifier is disconnected from the sense resistors. The voltage measure amplifier is still connected across the DUT, so DUT voltage measurements may still be made while in standby mode. Figure 3 shows the configuration of the PMU while in standby mode.

Table I. Standby Mode

STANDBY	Function
Low	Normal Force Mode
High	Standby Mode

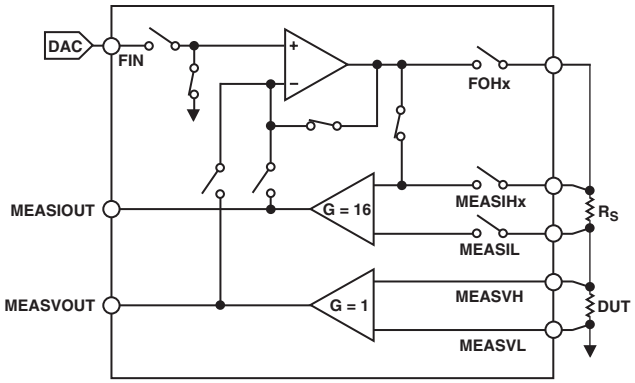


Figure 3. PMU in Standby Mode

Force Voltage or Force Current

FSEL is an input that determines whether the PPMU forces a voltage or current.

Table II. FSEL Function

FSEL	Function
Low	Voltage Force and Current Clamp with MEASIOUT Voltage
High	Current Force and Voltage Clamp with MEASVOUT Voltage

Measured Parameter

MEASOUT is a muxed output that tracks the sensed parameter, MSEL connects it to the output of either the current sense amplifier or the voltage sense amplifier, depending on which is the measured parameter of interest.

The MEASOUT pin will be connected back to an ADC to allow the measured value to be converted to a digital code.

Table III. MEASOUT Connected to Voltage or Current

MSEL	Function
Low	MEASOUT = DUT Voltage
High	MEASOUT = DUT Current

The MEASOUT pin may also be made high impedance through the MOEB logic input.

Table IV. MOEB Allows MEASOUT to Go High Impedance

MOEB	Function
Low	Enable MEASOUT Output
High	Hi-Z MEASOUT Output

Current Ranges
A number of current ranges are possible with the AD5520. The AM0, AM1, and AM2 pins are digital inputs used to establish full-scale current range of the PMU.

Table V. Selection of Current Range

AM0	AM1	AM2	Function
Low	Low	Low	Current Range MODE0 (up to 4 μA)
High	Low	Low	Current Range MODE1 (up to 40 μA)
Low	High	Low	Current Range MODE2 (up to 400 μA)
High	High	Low	Current Range MODE3 (up to 4 mA)
Low	Low	High	Current Range MODE4 (External Buffer Mode)
High	Low	High	Current Range MODE5 (External Buffer Mode)
Low	High	High	Standby (same as STANDBY = High)
High	High	High	Standby (same as STANDBY = High)

R_S Selection
The AD5520 is designed so that the voltage drop across each of the R_S resistors will be less than ±500 mV when maximum current is flowing through them. To support other current ranges, these sense resistor values may be changed. A force amplifier can drive a maximum of 6 mA. It is not recommended to increase the maximum current above the nominal range.

The two external current ranges use an external buffer to drive the required current. Our example uses 40 mA and 160 mA ranges. These ranges can be changed to suit user requirements for a high current range.

Force Control Amplifier
The force control amplifier requires external capacitors connected between the COMPOUTx and COMPINx pins. For stability with large capacitance at the DUT, the largest capacitance value (3000 pF) should be selected. The force control amplifier should always contribute the dominant pole in the control loop. Settling times will increase with larger capacitances. ACx inputs select which external compensation capacitor is used.

Table VI. AC0, AC1 Compensation Capacitor Selection

AC0	AC1	Function
Low	Low	Select External Compensation Capacitor 0
High	Low	Select External Compensation Capacitor 1
Low	High	Select External Compensation Capacitor 2

Comparator Function and Strobing
The AD5520 has an on-board window comparator that provides two bits of useful information, DUT too low or too high. CPSEL is the digital input that controls this function, selecting whether it should compare to the voltage sense or the current sense amplifier.

Table VII. Comparator Function Select

CPSEL	Function
Low	Compare CPL, CPH to MEASVOUT
High	Compare CPL, CPH to MEASIOUT

After CPSEL has selected which amplifier output is of interest, logic input CPCK is used to initiate comparator sampling and update the logic outputs CPOH and CPOL, indicating if the voltages at MEASIOUT or MEASVOUT have exceeded voltages set at CPL or CPH (thus providing DUT too high or DUT too low information). A rising edge on $\overline{STB}$ is required to clock the CPOH and CPOL data out.

Table VIII. CPCK Synchronous Logic Outputs

CPOH	Function
Low	MEASVOUT or MEASIOUT < CPH
High	MEASVOUT or MEASIOUT > CPH
CPOL	**Function**
Low	MEASVOUT or MEASIOUT > CPL
High	MEASVOUT or MEASIOUT < CPL

Clamp Function
Clamp circuitry is also included on chip, allowing the output of the force amplifier to be clamped in the event of the voltage at MEASIOUT and MEASVOUT exceeding CLL and CLH. The clamp circuitry play their role in the event of a short or open circuit. When in force current range, the voltage clamps protect the DUT in the event of an open circuit. Likewise, when forcing a voltage and a short circuit occurs, the current clamps will protect the DUT in this case. The clamps also function to protect the DUT in the event of a transient voltage or current spike that may occur when changing to a different operating mode or when programming the device to a different current range.

The digital output flags, which indicate a clamp limit has been hit, are CLHDETECT for the upper clamp and CLLDETECT output for the lower clamp.

Table IX. Clamp Detect Outputs

CLHDETECT	Function
Low	Upper Clamp Inactive
High	Upper Clamp Active
CLLDETECT	**Function**
Low	Lower Clamp Inactive
High	Lower Clamp Active

High Current Ranges
With the use of an external high current amplifier, two high current ranges are possible. The current range values can be selected as required in the application through appropriate selection of the sense resistors connected between MEASI5H, MEASI4H, and MEASIL. When one of these high current ranges (MODE 4 or MODE 5) is selected via the AMx control lines, the appropriate QM4 or QM5 output will be enabled. These outputs can thus be used to control relays connected in series with the high current amplifier as shown in Figure 8.

Table X. High Current Range Logic Outputs

QM4	QM5	Function
High	Low	Current Range MODE 4 Enable Output
Low	High	Current Range MODE 5 Enable Output

CIRCUIT OPERATION

Force Voltage

Most PMU measurements are performed while in force voltage and measure current modes, for example, when the device is used as a device power supply, or in continuity or leakage testing. In the force voltage mode, the voltage at analog input FIN is mapped directly to the voltage forced at the DUT.

When in force voltage and measure current modes, the maximum voltage applied to the input corresponds to the maximum current outputs. Figure 4 shows the transfer function when forcing a voltage.

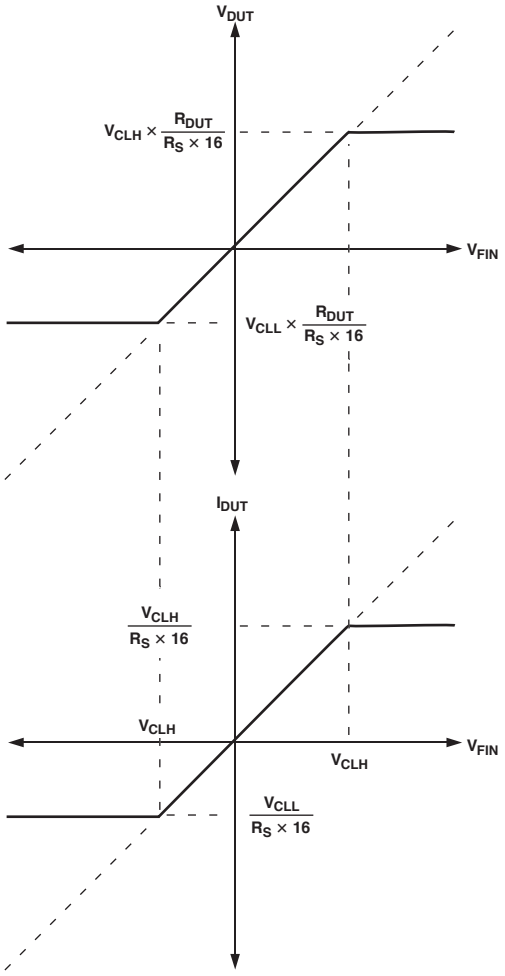
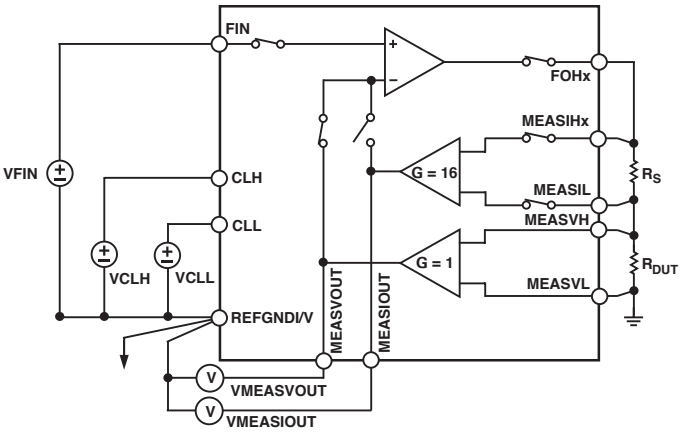


Figure 4. Voltage Force Transfer Function

Measure Current

Figure 5 shows a simplified diagram of the PMU when in force voltage mode. The control loop consists of the force amplifier with the voltage sense amplifier making up the feedback path. Current flowing through the DUT is measured by sensing the current flowing through a selectable sense resistor, which is in series with the DUT. The current sense amplifier (Gain = 16) generates a voltage at its output, which is proportional to the current flowing through the DUT. This voltage is compared to the CLL and CLH levels to ensure the clamp voltages have not been exceeded. Strobing CPCK and $\overline{STB}$ will provide information about the voltage level with respect to the comparator levels, CPH and CPL.



CONDITION	$V_{CLH} > I_{DUT} \times R_S \times 16$ $V_{CLL} < I_{DUT} \times R_S \times 16$	$V_{CLH} < I_{DUT} \times R_S \times 16$ $V_{CLL} < I_{DUT} \times R_S \times 16$	$V_{CLH} > I_{DUT} \times R_S \times 16$ $V_{CLL} > I_{DUT} \times R_S \times 16$
OUTPUT	$V_{DUT} = V_{FIN}$	$V_{DUT} = V_{CLH}$	$V_{DUT} = V_{CLL}$

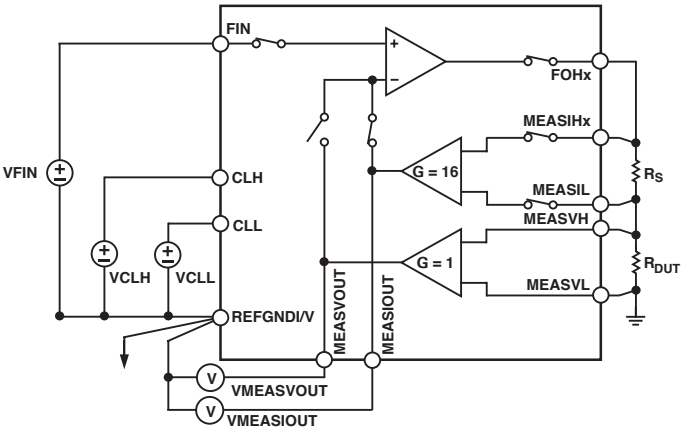
Figure 5. Voltage Force, Measure Current Mode

Force Current

In the force current mode, the voltage at FIN is now converted to a current through the following relationship:

$$Force\ Current = V_{FIN}/R_{SENSE}$$

Figure 6 shows a simplified diagram of the PMU when in force current mode. The control loop consists of the force amplifier with the current sense amplifier making up the feedback path. In this case, voltage at the DUT is sensed across the voltage measure amplifier (Gain = 1) and presented at the MEASVOUT output.



CONDITION	$V_{CLH} > V_{DUT}$ $V_{CLL} < V_{DUT}$	$V_{CLH} < V_{DUT}$ $V_{CLL} < V_{DUT}$	$V_{CLH} > V_{DUT}$ $V_{CLL} > V_{DUT}$
OUTPUT	$I_{DUT} = \frac{V_{FIN}}{R_S}$	$I_{DUT} = \frac{V_{CLH}}{R_S}$	$I_{DUT} = \frac{V_{CLL}}{R_S}$

Figure 6. Current Force, Voltage Measure Mode

Figure 7 illustrates the transfer function of the current force mode.

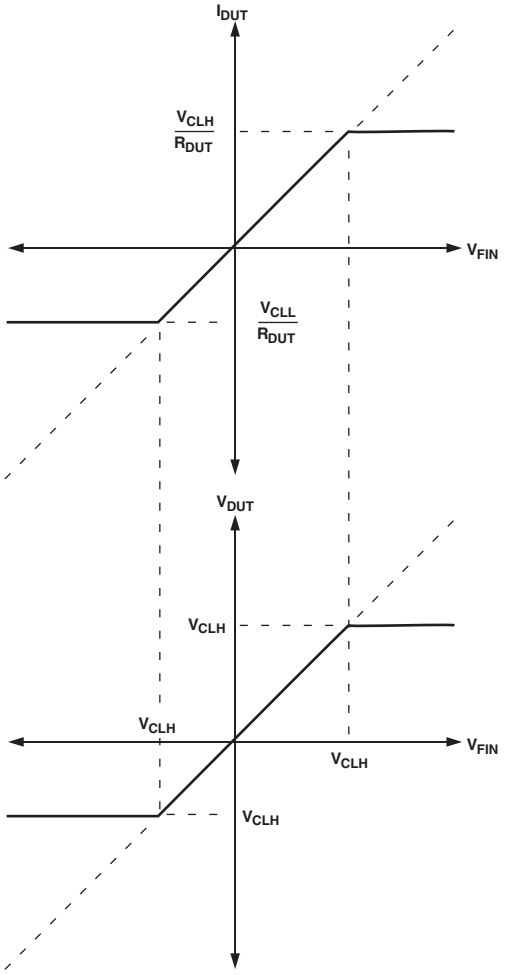


Figure 7. Current Force Transfer Function

Measure Voltage

A DUT voltage is tested via the voltage measure amplifier by a window comparator to ensure that CPH and CPL levels are not exceeded. In addition, the DUT voltage is automatically tested against the voltage levels at the clamp, and clamp flags are enabled if the DUT voltage exceeds either of the levels.

Short Circuit Protection

The AD5520 is designed to withstand a direct short circuit on any of the amplifier outputs.

SETTLING TIME CONSIDERATIONS

Fast throughput is a key requirement in automatic test equipment because it relates directly to the cost of manufacturing the DUT, thus reducing the time required to make a DAC measurement is of upmost importance. When taking measurements using a PMU, the limiting factor is usually the time it takes the output to settle to the required accuracy so a measurement can be taken. DUT capacitance, measurement accuracy, and the design of the PMU are the major contributors to this time. Figure 8 shows a simplified block diagram of the AD5520 PMU. In brief, the device consists of a force control amplifier, access to a number of selectable sense resistors, a voltage measure instrumentation amplifier, and a current measure instrumentation amplifier. To optimize the performance of the device, there are also nodes provided where external compensation capacitors are added. As mentioned, making an accurate measurement in the fastest time while avoiding overshoots and ringing is the key requirement in any ATE system. This in itself provides challenges. The external compensation capacitors set up different settling times or bandwidths on the force control amplifier, and, while one compensation capacitor value may suit one range, it may not suit other ranges. To optimize measurement performance and speed, differences in signal behavior on each range and frequency of use of each range need to be taken into account.

When selecting a faster settling time, there is a trade-off between the faster settling, overshoots, and ringing. A small compensation value will result in faster settling but may incur penalties in overshoots or ringing at the DUT. Compensation capacitor selection should be optimized to ensure minimum overshoots while still giving good settling time performance.

While careful selection of the compensation capacitor is required to minimize the settling time, another factor can greatly contribute to the overall settling of the loop if the feedback loop is broken in some manner and the force control amplifier goes to either the positive or negative rails. There is a finite amount of time required for the amplifier to recover from this condition, typically 85 μs, which adds to the settling of the loop. Ensuring that the force control amplifier never goes into saturation is the best solution. This solution can be helped by putting the device into standby mode at any time the operating mode or range selection is changed. In addition, ensure that the selected output range can supply the required current needed by the DUT.

PCB LAYOUT AND POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration to the power supply and the ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5520 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the PMU is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

This PMU should have ample supply bypassing of 10 μF in parallel with 0.1 μF on the supply located as close to the package as possible, ideally right up against the device. The 0.1 μF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching. Low ESR, 1 μF to 10 μF, tantalum or electrolytic capacitors should also be applied at the supplies to minimize transient disturbance and filter out low frequency ripple.

Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the reference inputs.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane while signal traces are placed on the solder side.

It is good practice to employ compact, minimum lead length PCB layout design. Leads to the input should be as short as possible to minimize IR drops and stray inductance.

TYPICAL CONNECTION CIRCUIT FOR THE AD5520

Figure 8 shows the AD5520 connected as it would be in a typical application. The external components required are three compensation capacitors and six sense resistors, depending on how many ranges are required. If high current ranges > 6 mA are required, an external amplifier must be used with relays to switch in the different current ranges to the DUT. Other components are also required to make the PMU function. The PMU requires a number of discrete voltage levels: five DAC levels for each PMU used in the system, two levels each for the comparator and clamps, and one voltage level for the AD5520 force input voltage. To utilize the information gathered from the DUT, an ADC (such as the AD7665 16-Bit ADC) must be connected to the MEASOUT pin to convert the measured current or voltage to the digital world for analysis.

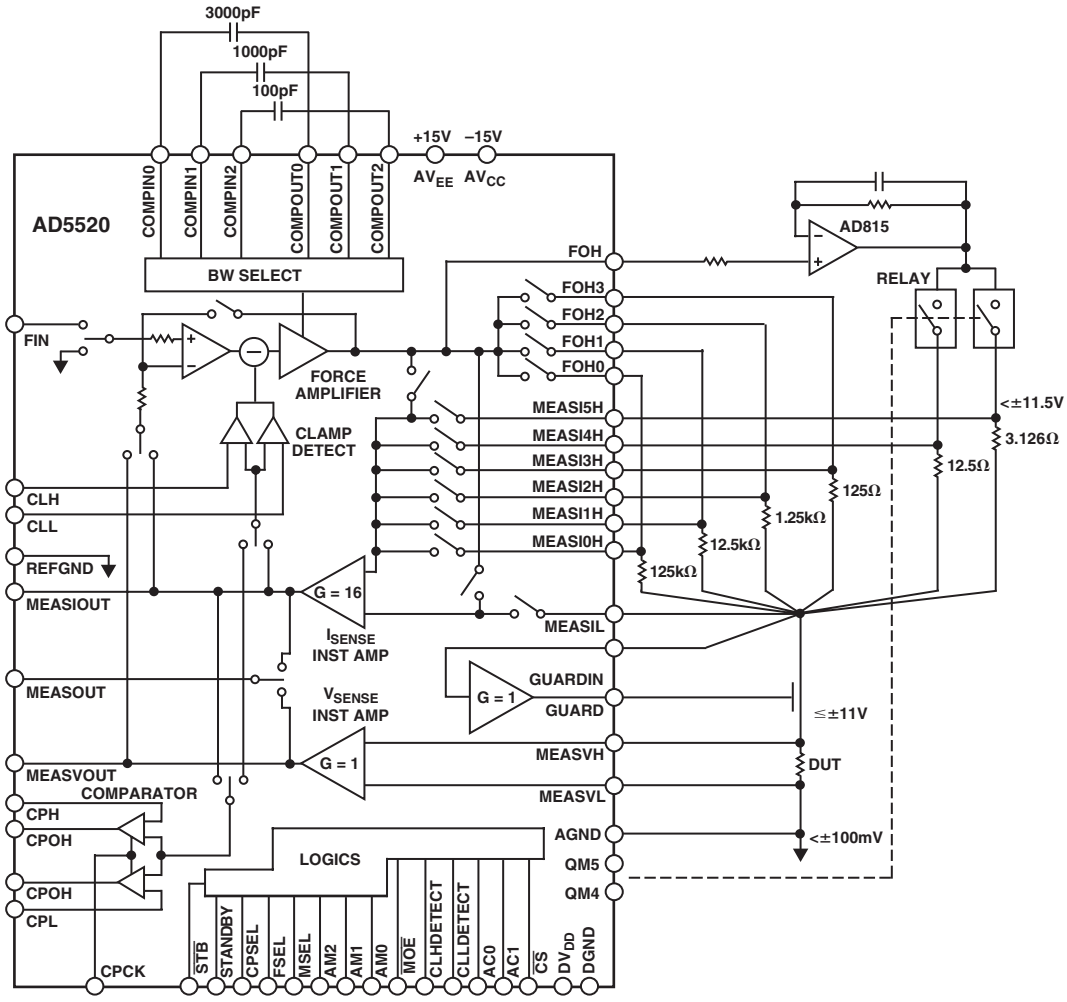


Figure 8. Typical Configuration of the AD5520 as Used in an ATE Circuit

TYPICAL APPLICATION CIRCUIT

Figure 9 shows the AD5520 as it would be used in an ATE system. This device could be used as a per pin parametric unit in order to speed up the rate at which testing could be done. It could also be used as a DUT power supply, as shown in the application circuit. The central PMU shown in the block diagram is usually a highly accurate PMU and is shared among a number of pins in the tester. In general, many discrete levels are required in an ATE system for the pin drivers, comparators, clamps, and active loads. DAC devices, such as the AD5379, offer a highly integrated solution for a number of these levels. The AD5379 is a dense 40-channel DAC designed with high channel requirements, like ATE in mind.

The flexible function of the AD5520 also makes it suited for use in instrumentation applications such as source measure units. Source measure units are programmable instruments capable of sourcing and measuring voltage or current simultaneously. The AD5520 provides a more integrated solution in such equipment.

EVALUATION BOARD FOR THE AD5520 PMU

A full featured evaluation kit is available for the AD5520. It consists of an evaluation board with direct hookup via a 36-way centronics connector to a PC. PC-based software to control the AD5520 is provided as part of the evaluation kit. The evaluation board schematic is shown in Figure 10. Note that V_{DD} and V_{SS} must provide sufficient headroom for the force and measure voltage range. In addition to the supply voltages for the evaluation board, it is also necessary to provide the following voltage levels for the clamp, comparator, and the force input pin—CLL, CLH, CPL, CPH, and FIN. SMB connections are provided for these voltage inputs. To use the evaluation board, it will also be necessary to provide a DUT connected via the gold pins.

Both AGND and DGND inputs are provided on the board. The AGND and DGND planes are connected at one location close to the AD5520. It is recommended not to connect AGND and DGND elsewhere in the system to avoid ground loop problems. REFGND is routed back to AGND at the power block to maintain a clean ground reference for accurate measurements.

Each supply is decoupled to the relevant ground plane with 10 μF and 0.1 μF capacitors. The device supply pin is again decoupled with a 10 μF and 0.1 μF capacitor pair to the relevant ground plane.

Care should be taken when replacing devices to ensure that the pins line up correctly with the PCB pads.

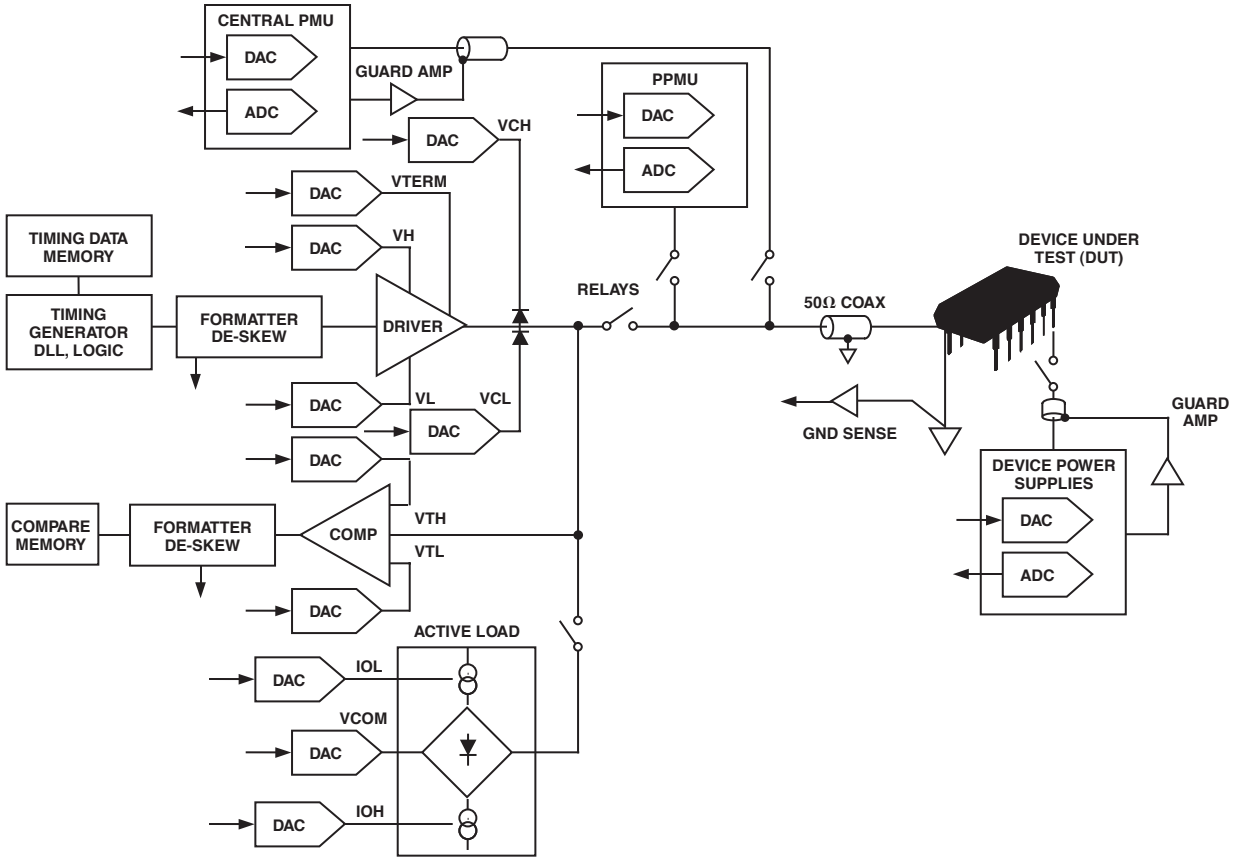


Figure 9. Typical Application ATE Circuit

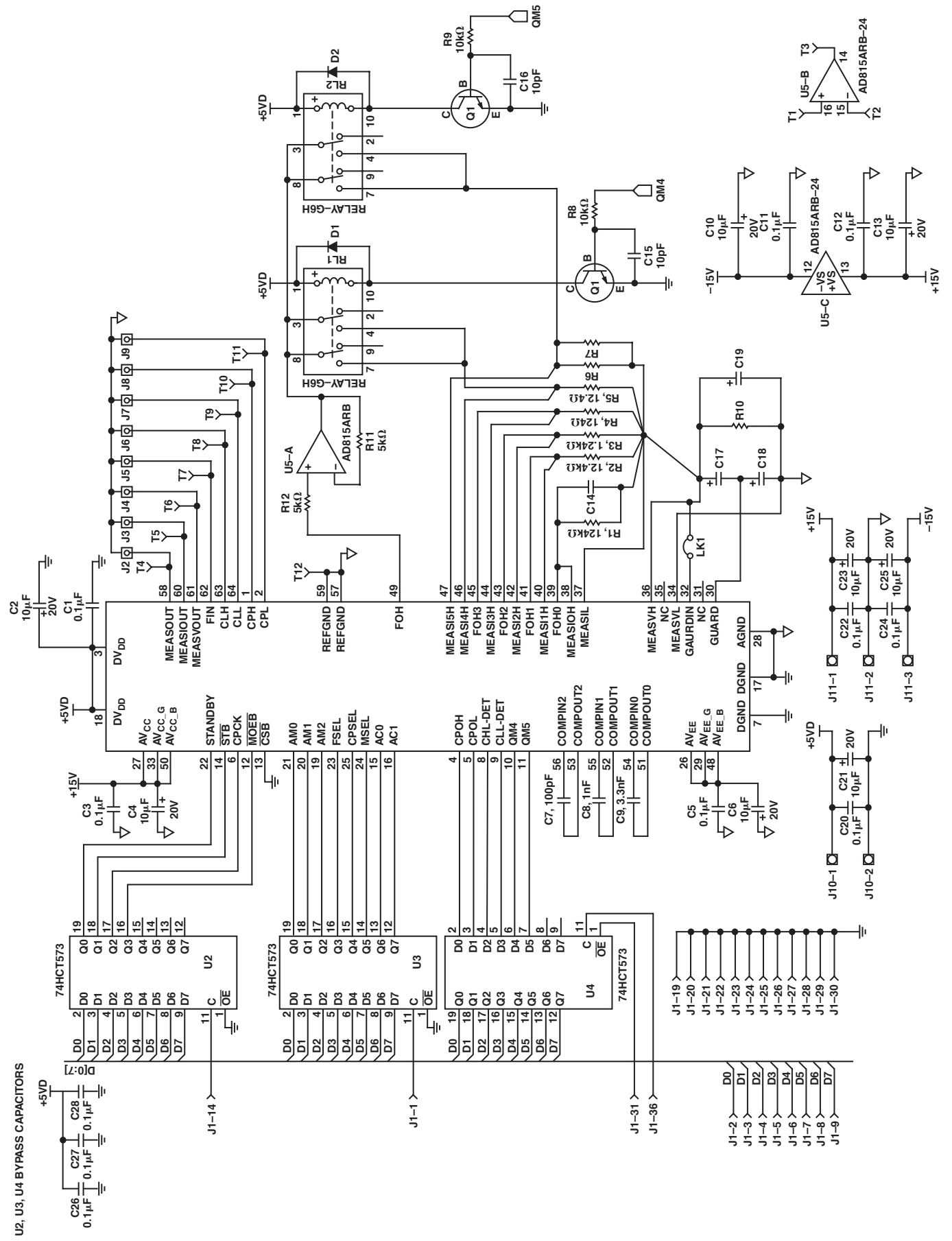
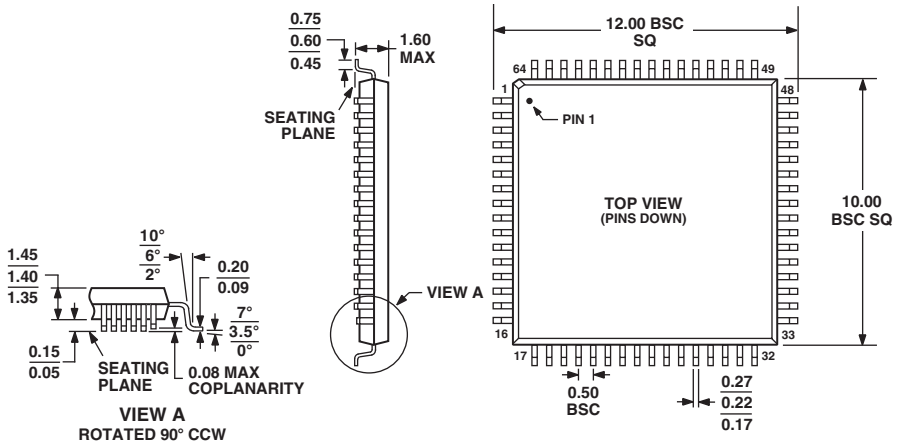


Figure 10. Evaluation Board Schematic

OUTLINE DIMENSIONS

64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-2)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026BCD

Revision History

Location	Page
10/03—Data Sheet changed from REV. 0 to REV. A.	
Changes to SPECIFICATIONS	3
Updated ORDERING GUIDE	5