Am6073

Companding D-to-A Converter for PCM Communication Systems

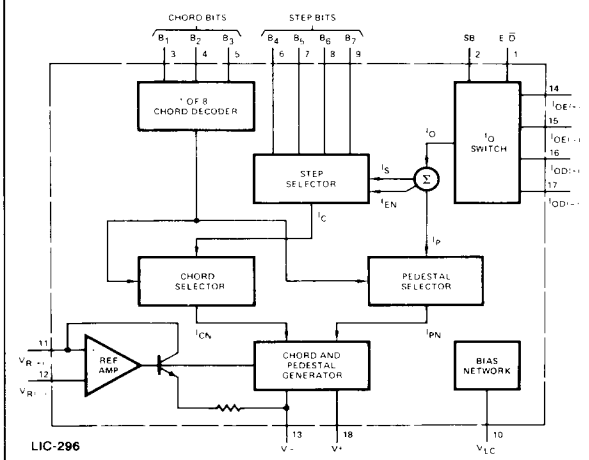
Distinctive Characteristics

- Tested to CCITT A-law tracking specification
- Absolute accuracy specified – includes all errors over temperature range
- Settling time 300ns typical
- Ideal for multiplexed PCM systems
- Output dynamic range of 62 dB
- Improved pin-for-pin replacement for DAC-87
- Microprocessor controlled operations
- Multiplying operation
- Negligible output noise
- Monotonicity guaranteed over entire dynamic range
- Wide output voltage compliance
- Low power consumption

GENERAL DESCRIPTION

The Am6073 is a monolithic 8-bit, companding digital-to-analog (D/A) data converter with true current outputs and large output voltage compliance for fast driving a variety of loads. The transfer function of the Am6073 complies with the CCITT A-87.6 companding law, and consists of 13 linear segments or chords. A particular chord is identified with the sign bit input, (SB), and three chord select input bits. Each chord contains 16 uniformly spaced linear steps which are determined by four step select input bits. The resulting dynamic range achieved with this 8-bit format is 62dB. Accuracy and monoticity are assured by the internal circuit design and are guaranteed over the full temperature range. The Am6073 is tested to the CCITT A-law compandor tracking specification for pulse code modulation (PCM) transmission systems. The application of the Am6073 in communication systems provides an increased signal-to-noise ratio, reduces system signal distortion, and stimulates wider usage of computerized channel switching. Other application areas include digital audio recording, voice synthesis, and secure communications. When used in PCM communication systems, the Am6073 functions as a complete PCM decoder with additional encoding capabilities which make it ideal for implementation in CODEC circuits.

FUNCTIONAL BLOCK DIAGRAM



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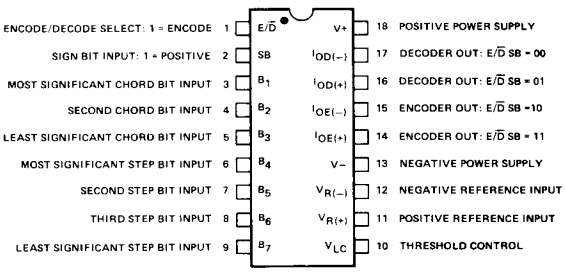
CONNECTION DIAGRAM
Am6073



Top View

Pin 1 is marked for orientation.

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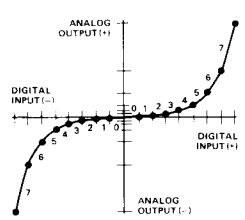
ORDERING INFORMATION

Part Number	Temperature	Accuracy
Am6073DM	–55°C to +125°C	Conforms to CCITT
Am6073DC	0°C to +70°C	A-law specification

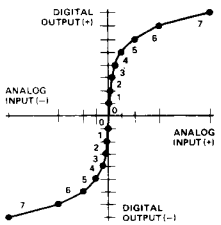
Other AMD Companding D/A Converters	
Am6070DM, DC	Conforms to industrial μ-law spec.
Am6071DM, DC	Conforms to industrial A-law spec.
AM6072DM, DC	Conforms to Bell D3 spec.

SIMPLIFIED CONVERSION TRANSFER FUNCTIONS

Decoder Characteristic



Encoder Characteristic



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MAXIMUM RATINGS above which useful life may be impaired

V+ Supply to V− Supply	36V	Operating Temperature	
V_{LC} Swing	V− plus 8V to V+	MIL Grade	−55°C to +125°C
Output Voltage Swing	V− plus 8V to V− plus 36V	COM'L Grade	0°C to +70°C
Reference Inputs	V− to V+	Storage Temperature	−65°C to +150°C
Reference Input Differential Voltage	±18V	Power Dissipation $T_A \leq 100°C$	500mW
Reference Input Current	1.25mA	For $T_A > 100°C$ derate at	10mW/°C
Logic Inputs	V− plus 8V to V− plus 36V	Lead Soldering Temperature	300°C (60 sec)

GUARANTEED FUNCTIONAL SPECIFICATIONS

Resolution	±128 Steps
Monotonicity	For both groups of 128 steps and over full operating temperature range
Dynamic Range	62 dB, (20 log ($I_{7,15}/I_{0,1}$))

ELECTRICAL CHARACTERISTICS (Note 1)

These specifications apply for $V_+ = +15V$, $V_- = -15V$, $I_{REF} = 512\mu A$, $0°C \leq T_A \leq +70°C$, for the commercial grade, $-55°C \leq T_A \leq +125°C$, for the military grade, and for all 4 outputs unless otherwise specified.

Parameter	Description		Test Conditions		Min.	Typ.	Max.	Unit
t_s	Settling Time		To within ±1/2 step at $T_A = 25°C$, Output switched from I_{ZS} to I_{FS}		–	300	500	ns
	Chord Endpoint Accuracy		$V_{REF} = +10{,}000V$ $R_{REF+} = 19.53k\Omega$ $R_{REF-} = 20k\Omega$ $-5V \leq V_{OUT} \leq +18V$		See Table 1 for absolute accuracy limits which cover all errors related to the transfer characteristic.			
	Step Nonlinearity							
I_{EN}	Encode Current							
$I_{FS}(D)$ $I_{FS}(E)$	Full Scale Current Deviation from Ideal							
$I_{O(+)} - I_{O(-)}$	Full Scale Current Symmetry Error Decode or Encode Pair							
I_{ZS}	Zero Scale Current							
ΔI_{FS}	Full Scale Current Drift							
V_{OC}	Output Voltage Compliance		Output within limits specified by Table 1		−5	–	+18	Volts
I_{DIS}	Disable Current		Leakage of output disabled by E/$\overline{D}$ or SB		–	5.0	50	nA
I_{FSR}	Output Current Range				0	2.0	4.2	mA
V_{IL}	Logic Input Levels	Logic "0"	$V_{LC} = 0V$		–	–	0.8	Volts
V_{IH}		Logic "1"			2.0	–	–	Volts
I_{IN}	Logic Input Current		$V_{IN} = -5V$ to $+18V$		–	–	40	μA
V_{IS}	Logic Input Swing		$V_- = -15V$		−5	–	+18	Volts
I_{BREF-}	Reference Bias Current				–	−1.0	−4.0	μA
dI/dt	Reference Input Slew Rate				0.12	0.25	–	mA/μs
$PSSI_{FS+}$ $PSSI_{FS-}$	Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)		$V+ = +4.5$ to $+18V$, $V- = -15V$		–	0.005	0.1	dB
			$V- = -10.8V$ to $-18V$, $V+ = +15V$		–	0.01	0.1	
I+	Power Supply Current		$V+ = +5V$ to $+15V$, $V- = -15V$, $I_{FS} = 2.0mA$		–	2.7	4.0	mA
I−					–	−6.7	−8.8	
P_D	Power Dissipation		$V- = -15V$, $V_{OUT} = 0V$ $I_{FS} = 2.0mA$	$V+ = +5V$	–	114	152	mW
				$V+ = +15V$	–	141	192	

Note 1. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) the step size is 1.0μA, while in the last chord near full scale (C_7) the step size is 64μA.

ELECTRICAL CHARACTERISTICS (Cont.)

TABLE I

ABSOLUTE DECODER OUTPUT CURRENT LEVELS IN μA

STEP	CHORD							
	0	1	2	3	4	5	6	7
0	.000	16.032	32.064	64.127	128.25	256.51	513.02	1026.04
	.500	16.500	33.000	66.000	132.00	264.00	528.00	1056.00
	1.000	16.982	33.964	67.927	135.85	271.71	543.42	1086.84
1	1.000	17.003	34.007	68.014	136.03	272.06	544.11	1088.22
	1.500	17.500	35.000	70.000	140.00	280.00	560.00	1120.00
	2.000	18.011	36.022	72.044	144.09	288.18	576.35	1152.70
2	2.103	17.975	35.950	71.900	143.80	287.60	575.20	1150.41
	2.500	18.500	37.000	74.000	148.00	296.00	592.00	1184.00
	2.971	19.040	38.080	76.161	152.32	304.64	609.29	1218.57
3	2.945	18.947	37.893	75.787	151.57	303.15	606.30	1212.59
	3.500	19.500	39.000	78.000	156.00	312.00	624.00	1248.00
	4.160	20.069	40.139	80.278	160.56	321.11	642.22	1284.44
4	4.248	19.918	39.837	79.673	159.35	318.69	637.39	1274.78
	4.500	20.500	41.000	82.000	164.00	328.00	656.00	1312.00
	4.767	21.099	42.197	84.394	168.79	337.58	675.16	1350.31
5	5.192	20.890	41.780	83.560	167.12	334.24	668.48	1336.96
	5.500	21.500	43.000	86.000	172.00	344.00	688.00	1376.00
	5.826	22.128	44.256	88.511	177.02	354.04	708.09	1416.18
6	6.136	21.862	43.723	87.447	174.89	349.79	699.57	1399.14
	6.500	22.500	45.000	90.000	180.00	360.00	720.00	1440.00
	6.885	23.157	46.314	92.628	185.26	370.51	741.02	1482.05
7	7.080	22.833	45.667	91.333	182.67	365.33	730.66	1461.33
	7.500	23.500	47.000	94.000	188.00	376.00	752.00	1504.00
	7.944	24.186	48.372	96.745	193.49	386.98	773.96	1547.92
8	8.025	23.805	47.610	95.220	190.44	380.88	761.76	1523.51
	8.500	24.500	49.000	98.000	196.00	392.00	784.00	1568.00
	9.004	25.215	50.431	100.862	201.72	403.45	806.89	1613.79
9	8.969	24.777	49.553	99.106	198.21	396.42	792.85	1585.70
	9.500	25.500	51.000	102.000	204.00	408.00	816.00	1632.00
	10.063	26.245	52.489	104.978	209.96	419.91	839.83	1679.66
10	9.913	25.748	51.496	102.993	205.99	411.97	823.94	1647.88
	10.500	26.500	53.000	106.000	212.00	424.00	848.00	1696.00
	11.122	27.274	54.548	109.095	218.19	436.38	872.76	1745.52
11	10.857	26.720	53.440	106.879	213.76	427.52	855.03	1710.07
	11.500	27.500	55.000	110.000	220.00	440.00	880.00	1760.00
	12.181	28.303	56.606	113.212	226.42	452.85	905.70	1811.39
12	11.801	27.691	55.383	110.766	221.53	443.06	886.12	1722.25
	12.500	28.500	57.000	114.000	228.00	456.00	912.00	1824.00
	13.241	29.332	58.664	117.329	234.66	469.32	938.63	1877.26
13	12.745	28.663	57.326	114.652	229.30	458.61	917.22	1834.43
	13.500	29.500	59.000	118.000	236.00	472.00	944.00	1888.00
	13.894	30.361	60.723	121.446	242.89	485.78	971.57	1943.13
14	14.089	29.635	59.269	118.539	237.08	474.15	948.31	1896.62
	14.500	30.500	61.000	122.000	244.00	488.00	976.00	1952.00
	14.923	31.391	62.781	125.562	251.12	502.25	1004.50	2009.00
15	15.060	30.606	61.231	122.425	244.85	489.70	979.40	1958.80
	15.500	31.500	63.000	126.000	252.00	504.00	1008.00	2016.00
	15.953	32.420	64.840	129.679	259.36	518.72	1037.43	2074.87
STEP SIZE	1	1	2	4	8	16	32	64

Minimum, ideal and maximum values are specified for each step. The minimum and maximum values are specified to comply with the CCITT A-law compandor tracking requirements. All four outputs are guaranteed, the encode outputs being specified to limits a half step higher than those shown above. This takes into account the combined effects of chord endpoint accuracy, step nonlinearity, encode current error, full scale current deviation from ideal, full scale symmetry error, zero scale current, full scale drift, and output impedance over the specified output voltage compliance range. Note that the guaranteed monotonicity ensures that adjacent step current levels will not overlap as might otherwise be implied from the minimum and maximum values shown in the above table.

TABLE 2

IDEAL DECODER OUTPUT VALUES EXPRESSED IN dB DOWN FROM OVERLOAD LEVEL (+3dBmo)

STEP	CHORD							
	0	1	2	3	4	5	6	7
0	−69.11	−38.74	−35.72	−26.70	−20.68	14.66	−8.64	−2.62
1	−59.57	−38.23	−32.21	−26.19	−20.17	−14.15	−8.13	−2.11
2	−55.13	−37.75	−31.73	−25.71	−19.68	−13.66	−7.64	−1.62
3	−52.21	−37.29	−31.27	−25.25	−19.23	−13.21	−7.19	−1.17
4	−50.03	−36.85	−30.83	−24.81	−18.79	−12.77	−6.75	−0.73
5	−48.28	−36.44	−30.42	−24.40	−18.38	−12.36	−6.34	−0.32
6	−46.83	−36.05	−30.03	−24.00	−17.98	−11.96	−5.94	+0.08
7	−45.59	−35.67	−29.65	−23.63	−17.61	−11.59	−5.57	+0.46
8	−44.50	−35.31	−29.29	−23.27	−17.24	−11.22	−5.20	+0.82
9	−43.54	−34.96	−28.94	−22.92	−16.90	−10.88	−4.86	+1.16
10	−42.67	−34.62	−28.60	−22.58	−16.56	−10.54	−4.52	+1.50
11	−41.88	−34.30	−28.28	−22.26	−16.24	−10.22	−4.20	+1.82
12	−41.15	−33.99	−27.97	−21.95	−15.93	−9.91	−3.89	+2.13
13	−40.48	−33.69	−27.67	−21.65	−15.63	−9.61	−3.59	+2.43
14	−39.86	−33.40	−27.38	−21.36	−15.34	−9.32	−3.30	+2.72
15	−39.28	−33.12	−27.10	−21.08	−15.06	−9.04	−3.02	+3.00

The −40dBmo, −50dBmo, and −55dBmo output points significant for the CCITT A-87.6 PCM system specification can be found between steps 13 and 14 on chord 0, steps 4 and 5 on chord 0, and steps 2 and 3 on chord 0, respectively. Outputs corresponding to points below −55dBmo are specified in Table 1 for an accuracy of ± a half step.

THEORY OF OPERATION

Functional Description

The Am6073 is an 8-bit, nonlinear, digital-to-analog converter with high impedance current outputs. The output current value is proportional to the product of the digital inputs and the input reference current. The full scale output current, I_{FS}, is specified by the input binary code 111 1111, and is a linear function of the reference current, I_{REF}. There are two operating modes, encode and decode, which are controlled by the Encode/Decode, (E/$\overline{D}$), input signal. A logic 1 applied to the E/$\overline{D}$ input places the Am6073 in the encode mode and current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output, depending on the state of the Sign Bit (SB) input. A logic 0 at the E/$\overline{D}$ input places the Am6073 in the decode mode.

The transfer characteristic is a piece-wise linear approximation to the CCITT A-87.6 logarithmic law which can be written as follows:

$$Y = 0.18\,(1 + \ln(A\,|X|))\ \mathrm{sgn}\,(X),\quad 1/A \leq |X| \leq 1$$
$$Y = 0.18\,(A\,|X|)\ \mathrm{sgn}\,(X),\quad 0 \leq |X| \leq 1/A$$

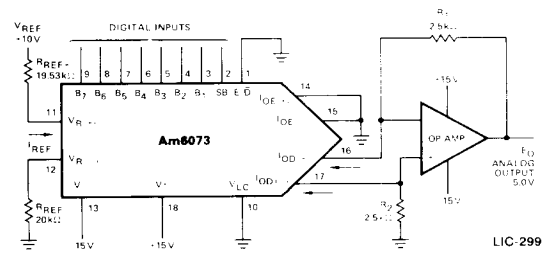
where: X = analog signal level normalized to unity (encoder input or decoder output)
Y = digital signal level normalized to unity (encoder output or decoder input)
A = 87.6

The current flows from the external circuit into one of four possible analog outputs determined by the SB and E/$\overline{D}$ inputs. The output current transfer function can be represented by a total of 16 segments or chords addressable through the SB input and three chord select bits. The two chords closest to the origin of the transfer function, chord 0 and chord 1, are made colinear and contiguous. The beginning of chord 0, specified by the input binary code 000 0000, is offset by +0.5μA. Each chord can be further divided into 16 steps, all of the same size. The step size changes from one chord to another, with the smallest step of 1.0μA found in the first two chords near zero output current, and the largest step of 64μA found in the last chord near full scale output current. This nonlinear feature provides exceptional accuracy for small signal levels. The accuracy for signal amplitudes corresponding to chords 0 and 1 is very close to that of an 11-bit linear, binary D/A converter. The ratio (in dB) between the chord endpoint current, (Step 15), and the current which corresponds to the preceding step, (Step 14), is maintained at about 0.3dB over the entire dynamic range, with the exception of chord 0. The difference between the ratios of full scale current to chord endpoint currents of adjacent chords is similarly maintained at 6dB over the entire dynamic range. Resulting signal-to-quantizing distortions due to non-uniform quantizing levels maintain an acceptably low value over a 40dB range of input speech signals. Note that the 62dB output dynamic range for the Am6073 is very close to the dynamic range of a sign plus 11-bit linear, binary D/A converter.

In order to achieve a smoother transition between adjacent chords, the step size between these chord end points is equal to 1.5 times the step size of the lower chord. Note that this does not apply to chord 0 and chord 1 where adjacent end points differ by only one step, because these two chords are colinear and have the same step sizes. Monotonic operation is guaranteed by the internal device design over the entire output dynamic range by specifying and maintaining the chord end points and step size deviations within the allowable limits.

Operating Modes

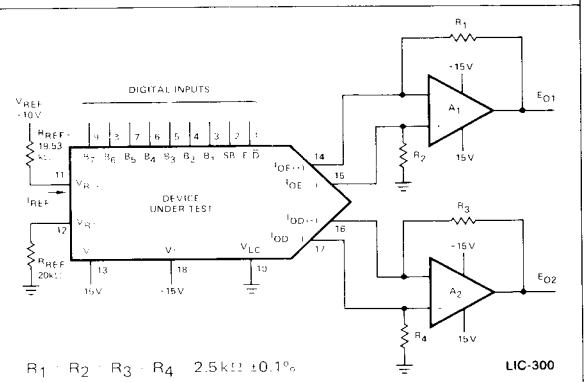
The basic converter function is conversion of digital input data into a corresponding analog current signal, i.e., the basic function is digital-to-analog decoding. The basic decoder connection for a sign plus 7-bit input configuration is shown in Figure 1. The corresponding dynamic range is 62dB, and input-output characteristics conform to the standard decoder transfer function with output current values specified in Table 1. The E/$\overline{D}$ input enables switching between the encode, $I_{OE(+)}$ or $I_{OE(-)}$, and the decode, $I_{OD(+)}$ or $I_{OD(-)}$, outputs. A typical encode/decode test circuit is shown in Figure 2. This circuit is used for output current measurements. When the E/$\overline{D}$ input is high, (a logic 1), the converter will assume the encode operating mode and the output current will flow into one of the I_{OE} outputs (as determined by the SB input). When operating in the encode mode as shown



$I_{REF} = V_{REF}/R_{REF}$
IDEAL VALUES: $I_{REF} = 512\mu A$, $I_{FS} = 2016\mu A$

	E/$\overline{D}$	SB	B_1	B_2	B_3	B_4	B_5	B_6	B_7	E_O
POSITIVE FULL SCALE	0	1	1	1	1	1	1	1	1	5.040V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.004V
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0.0012V
(−) ZERO SCALE	0	0	0	0	0	0	0	0	0	−0.0012V
(−) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	−0.004V
NEGATIVE FULL SCALE	0	0	1	1	1	1	1	1	1	−5.040V

Figure 1. Detailed Decoder Connections.



R_1 R_2 R_3 R_4 2.5kΩ ±0.1%

LINE SELECTION TABLE

TEST GROUP	E/$\overline{D}$	SB	OUTPUT MEASUREMENT	
1	1	1	$I_{OE(+)}$	(E_{O1}, R_1)
2	1	0	$I_{OE(-)}$	(E_{O1}, R_2)
3	0	1	$I_{OD(+)}$	(E_{O2}, R_3)
4	0	0	$I_{OD(-)}$	(E_{O2}, R_4)

Figure 2. Output Current DC Test Circuit.

in Figure 3, an offset current equal to a half step in each chord is required to obtain the correct encoder transfer characteristic. Since the size of this step varies from one chord to another, it cannot easily be added externally. As indicated in the block diagram this required half step of encode current, I_{EN}, is automatically added to the I_{OE} output through the internal chip design. This additional current will, for example, make the ideal full scale current in the encode mode larger than the same current in the decode mode by 32μA. Similarly, the current levels in the first chord near the origin will be offset by 0.5μA, which will bring the ideal encode current value for step 0 on chord 0 to ±1.0μA with respect to the corresponding decode current value of 0.5μA. This additional encode half step of current can be used for extension of the output dynamic range from 62dB to 66dB, when the converter is performing only the decode function. The corresponding decoder connection utilizes the E/$\overline{D}$ input as a ninth digital input and has the outputs $I_{OD(+)}$ and $I_{OE(+)}$ and the outputs $I_{OD(-)}$ and $I_{OE(-)}$ tied together, respectively.

When encoding or compression of an analog signal is required, the Am6072 can be used together with a Successive Approximation Register (SAR), comparator, and additional SSI logic elements to perform the A/D data conversion, as shown in Figure 3. The encoder transfer function, shown on page 1, characterizes this A/D converter system. The first task of this system is to determine the polarity of the incoming analog signal and to generate a corresponding SB input value. When the proper $\overline{\text{START}}$, ($\overline{\text{S}}$), and $\overline{\text{CONVERSION COMPLETE}}$, ($\overline{\text{CC}}$), signal levels are set, the first clock pulse sets the MSB output of the SAR, Am2502, to a logic 0 and sets all other parallel digital outputs to logic 1 levels. At the same time, the flip-flop is triggered, and its output provides the E/$\overline{D}$ input with a logic 0 level. No current flows into the I_{OE} outputs. This disconnects the converter from the comparator inputs, and the incoming analog signal can be compared with the ground applied to the opposite comparator input. The resulting comparator output is fed to the Am2502 serial data input, D, through an exclusive-or gate. At the same time, the second input to the same exclusive-or gate is held at a logic 0 level by the additional successive approximation logic shown in Figure 3. This exclusive-or gate inverts the comparator's outputs whenever a negative signal polarity is detected. This maintains the proper output current coding, i.e., all ones for full scale and all zeros for zero scale.

The second clock pulse changes the E/$\overline{D}$ input back to a logic 1 level because the $\overline{\text{CC}}$ signal changed. It also clocks the D input signal of the Am2502 to its MSB output, and transfers it to the SB input of the Am6073. Depending upon the SB input level, current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output of the Am6073.

Nine clock pulses are required to obtain a digital binary representation of the incoming analog signal at the eight Am2502 digital outputs. The resulting Am6073 analog output signal is compared with the analog input signal after each of the nine successive clock pulses. The analog signal should not be allowed to change its value during the data conversion time. In high speed systems, fast changes of the analog signals at the A/D system input are usually prevented by using sample and hold circuitry.

Additional Considerations and Recommendations

In Figure 1, an optional operational amplifier converts the Am6073 output current to a bipolar voltage output. When the SB input is a logic 1, sink current appears at the amplifier's negative input, and the amplifier acts as a current to voltage converter, yielding a positive voltage output. With the SB value at a logic 0, sink current appears at the amplifier's positive input. The amplifier behaves as a voltage follower, and the true current outputs will swing below ground with essentially no change in output current. The SB input steers current into the appropriate (+) or (−) output of the Am6073. The resulting operational amplifier's output in Figure 1 should ideally be symmetrical with resistors R1 and R2 matched.

In Figure 2, two operational amplifiers measure the currents of each of the four Am6073 analog outputs. Resistor tolerances of 0.1% give 0.1% output measurement error (approximately 2μA at full scale). The input offset currents of the A1 and A2 devices also increase output measurement error and this error is most significant near zero scale. The Am101A and 308 devices, for example, may be used for A1 and A2 since their maximum offset currents, which would add directly to the measurement error, are only 10nA and 1nA respectively. The input offset voltages of the A1 and A2 devices, with output resistor values of 2.5kΩ, also contribute to the output measurement error by a factor of 400nA for

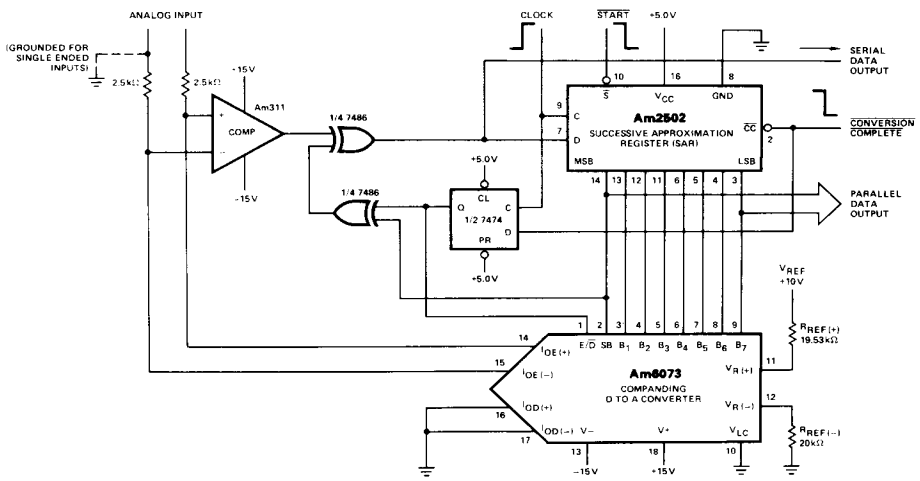


Figure 3. Detailed Encoder Connections. LIC-301

every mV of offset at the A1 and A2 outputs. Therefore, to minimize error, the offset voltages of A1 and A2 should be nulled.

The recommended operating range for the reference current I_{REF} is from 0.1mA to 1.0mA. The full scale output current, I_{FS}, is a linear function of the reference current, and may be calculated from the equation $I_{FS} = 3.94\ I_{REF}$. This tight relationship between I_{REF} and I_{FS} alleviates the requirement for trimming the I_{REF} current if the R_{REF} resistor values are within ±1% of the calculated value. Lower values of I_{REF} will reduce the negative power supply current, (I−), and will increase the reference amplifier negative common mode input voltage range.

The ideal value for the reference current $I_{REF} = V_{REF}/R_{REF}$ is 512μA. The corresponding ideal full scale decode and encode current values are 2016μA and 2048μA, respectively. A percentage change from the ideal I_{REF} value produced by changes in V_{REF} or R_{REF} values produces the same percentage change in decode and encode output current values. The positive voltage supply, V+, may be used, with certain precautions, for the positive reference voltage V_{REF}. In this case, the reference resistor $R_{REF(+)}$ should be split into two resistors and their junction bypassed to ground with a capacitor of 0.01μF. The total resistor value should provide the reference current I_{REF} = 512μA. The resistor $R_{REF(-)}$ value should be approximately equal to the $R_{REF(+)}$ value in order to compensate for the errors caused by the reference amplifier's input offset current.

An alternative to the positive reference voltage applications shown in Figures 1, 2 and 3 is the application of a negative voltage to the $V_{R(-)}$ terminal through the resistor $R_{REF(-)}$ with the $R_{REF(+)}$ resistor tied to ground. The advantage of this arrangement is the presence of very high impedance at the $V_{R(-)}$ terminal while the reference current flows from ground through $R_{REF(+)}$ into the $V_{R(+)}$ terminal.

The Am6073 has a wide output voltage compliance suitable for driving a variety of loads. With I_{REF} = 512μA and V− = −15V, positive voltage compliance is +18V and negative voltage compliance is −5.0V. For other values of I_{REF} and V−, the negative voltage compliance, $V_{OC(-)}$, may be calculated as follows:

$V_{OC(-)} = (V-) + 2(I_{REF} \cdot 1.55k\Omega) + 8.4V$,

where 1.55kΩ and 8.4V are equivalent worst case values for the Am6073.

The following table contains $V_{OC(-)}$ values for some specific V−, I_{REF}, and I_{FS} values.

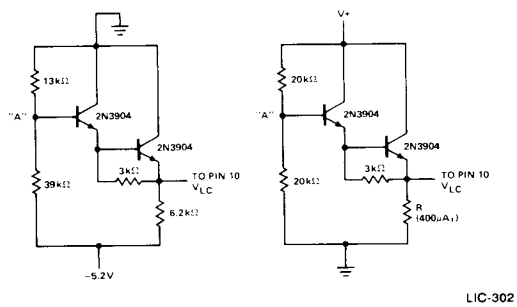
Negative Output Voltage Compliance $V_{OC(-)}$

V−	I_{REF} (I_{FS})		
	256μA (1mA)	512μA (2mA)	1024μA (4mA)
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

The V_{LC} input can accommodate various logic input switching threshold voltages allowing the Am6073 to interface with various logic families. This input should be placed at a potential which is 1.4V below the desired logic input switching threshold. Two external discrete circuits which provide this function for non-TTL driven inputs are shown in Figure 4. For TTL-driven logic inputs, the V_{LC} input should be grounded. If negative voltages are applied at the digital logic inputs, they must have a value which is more positive than the sum of the chosen V− value and +10V.

With a V− value chosen between −15V and −11V, the $V_{OC(-)}$, the input reference common mode voltage range, and the logic input negative voltage range are reduced by an amount equivalent to the difference between −15V and the V− value chosen.

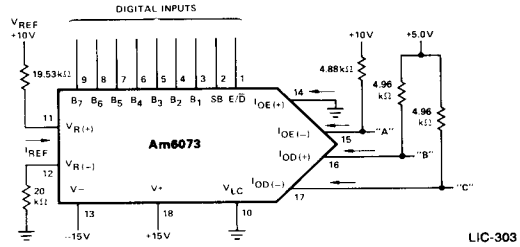
With a V+ value chosen between +5V and +15V, the reference amplifier common mode positive voltage range and the V_{LC} input values are reduced by an amount equivalent to the difference between +15V and the V+ value chosen.



LIC-302

(See Notes 2 and 3)

Figure 4. Interfacing Circuits for ECL, CMOS, HTL, and NMOS Logic Inputs.



LIC-303

INPUT CODE (E/D, SB, B_1, . . . , B_7)	OUTPUT VOLTAGE (V) "A"	"B"	"C"	DIFF
10 111 1111	0			
10 110 1111	+5.00	N/A	N/A	N/A
10 000 0000	+10.00			
01 111 1111		−5.00	+5.00	−10.00
01 110 1111		+0.00	+5.00	−5.00
01 000 0000	N/A	+5.00	+5.00	0
00 000 0000		+5.00	+5.00	0
00 110 1111		+5.00	+0.00	+5.00
00 111 1111		+5.00	−5.00	+10.00

Figure 5. Resistive Output Connections.

Notes: 2. Set the voltage "A" to the desired logic input switching threshold.
3. Allowable range of logic threshold is typically −5V to +13.5V when operating the companding DAC on +15V supplies.

ADDITIONAL DECODE OUTPUT CURRENT TABLES

Table 3
Normalized Decoder Output (Sign Bit Excluded)

STEP (S)		CHORD (C) 0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	1	33	66	132	264	528	1056	2112
1	0001	3	35	70	140	280	560	1120	2240
2	0010	5	37	74	148	296	592	1184	2368
3	0011	7	39	78	156	312	624	1248	2496
4	0100	9	41	82	164	328	656	1312	2624
5	0101	11	43	86	172	344	688	1376	2752
6	0110	13	45	90	180	360	720	1440	2880
7	0111	15	47	94	188	376	752	1504	3008
8	1000	17	49	98	196	392	784	1568	3136
9	1001	19	51	102	204	408	816	1632	3264
10	1010	21	53	106	212	424	848	1696	3392
11	1011	23	55	110	220	440	880	1760	3520
12	1100	25	57	114	228	456	912	1824	3648
13	1101	27	59	118	236	462	944	1888	3776
14	1110	29	61	122	244	488	976	1952	3904
15	1111	31	63	126	252	504	1008	2016	4032
STEP SIZE		2	2	4	8	16	32	64	128

The normalized decode current, ($I_{C,S}$), where C is chord number and S is step number, is calculated using: $I_{CS} = 2^C(S + 16.5)$ for $C \geq 1$, and $I_{C,S} = 2S + 1$ for $C = 0$. The ideal decode current, (I_{OD}), in μA is calculated using: $I_{OD} = (I_{C,S}/I_{7,15(norm.)}) \cdot I_{FS}(\mu A)$, where $I_{C,S}$ is the corresponding normalized current. To obtain normalized encode values the corresponding normalized half-step value should be added to all entries in Table 3.

Table 4
Decoder Step Size Summary

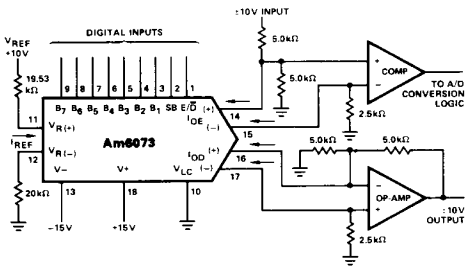
Chord	Step Size Normalized to Full Scale	Step Size in μA with 2016μA F. S.	Step Size as a % of Full Scale	Step Size in dB at Chord Endpoints	Step Size as a % of Reading at Chord Endpoints	Resolution & Accuracy of Equivalent Binary DAC
0	2	1.0	0.05%	0.58	6.45%	Sign + 11 Bits
1	2	1.0	0.05%	0.28	3.17%	Sign + 11 Bits
2	4	2.0	0.1%	0.28	3.17%	Sign + 10 Bits
3	8	4.0	0.2%	0.28	3.17%	Sign + 9 Bits
4	16	8.0	0.4%	0.28	3.17%	Sign + 8 Bits
5	32	16.0	0.8%	0.28	3.17%	Sign + 7 Bits
6	64	32.0	1.6%	0.28	3.17%	Sign + 6 Bits
7	128	64.0	3.2%	0.28	3.17%	Sign + 5 Bits

Table 5
Decoder Chord Size Summary

Chord	Chord Endpoints Normalized to Full Scale	Chord Endpoints in μA with 2016μA F. S.	Chord Endpoints as a % of Full Scale	Chord Endpoints in dB Down from Full Scale
0	31	15.5	0.77%	−42.28
1	63	31.5	1.56%	−36.12
2	126	63.0	3.13%	−30.10
3	252	126.0	6.25%	−24.08
4	504	252.0	12.5%	−18.06
5	1008	504.0	25.0%	−12.04
6	2016	1008.0	50.0%	−6.02
7	4032	2016.0	100%	0

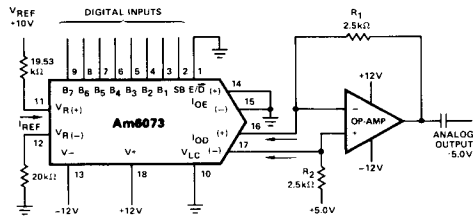
BASIC CIRCUIT CONNECTIONS

±10V RANGE ENCODER/DECODER CONNECTIONS



LIC-304

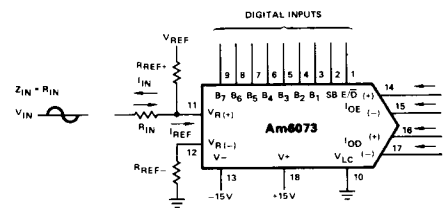
COMPLIANCE EXTENSION USING AC COUPLED OUTPUT



IDEAL VALUES:
$I_{REF} = 512\mu A$
$I_{FS} = 2016\mu A$

LIC-305

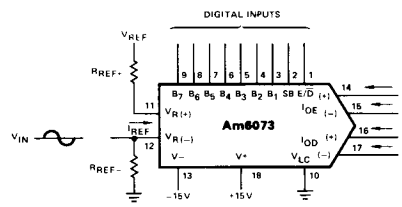
LOW INPUT IMPEDANCE CONNECTION



$I_{REF} = V_{IN}/R_{IN} + V_{REF}/R_{REF+}$
$I_{FS} \approx 4(I_{REF})$
$R_{REF-} = \{(R_{REF+})(R_{IN})\}/(R_{REF+} + R_{IN})$

LIC-306

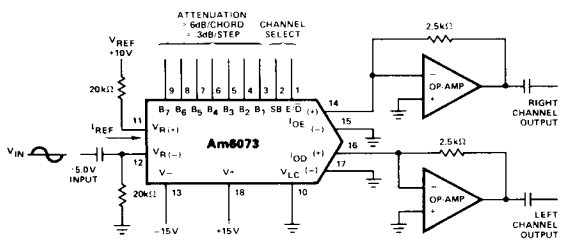
HIGH INPUT IMPEDANCE CONNECTION



$I_{REF} = (V_{REF} - V_{IN})/R_{REF+}$
$I_{FS} \approx 4(I_{REF})$

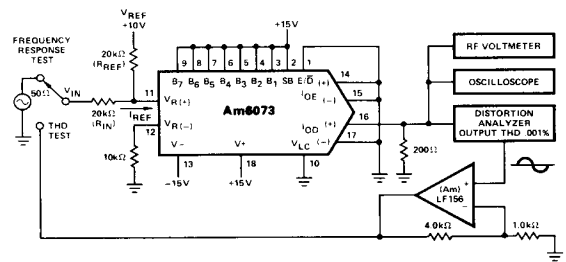
LIC-307

LOGARITHMIC DIGITAL GAIN CONTROL (Notes 4, 5)



LIC-308

REFERENCE AMPLIFIER DYNAMIC TEST CIRCUIT

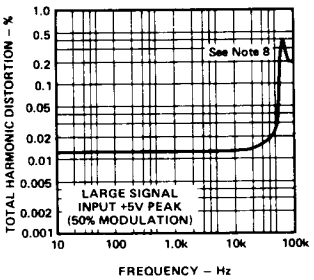


LIC-309

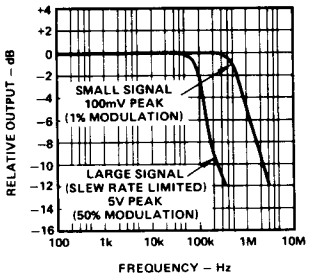
Notes: 4. Low distortion outputs are provided over 62dB range.
5. Up to 4 channels of output may be selected by E/$\overline{D}$ and SB logic inputs.

TYPICAL PERFORMANCE CURVES

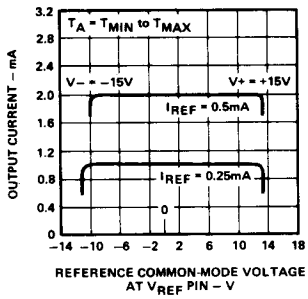
Reference Amplifier Total Harmonic Distortion Versus Frequency (80kHz Filter) (Notes 6, 7, 8)



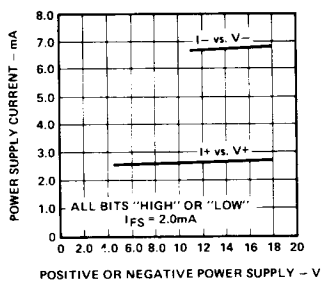
Reference Amplifier Input Frequency Response



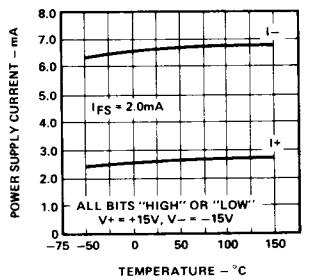
Reference Amplifier Input Common-Mode Range (Note 9)



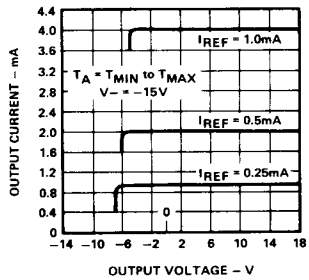
Power Supply Currents Versus Power Supply Voltages



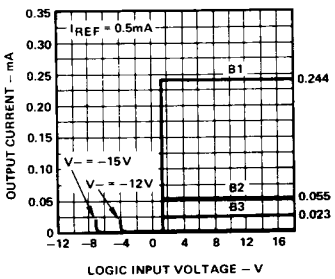
Power Supply Currents Versus Temperature



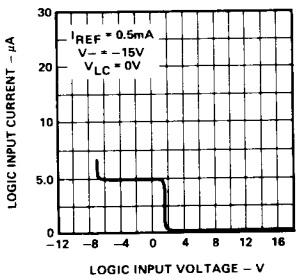
Output Current Versus Output Voltage (Output Voltage Compliance)



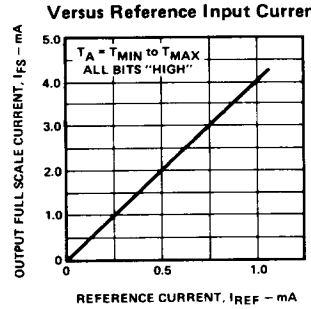
Bit Transfer Characteristics (Note 10)



Logic Input Current Versus Input Voltage and Logic Input Range (Note 11)



Output Full Scale Current Versus Reference Input Current

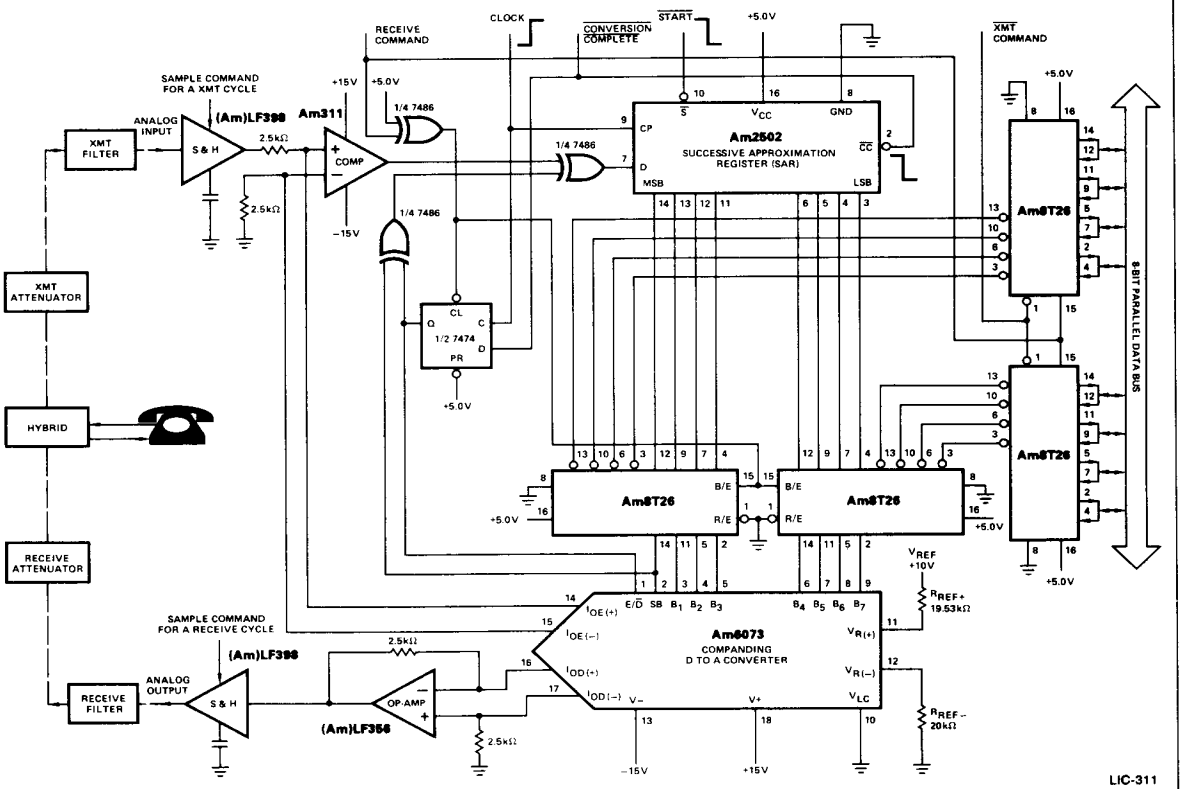


LIC-310

Notes:
6. THD is nearly independent of the logic input code.
7. Similar results are obtained for a high input impedance connection using $V_{R(-)}$ as an input.
8. Increased distortion above 50kHz is due to a slew rate limiting effect which determines the large signal bandwidth. For an input of ±2.5V peak (25% modulation), the bandwidth is 100kHz.
9. Positive common mode range is always (V+) –1.5V.
10. All bits are fully switched with less than a half step error at switching points which are guaranteed to lie between 0.8V and 2.0V over the operating temperature range.
11. The logic input voltage range is independent of the positive power supply and logic inputs may swing above the supply.

TIME SHARED CONVERTER CONNECTIONS

SINGLE CHANNEL PCM CODEC – PARALLEL DATA I/O

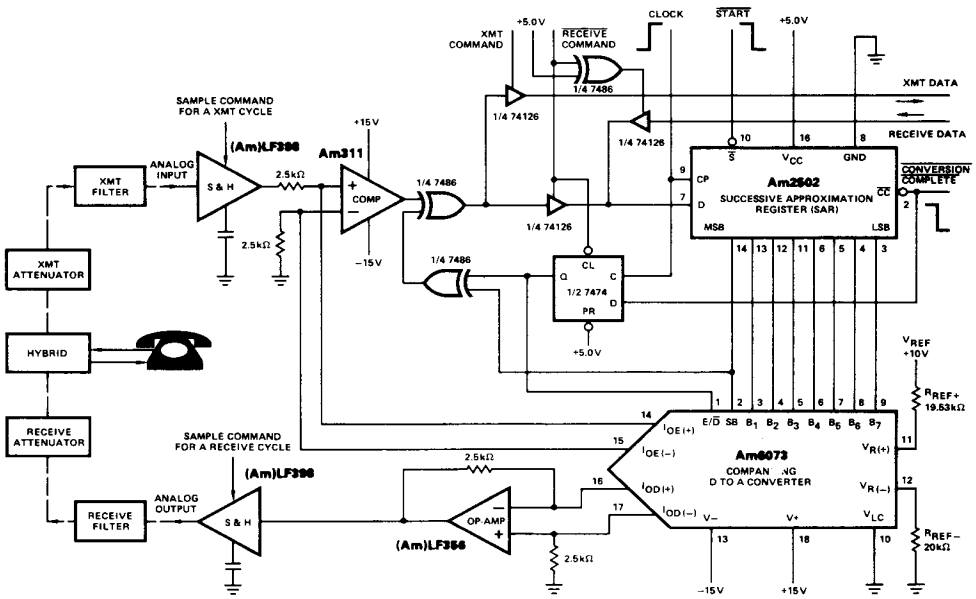


APPLICATION INFORMATION

1. To perform a transmit operation cycle the $\overline{\text{START}}$ pulse must be held low for one clock cycle; the receive operation is performed without the successive approximation register, SAR.
2. $\overline{\text{XMT}}$ and RECEIVE command signals are mutually exclusive.
3. Duration of the RECEIVE command signal must accommodate the Am6073 settling time plus the sampling time required by the sample and hold, (S & H), circuit used at the CODEC's analog output. The receiving data must not change during this time.
4. A $\overline{\text{XMT}}$ command signal must be issued after a high-to-low transition of the $\overline{\text{CONVERSION COMPLETE}}$, $\overline{\text{CC}}$, signal. Its duration depends on the time required by the digital time division switch circuitry to sample the 8-bit parallel transmit data bus.
5. Data conversion for a transmit operation is completed in 9 clock cycles because the SAR must be initialized before every new conversion. Data conversion for a receive operation corresponds to the Am6073 settling time; the receiving and transmit data transfers can be done simultaneously by employing separate transmit and receive data buses and utilizing data storage devices for the receive data.
6. A sample command pulse for a transmit operation can coincide with the $\overline{\text{START}}$ pulse; its duration depends on the sample and hold circuit used at the CODEC's analog input.
7. A sample command pulse for a receive operation must be delayed from a low-to-high transition of the RECEIVE command signal by an amount equal to the Am6073 settling time. Its termination can coincide with a high-to-low transition of the RECEIVE command signal.
8. The code assignment for outgoing or incoming parallel data provides uncomplemented binary values for signal sign and magnitude. The data bus, as a result, yields "high zeros" density for small signal amplitudes.

TIME SHARED CONVERTER CONNECTIONS (Cont.)

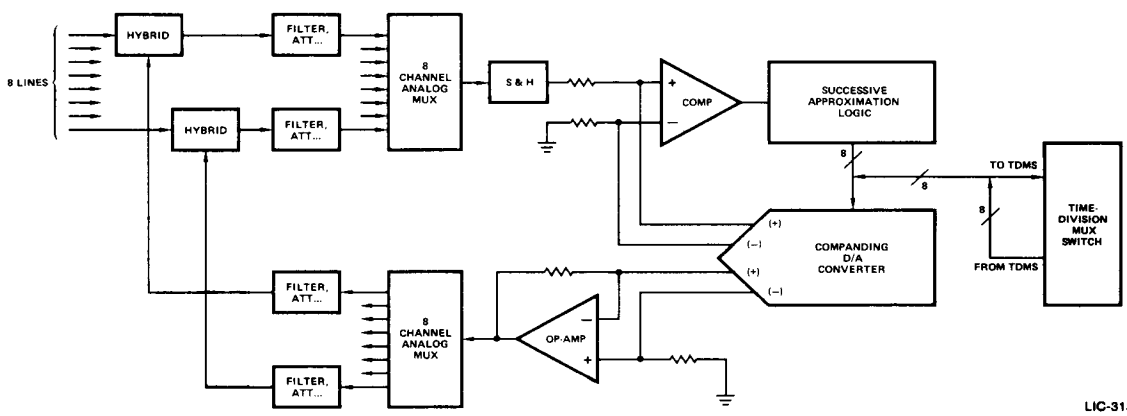
SINGLE CHANNEL PCM CODEC – SERIAL DATA I/O



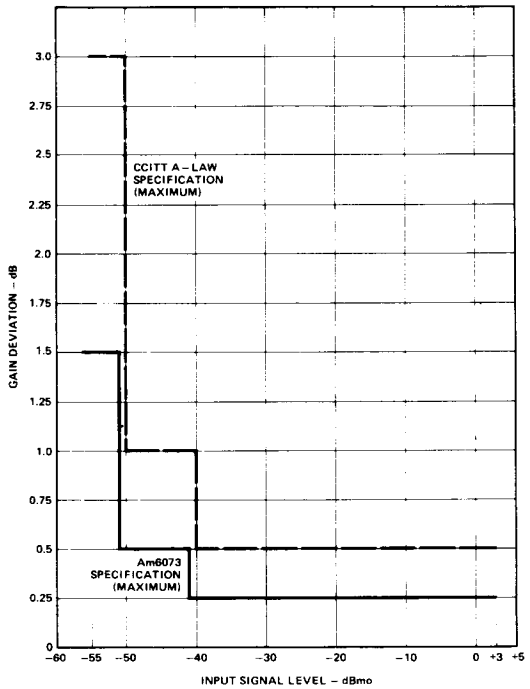
APPLICATION INFORMATION

1. Before beginning either a transmit or a receive operation, the $\overline{\text{START}}$ signal must be held low for one complete clock cycle.
2. XMT and $\overline{\text{RECEIVE}}$ command signals are mutually exclusive. Their durations must accommodate the time required for conversion of an outgoing or an incoming series of 8 digital bits, respectively.
3. Data conversion for either operation, transmit or receive, is completed in 9 clock cycles.
4. During the receive cycle the successive approximation register, SAR, is acting as a serial-in to parallel-out shift register, with data supplied from data storage devices.
5. A sample command pulse for a transmit cycle must be issued before a XMT command signal; its duration depends on the sample and hold, S & H, circuit used.
6. A sample command pulse for a receive cycle must be delayed by a time equal to the Am6073 settling time after a high-to-low transition of the $\overline{\text{CONVERSION COMPLETE}}$, $\overline{\text{CC}}$, signal occurs.
7. The code assignment for outgoing or incoming parallel data provides uncomplemented binary values for signal sign and magnitude. The data bus, as a result, yields "high zeros" density for small signal amplitudes.

8 LINE CODEC TDM PCM/PABX SYSTEM – BLOCK DIAGRAM

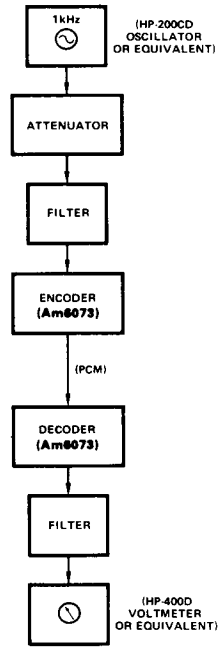


CCITT A–LAW COMPANDOR TRACKING SPECIFICATION



LIC-314

COMPANDOR TRACKING TEST BLOCK DIAGRAM



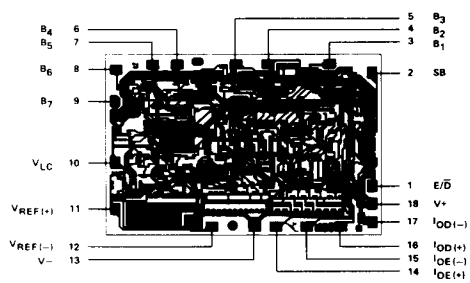
LIC-315

CCITT NOISE AND DISTORTION SPECIFICATION

The Am6073 has a negligible idle channel noise contribution. Signal-to-quantizing-distortion ratio, (S/D), is guaranteed to exceed the minimum values specified for PCM channels at audio frequencies as follows:

Input Level 1020 Hz Sinewave	S/D, C-Message Weighting
0 to –30 dBmo	33 dB
At –40 dBmo	27 dB
At –45 dBmo	22 dB

Metallization and Pad Layout



80 X 114 Mils