

32-BIT CMOS

**Intergraph Corp.
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Status: The company has shipped over 70,000 CLIPPER modules through July 1991, giving CLIPPER a large installed base. Intergraph accounts for most of the CLIPPER sales.

HARDWARE

SOFTWARE



II DATA-MOVEMENT INSTRUCTIONS

III PROGRAM-MANIPULATION INSTR

IV PROGRAM-STATUS-MANIP INSTR

V SPECIAL INSTRUCTIONS

Specification summary: For optimum performance, the C411 utilizes a large external cache to supply instructions and data on every clock cycle at 50 MHz. The processor uses separate 64-bit input and 32-bit output buses to support the CPU's data and instruction bandwidth requirements. Fast IEEE 754 floating-point operations are executed by the C421 coprocessor also running at 50 MHz. The C411 CPU can be purchased individually or as a pair with the C421 FPU coprocessor. Both are available in 299-pin PGA packages. Future versions of the C400 family are planned to operate at speeds greatly in excess of 50 MHz.

Software notes:

1. The C300's 164 instructions are a balance between 1-cycle-RISC and multicycle-CISC commands. Hardwired architecture in the C400 allows most instructions to execute in one clock cycle. C400 superscalar operations issue multiple instructions on each clock cycle.
2. The C411 CPU and C421 FPU instructions are compatible with the C300.
3. The C421 is compatible with the IEEE 754 floating-point standard.

SUPPORT

SOFTWARE

Intergraph offers a set of optimizing compilers for C and FORTRAN, and a performance-tuned operating system kernel for the CLIPPER C411/C421. More than 750 third-party packages are available, including compilers for LISP, Ada, and other languages; tools and utilities; end-user application packages in the areas of Mechanical/Manufacturing, Architecture/Facility Management, Electronic Design, Utilities and Public Works, Mapping/GIS, Publishing, and more.