SMALL-OUTLINE DRAM MODULE

MT4LDT164H(X)(S),
MT8LDT264H(X)(S)

For the latest data sheet revisions, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- JEDEC pinout in a 144-pin, small-outline, dual in-line memory module (DIMM)
- 8MB (1 Meg x 64) and 16MB (2 Meg x 64)
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR) and HIDDEN
- Optional Self Refresh Mode (S)
- 1,024-cycle refresh distributed across 16ms (8MB) or 2,048-cycle refresh distributed across 32ms (16MB) or self refresh distributed across 128ms
- FAST-PAGE-MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles
- Serial presence-detect (SPD)

OPTIONS — MARKING

- Package
  144-pin Small-Outline DIMM (gold) — G
- Timing
  50ns access — -5*
  60ns access — -6
- Access Cycles
  FAST PAGE MODE — None
  EDO PAGE MODE — X
- Refresh Rates
  Standard Refresh — None
  Self Refresh (128ms period) — S

*EDO version only

KEY TIMING PARAMETERS

EDO Operating Mode

SPEED	tRC	tRAC	tPC	tAA	tCAC	tCAS
-5	84ns	50ns	20ns	25ns	13/15**ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

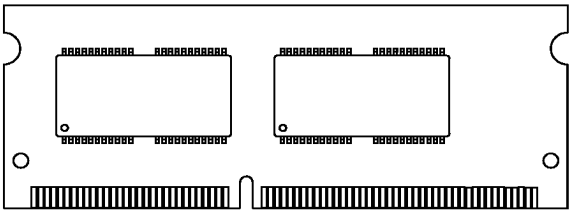
**8MB DIMM

FPM Operating Mode

SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns

PIN ASSIGNMENT (Front View)

144-Pin Small-Outline DIMM



PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	VSS	2	VSS	73	OE#	74	RFU
3	DQ0	4	DQ32	75	VSS	76	VSS
5	DQ1	6	DQ33	77	RSVD	78	RSVD
7	DQ2	8	DQ34	79	RSVD	80	RSVD
9	DQ3	10	DQ35	81	VDD	82	VDD
11	VDD	12	VDD	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	VSS	92	VSS
21	VSS	22	VSS	93	DQ20	94	DQ52
23	CAS0#	24	CAS4#	95	DQ21	96	DQ53
25	CAS1#	26	CAS5#	97	DQ22	98	DQ54
27	VDD	28	VDD	99	DQ23	100	DQ55
29	A0	30	A3	101	VDD	102	VDD
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	NC (A11)
35	VSS	36	VSS	107	VSS	108	VSS
37	DQ8	38	DQ40	109	A9	110	NC (A12)
39	DQ9	40	DQ41	111	A10	112	NC (A13)
41	DQ10	42	DQ42	113	VDD	114	VDD
43	DQ11	44	DQ43	115	CAS2#	116	CAS6#
45	VDD	46	VDD	117	CAS3#	118	CAS7#
47	DQ12	48	DQ44	119	VSS	120	VSS
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	VSS	56	VSS	127	DQ27	128	DQ59
57	RSVD	58	RSVD	129	VDD	130	VDD
59	RSVD	60	RSVD	131	DQ28	132	DQ60
61	RFU	62	RFU	133	DQ29	134	DQ61
63	VDD	64	VDD	135	DQ30	136	DQ62
65	RFU	66	RFU	137	DQ31	138	DQ63
67	WE#	68	RFU	139	VSS	140	VSS
69	RAS0#	70	NC	141	SDA	142	SCL
71	NC	72	NC	143	VDD	144	VDD

NOTE: Symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

PART NUMBERS

EDO Operating Mode

PART NUMBER	CONFIGURATION	REFRESH
MT4LDT164HG-x X	1 Meg x 64	Standard
MT4LDT164HG-x XS	1 Meg x 64	Self
MT8LDT264HG-x X	2 Meg x 64	Standard
MT8LDT264HG-x XS	2 Meg x 64	Self

x = speed

FPM Operating Mode

PART NUMBER	CONFIGURATION	REFRESH
MT4LDT164HG-x	1 Meg x 64	Standard
MT4LDT164HG-x S	1 Meg x 64	Self
MT8LDT264HG-x	2 Meg x 64	Standard
MT8LDT264HG-x S	2 Meg x 64	Self

x = speed

GENERAL DESCRIPTION

The MT4LDT164H(X)(S) and MT8LDT264H(X)(S) are randomly accessed 8MB and 16MB memories organized in a small-outline x64 configuration. They are specially processed to operate from 3V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the 20/21 address bits which are entered 10 bits (A0-A10) at a time. RAS# is used to latch the first 11 bits and CAS# the latter 10 bits.

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. If WE# goes LOW prior to CAS# going LOW, the output pin(s) remain open (High-Z) until the next CAS# cycle.

FAST PAGE MODE

FAST-PAGE-MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST-PAGE-MODE cycle is always initiated with a row address strobed in by RAS#, followed by a column address strobed in by CAS#. Additional columns may be accessed by providing valid column addresses, strobing CAS# and holding RAS# LOW, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST-PAGE-MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" option, is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipeline READs.

FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after CAS# goes HIGH, as long as RAS# and OE# are held LOW and WE# is held HIGH. (Refer to the 1 Meg x 16 (MT4LC1M16E5) DRAM data sheet for additional information on EDO functionality.)

REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses are executed at least every ^{t}REF, regardless of sequence. The CBR Refresh cycle will invoke the internal refresh counter for automatic RAS# addressing.

An optional self refresh mode is also available. The "S" option allows the user the choice of a fully static, low-power data retention mode or a dynamic refresh mode at the extended refresh period of 128ms. The optional self refresh feature is initiated by performing a CBR REFRESH cycle and holding RAS# LOW for the specified ^{t}RASS.

The self refresh mode is terminated by driving RAS# HIGH for a minimum time of ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting self refresh. However, if the DRAM controller utilizes a RAS#-ONLY or burst refresh sequence, all rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time.

SERIAL PRESENCE-DETECT OPERATION

This module family incorporates serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various DRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals.

SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

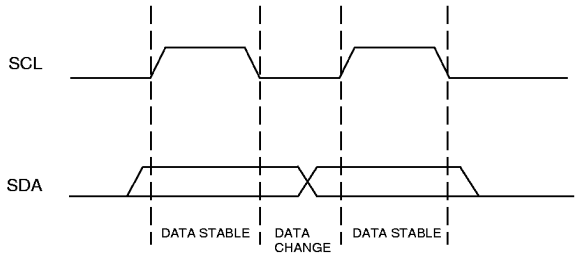


Figure 1
DATA VALIDITY

SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

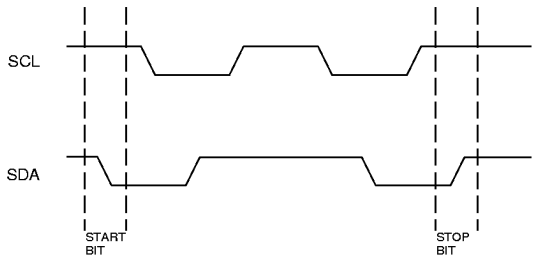


Figure 2
DEFINITION OF START AND STOP

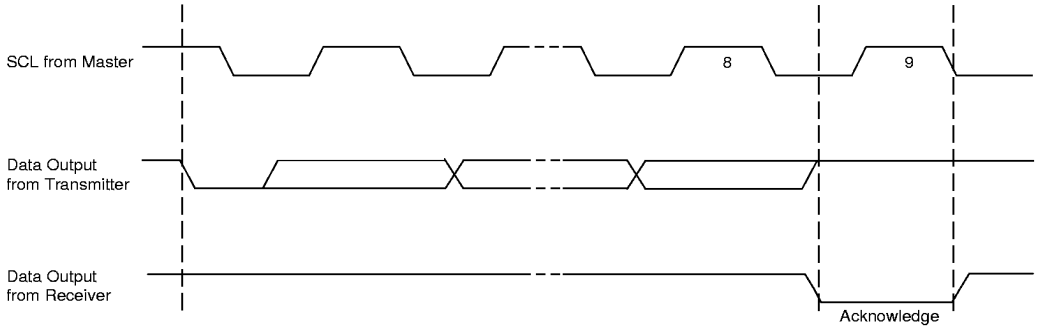
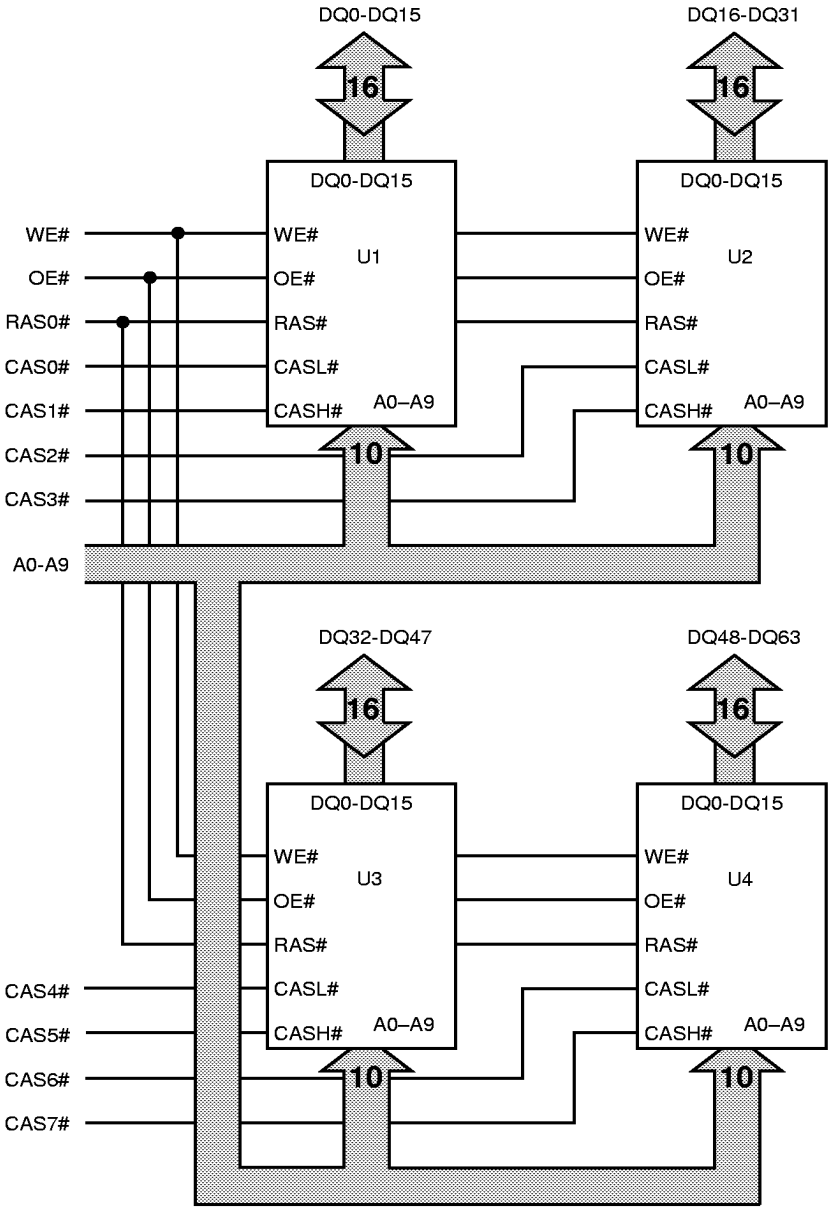
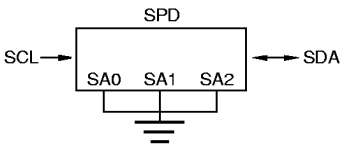


Figure 3
ACKNOWLEDGE RESPONSE FROM RECEIVER

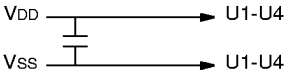
FUNCTIONAL BLOCK DIAGRAM
MT4LDT164H (8MB)



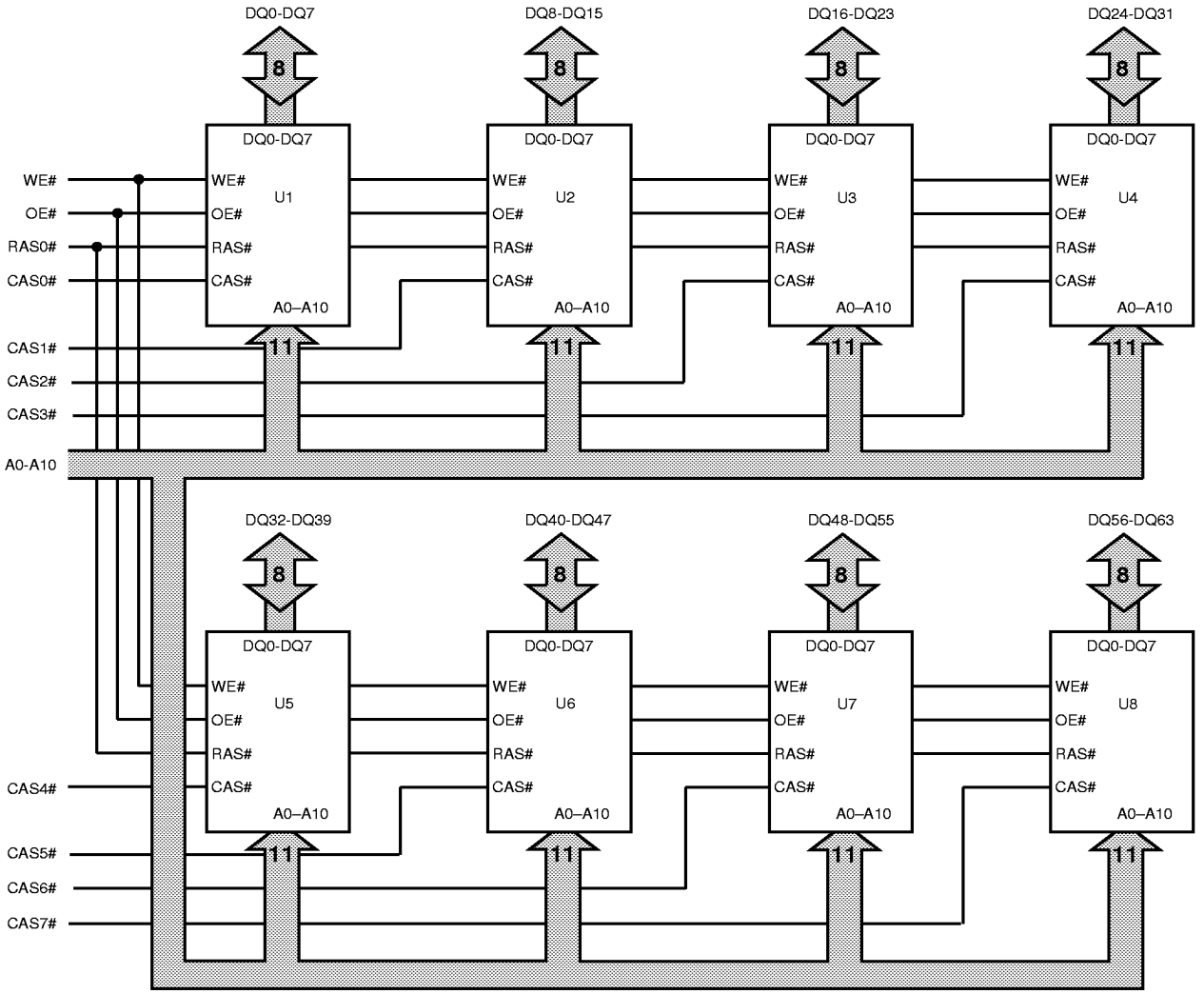


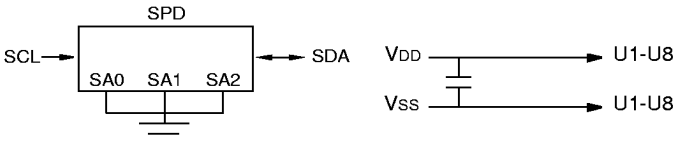
U1-U4 = MT4LC1M16C3(S) FAST PAGE MODE

U1-U4 = MT4LC1M16E5(S) EDO PAGE MODE



FUNCTIONAL BLOCK DIAGRAM
MT8LDT264H (16MB)





U1-U8 = MT4LC2M8B1(S) FAST PAGE MODE

U1-U8 = MT4LC2M8E7(S) EDO PAGE MODE

SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	ENTRY (VERSION)	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
0	NUMBER OF BYTES USED BY MICRON	128	1	0	0	0	0	0	0	0	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256	0	0	0	0	1	0	0	0	08
2	MEMORY TYPE	FAST PAGE MODE	0	0	0	0	0	0	0	1	01
		EDO PAGE MODE	0	0	0	0	0	0	1	0	02
3	NUMBER OF ROW ADDRESSES	10 (8MB)	0	0	0	0	1	0	1	0	0A
		11 (16MB)	0	0	0	0	1	0	1	1	0B
4	NUMBER OF COLUMN ADDRESSES	10	0	0	0	0	1	0	1	0	0A
5	NUMBER OF BANKS	1	0	0	0	0	0	0	0	1	01
6	DATA WIDTH	x64	0	1	0	0	0	0	0	0	40
7	DATA WIDTH (continued)	NONE	0	0	0	0	0	0	0	0	00
8	VOLTAGE INTERFACE	LVTTL	0	0	0	0	0	0	0	1	01
9	RAS# ACCESS TIME (^{t}RAC)	50ns	0	0	1	1	0	0	1	0	32
		60ns	0	0	1	1	1	1	0	0	3C
10	CAS# ACCESS TIME (^{t}CAC)	13ns	0	0	0	0	1	1	0	1	0D
		15ns	0	0	0	0	1	1	1	1	0F
11	MODULE CONFIGURATION TYPE	NONPARITY	0	0	0	0	0	0	0	0	00
12	REFRESH RATES	15.625µs/NORMAL	0	0	0	0	0	0	0	0	00
		8X–125µs/SELF (8MB)	1	0	0	0	0	1	0	1	85
		4X–62.5µs/SELF (16MB)	1	0	0	0	0	1	0	0	84
13	DRAM WIDTH (PRIMARY DRAM)	x16 (8MB)	0	0	0	1	0	0	0	0	10
		x8 (16MB)	0	0	0	0	1	0	0	0	08
14	ERROR CHECKING DRAM DATA WIDTH	NONE	0	0	0	0	0	0	0	0	00
15-61	RESERVED		0	0	0	0	0	0	0	0	00
62	SPD REVISION	REV. 0	0	0	0	0	0	0	0	0	00
63	CHECKSUM FOR BYTES 0-62		x	x	x	x	x	x	x	x	xx
64	MANUFACTURER'S JEDEC ID CODE	MICRON	0	0	1	0	1	1	0	0	2C
65-71	MANUFACTURER'S JEDEC CODE (CONT.)		1	1	1	1	1	1	1	1	FF
72	MANUFACTURING LOCATION		0	0	0	0	0	0	0	1	01
			0	0	0	0	0	0	1	0	02
			0	0	0	0	0	0	1	1	03
			0	0	0	0	0	1	0	0	04
73-90	MODULE PART NUMBER (ASCII)		x	x	x	x	x	x	x	x	xx
91	PCB IDENTIFICATION CODE	1	0	0	0	0	0	0	0	1	01
		2	0	0	0	0	0	0	1	0	02
		3	0	0	0	0	0	0	1	1	03
		4	0	0	0	0	0	1	0	0	04
92	IDENTIFICATION CODE (CONT.)	0	0	0	0	0	0	0	0	0	00
93	YEAR OF MANUFACTURE IN BCD		x	x	x	x	x	x	x	x	xx
94	WEEK OF MANUFACTURE IN BCD		x	x	x	x	x	x	x	x	xx
95-98	MODULE SERIAL NUMBER		x	x	x	x	x	x	x	x	xx
99-125	MANUFACTURE SPECIFIC DATA (RSVD)		–	–	–	–	–	–	–	–	–

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
2. x = Variable Data.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply Relative to V_{SS} ..... -1V to +4.6V
Voltage on Inputs or I/O Pins
Relative to V_{SS} ..... -1V to +4.6V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 4W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE		V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs		V_{IH}	2	V_{DD} + 0.3	V	31
INPUT LOW VOLTAGE: Logic 0; All inputs		V_{IL}	-0.5	0.8	V	31
INPUT LEAKAGE CURRENT:	RAS0#	I_{I1}	-16	16	µA	23
Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V	A0-A10, WE#, OE#	I_{I2}	-16	16	µA	23
(All other pins not under test = 0V)	CAS0#-CAS7#	I_{I3}	-2	2	µA	
OUTPUT LEAKAGE CURRENT: DQ is disabled; 0V ≤ V_{OUT} ≤ V_{DD} + 0.3V	DQ0-DQ63	I_{OZ}	-5	5	µA	
OUTPUT LEVELS: Output High Voltage (I_{OUT} = -2mA)		V_{OH}	2.4	–	V	
Output Low Voltage (I_{OUT} = 2mA)		V_{OL}	–	0.4	V	

I_{CC} OPERATING CONDITIONS AND MAXIMUM LIMITS

(Notes: 1, 5, 6) (V_{DD} = +3.3V ±0.3V)

			MAX			
PARAMETER/CONDITION	SYMBOL	SIZE	-5*	-6	UNITS	NOTES
STANDBY CURRENT: TTL (RAS# = CAS# = V_{IH})	I_{CC1}	8MB 16MB	4 8	4 8	mA	
STANDBY CURRENT: CMOS (RAS# = CAS# = V_{DD} - 0.2V)	I_{CC2}	8MB 16MB	2 8	2 8	mA	26
	I_{CC2} (S only)	8MB 16MB	0.6 1.2	0.6 1.2	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: ^{t}RC = ^{t}RC [MIN])	I_{CC3}	8MB 16MB	720 880	680 800	mA	3, 22
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^{t}PC = ^{t}PC [MIN]; ^{t}CP, ^{t}ASC = 10ns)	I_{CC4}	8MB 16MB	– –	360 640	mA	3, 22
OPERATING CURRENT: EDO PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^{t}PC = ^{t}PC [MIN])	I_{CC5} (X only)	8MB 16MB	560 880	520 800	mA	3, 22
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: ^{t}RC = ^{t}RC [MIN])	I_{CC6}	8MB 16MB	720 880	680 800	mA	3, 22
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^{t}RC = ^{t}RC [MIN])	I_{CC7}	8MB 16MB	720 880	680 800	mA	3, 4
REFRESH CURRENT: Self ("S" version only) Average power supply current: CBR cycling with RAS# ≥ $^{t}RASS$ (MIN) and CAS# held LOW; WE# = V_{DD} - 0.2V; A0-A10 OE# and D_{IN} = V_{DD} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	8MB 16MB	1.2 2.4	1.2 2.4	mA	3, 4

* EDO version only

CAPACITANCE

		MAX			
PARAMETER	SYMBOL	8MB	16MB	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}	24	46	pF	2
Input Capacitance: WE#, OE#, RAS0#	C_{I2}	32	62	pF	2
Input Capacitance: CAS0#-CAS7#	C_{I3}	10	20	pF	2
Input/Output Capacitance: DQ0-DQ63	C_{IO1}	10	18	pF	2
Input/Output Capacitance: SDA, SCL	C_{IO2}	10	10	pF	2

FAST PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 12, 19) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6			
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Access time from column address	^tAA		30	ns	
Column-address hold time (referenced to RAS#)	^tAR	45		ns	
Column-address setup time	^tASC	0		ns	
Row-address setup time	^tASR	0		ns	
Column address to WE# delay time	^tAWD	55		ns	28
Access time from CAS#	^tCAC		15	ns	
Column-address hold time	^tCAH	10		ns	
CAS# pulse width	^tCAS	15	10,000	ns	
CAS# LOW to "Don't Care" during Self Refresh	^tCHD	15		ns	27
CAS# hold time (CBR Refresh)	^tCHR	10		ns	4
CAS# to output in Low-Z	^tCLZ	3		ns	21
CAS# precharge time	^tCP	10		ns	13
Access time from CAS# precharge	^tCPA		35	ns	
CAS# to RAS# precharge time	^tCRP	5		ns	
CAS# hold time	^tCSH	60		ns	
CAS# setup time (CBR Refresh)	^tCSR	5		ns	
CAS# to WE# delay time	^tCWD	40		ns	28
WRITE command to CAS# lead time	^tCWL	15		ns	
Data-in hold time	^tDH	10		ns	18
Data-in setup time	^tDS	0		ns	18
Output disable	^tOD	3	15	ns	
Output enable	^tOE		15	ns	
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^tOEH	15		ns	29
Output buffer turn-off delay	^tOFF	3	15	ns	17, 24
OE# setup prior to RAS# during HIDDEN REFRESH cycle	^tORD	0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPRWC	85		ns	
Access time from RAS#	^tRAC		60	ns	
RAS# to column-address delay time	^tRAD	15		ns	15
Row-address hold time	^tRAH	10		ns	
RAS# pulse width	^tRAS	60	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	^tRASP	60	125,000	ns	

FAST PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 12, 19) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6			
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
RAS# pulse width during Self Refresh	^{t}RASS	100		µs	27
Random READ or WRITE cycle time	^{t}RC	110		ns	
RAS# to CAS# delay time	^{t}RCD	20		ns	14
READ command hold time (referenced to CAS#)	^{t}RCH	0		ns	16
READ command setup time	^{t}RCS	0		ns	
Refresh period (1,024 cycles)	^{t}REF		16	ms	
Refresh period (2,048 cycles)	^{t}REF		32	ms	
Refresh period "S" version	^{t}REF		128	ms	27
RAS# precharge time	^{t}RP	40		ns	
RAS# to CAS# precharge time	^{t}RPC	0		ns	
RAS# precharge time exiting Self Refresh	^{t}RPS	110		ns	27
READ command hold time (referenced to RAS#)	^{t}RRH	0		ns	16
RAS# hold time	^{t}RSH	15		ns	
READ-WRITE cycle time	^{t}RWC	155		ns	
RAS# to WE# delay time	^{t}RWD	85		ns	28
WRITE command to RAS# lead time	^{t}RWL	15		ns	
Transition time (rise or fall)	^{t}T	2	50	ns	
WRITE command hold time	^{t}WCH	10		ns	
WRITE command hold time (referenced to RAS#)	^{t}WCR	45		ns	
WE# command setup time	^{t}WCS	0		ns	28
WRITE command pulse width	^{t}WP	10		ns	
WE# hold time (CBR Refresh)	^{t}WRH	10		ns	
WE# setup time (CBR Refresh)	^{t}WRP	10		ns	

EDO PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 12, 19) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column address	^tAA		25		30	ns	
Column-address setup to CAS# precharge	^tACH	12		15		ns	
Column-address hold time (referenced to RAS#)	^tAR	38		45		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Column address to WE# delay time	^tAWD	42		49		ns	28
Access time from CAS#	^tCAC		13/15*		15*	ns	
Column-address hold time	^tCAH	8		10		ns	
CAS# pulse width	^tCAS	8	10,000	10	10,000	ns	
CAS# LOW to "Don't Care" during Self Refresh	^tCHD	15		15		ns	27
CAS# hold time (CBR Refresh)	^tCHR	8		10		ns	4
CAS# to output in Low-Z	^tCLZ	0		0		ns	
Data output hold after next CAS# LOW	^tCOH	3		3		ns	
CAS# precharge time	^tCP	8		10		ns	13
Access time from CAS# precharge	^tCPA		28		35	ns	
CAS# to RAS# precharge time	^tCRP	5		5		ns	
CAS# hold time	^tCSH	38		45		ns	
CAS# setup time (CBR Refresh)	^tCSR	5		5		ns	
CAS# to WE# delay time	^tCWD	28		35		ns	28
WRITE command to CAS# lead time	^tCWL	8		10		ns	
Data-in hold time	^tDH	8		10		ns	18
Data-in setup time	^tDS	0		0		ns	18
Output disable	^tOD	0	12	0	15	ns	
Output enable	^tOE		12		15	ns	
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^tOEH	8		10/12**		ns	29
OE# HIGH hold from CAS# HIGH	^tOEHC	5		10		ns	29
OE# HIGH pulse width	^tOEP	5		5		ns	
OE# LOW to CAS# HIGH setup time	^tOES	4		5		ns	
Output buffer turn-off delay	^tOFF	0	12	0	15	ns	17, 24

* 8MB DIMM
**16MB DIMM

EDO PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 12, 19) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
OE# setup prior to RAS# during HIDDEN REFRESH cycle	tORD	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	tPC	20		25		ns	
EDO-PAGE-MODE READ-WRITE cycle time	tPRWC	47		56		ns	
Access time from RAS#	tRAC		50		60	ns	
RAS# to column-address delay time	tRAD	9		12		ns	15
Row-address hold time	tRAH	9		10		ns	
RAS# pulse width	tRAS	50	10,000	60	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	tRASP	50	125,000	60	125,000	ns	
RAS# pulse width during Self Refresh	tRASS	100		100		µs	27
Random READ or WRITE cycle time	tRC	84		104		ns	
RAS# to CAS# delay time	tRCD	11		14		ns	14
READ command hold time (referenced to CAS#)	tRCH	0		0		ns	16
READ command setup time	tRCS	0		0		ns	
Refresh period (1,024 cycles) (8MB)	tREF		16		16	ms	
Refresh period (2,048 cycles) (16MB)	tREF		32		32	ms	
Refresh period "S" version	tREF		128		128	ms	
RAS# precharge time	tRP	30		40		ns	
RAS# to CAS# precharge time	tRPC	5		5		ns	
RAS# precharge time exiting Self Refresh	tRPS	90		105		ns	27
READ command hold time (referenced to RAS#)	tRRH	0		0		ns	16
RAS# hold time	tRSH	13		15		ns	
READ-WRITE cycle time	tRWC	116		140		ns	
RAS# to WE# delay time	tRWD	67		79		ns	28
WRITE command to RAS# lead time	tRWL	13		15		ns	
Transition time (rise or fall)	tT	2	50	2	50	ns	
WRITE command hold time	tWCH	8		10		ns	
WRITE command hold time (referenced to RAS#)	tWCR	38		45		ns	
WE# command setup time	tWCS	0		0		ns	28
Output disable delay from WE#	tWHZ	0	12	0	15	ns	
WRITE command pulse width	tWP	5		5		ns	
WE# pulse to disable at CAS# HIGH	tWPZ	10		10		ns	
WE# hold time (CBR Refresh)	tWRH	8		10		ns	
WE# setup time (CBR Refresh)	tWRP	8		10		ns	

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS

(Notes: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	$V_{DD} \times 0.7$	$V_{DD} + 0.5$	V	
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	$V_{DD} \times 0.3$	V	
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V	
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA	
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA	
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = GND or 3.3V +10%	I_{SB}	–	30	µA	
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{CC}	–	2	mA	

SERIAL PRESENCE-DETECT EEPROM AC ELECTRICAL CHARACTERISTICS

(Notes: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^tAA	0.3	3.5	µs	
Time the bus must be free before a new transition can start	^tBUF	4.7		µs	
Data-out hold time	^tDH	300		ns	
SDA and SCL fall time	^tF		300	ns	
Data-in hold time	$^tHD:DAT$	0		µs	
Start condition hold time	$^tHD:STA$	4		µs	
Clock HIGH period	^tHIGH	4		µs	
Noise suppression time constant at SCL, SDA inputs	^tI		100	ns	
Clock LOW period	^tLOW	4.7		µs	
SDA and SCL rise time	^tR		1	µs	
SCL clock frequency	^tSCL		100	KHz	
Data-in setup time	$^tSU:DAT$	250		ns	
Start condition setup time	$^tSU:STA$	4.7		µs	
Stop condition setup time	$^tSU:STO$	4.7		µs	
WRITE cycle time	^tWR		10	ms	30

NOTES

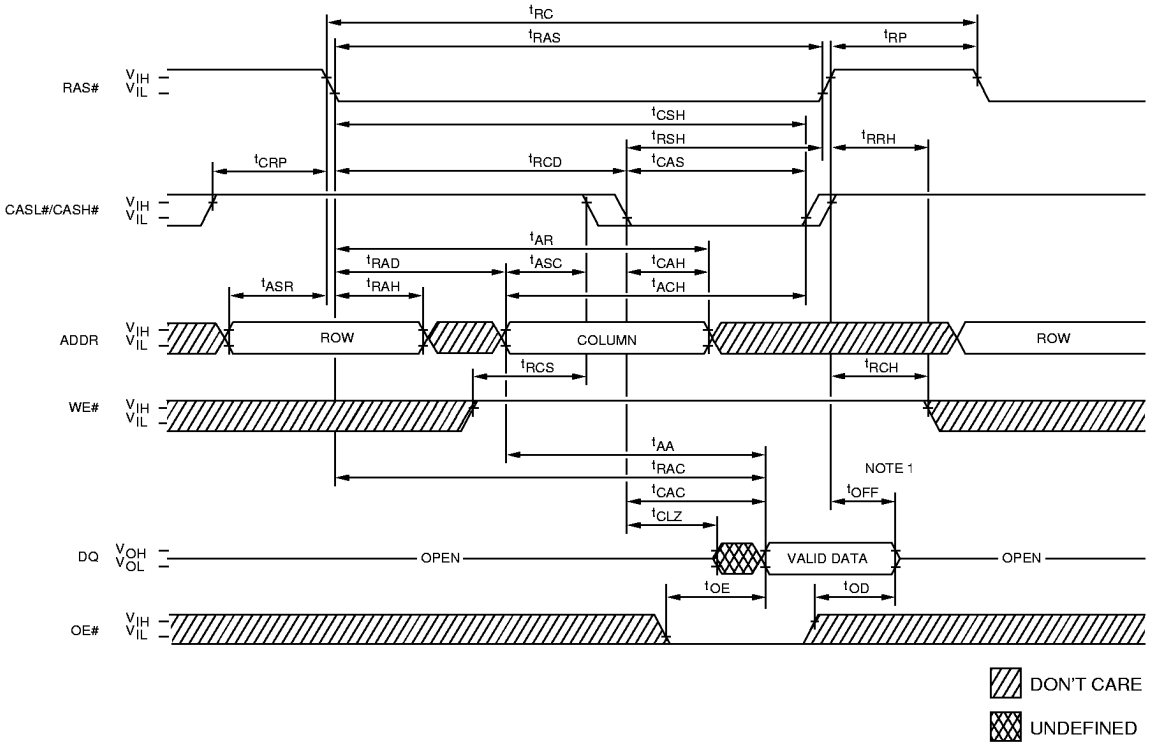
1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{DD} = +3.3V; f = 1 MHz.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# REFRESH cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 5ns for FPM and ^{t}T = 2.5ns for EDO.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH}, data output is High-Z.
11. If CAS# = V_{IL}, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF and V_{OL} = 0.8V and V_{OH} = 2V.
13. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ^{t}CP.
14. The ^{t}RCD (MAX) limit is no longer specified. ^{t}RCD (MAX) was specified as a reference point only. If ^{t}RCD was greater than the specified ^{t}RCD (MAX) limit, then access time was controlled exclusively by ^{t}CAC (^{t}RAC [MIN] no longer applied). With or without the ^{t}RCD (MAX) limit, ^{t}AA and ^{t}CAC must always be met.
15. The ^{t}RAD (MAX) limit is no longer specified. ^{t}RAD (MAX) was specified as a reference point only. If ^{t}RAD was greater than the specified ^{t}RAD (MAX) limit, then access time was controlled exclusively by ^{t}AA (^{t}RAC and ^{t}CAC no longer applied). With or without the ^{t}RAD (MAX) limit, ^{t}AA, ^{t}RAC and ^{t}CAC must always be met.
16. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
17. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
18. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
19. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted. Additionally, with EDO, WE# must be pulsed during CAS# HIGH time in order to place I/O buffers in High-Z.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
21. The 3ns minimum is a parameter guaranteed by design.
22. Column address changed once each cycle.
23. 8MB module values will be half of those shown.
24. For the FPM option, ^{t}OFF is determined by the first RAS# or CAS# signal to transition HIGH. In comparison, ^{t}OFF on an EDO option is determined by the latter of the RAS# and CAS# signals to transition HIGH.
25. Applies to both EDO and FPM operating modes.
26. All other inputs at 0.2V or V_{DD} - 0.2V.
27. "S" version only.
28. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}WCS < ^{t}WCS (MIN) and ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW result in a LATE WRITE (OE#-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
29. LATE WRITE and READ-MODIFY-WRITE cycles

NOTES (continued)

must have both ^{t}OD and ^{t}OEH met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS# remains LOW and OE# is taken back LOW after ^{t}OEH is met. If CAS# goes HIGH prior to OE# going back LOW, the DQs will remain open.

30. The SPD EEPROM WRITE cycle time (^{t}WR) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.
31. V_{IH} overshoot: V_{IH} (MAX) = V_{DD} + 2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate.

READ CYCLE [25]



FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

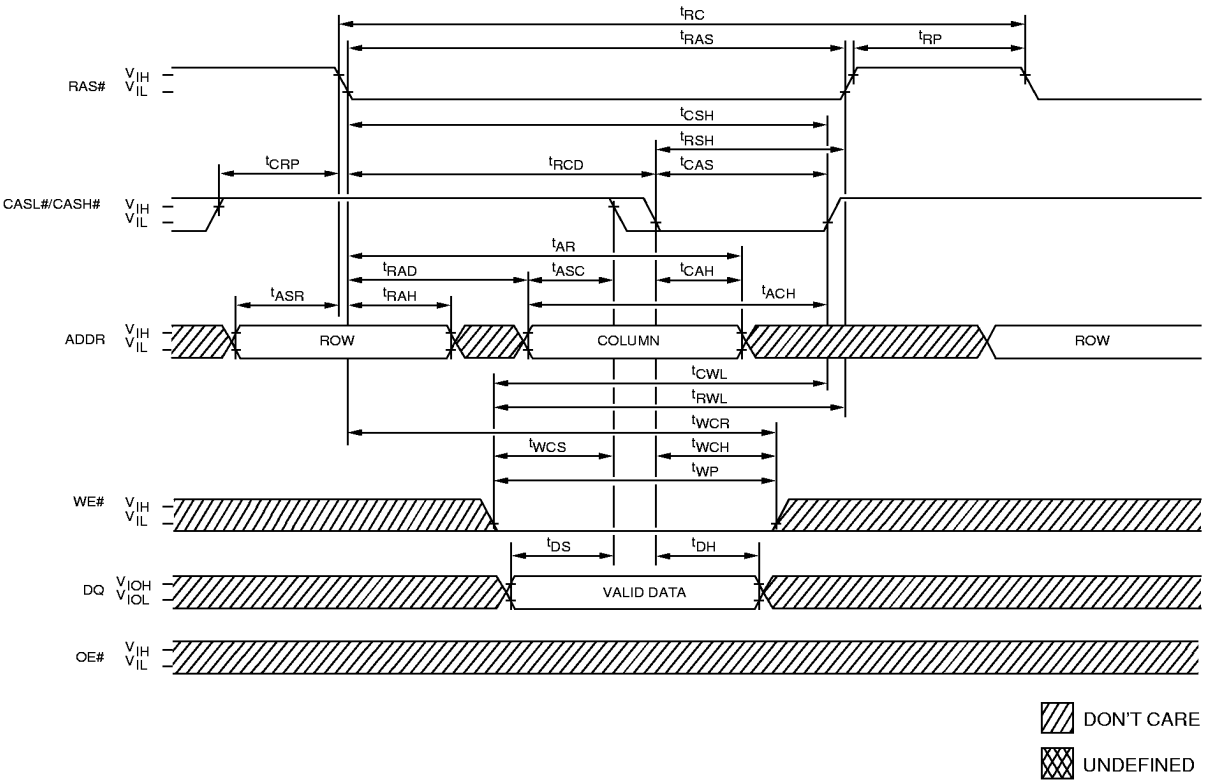
	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tAA		25		30	ns
tACH (EDO)	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC (EDO)		13/15**		15	ns
tCAH	8		10		ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCAS (FPM)	–	–	15	10,000	ns
tCLZ (EDO)	0		0		ns
tCLZ (FPM)	–		3		ns
tCRP	5		5		ns
tCSH (EDO)	38		45		ns
tCSH (FPM)	–		60		ns
tOD (EDO)	0	12	0	15	ns
tOD (FPM)	–	–	3	15	ns
tOE		12		15	ns

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tOFF (EDO)	0	12	0	15	ns
tOFF (FPM)	–	–	3	15	ns
tRAC		50		60	ns
tRAD (EDO)	9		12		ns
tRAD (FPM)	–		15		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRC (EDO)	84		104		ns
tRC (FPM)	–		110		ns
tRCD (EDO)	11		14		ns
tRCD (FPM)	–		20		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

*EDO version only
**8MB DIMM

NOTE: 1. For EDO, tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs last. For FPM, tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs first.

EARLY WRITE CYCLE [25]



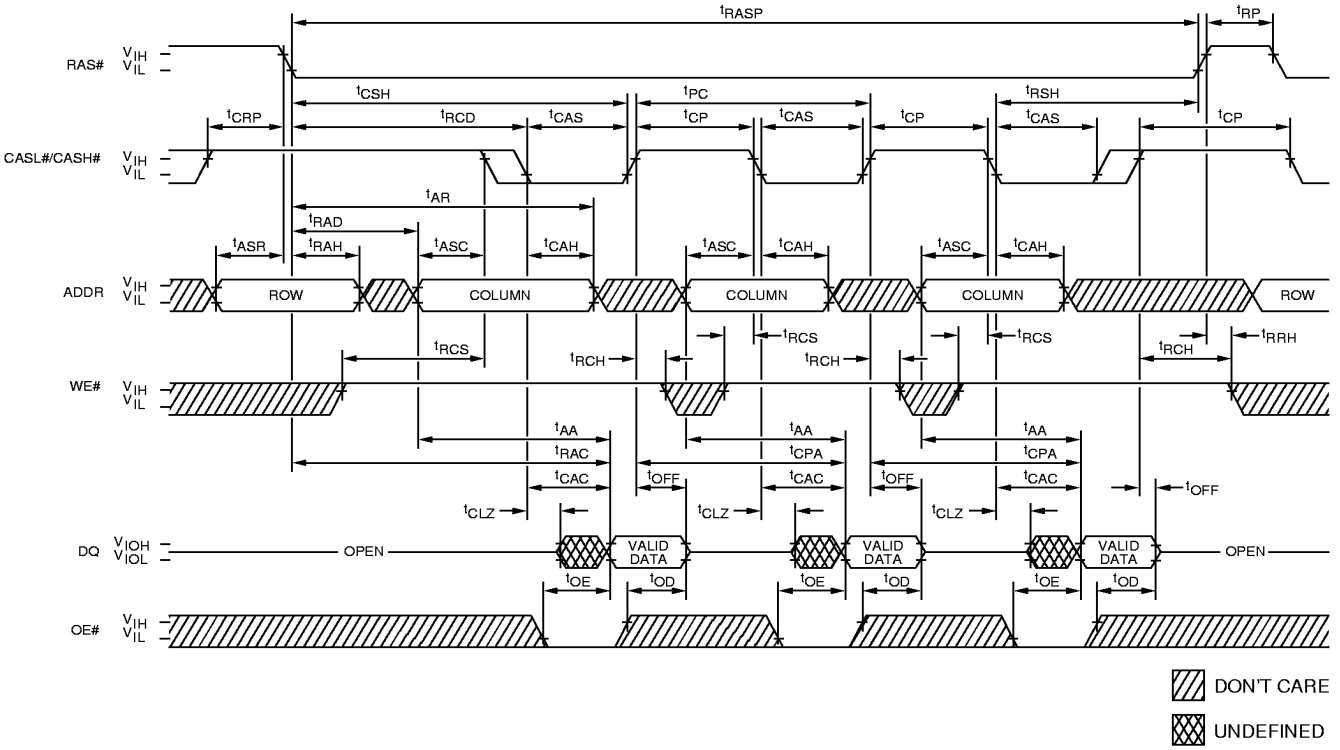
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tACH (EDO)	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS (FPM)	–	–	15	10,000	ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCRP	5		5		ns
tCSH (FPM)	–		60		ns
tCSH (EDO)	38		45		ns
tCWL (FPM)	–		15		ns
tCWL (EDO)	8		10		ns
tDH	8		10		ns
tDS	0		0		ns
tRAD (FPM)	–		15		ns

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tRAD (EDO)	9		12		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRC (FPM)	–		110		ns
tRC (EDO)	84		104		ns
tRCD (FPM)	–		20		ns
tRCD (EDO)	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR	38		45		ns
tWCS	0		0		ns
tWP (FPM)	–		10		ns
tWP (EDO)	5		5		ns

*EDO version only

FAST-PAGE-MODE READ CYCLE

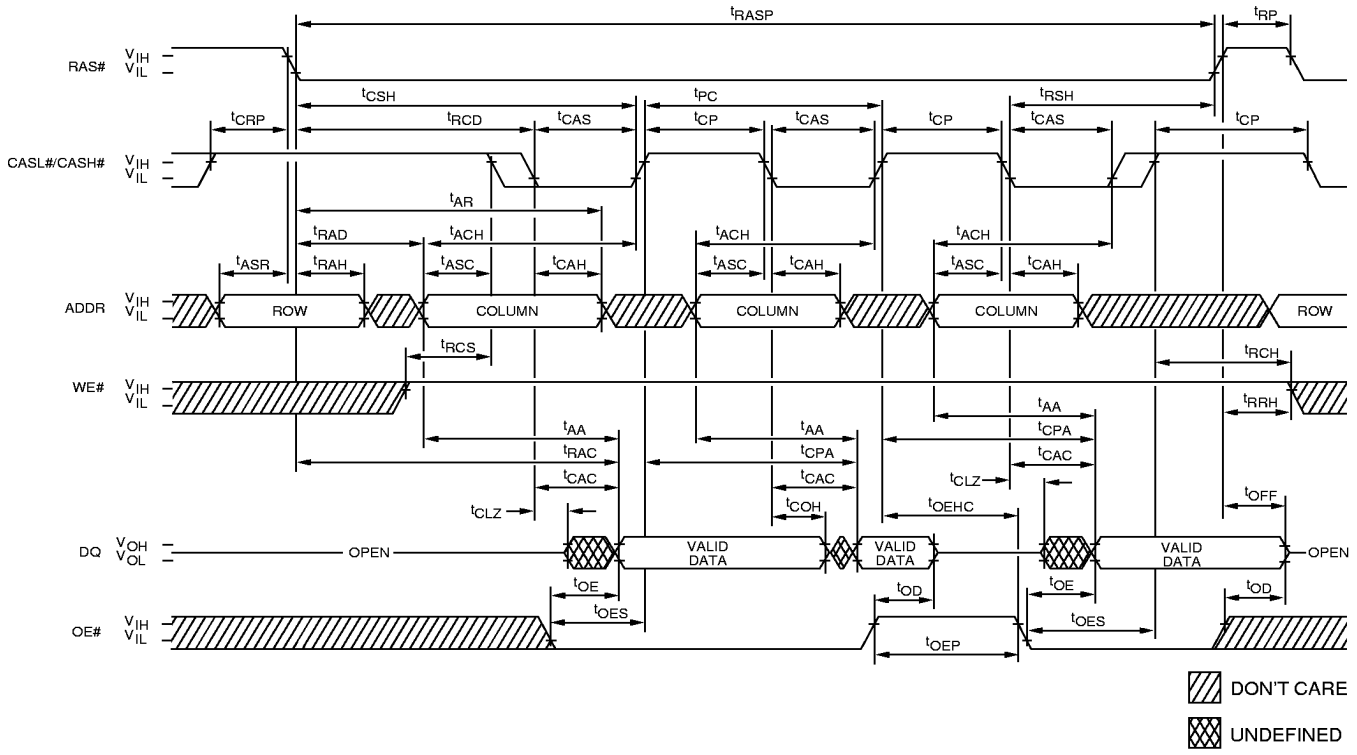


FAST PAGE MODE TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	3		ns
tCP	10		ns
tCPA		35	ns
tCRP	5		ns
tCSH	60		ns
tOD	3	15	ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOE		15	ns
tOFF	3	15	ns
tPC	35		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	125,000	ns
tRCD	20		ns
tRCH	0		ns
tRCS	0		ns
tRP	40		ns
tRRH	0		ns
tRSH	15		ns

EDO-PAGE-MODE READ CYCLE



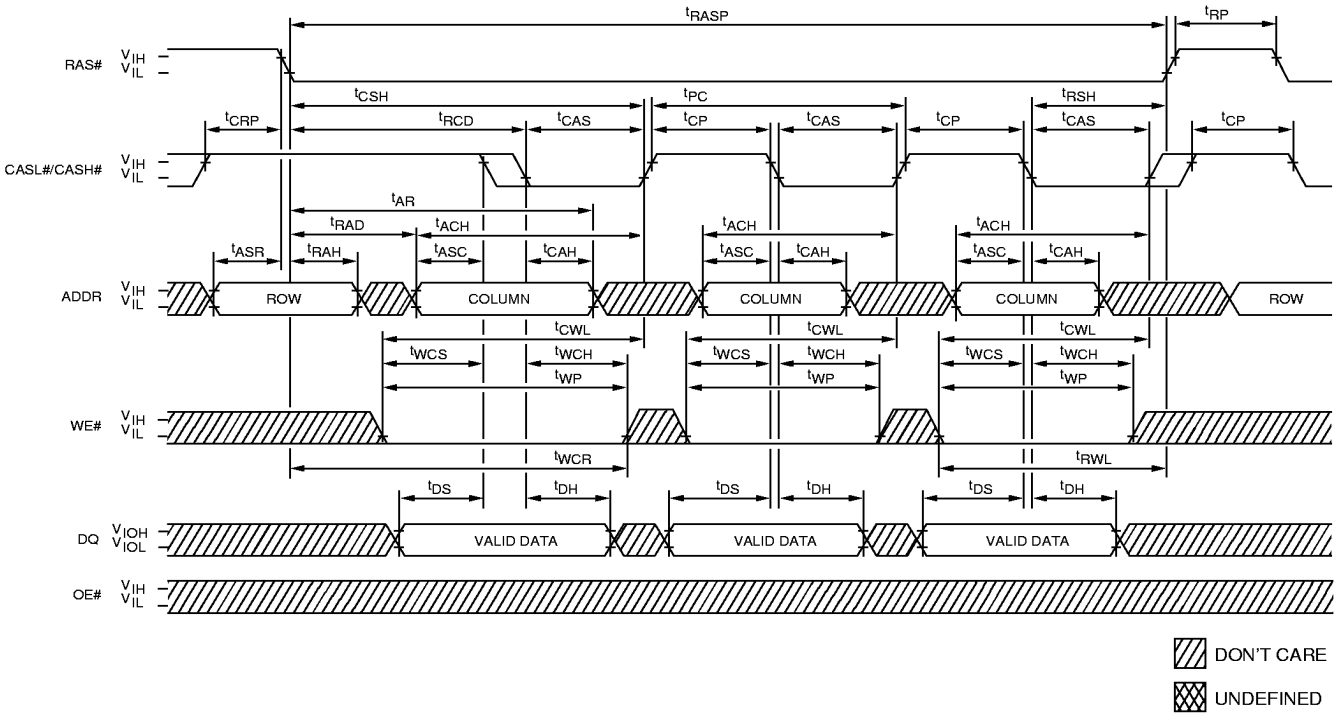
EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13/15*		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tOD	0	12	0	15	ns
tOE		12		15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOEHC	5		10		ns
tOEP	5		5		ns
tOES	4		5		ns
tOFF	0	12	0	15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

*8MB DIMM

FAST/EDO-PAGE-MODE EARLY WRITE CYCLE [25]



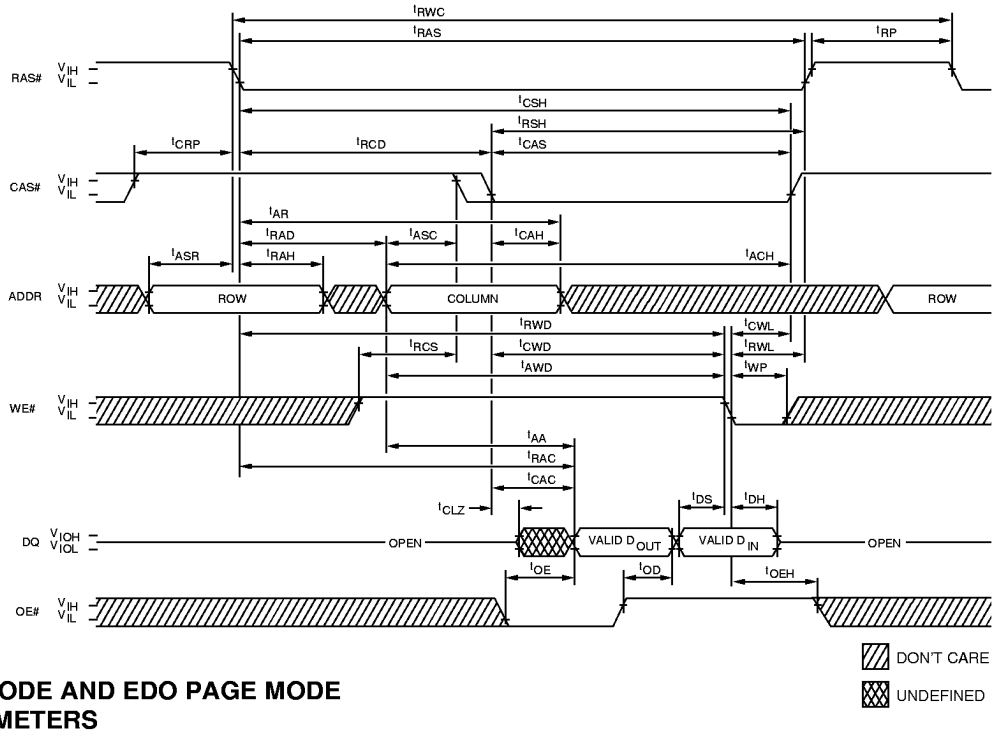
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tACH (EDO)	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCAS (FPM)	–	–	15	10,000	ns
tCP	8		10		ns
tCRP	5		5		ns
tCSH (EDO)	38		45		ns
tCSH (FPM)	–		60		ns
tCWL (EDO)	8		10		ns
tCWL (FPM)	–		15		ns
tDH	8		10		ns
tDS	0		0		ns
tPC (EDO)	20		25		ns

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tPC (FPM)	–		35		ns
tRAD (EDO)	9		12		ns
tRAD (FPM)	–		15		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD (EDO)	11		14		ns
tRCD (FPM)	–		20		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR	38		45		ns
tWCS	0		0		ns
tWP (EDO)	5		5		ns
tWP (FPM)	–		10		ns

*EDO version only

READ-WRITE CYCLE [25]
(LATE WRITE and READ-MODIFY-WRITE cycles)



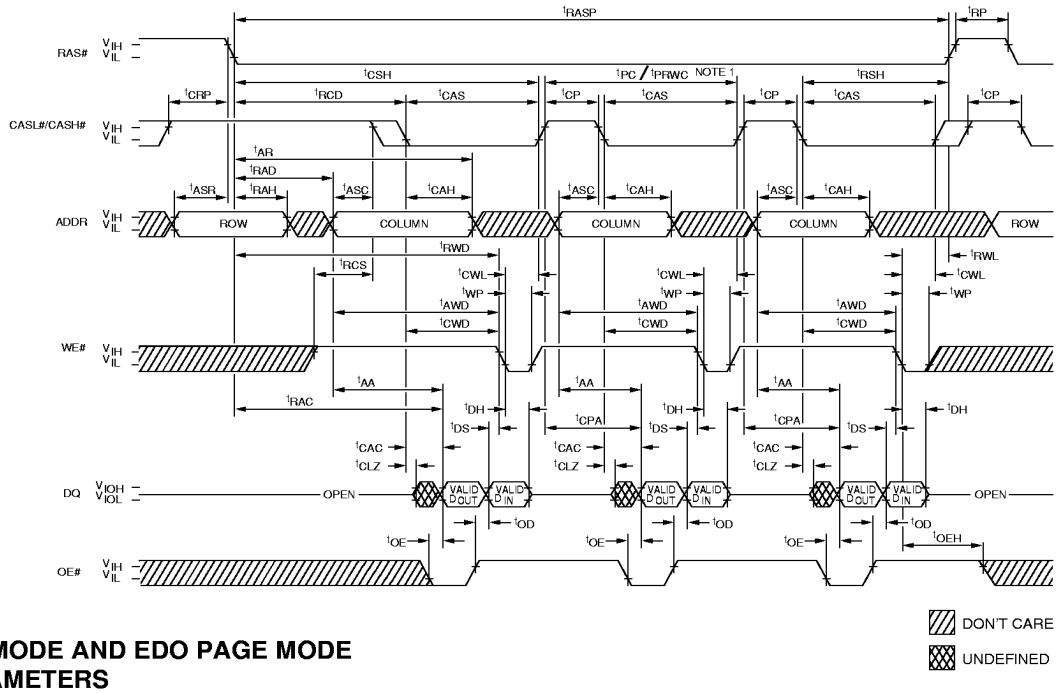
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5* MIN	-5* MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH (EDO)	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	42		49		ns
tCAC		13/15**		15	ns
tCAH	8		10		ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCAS (FPM)	–	–	15	10,000	ns
tCLZ (EDO)	0		0		ns
tCLZ (FPM)	–		3		ns
tCRP	5		5		ns
tCSH (EDO)	38		45		ns
tCSH (FPM)	–		60		ns
tCWD (EDO)	28		35		ns
tCWD (FPM)	–		40		ns
tCWL (EDO)	8		10		ns
tCWL (FPM)	–		15		ns
tDH	8		10		ns
tDS	0		0		ns
tOD (EDO)	0	12	0	15	ns

SYMBOL	-5* MIN	-5* MAX	-6 MIN	-6 MAX	UNITS
tOD (FPM)	–	–	3	15	ns
tOE		12		15	ns
tOEH (EDO)	8		10/12***		ns
tOEH (FPM)	–		15		ns
tRAC		50		60	ns
tRAD (EDO)	9		12		ns
tRAD (FPM)	–		15		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRCD (EDO)	11		14		ns
tRCD (FPM)	–		20		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWC (EDO)	116		140		ns
tRWC (FPM)	–		155		ns
tRWD (EDO)	67		79		ns
tRWD (FPM)	–		85		ns
tRWL	13		15		ns
tWP (EDO)	5		5		ns
tWP (FPM)	–		10		ns

* EDO version only
** 8MB DIMM
*** 16MB DIMM

FAST/EDO-PAGE-MODE READ-WRITE CYCLE [25]
(LATE WRITE and READ-MODIFY-WRITE cycles)



FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

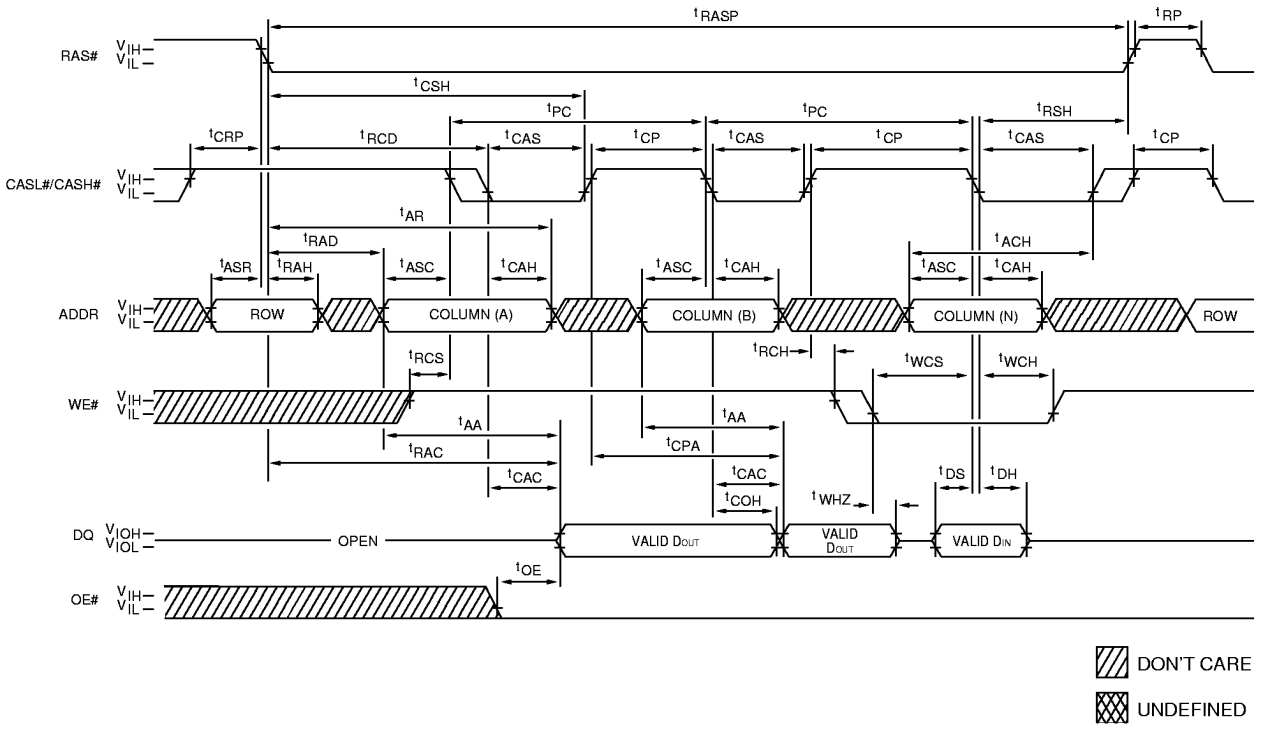
SYMBOL	-5* MIN	-5* MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	42		49		ns
tCAC		13/15**		15	ns
tCAH	8		10		ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCAS (FPM)	–	–	15	10,000	ns
tCLZ (EDO)	0		0		ns
tCLZ (FPM)	–		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH (EDO)	38		45		ns
tCSH (FPM)	–		60		ns
tCWD (EDO)	28		35		ns
tCWD (FPM)	–		40		ns
tCWL (EDO)	8		10		ns
tCWL (FPM)	–		15		ns
tDH	8		10		ns
tDS	0		0		ns
tOD (EDO)	0	12	0	15	ns

SYMBOL	-5* MIN	-5* MAX	-6 MIN	-6 MAX	UNITS
tOD (FPM)	–	–	3	15	ns
tOE		12		15	ns
tOEH (EDO)	8		10/12***		ns
tOEH (FPM)	–		15		ns
tPC (EDO)	20		25		ns
tPC (FPM)	–		35		ns
tPRWC (EDO)	47		56		ns
tPRWC (FPM)	–		85		ns
tRAC		50		60	ns
tRAD (EDO)	9		12		ns
tRAD (FPM)	–		15		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD (EDO)	11		14		ns
tRCD (FPM)	–		20		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWD (EDO)	67		79		ns
tRWD (FPM)	–		85		ns
tRWL	13		15		ns
tWP (EDO)	5		5		ns
tWP (FPM)	–		10		ns

NOTE: 1. tPC is for LATE WRITE cycles only.

* EDO version only
** 8MB DIMM
*** 16MB DIMM

EDO-PAGE-MODE READ EARLY WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



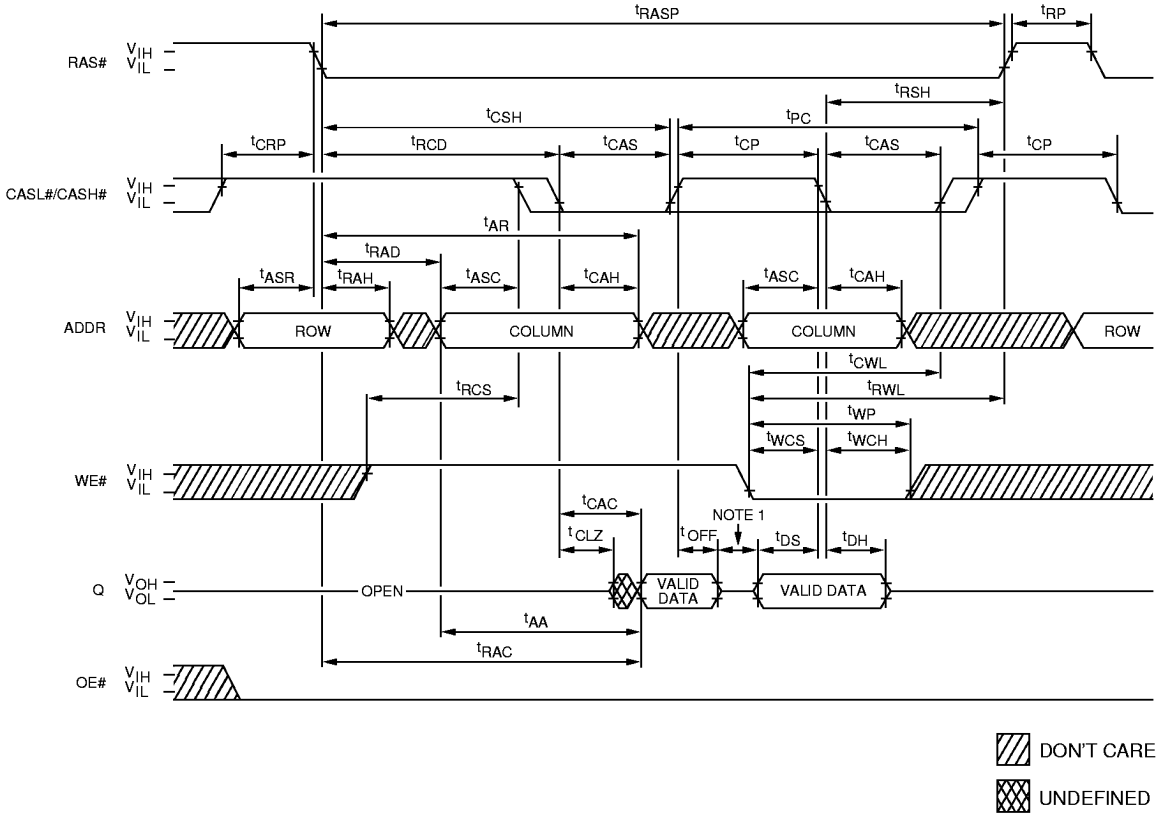
EDO PAGE MODE
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13/15*		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE		12		15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tWCH	8		10		ns
tWCS	0		0		ns
tWHZ	0	12	0	15	ns

*8MB DIMM

FAST-PAGE-MODE READ EARLY WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



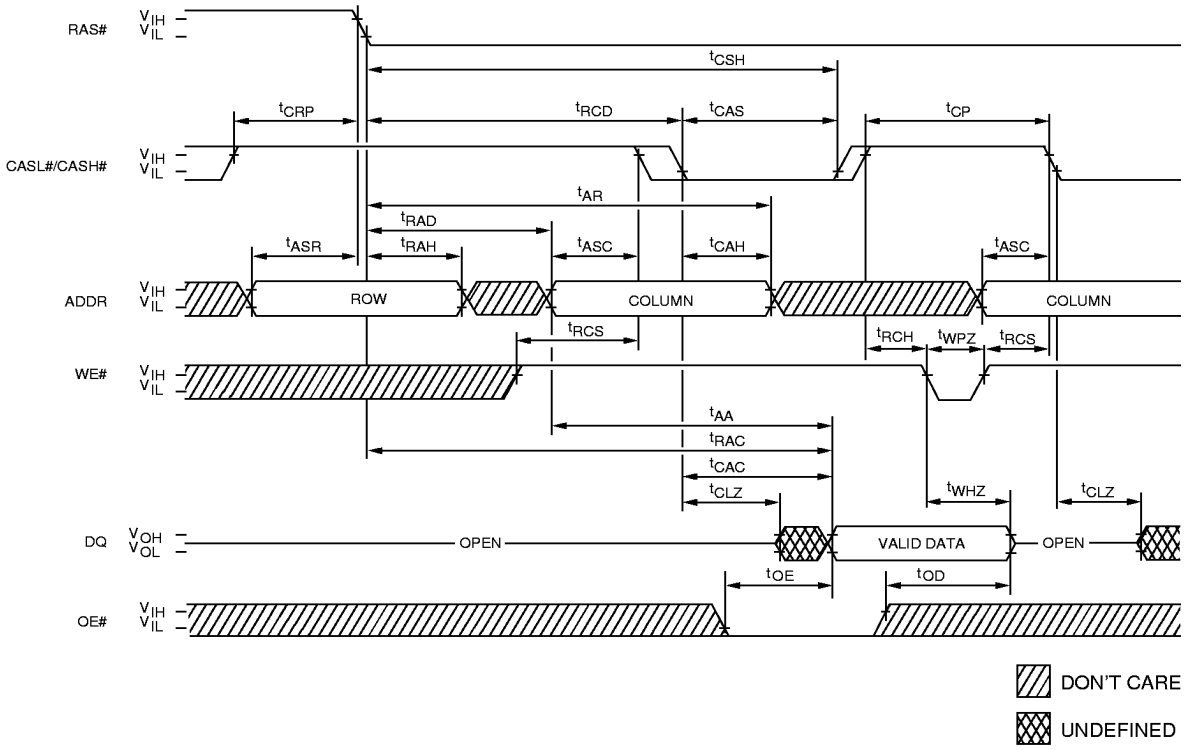
FAST PAGE MODE TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	3		ns
tCP	10		ns
tCRP	5		ns
tCSH	60		ns
tCWL	15		ns
tDH	10		ns
tDS	0		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOFF	3	15	ns
tPC	35		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	125,000	ns
tRCD	20		ns
tRCS	0		ns
tRP	40		ns
tRSH	15		ns
tRWL	15		ns
tWCH	10		ns
tWCS	0		ns
tWP	10		ns

NOTE: 1. Do not drive data prior to tristate.

EDO READ CYCLE
(with WE#-controlled disable)



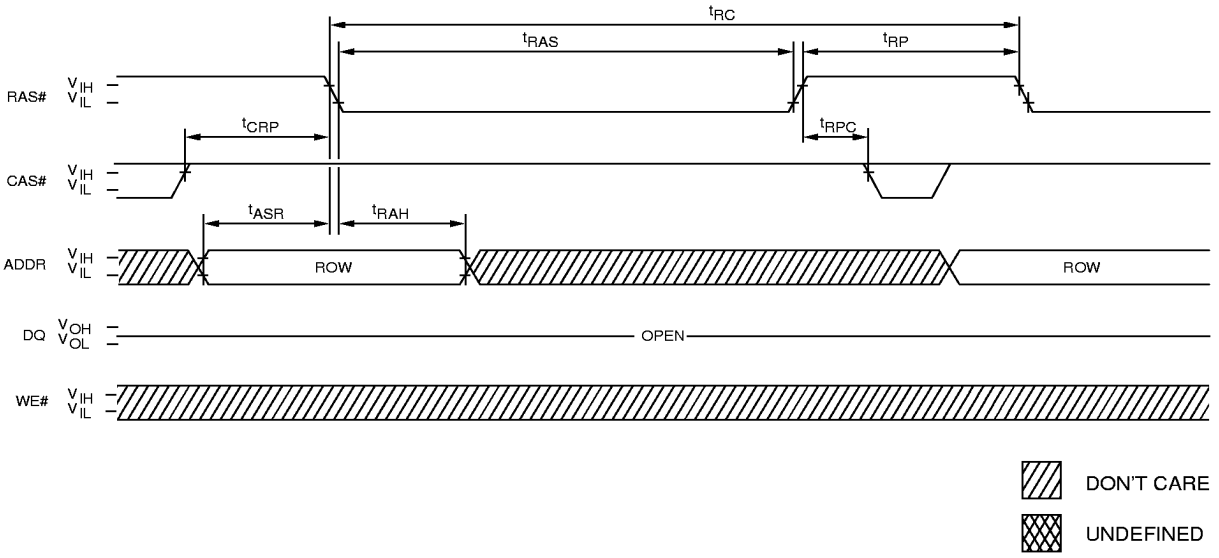
EDO PAGE MODE
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13/15*		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSH	38		45		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOD	0	12	0	15	ns
tOE		12		15	ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tWHZ	0	12	0	15	ns
tWPZ	10		10		ns

*8MB DIMM

RAS#-ONLY REFRESH CYCLE [25]



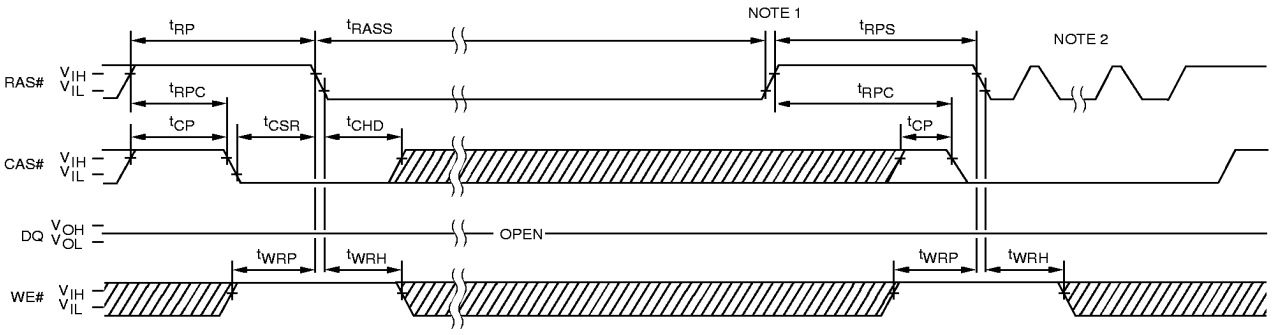
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5* MIN	-5* MAX	-6 MIN	-6 MAX	UNITS
tASR	0		0		ns
tCRP	5		5		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRC (FPM)	–		110		ns

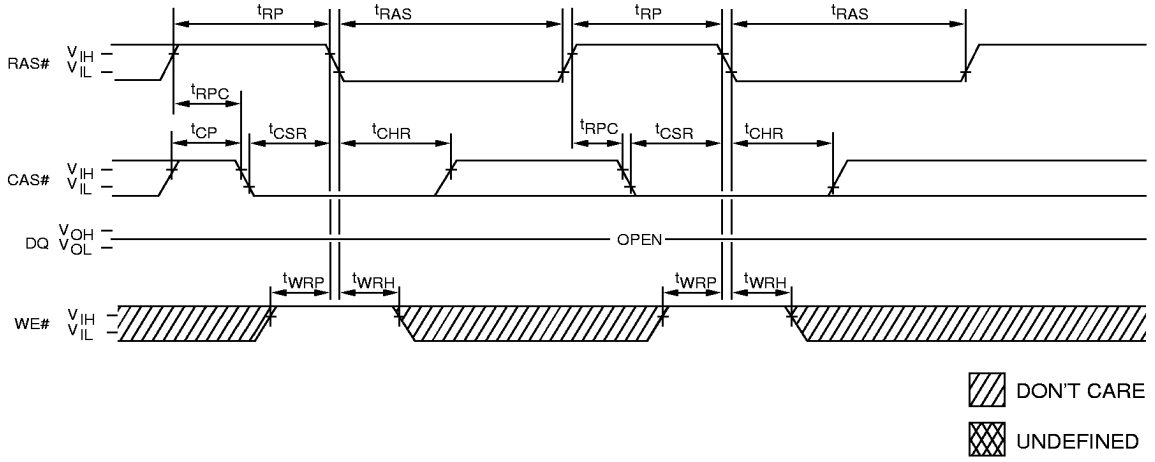
SYMBOL	-5* MIN	-5* MAX	-6 MIN	-6 MAX	UNITS
tRC (EDO)	84		104		ns
tRP	30		40		ns
tRPC (FPM)	–		0		ns
tRPC (EDO)	5		5		ns

*EDO version only

SELF REFRESH CYCLE [25, 27]
(Addresses and OE# = DON'T CARE)



CBR REFRESH CYCLE [25]
(Addresses = DON'T CARE)



FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

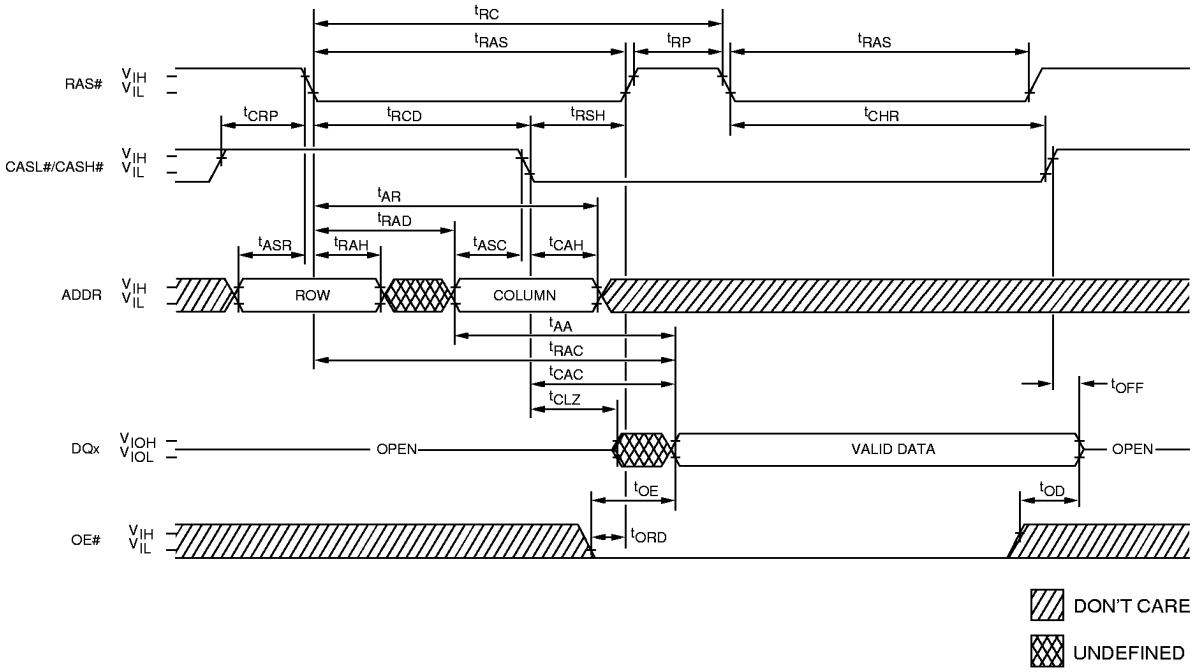
	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tCHD	15		15		ns
tCHR	8		10		ns
tCP	8		10		ns
tCSR	5		5		ns
tRAS	50	10,000	60	10,000	ns
tRASS	100		100		µs
tRP	30		40		ns

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tRPC (FPM)	–		0		ns
tRPC (EDO)	5		5		ns
tRPS (EDO)	90		105		ns
tRPS (FPM)	–		110		ns
tWRH	8		10		ns
tWRP	8		10		ns

*EDO version only

NOTE: 1. Once tRASS (MIN) is met and RAS# remains LOW, the DRAM will enter self refresh mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

HIDDEN REFRESH CYCLE [20, 25]
(WE# = HIGH)



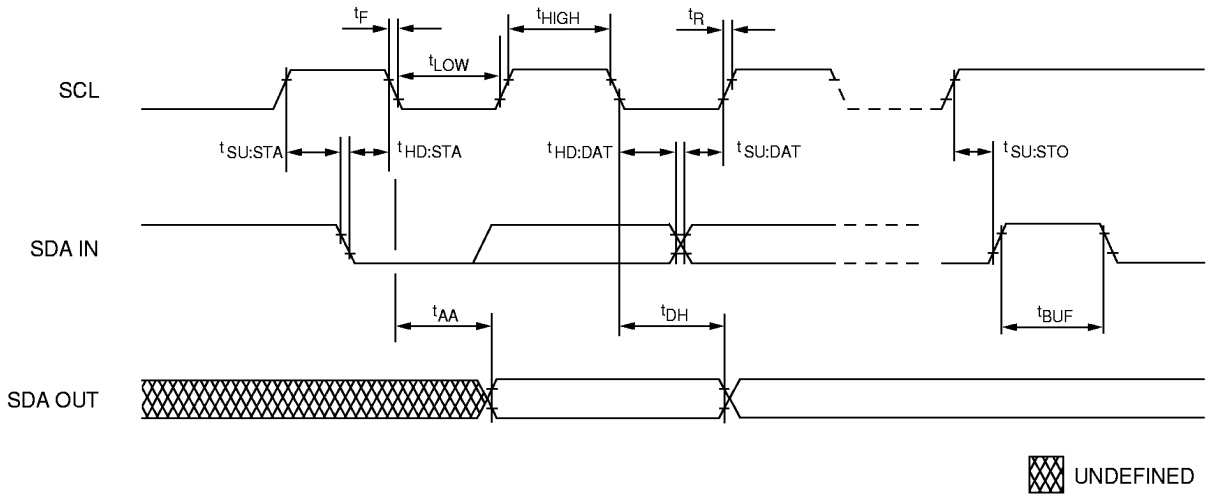
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13/15**		15	ns
tCAH	8		10		ns
tCHR	8		10		ns
tCLZ (FPM)	–		3		ns
tCLZ (EDO)	0		0		ns
tCRP	5		5		ns
tOD (FPM)	–	–	3	15	ns
tOD (EDO)	0	12	0	15	ns
tOE		12		15	ns
tOFF (FPM)	–	–	3	15	ns

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tOFF (EDO)	0	12	0	15	ns
tORD	0		0		ns
tRAC		50		60	ns
tRAD (FPM)	–		15		ns
tRAD (EDO)	9		12		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRC (FPM)	–		110		ns
tRC (EDO)	84		104		ns
tRCD (FPM)	–		20		ns
tRCD (EDO)	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns

* EDO version only
** 8MB DIMM

SPD EEPROM



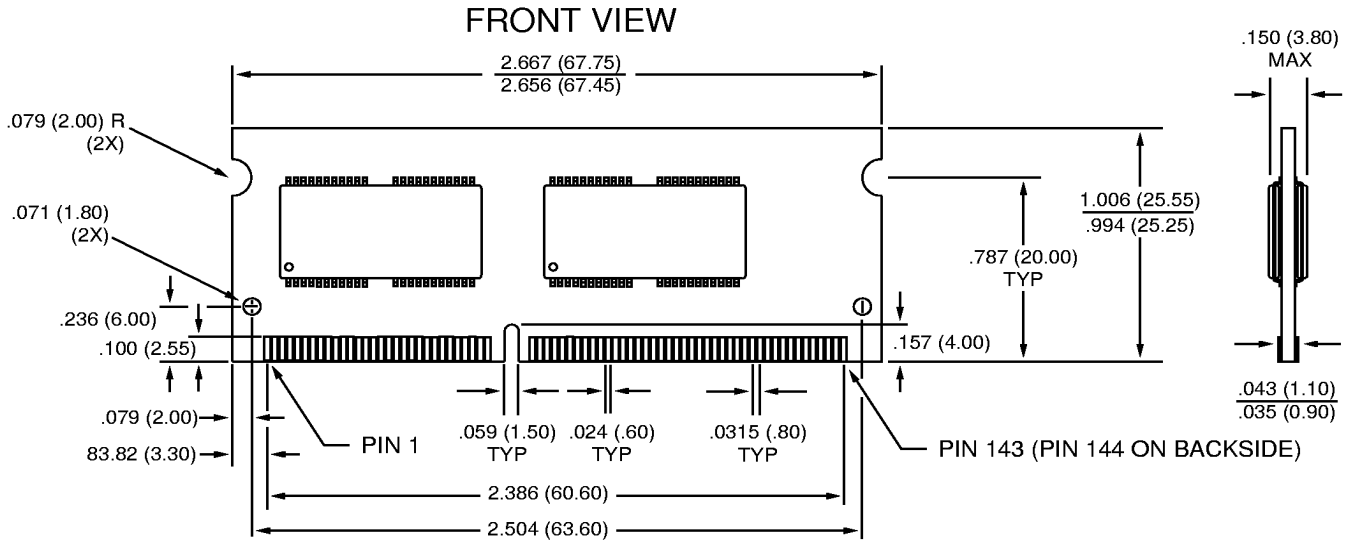
SERIAL PRESENCE-DETECT EEPROM TIMING PARAMETERS

SYMBOL	MIN	MAX	UNITS
tAA	0.3	3.5	µs
tBUF	4.7		µs
tDH	300		ns
tF		300	ns
tHD:DAT	0		µs
tHD:STA	4		µs

SYMBOL	MIN	MAX	UNITS
tHIGH	4		µs
tLOW	4.7		µs
tR		1	µs
tSU:DAT	250		ns
tSU:STA	4.7		µs
tSU:STO	4.7		µs

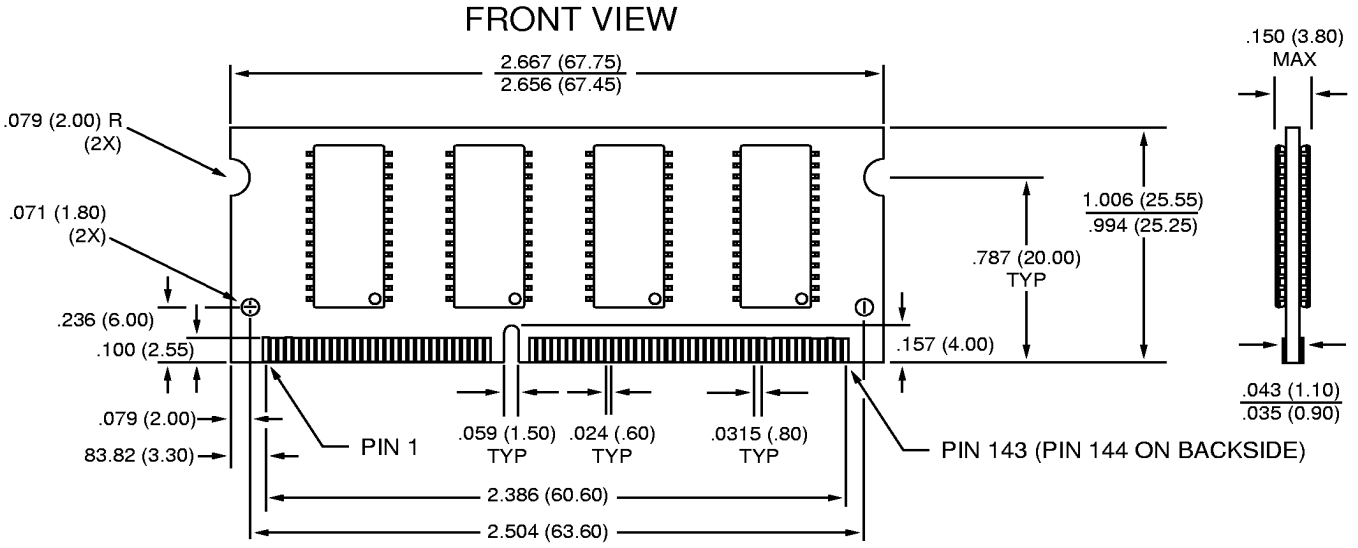
144-PIN SODIMM

DG-5



144-PIN SODIMM

DG-6



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.