Features

- Supports AT&T TR62411 Stratum 4 and Stratum 4 Enhanced for DS1 interfaces and for ETSI ETS 300 011, TBR 4, TBR 12, and TBR 13 for E1 interfaces
- Supports ITU-T G.812 Type IV clocks for 1.544kbit/s interfaces and 2.048kbit/s interface
- Provides C1.5, $\overline{C3}$, C2, $\overline{C4}$, C8, C6, $\overline{C16}$ and C19 output clock signals
- Provides five kinds of 8kHz ST-BUS framing signals
- Input reference frequency 1.544MHz, 2.048MHz or 8kHz selectable
- Normal or Free-Run operating modes available
- Power supply: 5V (4408) and 3.3V(4408L)

Applications

- Synchronization and timing control for multitrunk T1 and E1 systems, STS-3/OC3 systems
- ST-BUS clock and frame pulse sources
- Primary Trunk Rate Converters

Introduction

PT7A4408/4408L employs a digital phase-locked loop (DPLL) to provide timing and synchronizing signals for multitrunk T1 and E1 primary rate transmission links, and for STS-3/OC3 links. The ST-BUS clock and framing signals are phase-locked to input reference signals of either 2.048 MHz, 1.544MHz or 8 kHz.

The PT7A4408/4408L meets the requirements for AT&T TR62411 Stratum 4 and Stratum 4 Enhanced, and ETSI ETS 300 011 in jitter tolerance, jitter transfer, intrinsic jitter, frequency accuracy, capture range, phase slope, etc.

The PT7A4408/4408L operates in Normal or Free-run Mode.

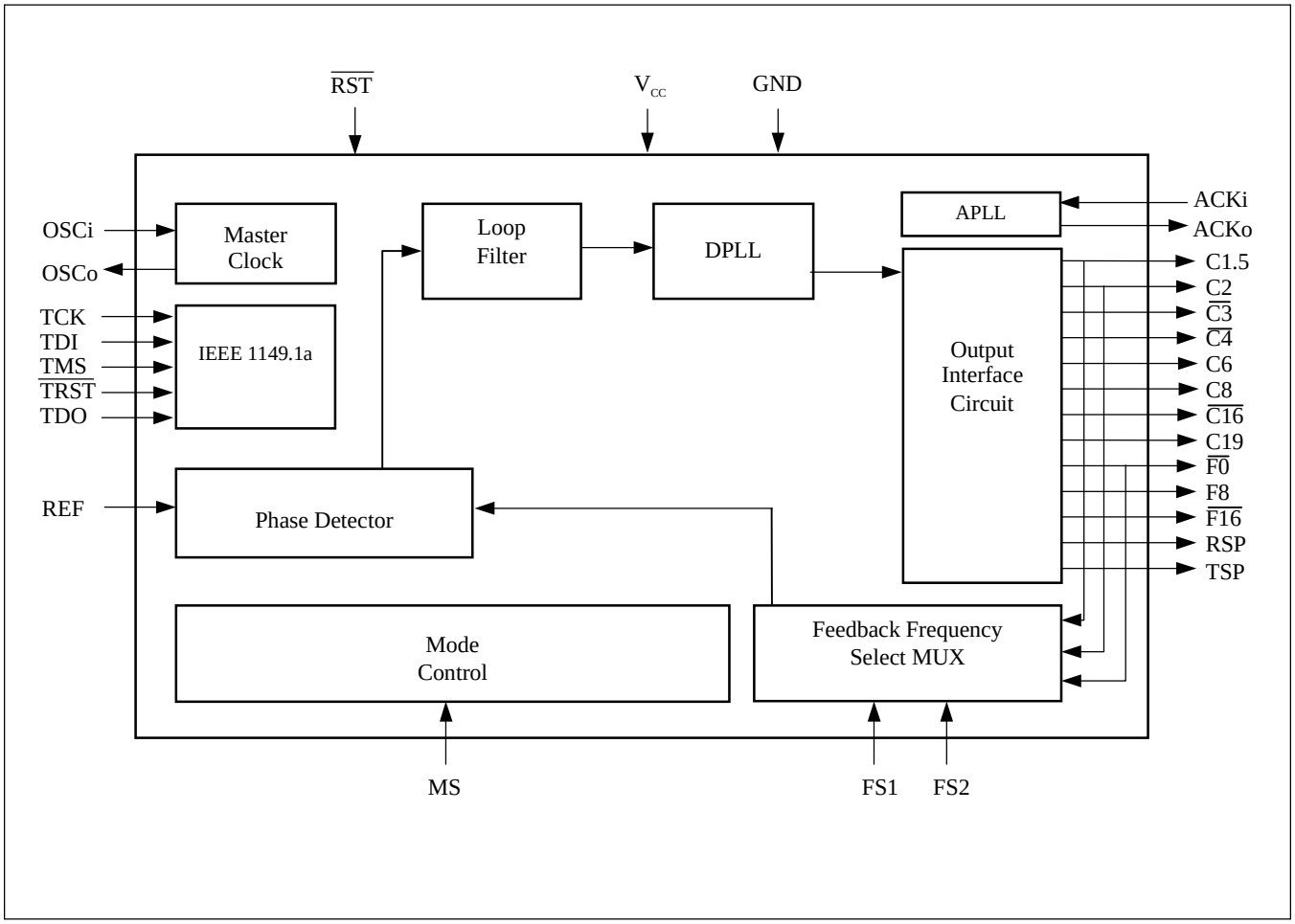
Ordering Information

Part Number	Package
PT7A4408J	44-Pin PLCC
PT7A4408LJ	44-Pin PLCC

Contents

Block Diagram

Figure 1. Block Diagram



Pin Information

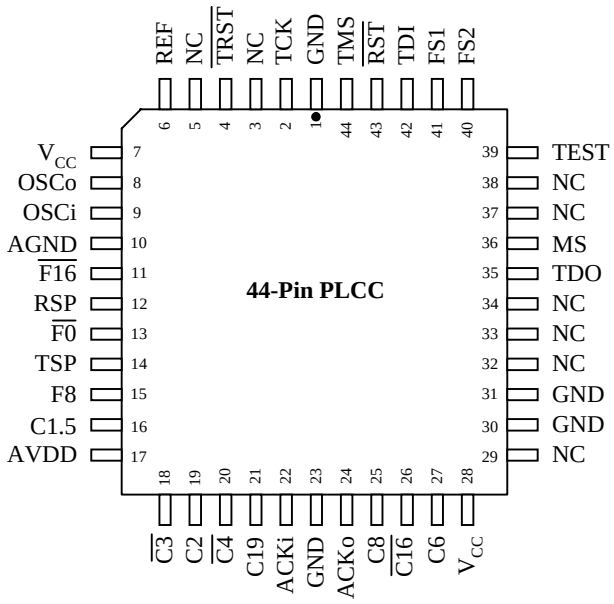
Pin Assignment

Table 1. Pin Assignment

Group	Symbol	Function
Chip Clock	OSCi, OSCo, ACKi, ACKo	Clock
Power & Ground	V_{CC}, AVDD, GND, AGND	Power
Clock and Framing Outputs	C1.5, $\overline{C3}$, C2, $\overline{C4}$, C6, C8, $\overline{C16}$, C19, $\overline{F0}$, F8, $\overline{F16}$, RSP, TSP	Clock and Framing Signals
Control Signals	MS, FS1, FS2, $\overline{RST}$	Control
Reference Inputs	REF	Reference Clock
IEEE 1149.1a	TCK, TDI, TMS, $\overline{TRST}$, TDO	IEEE 1149.1a Interface

Pin Configuration

Figure 2. Pin Configuration



Top View

Pin Description

Table 2. Pin Description

Pin	Name	Type	Description
1, 23, 30, 31	GND	Ground	**Digital Ground**
2	TCK	I	**Test Clock (TTL Input):** Provides the clock to the JTAG test logic. This pin is internally pulled up to V_{CC}.
3, 5, 29, 32-34, 37, 38	NC	-	**No connection**
4	$\overline{TRST}$	I	**Test Reset (TTL Input):** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin is internally pulled down to GND.
6	REF	I	**Reference (TTL):** The reference signal, internally pulled down to GND.
7, 28	V_{CC}	Power	**Power supply** 5V for PT7A4408J. 3.3V for PT7A4408LJ
8	OSCo	O	**Oscillator master clock output (CMOS):** Output of 20MHz master clock
9	OSCi	I	**Oscillator master clock input (CMOS):** Input of 20MHz master clock (can be connected directly to a clock source)
10	AGND	Ground	**Analog Ground**
11	$\overline{F16}$	O	**Frame pulse ST-BUS 16.384Mb/s (CMOS**): 8kHz frame signal with 61ns low level pulse that marks the beginning of a ST-BUS frame, typically used for ST-BUS opetation at 8.192Mb/s. See figure 10.
12	RSP	O	**Receive Sync Pulse (CMOS Output).** This is an 8kHz 488ns active high framing pulse, which marks the end of an ST-BUS frame. See Figure 11.
13	$\overline{F0}$	O	**Frame pulse ST-BUS 2.048 Mb/s (CMOS**): 8kHz frame signal with 244ns low level pulse that marks the beginning of a ST-BUS frame e, typically used for ST-BUS opetation at 2.048Mb/s. See figure 10.
14	TSP	O	**Transmit Sync Pulse (CMOS Output).** This is an 8kHz 488ns active high framing pulse, which marks the beginning of an ST-BUS frame. See Figure 11.
15	F8	O	**Frame pulse ST-BUS 8.192 Mb/s (CMOS**): 8kHz frame signal with 122ns high level pulse that marks the beginning of a ST-BUS frame
16	C1.5	O	**1.544 MHz clock (CMOS):** This output is used in T1 applications.
17	AVDD	Power	**Analog Power Supply:** 5V for PT7A4408J and 3.3V for PT7A4408LJ
18	$\overline{C3}$	O	**3.088 MHz clock (CMOS):** This output is used in T1 applications.
19	C2	O	**2.048 MHz clock (CMOS):** This output is used for ST-BUS operation at 2.048Mb/s.
20	$\overline{C4}$	O	**4.096 MHz clock (CMOS):** This output is used for ST-BUS operation at 2.048Mb/s and 4.096Mb/s.
21	C19	O	**Clock 19.44MHz (CMOS Output).** This output is used in OC3/STS-3 applications.
22	ACKi	I	**Analog PLL Clock Input (CMOS Input).** This input clock is a reference for an internal analog PLL. This pin is internally pulled down to GND.
24	ACKo	O	**Analog PLL Clock Output (CMOS Output)**. This output clock is generated by the internal analog PLL.

Table 2. Pin Description (continued)

Pin	Name	Type	Description
25	C8	O	**8.192 MHz clock (CMOS):** This output is used for ST-BUS operation at 8.192Mb/s.
26	$\overline{C16}$	O	**16.384 MHz clock (CMOS):** This output is used for ST-BUS operation with a 16.384MHz clock.
27	C6	O	**Clock 6.312 MHz (CMOS Output)**. This output is used for DS2 applications.
35	TDO	O	**Test Serial Data Out (TTL Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enable.
36	MS	I	**Mode/Control Select (TTL):** determines the operating states, Normal or Free-Run.
39	TEST	I	**Test (TTL Input).** This input is normally tied low. When pulled high, it enables internal test modes. This pin is internally pulled down to GND.
40	FS2	I	**Frequency Select 2 (TTL)**:Together with FS1, selects one of the three DPLL feedback frequencies to match the desired Input Reference Frequency (8 kHz, 1.544 MHz or 2.048 MHz).
41	FS1	I	**Frequency Select 1 (TTL):** Refer to the pin description of FS2.
42	TDI	I	**Test Serial Data In (TTL Input).** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to $V_{CC..}$
43	$\overline{RST}$	I	**Reset (Schmitt):** Resets the device when at low logic level. Reset is needed whenever the operating mode is changed, or the reference signal frequency is switched or when power-up; so as to ensure proper operation of the device. Following Reset, the output clocks and frame signals are phase-aligned with the input reference source.
44	TMS	I	**Test Mode Select (TTL Input).** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to $V_{CC..}$

Functional Description

Overall Operation

The PT7A4408/4408L is a multitrunk synchronizer that provides the clock and frame signals for T1 and E1 primary rate digital transmission links, and STS-3/OC3 links.

It basically consists of the Clock Generator, Mode Control, Digital Phase- Locked Loop (DPLL), Analog Phase- Locked Loop (APLL) and Output Interface Circuit.

The DPLL circuit provides synchronization of the output signals with any given input reference signal.

Master Clock

The PT7A4408/4408L uses either an external clock source or an external crystal and a few discrete components with its internal oscillator as the master clock.

Feedback Frequency Select MUX

The feedback frequency is selected by FS1 and FS2 (as shown in Table 3) to match the particular incoming reference frequency (1.544MHz, 2.048MHz or 8kHz). A reset ($\overline{RST}$) must be performed after every frequency select input change.

Table 3. Feedback Frequency Selection

FS2	FS1	Input Frequency
0	0	Reserved
0	1	8kHz
1	0	1.544MHz
1	1	2.048MHz

Digital Phase-Locked Loop (DPLL)

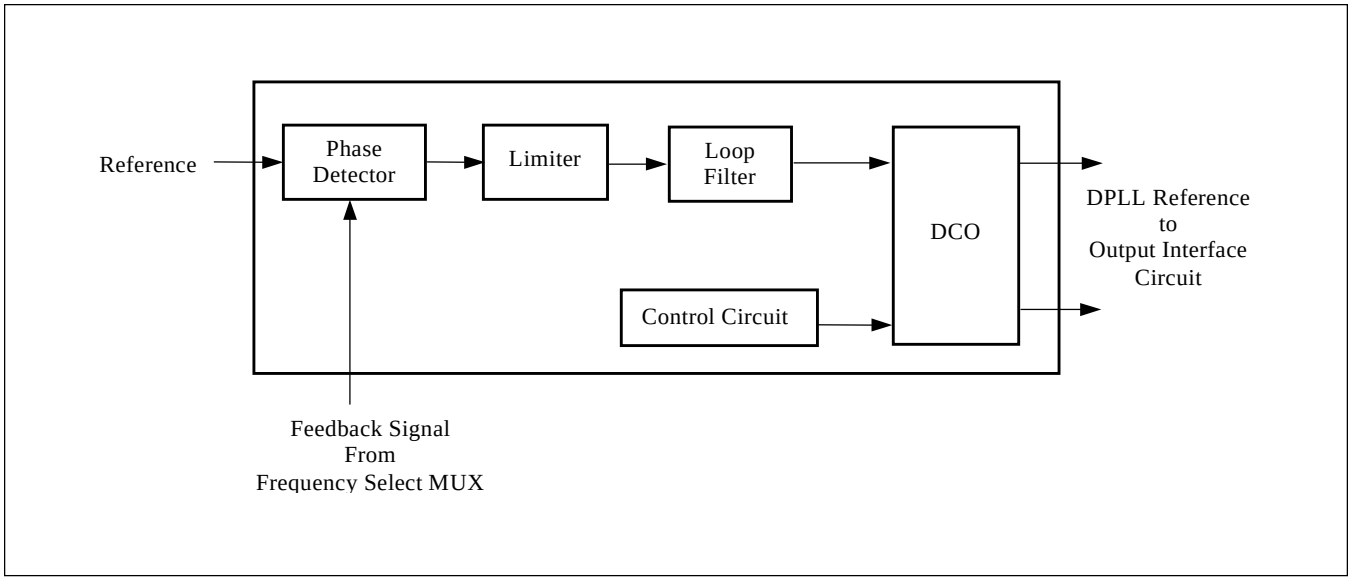
The DPLL consists of the Phase Detector, Limiter, Loop Filter, Digitally Controlled Oscillator (DCO) and Control Circuit. See Figure 3 for the block diagram of DPLL.

The Reference is sent to Phase Detector for comparison with the Feedback Signal from the Feedback Frequency Select MUX. An error signal corresponding to their instantaneous phase difference is produced and sent to the Limiter.

The Limiter amplifies this error signal to ensure the DPLL responds to all input transient conditions with a maximum output phase slope of 5ns per 125µs. This performance easily meets the maximum phase slope of 7.6ns per 125µs or 81ns per 1.326ms specified by AT&T TR62411.

The Loop Filter is a 1.9Hz low pass filter for all three reference frequency selections: 8kHz, 1.544MHz and 2.048MHz. The filter ensures that the jitter transfer requirements in ETS 300-011 and AT&T TR62411 are met.

Figure 3. Block Diagram of DPLL



The Control Circuit decides Normal or Freerun state.

The Error Signal, after limited and filtered, is sent to Digitally Controlled Oscillator. Based on the processed error value, the DCO will generate the corresponding digital output signals for the Tapped Delay Line in the Output Interface Circuit to produce 12.352MHz, 12.624MHz, 19.44MHz and 16.384MHz signals. The DCO synchronization method depends upon the PT7A4408/4408L operating state, as follows:

In Normal state, the DCO generates four output signals which are frequency and phase locked to the selected input reference signal.

In Free-Run state, the DCO is free running with an accuracy equal to that of the OSCi 20MHz source.

Output Interface Circuit

The Output Interface Circuit consists of the Tapped Delay Line and E1/T1 Dividers as shown in Figure 4.

Signals from the DCO are sent to Tapped Delay Line to generate four clock signals, 16.384MHz, 12.624MHz, 19.44MHz and 12.352MHz, which are divided in the T1 and E1 Dividers respectively to provide needed clock and frame signals.

The T1 Divider uses the 12.352MHz signal to generate two clock signals, C1.5 and $\overline{C3}$. They have a nominal 50% duty cycle.

The DS2 Divider uses 12.624MHz signal to generate clock signal C6.

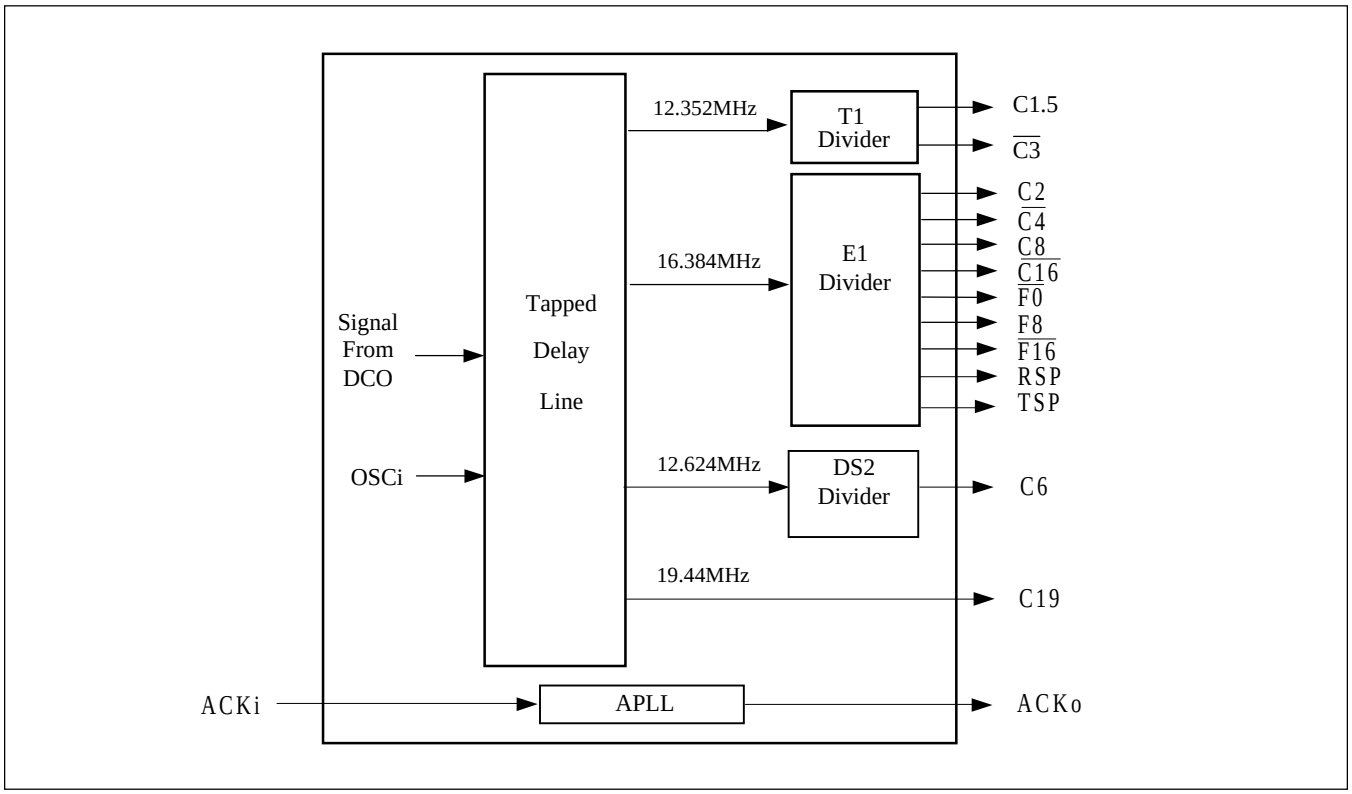
Clock signal C19 is generated from 19.44MHz by tapped Delay Line.

The E1 Divider uses the 16.384MHz signal to generate four clock signals and three frame signals, i.e., C2, $\overline{C4}$, C8, $\overline{C16}$, $\overline{F0}$, F8 and $\overline{F16}$. The frame signals are generated directly from the $\overline{C16}$ signal.

The C2, $\overline{C4}$, C8 and $\overline{C16}$ signals have nominal 50% duty cycle.

All the frame and clock outputs are locked to each other for all operating states. They have limited driving capability and should be buffered when driving high capacitance (e.g., 30pF) loads.

Figure 4. Block Diagram of Output Interface Circuit



Mode Controller

The Mode Controller determines whether the PT7A4408/4408L operates in Normal or Free-Run state.

All state changes are synchronous with the rising edge of F8. See the Modes of Operation section for complete details.

APLL

The analog PLL is intended to be used to achieve a 50% Duty cycle output clock. Connecting C19 to ACKi will generate a phase locked 19.44 MHz ACKo output with a nominal 50% duty cycle and a maximum peak-to-peak unfiltered jitter of 0.174 U.I. . The analog PLL has an intrinsic jitter of less than 0.01 U.I. In order to achieve this low jitter level separate pins are provided to power (AVDD, AGND) the APLL.

Modes of Operation

The PT7A4408/4408L operates in Normal or Free-Run controlled by pin MS.

MS = 0: Normal
MS = 1: Freerun

Normal State

In Normal State, the PT7A4408/4408L output signals are synchronized with input reference.

In this state, the input reference signal is used as reference for the DPLL phase detector.

Free-Run State

Typically the Free-Run State is used when a master clock is required or immediately following system power-up before network synchronization is achieved.

In Free-Run State, the outputs of the PT7A4408/4408L are uncorrelated with the input reference signal and the stored information of output reference. Instead, these output signals are based solely on the master clock frequency (OSCi). The accuracy of the output clock is equal to the accuracy of the master clock (OSCi).

Applications Information

Master Clock

The PT7A4408/4408L uses either an external clock source or an external crystal as the master timing source.

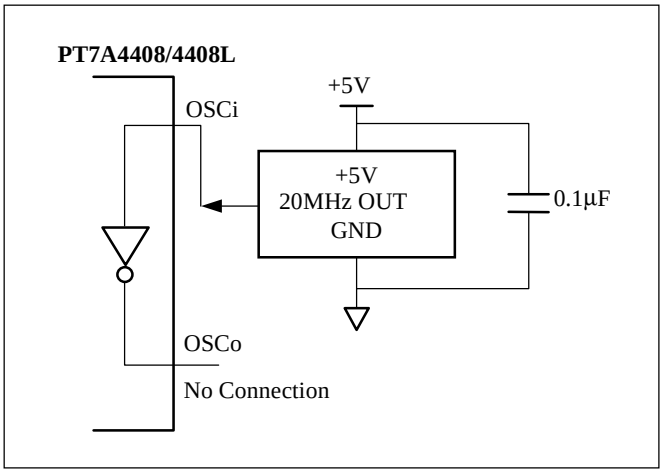
In Free-Run State, the frequency tolerance of the PT7A4408/4408L output clocks are equal to the frequency tolerance of the timing source. In an application, if an accurate Free-Run State is not required, the tolerance of the master timing source may be 100ppm. If required, the tolerance must be no greater than 32ppm.

The capture range of PT7A4408/4408L will also be considered when deciding the accuracy of the master timing source. The sum of the accuracy of the master timing source and the capture range of the PT7A4408/4408L will always equal 230ppm. For example, if the master timing source is 100ppm, the capture range will be 130ppm.

• Clock Oscillator

If using an external clock source, its output pin should be connected directly (not AC coupled) to the OSCi pin of the PT7A4408/4408L and the OSCo pin of PT7A4408/4408L can be left open as shown in Figure 5 or connected as an output pin.

Figure 5. Clock Oscillator Connection



When selecting the clock oscillator, following specifications should be considered. They are

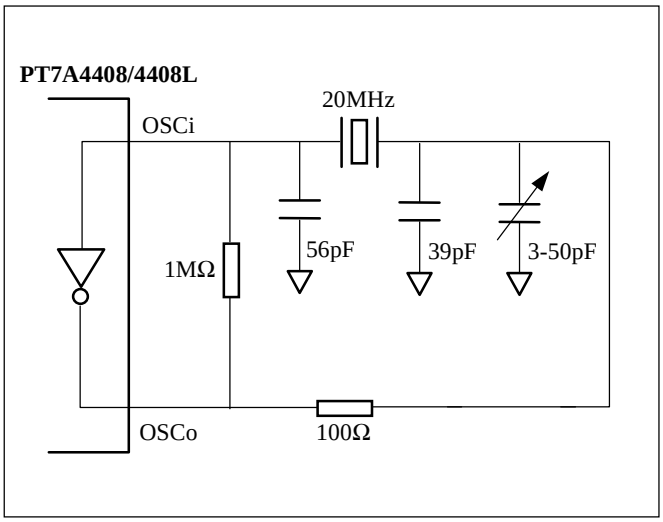
- absolute frequency
- frequency change over temperature
- output rise and fall time
- output level
- duty cycle

Refer to AC Electrical Characteristics.

• Crystal Oscillator

If a crystal oscillator is selected as the master timing source, it should be connected to the PT7A4408/4408L as shown in Figure 6.

Figure 6. Crystal Oscillator Connection



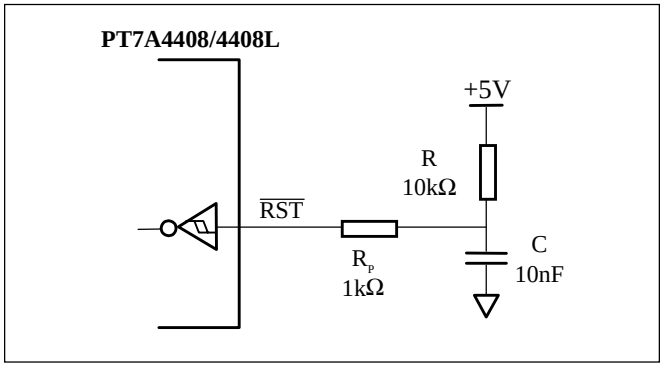
The crystal specification is as follows:

- Frequency:	20MHz
- Tolerance:	as required
- Oscillation Mode:	Fundamental
- Resonance Mode:	Parallel
- Load Capacitance:	32pF
- Maximum Series Resistance:	35Ω
- Approximate Drive Level:	1mW

Reset Circuit

A simple power up reset circuit with about a 50µs reset active (low) time is shown in Figure 7. Resistor R_p is for protection only. The reset low time is not critical but should be greater than 300ns.

Figure 7. Power-up Reset Circuit



Detailed Specifications

Definitions of Critical Performance Specifictions

Intrinsic Jitter: Intrinsic jitter is the jitter produced by the synchronizing circuit. It is measured by applying a reference signal with no jitter to the input of the device, and measuring its output jitter. Intrinsic jitter may also be measured when the device is in a non-synchronizing mode - such as free running or holdover - by measuring the output jitter of the device. Intrinsic jitter is usually measured with various band limiting filters depending on the applicable standards.

Jitter Tolerance: Jitter tolerance is a measure of the ability of a PLL to operate properly (i.e., remain in lock and/or regain lock in the presence of large jitter magnitudes at various jitter frequencies) when jitter is present on its reference. The applicable standard specifies how much jitter to apply to the reference when testing for jitter tolerance.

Jitter Transfer: Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device with respect to a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standards.

Its 3 possible input frequencies and 9 outputs give the PT7A4408/4408L 27 possible jitter transfer combinations. However, only three cases of the jitter transfer specifications are given in the AC Electrical Characteristics; as the remaining combinations can be derived from them.

For the PT7A4408/4408L, two internal elements determine the jitter attenuation. They are internal 1.9Hz low pass loop filter and phase slope limiter. The phase slope limiter limits the output phase slope to 5ns/125µs. Therefore, if the input signal exceeds this rate, such as for very large amplitude low frequency input jitter, the maximum output phase slope will be limited (i.e., attenuated) to 5ns/125µs.

It should be noted that 1UI at 1.544MHz (644ns) is not equal to 1UI at 2.048MHz (488ns). A transfer value using different input and output frequencies must be calculated in common units (e.g., seconds) as shown in the following example.

Example : When the T1 input jitter is 20UI (T1 UI Units) and the T1 to T1 jitter attenuation is 18dB, The T1 and E1 output jitter can be calculated as follows:

$$J_{T1o} = J_{T1i} \times 10^{\left(\frac{-A}{20}\right)} = 20 \times 10^{\left(\frac{-18}{20}\right)} = 2.5UI$$

$$J_{E1o} = J_{T1o} \times \left(\frac{1UIT1}{1UIE1}\right) = J_{T1o} \times \left(\frac{644ns}{488ns}\right) = 3.3UI$$

Using the above method, the jitter attenuation can be calculated for all combinations of inputs and outputs based on the three jitter transfer functions provided.

Note that the resulting jitter transfer functions for all combinations of inputs (8kHz, 1.544MHz, 2.048MHz) and outputs (8kHz, 1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, 16.384MHz, 6.312MHz, 19.44MHz) for a given input signal (jitter frequency and jitter amplitude) are the same.

Since intrinsic jitter is always present, jitter attenuation will appear to be lower for small input jitter signals than for large ones. Consequently, accurate jitter transfer function measurements are usually made with large input jitter signals (e.g., 75% of the specified maximum jitter tolerance).

Frequency Accuracy: Frequency accuracy is defined as the absolute tolerance of an output clock signal when it is not locked to an external reference, but is operating in a free running mode. For the PT7A4408/4408L, the Free-Run accuracy is equal to the Master Clock (OSCi) accuracy.

Lock Range: If the PT7A4408/4408L DPLL is already in a state of synchronization ("lock") with the incoming reference signal, it is able to track this signal to maintain lock as its frequency varies over a certain range, called the Lock Range. The size of Lock Range is related to the range of the Digitally Controlled Oscillators and is equal to 230ppm minus the accuracy of the master clock (OSCi). For example, a 32ppm master clock results in a Lock Range of 198ppm.

Capture Range: The PT7A4408/4408L DPLL is not at present in a state of synchronization (lock) with the incoming reference signal, it is able to initiate (acquire) lock only if the signal's frequency is within a certain range, called the Capture Range. For any PLL, no portion of the Capture Range can fall outside the Lock Range, and, in general, the Capture Range is more narrow than the Lock Range. However, owing to the design of its Phase Detector, the PT7A4408/4408L's Capture Range is equal to its Lock Range.

Phase Slope: Phase slope is measured in seconds per second and is the rate at which a given signal changes phase with respect to an ideal signal of constant frequency. The given signal is typically the output signal. The ideal signal is of constant frequency and is nominally equal to the value of the final output signal or final input signal.

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Ambient Temperature with Power Applied ..... -40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V_{CC} Only) ..... -0.3 to 7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only) .. -0.3 to 7.0V
DC Input Voltage ..... -0.3 to 7.0V
DC Output Current 120mA
Power Dissipation 900mW

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Sym	Description	Test Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage for 4408	Over Recommended Operating Conditions	4.5	5.0	5.5	V
	Supply Voltage for 4408L		3.0	3.3	3.6	V
T_A	Operating Temperature		-40	25	85	°C

DC Electrical and Power Supply Characteristics

Table 5. DC Electrical and Power Supply Characteristics

Sym	Description	Device	Test Conditions	Min	Typ	Max	Units
I_{CCQ}	Quiescent Power Supply Current	4408	OSCi = 0V, Note 2			20	mA
		4408L				10	mA
I_{CC}	Supply Current	4408	OSCi = Clock, Note 2			60	mA
		4408L				35	mA
		4408	OSCi = Crystal, Note 2			70	mA
		4408L				40	mA
V_{IH}	TTL HIGH Input Voltage-All pins except OSCi, $\overline{RST}$			2.0			V
V_{IL}	TTL LOW Input Voltage-All pins except OSCi, $\overline{RST}$					0.8	V
V_{CIH}	CMOS HIGH Input Voltage-OSCi pin			$0.7V_{CC}$			V
V_{CIL}	CMOS LOW Input Voltage-OSCi pin					$0.3V_{CC}$	V
V_{SIH}	Schmitt HIGH Input Voltage-$\overline{RST}$ pins	4408		3.6			V
		4408L		2.6			V
V_{SIL}	Schmitt LOW Input Voltage-$\overline{RST}$ pins	4408				1.8	V
		4408L				1.1	V
V_{HYS}	Schmitt Hysteresis Voltage-$\overline{RST}$ pins			0.4			V
I_{IL}	Input Leakage Current - Pins: TCK, REF, TDI, TMS	4408	$V_I = V_{CC}$ or 0V	-140			µA
		4408L		-100			µA
	Input Leakage Current - Pins: $\overline{TRST}$, ACKi, MS, TEST	4408				140	µA
		4408L				100	µA
	Input Leakage Current - other pins			-10		10	µA
V_{OH}	HIGH Output Voltage	4408	I_{OH} = -4mA	2.4			V
		4408L		2.0			V
V_{OL}	LOW Output Voltage		I_{OL} = 4mA			0.8	V

Note:
1. Supply voltages and operating temperature are as per Recommended Operating Conditions.
2. MS = V_{CC}, FS1 = V_{CC} , FS2= GND, other inputs connected to GND.
3. All outputs are unloaded except for V_{OH} and V_{OL} measurement.

AC Electrical Characteristics

Performance

Table 6. Performance

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Free-Run State Accuracy with OSCi at: 0ppm	5-8	0		0	ppm
	Free-Run State Accuracy with OSCi at: 32ppm	5-8	-32		+32	ppm
	Free-Run State Accuracy with OSCi at: 100ppm	5-8	-100		+100	ppm
	DPLL Capture Range With OSCi at: 0ppm	3, 6-8	-190		+230	ppm
	DPLL Capture Range With OSCi at: 32ppm	3, 6-8	-158		+198	ppm
	DPLL Capture Range With OSCi at: 100ppm	3, 6-8	-90		+130	ppm
	APLL Capture Range	43	10		30	MHz
	Phase Lock Time	3, 6-14			23	s
	Output Phase Slope	3-14, 27			45	µs/s
	Reference Input for Auto-Holdover with:8kHz	3, 6, 9-11	<-30k	or	>+30k	ppm
	Reference Input for Auto-Holdover with:1.544MHz	3, 7, 9-11	<-30k	or	>+30k	ppm
	Reference Input for Auto-Holdover with:2.048MHz	3, 8-11	<-30k	or	>+30k	ppm

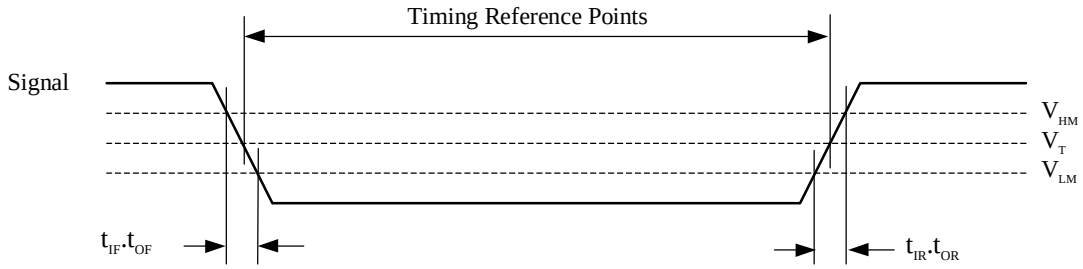
* Refer to the **Test Conditions** on Page 25 for details.

Voltage Levels for Timing Parameter Measurement

Table 7. Voltage Levels for Timing Parameter Measurement

Sym	Description	Schmitt	TTL	CMOS	Units
V_T	Threshold Voltage	$0.5V_{CC}$	1.5	$0.5V_{CC}$	V
V_{HM}	Rising and Falling Threshold Voltage High	$0.7V_{CC}$	2.0	$0.7V_{CC}$	V
V_{LM}	Rising and Falling Threshold Voltage Low	$0.3V_{CC}$	0.8	$0.3V_{CC}$	V

Figure 8. Voltage Levels for Timing Parameter Measurement



Input and Output Timing

Table 8. Input and Output Timing of 4408

Sym	Description	Test Conditions*	Min	Typ	Max	Units
t_{RW}	Reference Input pulse Width High or Low	3, 6-11, 39	100			ns
t_{IRF}	Reference Input Rising or Falling Time				10	ns
t_{R8D}	8kHz Reference Input to F8 Delay	3, 6-14, 21, 23, 38	-28		-1	ns
t_{R15D}	1.544kHz Reference Input to F8 Delay		337		363	ns
t_{R2D}	2.048kHz Reference Input to F8 Delay		217		238	ns
t_{F0D}	F8 to $\overline{F0}$ Delay	3-14, 21, 39	110		134	ns
t_{F16D}	F8 to $\overline{F16}$ Delay	3-14, 21	19		44	ns
t_{C15D}	F8 to C1.5 Delay	3-14, 21, 39	-45		-31	ns
t_{C6D}	F8 to C6 Delay		-8		9	ns
t_{C3D}	F8 to $\overline{C3}$ Delay		-46		-31	ns
t_{C2D}	F8 to C2 Delay		-10		5	ns
t_{C4D}	F8 to $\overline{C4}$ Delay		-10		5	ns
t_{C8D}	F8 to C8 Delay		-10		5	ns
t_{C16D}	F8 to $\overline{C16}$ Delay		-10		5	ns
t_{TSPD}	F8 to TSP Delay		-10		10	ns
t_{RSPD}	F8 to RSP Delay		-10		10	ns
t_{C19D}	F8 to C19 Delay		0		52	ns
t_{C15W}	C1.5 Pulse Width High or Low		309		339	ns
t_{C3W}	$\overline{C3}$ Pulse Width High or Low		149		175	ns
t_{C6W}	C6 Pulse Width High or Low		72		86	ns
t_{C2W}	C2 Pulse Width High or Low		230		258	ns
t_{C4W}	$\overline{C4}$ Pulse Width High or Low		111		133	ns
t_{C8W}	C8 Pulse Width High or Low		52		70	ns

* Refer to the **Test Conditions** on Page 25 for details.

Table 9. Input and Output Timing of 4408L

Sym	Description	Test Conditions*	Min	Typ	Max	Units
t_{RW}	Reference Input pulse Width High or Low	3, 6-11, 39	100			ns
t_{IRF}	Reference Input Rising or Falling Time				10	ns
t_{R8D}	8kHz Reference Input to F8 Delay	3, 6-14, 21, 23, 38	-21		6	ns
t_{R15D}	1.544kHz Reference Input to F8 Delay		345		371	ns
t_{R2D}	2.048kHz Reference Input to F8 Delay		232		248	ns
t_{F0D}	F8 to $\overline{F0}$ Delay	3-14, 21, 39	112		138	ns
t_{F16D}	F8 to $\overline{F16}$ Delay	3-14, 21	19		44	ns
t_{C15D}	F8 to C1.5 Delay	3-14, 21, 39	-47		-31	ns
t_{C6D} [1)]	F8 to C6 Delay		-9		9	ns
t_{C3D}	F8 to $\overline{C3}$ Delay		-49		-32	ns
t_{C2D}	F8 to C2 Delay		-11		4	ns
t_{C4D}	F8 to $\overline{C4}$ Delay		-11		4	ns
t_{C8D}	F8 to C8 Delay		-11		4	ns
t_{C16D}	F8 to $\overline{C16}$ Delay		-11		4	ns
t_{TSPD} [1)]	F8 to TSP Delay		-10		10	ns
t_{RSPD} [1)]	F8 to RSP Delay		-10		10	ns
t_{C19D} [1)]	F8 to C19 Delay		0		52	ns
t_{C15W}	C1.5 Pulse Width High or Low		309		339	ns
t_{C3W}	$\overline{C3}$ Pulse Width High or Low		149		175	ns
t_{C6W} [1)]	C6 Pulse Width High or Low		72		86	ns
t_{C2W}	C2 Pulse Width High or Low		230		258	ns
t_{C4W}	$\overline{C4}$ Pulse Width High or Low		111		133	ns
t_{C8W}	C8 Pulse Width High or Low		52		70	ns

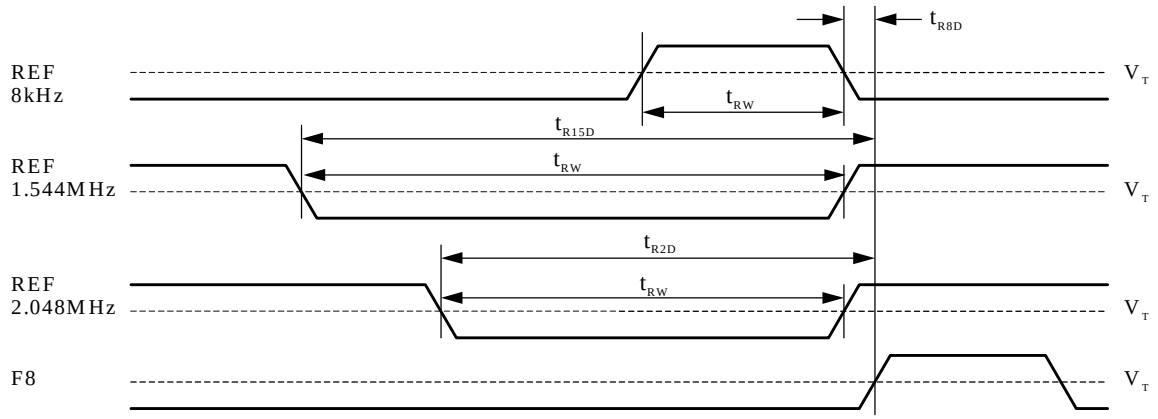
* Refer to the **Test Conditions** on Page 25 for details.

Table 10. Input and Output Timing (Continued)

Sym	Description	Test Conditions*	Min	Typ	Max	Units
t_{C16WL}	$\overline{C16}$ Pulse Width Low	3-14, 21	26		37	ns
t_{TSPW}	TSP Pulse Width High		478		494	ns
t_{RSPW}	RSP Pulse Width High		478		495	ns
t_{C19W}	C19 Pulse Width High or Low		16		36	ns
t_{F0WL}	$\overline{F0}$ Pulse Width Low	3-14, 21, 39	230		258	ns
t_{F8WH}	F8 Pulse Width High		111		133	ns
t_{F16WL}	$\overline{F16}$ Pulse Width Low		52		70	ns
t_{ORF}	Output Clock and Frame Pulse Rising or Falling Time				9	ns
t_S	Input Controls Setup Time		100			ns
t_H	Input Controls Hold Time		100			ns

* Refer to the **Test Conditions** on Page 25 for details.

Figure 9. Input to Output Timing (Normal State, after $\overline{RST}$)



Note: Input to output delay values are valid after a $\overline{RST}$ with no further state changes.

Figure 10. Output Timing

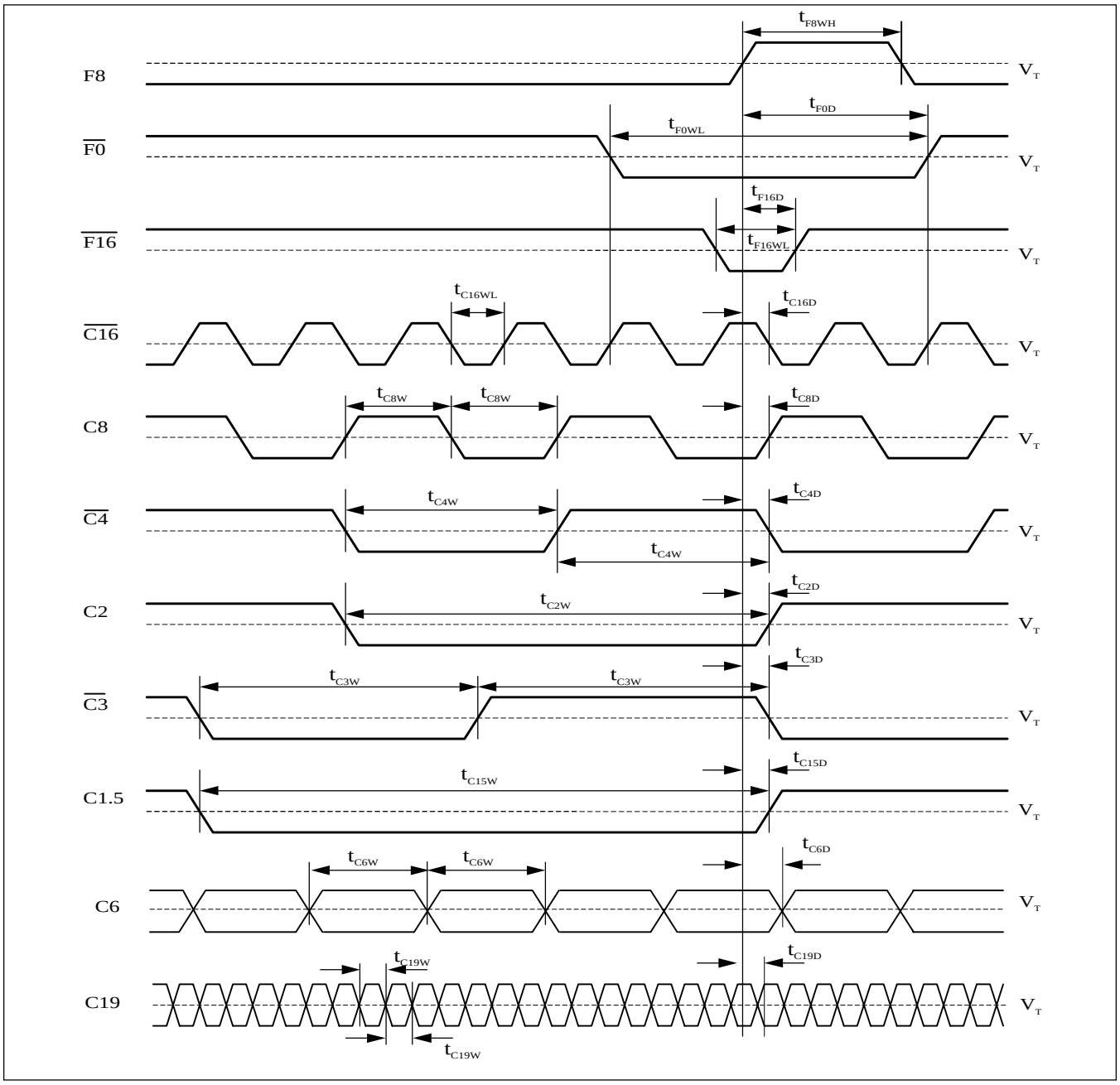


Figure 11. Output Timing

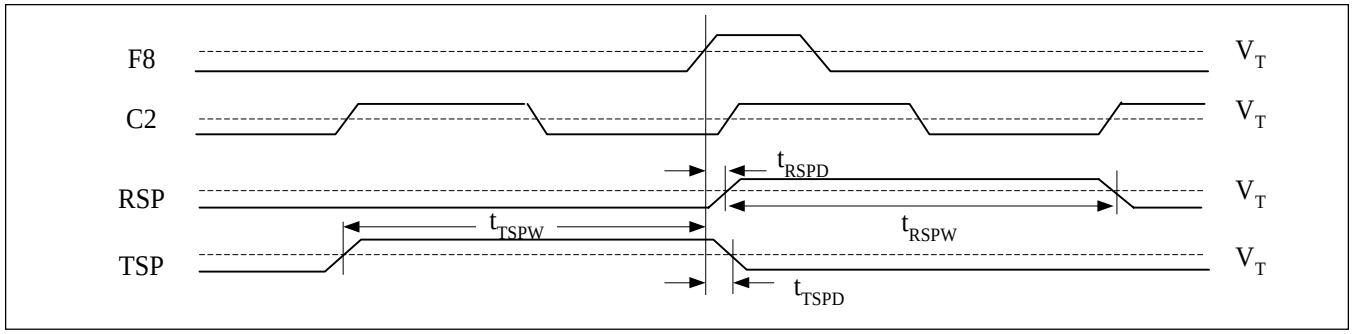
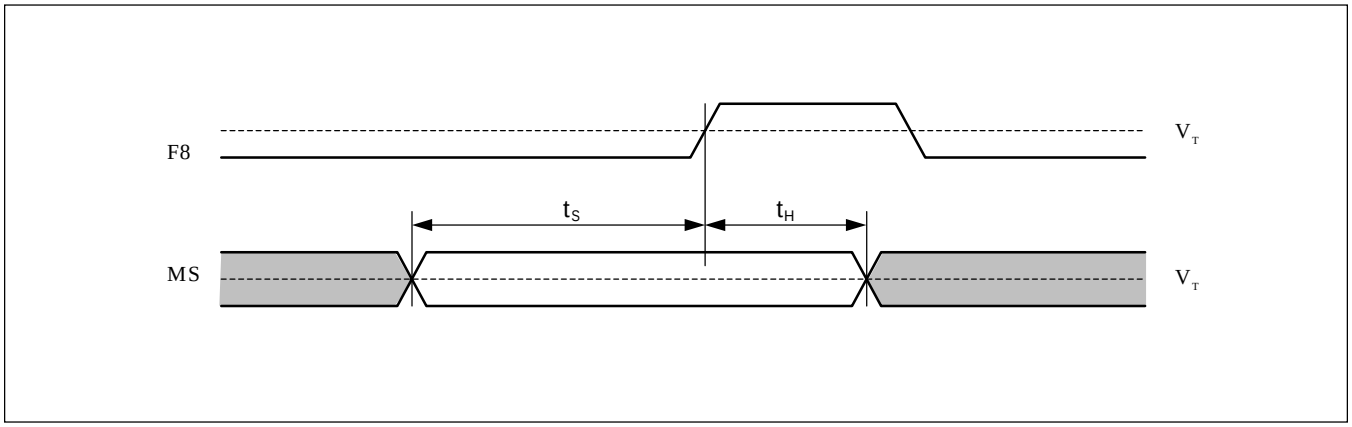


Figure 12. Setup and Hold Timing of Input Controls



Intrinsic Jitter Unfiltered

Table 11. Intrinsic Jitter Unfiltered

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Instrinsic Jitter at F8 (8kHz)	3-14, 21-24, 28			0.0002	UIpp
	Instrinsic Jitter at $\overline{F0}$ (8kHz)				0.0002	UIpp
	Instrinsic Jitter at $\overline{F16}$ (8kHz)				0.0002	UIpp
	Instrinsic Jitter at C1.5 (1.544MHz)	3-14, 21-24, 29			0.030	UIpp
	Instrinsic Jitter at C2 (2.048MHz)	3-14, 21-24, 30			0.040	UIpp
	Instrinsic Jitter at $\overline{C3}$ (3.088MHz)	3-14, 21-24, 31			0.060	UIpp
	Instrinsic Jitter at $\overline{C4}$ (4.096MHz)	3-14, 21-24, 32			0.080	UIpp
	Instrinsic Jitter at C6 (6.312MHz)	3-14, 21-24, 41			0.120	UIpp
	Instrinsic Jitter at C8 (8.192MHz)	3-14, 21-24, 33			0.160	UIpp
	Instrinsic Jitter at $\overline{C16}$ (16.384MHz)	3-14, 21-24, 34			0.320	UIpp
	Instrinsic Jitter at C19 (19.44MHz)	3-14, 21-24, 42			0.230	UIpp
	Instrinsic Jitter at TSP (8kHz)	3-14, 21-24, 28			0.0002	UIpp
	Instrinsic Jitter at RSP (8kHz)	3-14, 21-24, 28			0.0002	UIpp

* Refer to the **Test Conditions** on Page 25 for details.

C1.5 (1.544MHz) Instrinsic Jitter Filtered

Table 12. C1.5 (1.544MHz) Instrinsic Jitter Filtered

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Instrinsic Jitter (4Hz to 100kHz Filter)	3-14, 21-24, 29			0.015	UIpp
	Instrinsic Jitter (10Hz to 40kHz Filter)				0.010	UIpp
	Instrinsic Jitter (8kHz to 40kHz Filter)				0.010	UIpp
	Instrinsic Jitter (10Hz to 8kHz Filter)				0.005	UIpp

* Refer to the **Test Conditions** on Page 25 for details.

C2 (2.048MHz) Instrinsic Jitter Filtered

Table 13. C2 (2.048MHz) Instrinsic Jitter Filtered

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Instrinsic Jitter (4Hz to 100kHz Filter)	3-14, 21-24, 30			0.015	UIpp
	Instrinsic Jitter (10Hz to 40kHz Filter)				0.010	UIpp
	Instrinsic Jitter (8kHz to 40kHz Filter)				0.010	UIpp
	Instrinsic Jitter (10Hz to 8kHz Filter)				0.005	UIpp

* Refer to the **Test Conditions** on Page 25 for details.

8kHz Input to 8kHz Output Jitter Transfer

Table 14. 8kHz Input to 8kHz Output Jitter Transfer

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Jitter Attenuation for 1Hz with 0.01UIpp Input	3, 6, 9-14, 21, 22, 24, 28, 35	0		6	dB
	Jitter Attenuation for 1Hz with 0.54UIpp Input		6		16	dB
	Jitter Attenuation for 10Hz with 0.10UIpp Input		12		22	dB
	Jitter Attenuation for 60Hz with 0.10UIpp Input		28		38	dB
	Jitter Attenuation for 300Hz with 0.10UIpp Input		42			dB
	Jitter Attenuation for 3600Hz with 0.005UIpp Input		45			dB

* Refer to the **Test Conditions** on Page 25 for details.

1.544MHz Input to 1.544MHz Output Jitter Transfer

Table 15. 1.544MHz Input to 1.544MHz Output Jitter Transfer

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Jitter Attenuation for 1Hz with 20UIpp Input	3, 7, 9-14, 21, 22, 24, 29, 35	0		6	dB
	Jitter Attenuation for 1Hz with 104UIpp Input		6		16	dB
	Jitter Attenuation for 10Hz with 20UIpp Input		12		22	dB
	Jitter Attenuation for 60Hz with 20UIpp Input		28		38	dB
	Jitter Attenuation for 300Hz with 20UIpp Input		42			dB
	Jitter Attenuation for 10kHz with 0.3UIpp Input		45			dB
	Jitter Attenuation for 100kHz with 0.3UIpp Input		45			dB

* Refer to the **Test Conditions** on Page 25 for details.

2.048MHz Input to 2.048MHz Output Jitter Transfer

Table 16. 2.048MHz Input to 2.048MHz Output Jitter Transfer

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Jitter at Output for 1Hz 3.00UIpp Input	3,8,9-14,21,22,24,30,35			2.9	UIpp
		3,8,9-14,21,22,24,30,36			0.09	UIpp
	Jitter at Output for 3Hz 2.33UIpp Input	3,8,9-14,21,22,24,30,35			1.3	UIpp
		3,8,9-14,21,22,24,30,36			0.10	UIpp
	Jitter at Output for 5Hz 2.07UIpp Input	3,8,9-14,21,22,24,30,35			0.80	UIpp
		3,8,9-14,21,22,24,30,36			0.10	UIpp
	Jitter at Output for 10Hz 1.76UIpp Input	3,8,9-14,21,22,24,30,35			0.40	UIpp
		3,8,9-14,21,22,24,30,36			0.10	UIpp
	Jitter at Output for 100Hz 1.50UIpp Input	3,8,9-14,21,22,24,30,35			0.06	UIpp
		3,8,9-14,21,22,24,30,36			0.05	UIpp
	Jitter at Output for 2400Hz 1.50UIpp Input	3,8,9-14,21,22,24,30,35			0.04	UIpp
		3,8,9-14,21,22,24,30,36			0.03	UIpp
	Jitter at Output for 100kHz 0.20UIpp Input	3,8,9-14,21,22,24,30,35			0.04	UIpp
		3,8,9-14,21,22,24,30,36			0.02	UIpp

* Refer to the **Test Conditions** on Page 25 for details.

8kHz Input Jitter Tolerance

Table 17. 8kHz Input Jitter Tolerance

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Jitter Tolerance for 1Hz Input	3,6,9-14,21,22,24-26,28	0.80			UIpp
	Jitter Tolerance for 5Hz Input		0.70			UIpp
	Jitter Tolerance for 20Hz Input		0.60			UIpp
	Jitter Tolerance for 300Hz Input		0.20			UIpp
	Jitter Tolerance for 400Hz Input		0.15			UIpp
	Jitter Tolerance for 700Hz Input		0.08			UIpp
	Jitter Tolerance for 2400Hz Input		0.02			UIpp
	Jitter Tolerance for 3600Hz Input		0.01			UIpp

* Refer to the **Test Conditions** on Page 25 for details.

1.544MHz Input Jitter Tolerance

Table 18. 1.544MHz Input Jitter Tolerance

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Jitter Tolerance for 1Hz Input	3,7,9-14,21,22,24-26,29	150			UIpp
	Jitter Tolerance for 5Hz Input		140			UIpp
	Jitter Tolerance for 20Hz Input		130			UIpp
	Jitter Tolerance for 300Hz Input		35			UIpp
	Jitter Tolerance for 400Hz Input		25			UIpp
	Jitter Tolerance for 700Hz Input		15			UIpp
	Jitter Tolerance for 2400Hz Input		4			UIpp
	Jitter Tolerance for 10kHz Input		1			UIpp
	Jitter Tolerance for 100kHz Input		0.5			UIpp

* Refer to the **Test Conditions** on Page 25 for details.

2.048MHz Input Jitter Tolerance

Table 19. 2.048MHz Input Jitter Tolerance

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Jitter Tolerance for 1Hz Input	3,8,9-14,21,22,24-26,30	150			UIpp
	Jitter Tolerance for 5Hz Input		140			UIpp
	Jitter Tolerance for 20Hz Input		130			UIpp
	Jitter Tolerance for 300Hz Input		50			UIpp
	Jitter Tolerance for 400Hz Input		40			UIpp
	Jitter Tolerance for 700Hz Input		20			UIpp
	Jitter Tolerance for 2400Hz Input		5			UIpp
	Jitter Tolerance for 10kHz Input		1			UIpp
	Jitter Tolerance for 100kHz Input		1			UIpp

* Refer to the **Test Conditions** on Page 25 for details.

OSCi 20MHz Master Clock Input

Table 20. OSCi 20MHz Master Clock Input

Sym	Description	Test Conditions*	Min	Typ	Max	Units
	Tolerance	15, 18	0		0	ppm
		16, 19	-32		+32	ppm
		17, 20	-100		+100	ppm
	Duty Cycle		40		60	%
	Rising Time				10	ns
	Falling Time				10	ns

* Refer to the **Test Conditions** on Page 25 for details.

Notes:

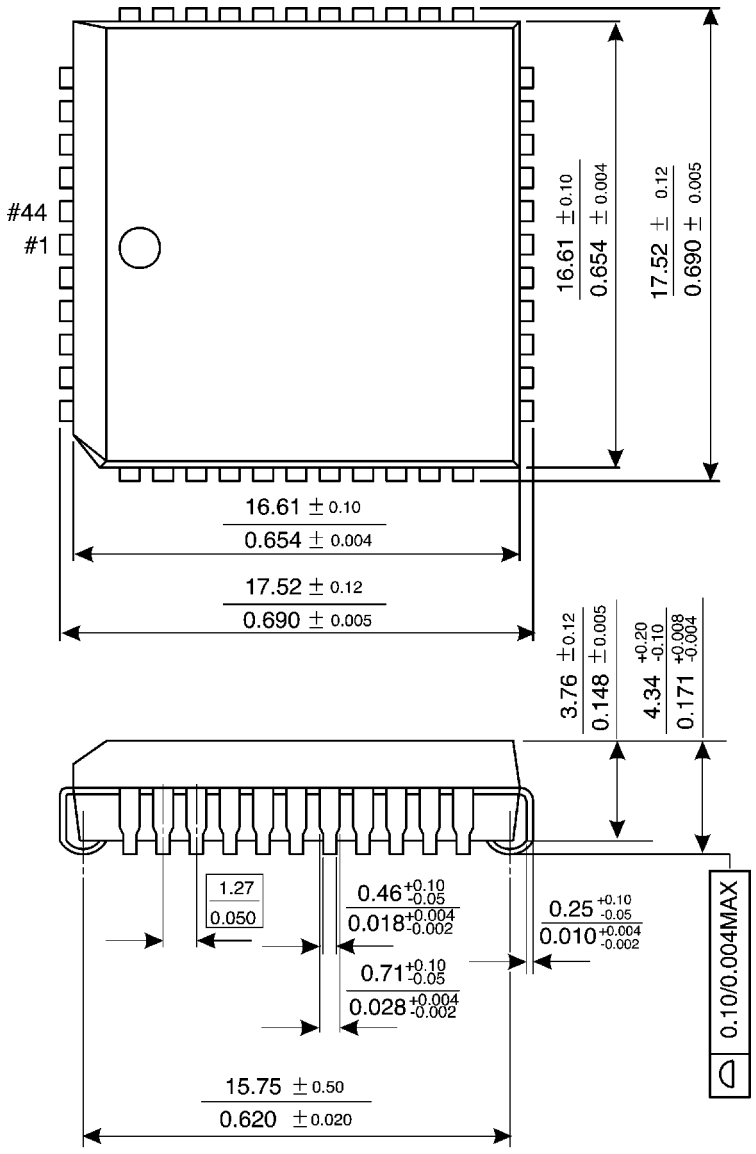
1. Voltages are with respect to ground (GND) unless otherwise stated.
2. Supply voltage and operation temperature are as per Recommended Operating Conditions.
3. Timing parameters are as per AC Electrical Characteristics - Voltage Levels for Timing Parameter Measurement.

Test Conditions:

1.
2.
3. Normal State selected.
4.
5. Free-Run State selected.
6. 8kHz frequency source selected.
7. 1.544MHz frequency source selected.
8. 2.048MHz frequency source selected.
9. Master clock input OSCi at 20MHz ±0ppm.
10. Master clock input OSCi at 20MHz ±32ppm.
11. Master clock input OSCi at 20MHz ±100ppm.
12. Selected reference input at ±0ppm.
13. Selected reference input at ±32ppm.
14. Selected reference input at ±100ppm.
15. For Free-Run State of ±0ppm.
16. For Free-Run State of ±32ppm.
17. For Free-Run State of ±100ppm.
18. For capture range of ±230ppm.
19. For capture range of ±198ppm.
20. For capture range of ±130ppm.
21. 25pF capacitive load.
22. OSCi Master Clock Jitter is less than 2ns p-p, or 0.04UI p-p where 1UI p-p = 1/20MHz.
23. Jitter on reference input is less than 7ns p-p.
24. Applied jitter is sinusoidal.
25. Minimum applied input jitter magnitude to regain synchronization.
26. Loss of synchronization is obtained at slightly higher input jitter amplitudes.
27. Within 10ms of the state, reference or input change.
28. 1UIpp = 125µs for 8kHz signals.
29. 1UIpp = 648ns for 1.544MHz signals.
30. 1UIpp = 488ns for 2.048MHz signals.
31. 1UIpp = 324ns for 3.088MHz signals.
32. 1UIpp = 244ns for 4.096MHz signals.
33. 1UIpp = 122ns for 8.192MHz signals.
34. 1UIpp = 61ns for 16.384MHz signals.
35. No filter.
36. 40Hz to 100kHz bandpass filter.
37. With respect to reference input signal frequency.
38. After a $\overline{RST}$
39. Master clock duty cycle 40% to 60%.
40. In Normal State and phase locked.
41. 1UIpp = 162ns for 6.312MHz signals.
42. 1UIpp = 51ns for 19.44MHz signals.

Mechanical Specifications

Figure 13. 44-pin PLCC



Dimensions in Millimeters/Inches

Note

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