

Absolute Maximum Ratings ⁽¹⁾

Operating Temperature	T_{OPR}	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Input voltages (including N.C. pins) with Respect to GND	V_{IN}	-1.0 to +7.0	V
Output voltages with respect to GND	V_{OUT}	-1.0 to +7.0	V

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

		<i>min</i>	<i>typ</i>	<i>max</i>	
DC Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-	-	0.8	V
Input High Voltage	V_{IH}	2.0	-	-	V
Operating Temp Range	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (I Suffix)
	T_{AM}	-55	-	125	°C (M, MB Suffix)

DC Electrical Characteristics ($T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$)

Parameter	Symbol	Test Condition	<i>min</i>	<i>max</i>	Unit
Input Leakage Current A0~A15, \overline{OE}	I_{L1}	$V_{IN} = \text{GND to } V_{CC}$	-	± 40	μA
WE1~4, CS1~4	I_{L2}	$V_{IN} = \text{GND to } V_{CC}$	-	± 10	μA
Output Leakage Current 32 bit	I_{LO}	$V_{IN} = \text{GND to } V_{CC}, \overline{CS}^{(1)} = V_{IH}$	-	± 40	μA
Operating Supply Current 32 bit	I_{CC32}	$\overline{CS}^{(1)} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}, I_{OUT} = 0\text{mA}, f = 5\text{MHz}^{(2)}$	-	200	mA
16 bit	I_{CC16}	As above	-	106	mA
8 bit	I_{CC8}	As above	-	59	mA
Standby Supply Current TTL levels	I_{SB1}	$\overline{CS}^{(1)} = V_{IH}, I_{IO} = 0\text{mA}, \text{Other Inputs} = V_{IH}$	-	12	mA
CMOS levels	I_{SB2}	$\overline{CS}^{(1)} = V_{CC} - 0.3\text{V}, I_{IO} = 0\text{mA}, \text{Other Inputs} = V_{CC}$	-	2	mA
Output Low Voltage	V_{OL}	$I_{OL} = 2.1\text{mA}$	-	0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -400\mu\text{A}$	2.4	-	V

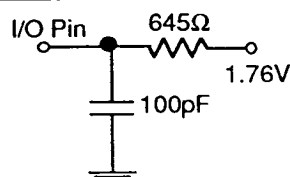
Notes (1) \overline{CS} above are accessed through CS1-4. These inputs must be operated simultaneously for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

Capacitance ($T_A = 25^{\circ}\text{C}$, $f = 1\text{MHz}$) Note: These parameters are calculated, not measured.

Parameter	Symbol	Test Condition	<i>typ</i>	<i>max</i>	Unit
Input Capacitance A0~A15, \overline{OE}	C_{IN1}	$V_{IN} = 0\text{V}$	-	20	pF
WE1~4, CS1~4	C_{IN2}	$V_{IN} = 0\text{V}$	-	60	pF
Output Capacitance 32 bit	C_{OUT32}	$V_{OUT} = 0\text{V}$	-	20	pF

AC Test Conditions**Output Load**

- * Input pulse levels: 0.0V to 3.0V
- * Input rise and fall times: 5ns
- * Input and Output timing reference levels: 1.5V
- * $V_{CC} = 5\text{V} \pm 10\%$
- * Module tested in 32 bit mode.

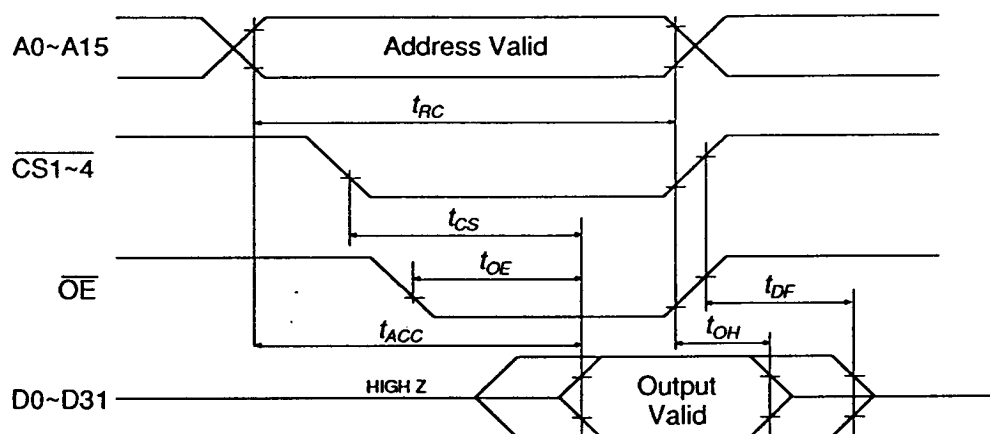


AC READ CHARACTERISTICS**Read Cycle**

Parameter	Symbol	-12		-15		-20		-25		Unit
		min	max	min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	-	150	-	200	-	250	-	ns
Address to Output Delay	t_{ACC}	-	120	-	150	-	200	-	250	ns
\overline{CS} to Output Delay	t_{CS}	-	120	-	150	-	200	-	250	ns
\overline{OE} to Output Delay	t_{OE}	0	50	0	50	0	50	0	50	ns
\overline{CS} or \overline{OE} to Output Float ^(1,2)	t_{DF}	0	50	0	50	0	50	0	50	ns
Output Hold from \overline{OE} , \overline{CS} or Address, (whichever occurred first)	t_{OH}	0	-	0	-	0	-	0	-	ns

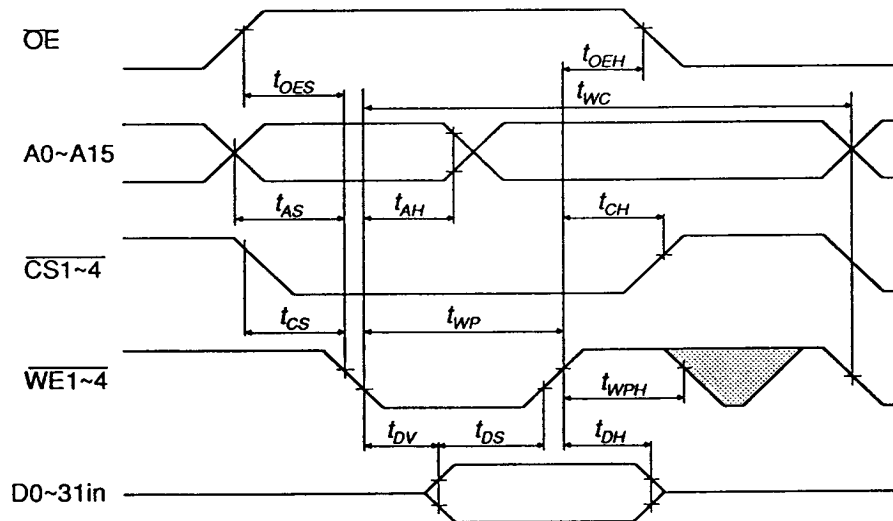
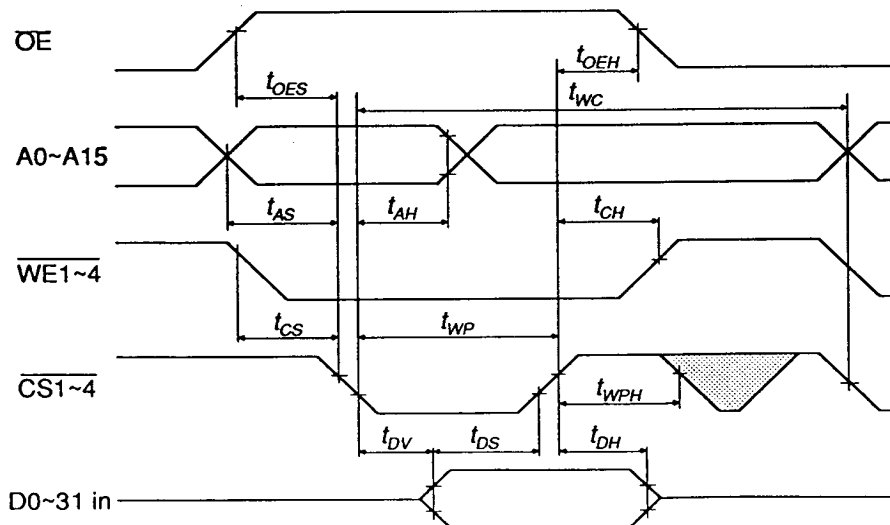
Notes: (1) t_{DF} is specified from \overline{OE} or $\overline{CS1-4}$ whichever occurs first ($C_L = 5pF$).

(2) This parameter is only sampled and is not 100% tested.

Read Cycle Timing Waveform

AC WRITE CHARACTERISTICS**Write Cycle**

Parameter	Symbol	min	typ	max	Unit
Address Set-up Time	t_{AS}	0	-	-	ns
OE Set-up Time	t_{OES}	10	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
Chip Select Set-up Time	t_{CS}	0	-	-	ns
Chip Select Hold Time	t_{CH}	0	-	-	ns
Write Pulse Width (\overline{WE} or \overline{CS})	t_{WP}	100	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data, OE Hold Time	t_{DH}, t_{OEH}	10	-	-	ns
Time to Data Valid	t_{DV}	-	-	1	μ s
Write Cycle Time	t_{WC}	-	5	10	ms

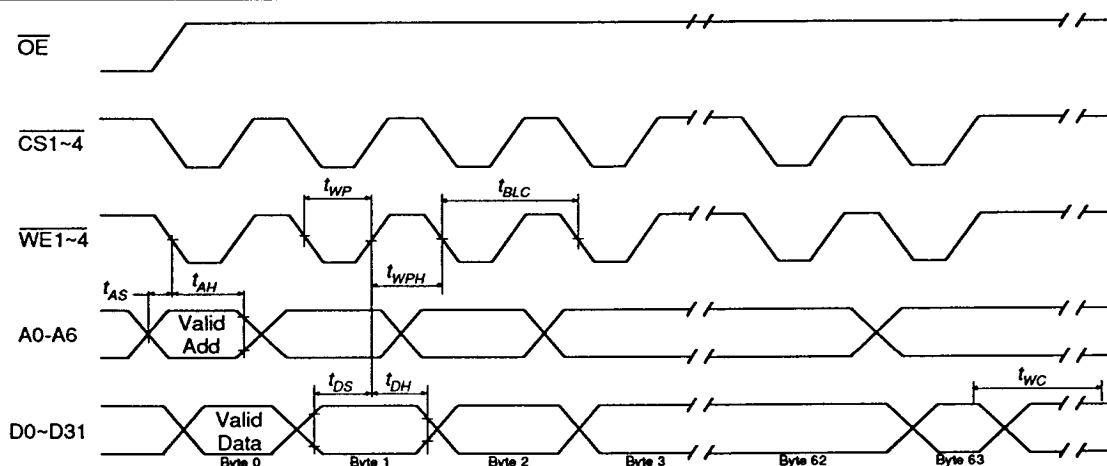
AC Write Waveform - \overline{WE} Controlled**AC Write Waveform - \overline{CS} Controlled**

PAGE MODE WRITE CHARACTERISTICS

Write Cycle

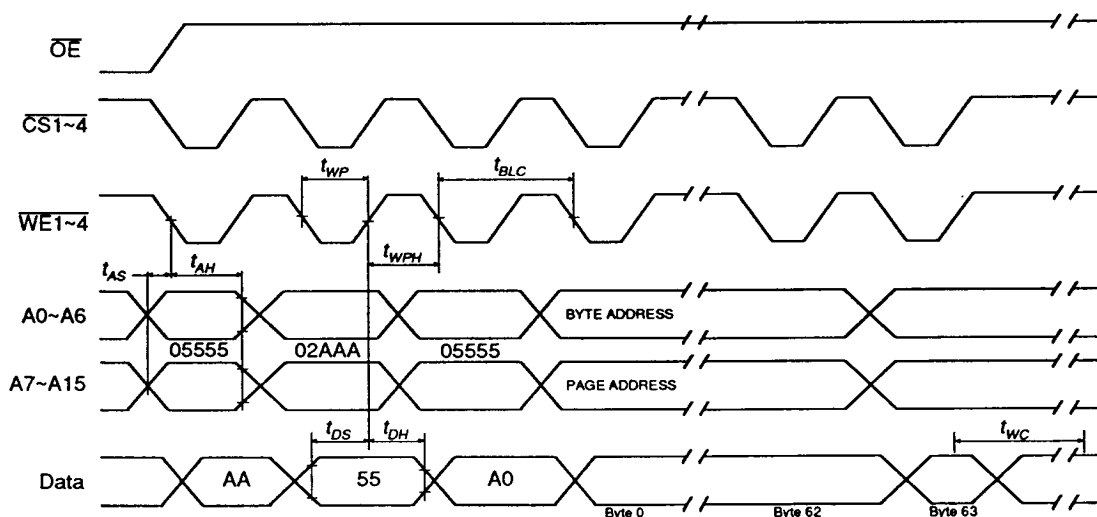
Parameter	Symbol	min	typ	max	Unit
Write Cycle Time	t_{WC}	-	-	10	ms
Address Set-up Time	t_{AS}	0	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data Hold Time	t_{DH}	10	-	-	ns
Write Pulse Width	t_{WP}	100	-	-	ns
Byte Load Cycle Time	t_{BLC}	0.2	-	200	μ s
Write Pulse Width High	t_{WPH}	100	-	-	ns

Page Mode Write Waveform



Note: A7 through A15 must specify the page address during each high to low transition of \overline{WE} (or \overline{CS}). \overline{OE} must be high only when \overline{WE} and \overline{CS} are both low.

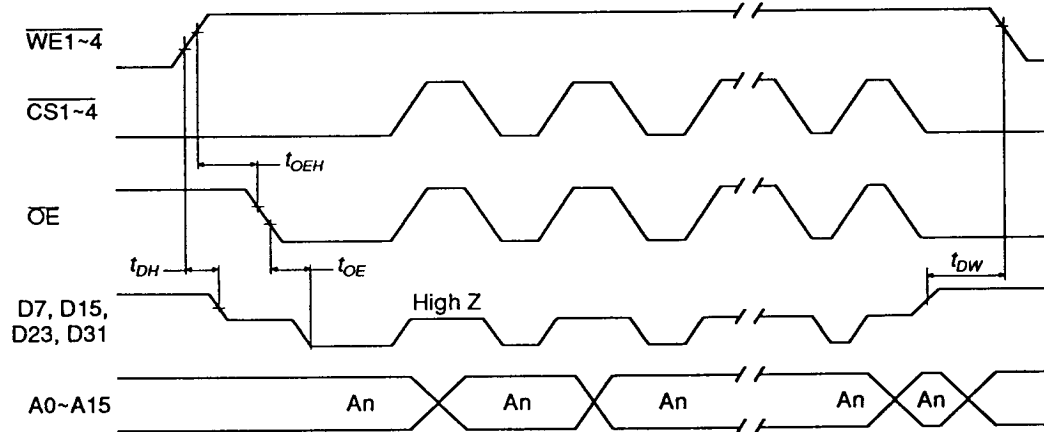
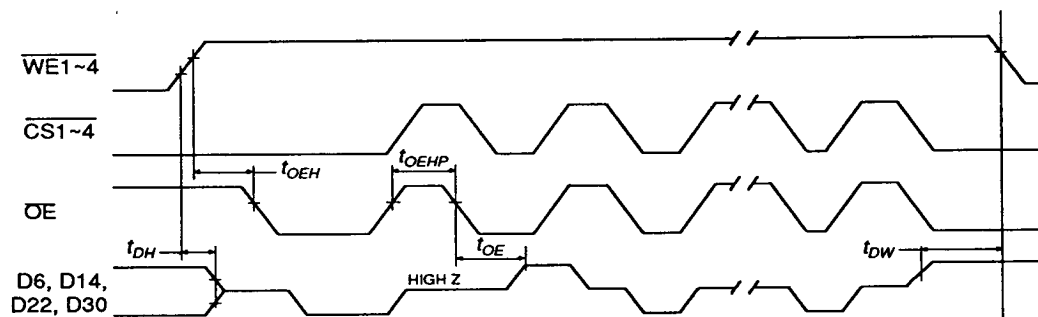
Software Protected Write Waveform



Notes: (1) A7 through A15 must specify the page address during each high to low transition of \overline{WE} (or \overline{CS}). \overline{OE} must be high only when \overline{WE} and \overline{CS} are both low.
 (2) The example above is for the PUMA 2E2000 module operating in 8 bit mode.

DATA Polling and Toggle Bit Characteristics

Parameter	Symbol	min	typ	max	Unit
Data Hold Time	t_{DH}	10	-	-	ns
Output Enable Hold Time	t_{OEHP}	10	-	-	ns
Output Enable to Output Delay	t_{OE}	-	-	100	ns
Output Enable High Pulse	t_{OEHP}	150	-	-	ns
Delay to nex Write	t_{DW}	10	-	-	μ s

DATA Polling Waveform**Toggle Bit Waveform**

- Notes : (1) Polling operations are by definition Read Cycles and therefore subject to Read Cycle timings.
 (2) Beginning and ending state of D6 may vary.
 (3) Any address location may be used but the address should not vary.

DEVICE OPERATION

In the following, \overline{CS} refers to CS1~4 and \overline{WE} to WE1~4.

Read

The PUMA 2E2000 is accessed in the same way as a static RAM, with the data stored at the memory location determined by the address pins being placed on the output pins when \overline{CS} and \overline{OE} are low, and \overline{WE} are high. Whenever \overline{CS} or \overline{OE} are high, the outputs are in the OFF or high impedance state.

Write

A low pulse on \overline{WE} with \overline{CS} low or a low pulse on \overline{CS} with \overline{WE} low indicates a write cycle. The address is latched on the falling edge of \overline{CS} or \overline{WE} , and the data is latched on the first rising edge of \overline{CS} or \overline{WE} . Once a byte write has begun it will automatically time itself to completion.

Page Mode Write

This operation mode allows 1 to 128 bytes of data to be loaded into a device, which are then simultaneously written. Once the first byte has been written, each subsequent byte must have the high to low transition of \overline{WE} (or \overline{CS}) within 200 μ s of the same transition of the previous byte. If this 200 μ s time is exceeded, the load period ends and internal programming starts. A7 to A15 specify the page address (which must be valid during the above transitions) and A0 to A6 specify which bytes within the page are to be written. Note that the bytes may be loaded in any order and may be changed within the same load period.

Using the Page Operation Mode allows the entire module to be written in 2.5 seconds, giving an effective 32 bit Write time of less than 39 μ s

DATA Polling

In order to detect the end of a Write Cycle, two methods are provided. During a Write operation (Byte or Page) an attempt to read the last byte written will result in the complement of the written data appearing on D7 (or D15, D23 or D31, depending on the device selected). Once the Write Cycle is complete, true data appears on the outputs and the next Write Cycle may begin. Using this method of indicating the end of a Write can effectively reduce the total write time by 50%.

Toggle Bit

In addition to DATA polling, another method is provided

to determine the end of a Write Cycle. During a write operation successive attempts to read data will result in D6 (or D14, D22 or D30, depending on the device selected) toggling between 1 and 0. Once a write is complete, this toggling will stop and valid data will be read as normal, allowing the next write cycle to be performed. This can eliminate the software housekeeping chore of saving and fetching the last address and data written in order to implement DATA polling. This can be especially helpful in an array composed of multiple PUMA 2E2000 modules that are frequently updated.

Data Protection

Both hardware and software protection is provided as described below.

Four types of hardware protection give high security against accidental writes:

- (a) If $V_{cc} \leq 3.0V$, Write is inhibited
- (b) \overline{OE} low, \overline{CS} or \overline{WE} high inhibits inadvertent Write Cycles during power-on and power-off. Write Cycle timing specifications must be observed concurrently.
- (c) Pulses of less than 10ns on \overline{WE} do not initiate a Write Cycle.

Software controlled data protection, once enabled by the user, means that a software algorithm must be used before any write can be performed. To enable this feature the algorithm opposite is followed, and must be reused for each subsequent write operation. Once set the data protection remains operational until it is disabled by the using the second algorithm opposite; power transitions will not reset this feature.

Operating Modes

The table below shows the logic inputs required to control the operating modes of each EEPROM on the PUMA 2E2000.

MODE	\overline{CS}	\overline{OE}	\overline{WE}	Outputs
Read	0	0	1	Data Out
Write ⁽¹⁾	0	1	0	Data In
Standby	1	X	X	High Z
Write Inhibit	X	X	1	
Write Inhibit	X	0	X	
Output Disable	X	1	X	High Z

1 = V_{IH} 0 = V_{IL} X = Don't care

Note: (1) Refer to AC Programming Waveforms

Software Data Protection

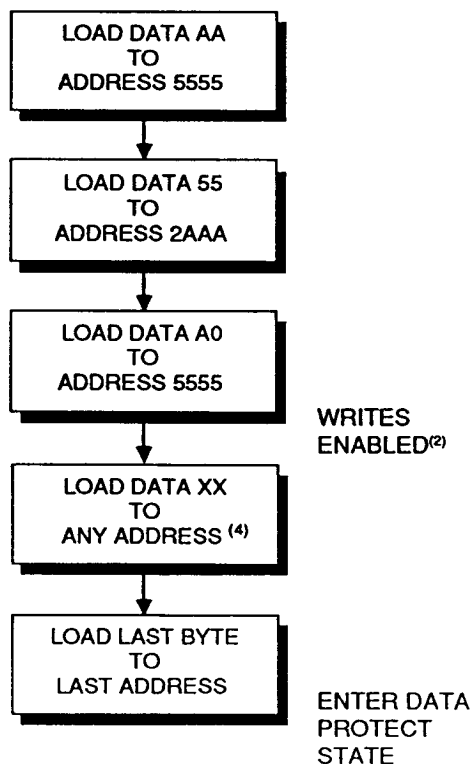
The algorithms below describe the process by which an individual 64K x 8 device on the PUMA may be software write protected and unprotected. Thus, these algorithms apply to the PUMA operating in 8 bit mode; if 16 or 32 bit modes are being used, then the relevant data would be placed on the 16 or 32 bit buses as two or four 8 bit bytes respectively e.g. 5555_H and 55555555_H. In the case of 16 bit mode, this process would be repeated twice with the appropriate devices selected.

The PUMA 2E2000 is shipped with data Protection **NOT ENABLED**. In this mode data should be protected during power-up and power-down operations through the use of external circuits.

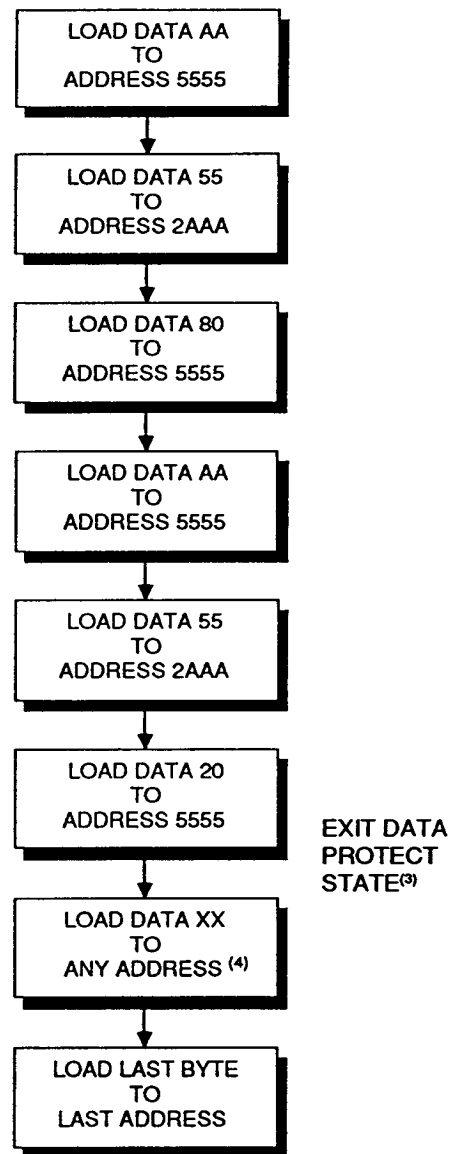
Once data protection has been enabled it is set for the life of the device unless the reset algorithm is followed. In protected mode write operations to the device(s) on the PUMA must be preceded by a series of three write operations to three specific locations, after which 1 to 128 bytes of data may be written. Once the page load cycle is complete, the device(s) return to the data protected state.

NOTE: Once Initiated, the sequence of write operations to Enable and Disable Write Protect should not be interrupted.

Enable Algorithm^{(1) (5)}



Disable Algorithm⁽¹⁾



Notes:

- (1) Data Format I/O7-I/O0 (Hex);
Address Format: A14-A0 (Hex) (A15 don't care).
Once Initiated, this sequence of write operations should not be interrupted.
- (2) Enable Write Protect state will be initiated at end of write even if no other data is loaded.
- (3) Disable Write Protect state will be initiated at end of write period even if no other data is loaded.
- (4) 1 to 128 bytes of data may be loaded.

Military Screening Procedure

Module Screening Flow for high reliability non compliant product processed to MIL-STD883C method 5004 is detailed below:

MB MODULE SCREENING FLOW		
SCREEN	TEST METHOD	LEVEL
Visual and Mechanical External visual Temperature cycle	2017 Condition B or manufacturers equivalent 1010 Condition C (10 Cycles, -65°C to +150°C)	100% 100%
Burn-In Pre-Burn-in electrical Burn-in	Per applicable Device Specifications at $T_A=+25^\circ\text{C}$ Method 1015, Condition D, $T_A=+125^\circ\text{C}$, 160hrs min	100% 100%
Final Electrical Tests Static (DC) Functional Switching (AC)	Per applicable Device Specification a) @ $T_A=+25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes a) @ $T_A=+25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes a) @ $T_A=+25^\circ\text{C}$ and power supply extremes b) @ temperature and power supply extremes	100% 100% 100% 100% 100% 100%
Percent Defective allowable (PDA)	Calculated at Post Burn-in at $T_A=+25^\circ\text{C}$	5%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

PUMA 2E2000MB-20

Speed	12 = 120 ns 15 = 150 ns 20 = 200 ns 25 = 250 ns
Temp. range/screening	Blank = Commercial Temperature I = Industrial Temperature M = Military Temperature MB = Processed to MIL-STD-883C Method 5004, non compliant.
Organization	2000 = 64K x 32, user configurable as 128K x 16 and 256K x 8
Memory Type	E = EEPROM
Package	PUMA 2 = 66 pin Ceramic PGA

The policy of the company is one of continuous development and while the information presented in this data sheet is believed to be accurate, no liability is assumed for any data contained within. The company reserves the right to make changes without notice at any time.

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