mosaic

Mosaic Semiconductor Inc.

128K x 32 FLASH MODULE

PUMA 67F4000-15/20/25

Issue 1.1 : May 1994

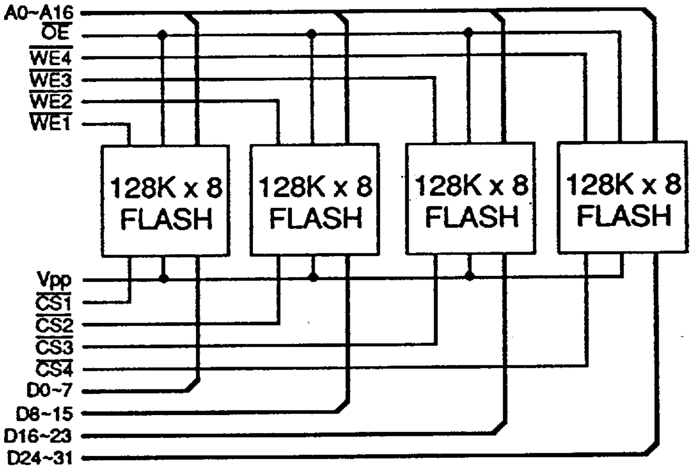
ADVANCE PRODUCT INFORMATION

4,194,304 bit CMOS FLASH Memory Module

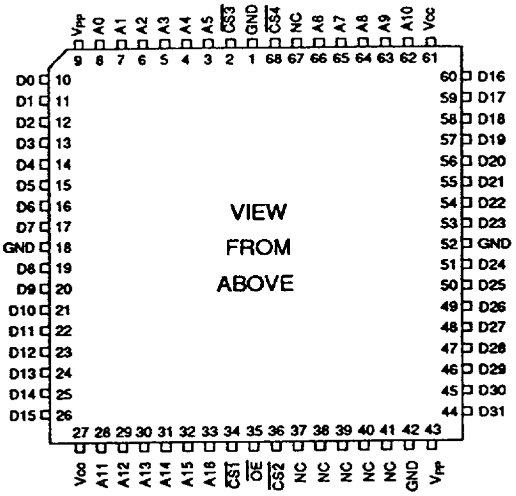
Features

Fast access times of 150/200/250 ns.
User Configurable as 32 / 16 / 8 bit wide.
Operating Power @ 1MHz 120 / 70 / 45 mW (typical).
Low Power Standby 400 µW (maximum).
Single High Voltage for Erase/Write : V_{PP}=12.0V ± 0.6.
Byte Write Time of 25 µs (typical).
Automatic On-Chip Erase Function with Status Polling.
Flash Electrical Erase of Module, 1 second (typical).
10^4 Erase/Write Cycle Endurance minimum.
On board decoupling capacitors.
Module Components may be processed to MIL-STD-883, non-compliant.

Block Diagram



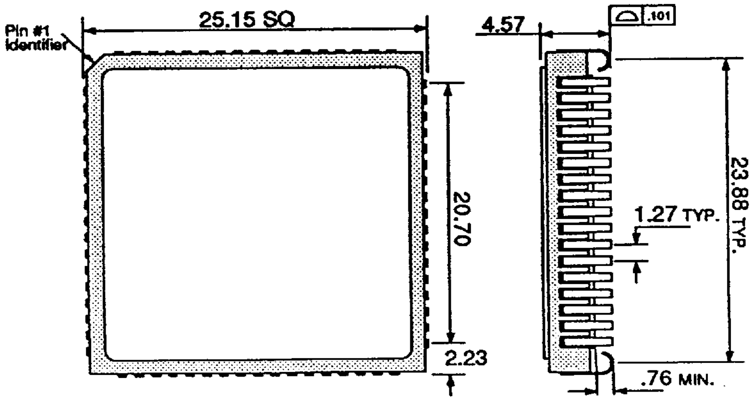
Pin Definition



Pin Functions

A0-A16	Address Inputs
D0-D31	Data Input/Output
CS1-4	Chip Selects
OE	Output Enable
WE1-4	Write Enables
V_{PP}	Write/Erase Input Voltage
V_{CC}	Power (+5V)
GND	Ground

Package Details Dimensions in mm (inches).



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GENERAL DESCRIPTION

The PUMA 2F4000 is a 4,194,304 bit CMOS FLASH memory device. Using $\overline{CS1\text{-}4}$, its' outputs are configurable as 8, 16 or 32 bits wide, allowing flexibility in a wide range of applications.

FLASH memory combines the functionality of EPROM with on-board electrical Write/Erasure. The PUMA 2F4000 utilizes devices which use a Command Register to manage these functions, allowing fixed power supply during Write/Erase and maximum EPROM compatibility. During Write cycles, the command register internally latches address and data needed for the Write and Erase operations, thus simplifying the external control circuitry.

When normal TTL/CMOS logic levels are applied to the V_{PP} pin, the module displays normal EPROM Read, Standby and Output Disable. However, when high voltage (V_{PPH}) is applied to V_{PP} the Write /Erase options are available as well as the Read.

FLASH technology reliably stores data even after 10,000 Write/Erase cycles and utilizes a single program supply of 12V±5%. Additionally, the interactive program algorithm allows a typical room temperature program time of less than 4 seconds for the entire module (in 32 bit mode). The typical module erasure time is less than 1 second.

Absolute Maximum Ratings (1)

Temperature Under Bias	T_{OPR}	-55 to +125 °C
Storage Temperature	T_{STG}	-65 to +150 °C
Voltage on Any Pin with respect to GND (2)	$V_{IN,OUT}$	-0.3 to + 6.5 V
Voltage on A9 pin with respect to GND (2)	V_{ID}	-0.3 to 13.5 V
Voltage on V_{PP} pin with respect to GND	V_{PP}	-0.3 to +14.0 V
V_{CC} Supply Voltage (2)	V_{CC}	-0.3 to +5.5 V

Notes :(1) Stresses above those listed may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_{IN}, V_{OUT}, V_{ID} minimum = -2.0V for pulse width of less than 20 ns.

Recommended Operating Conditions

			min	*typ*	*max*	
Supply Voltage		V_{CC}	4.5	5.0	5.5	V
Programming Voltage	Read	V_{PPL}	V_{CC}-1.0	-	V_{CC}	V
	Write/Erase/Verify	V_{PPH}	11.4	12.0	12.6	V
Identifier Voltage		V_{ID}	11.4	12.0	12.6	V
Input High Voltage	TTL	V_{IH}	2.2	-	V_{CC}+1.0	V
Input Low Voltage	TTL	V_{IL}	-0.3	-	0.8	V
Operating Temperature		T_A	0	-	70	°C
		T_{AI}	-40	-	85	°C (-I suffix)
		T_{AI}	-55	-	125	°C (-M,-MB suffix)

Capacitance (T_A=25°C,f=1MHz)

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	$\overline{CS1\text{-}4}$, $\overline{WE1\text{-}4}$	C_{IN1}	V_{IN}=0V	-	16	pF
	Other pins	C_{IN2}	V_{IN}=0V	-	34	pF
Output Capacitance	32 bit	C_{OUT32}	V_{OUT}=0V	-	22	pF

Note : These parameters are calculated, not measured.

DC Electrical Characteristics (T_A=-55°C to +125°C, V_{CC}=5V ± 10%)

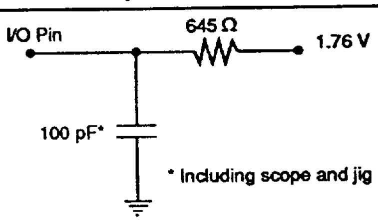
Parameter		Symbol	Test Condition	min	typ[2]	max	Unit
I/P Leakage Current	Address, $\overline{OE}$	I_{LI1}	V_{IN}=0V to V_{CC}, V_{PP}=V_{PPL} or V_{PPH}	-	-	8	µA
	$\overline{WE1-4}$, $\overline{CS1-4}$	I_{LI2}	As above	-	-	2	µA
Output Leakage Current	32 bit	I_{LO}	V_{OUT}=0V to V_{CC}, V_{PP}=V_{PPL} or V_{PPH}, 8 bit	-	-	2	µA
V_{PP} Current		I_{PP1}	V_{PP}=5.5V	-	-	2	mA
		I_{PP2}	V_{PP}=12.6V	-	-	4	mA
V_{CC} Read Current	32 bit	I_{CCR132}	$\overline{CS}$=V_{IL}(1), $\overline{OE}$=V_{IH}, I_{OUT}=0mA, f=1MHz	-	24	80	mA
	16 bit	I_{CCR116}	As above	-	14	46	mA
	8 bit	I_{CCR18}	As above	-	9	29	mA
	32 bit	I_{CCR832}	$\overline{CS}$=V_{IL}(1), $\overline{OE}$=V_{IH}, I_{OUT}=0mA, f=6.67MHz	-	100	240	mA
	16 bit	I_{CCR816}	As above	-	52	126	mA
	8 bit	I_{CCR88}	As above	-	28	69	mA
V_{CC} Write/Erase Current	32 bit	I_{CCE32}	$\overline{CS}$=V_{IL}(1), V_{PP}=V_{PPH}, Write/Erase in progress	-	20	80	mA
	16 bit	I_{CCE16}	As above	-	12	46	mA
	8 bit	I_{CCE8}	As above	-	8	29	mA
V_{CC} Auto Erase Current	32 bit	I_{CCA32}	$\overline{CS}$=V_{IL}(1), V_{PP}=V_{PPH}, Auto Erase in progress	-	40	200	mA
	16 bit	I_{CCA16}	As above	-	22	106	mA
	8 bit	I_{CCA8}	As above	-	13	59	mA
V_{PP} Write/Erase Current	32 bit	I_{PPE32}	$\overline{CS}$=V_{IL}(1), V_{PP}=V_{PPH}, Write/Erase in progress	-	40	160	mA
	16 bit	I_{PPE16}	As above	-	22	86	mA
	8 bit	I_{PPE8}	As above	-	13	49	mA
V_{PP} Auto Erase Current	32 bit	I_{PPA32}	$\overline{CS}$=V_{IL}(1), V_{PP}=V_{PPH}, Auto Erase in progress	-	140	400	mA
	16 bit	I_{PPA16}	As above	-	72	206	mA
	8 bit	I_{PPA8}	As above	-	38	109	mA
Standby Supply Current	TTL	I_{SB1}	V_{CC}=V_{CC} max, $\overline{CS}$=V_{IH}(1)	-	-	3	mA
	CMOS	I_{SB2}	V_{CC}=V_{CC} max, $\overline{CS}$=V_{CC}(1)	-	-	500	µA
Output Low Voltage		V_{OL}	I_{OL}=2.1mA.	-	-	0.45	V
Output High Voltage	TTL loading	V_{OH}	I_{OH}=-400µA.	2.4	-	-	V

Notes (1) $\overline{CS}$ above are accessed through $\overline{CS1-4}$. These inputs must be operated simultaneously for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.
(2) Typical figures are measured at 25°C and nominal V_{CC}
(3) Maximum active current is the sum of I_{CC} and I_{PP}.
(4) **CAUTION:** the PUMA 67F4000 must not be removed from or inserted into a socket when V_{CC} or V_{PP} is applied.

AC Test Conditions

* Input pulse levels: 0.45V to 2.4V.
* Input rise and fall times: ≤ 10ns.
* Input and Output timing reference levels: 1.5V
* Output load : see diagram.
* Module is tested in 32 bit mode.

Output Load

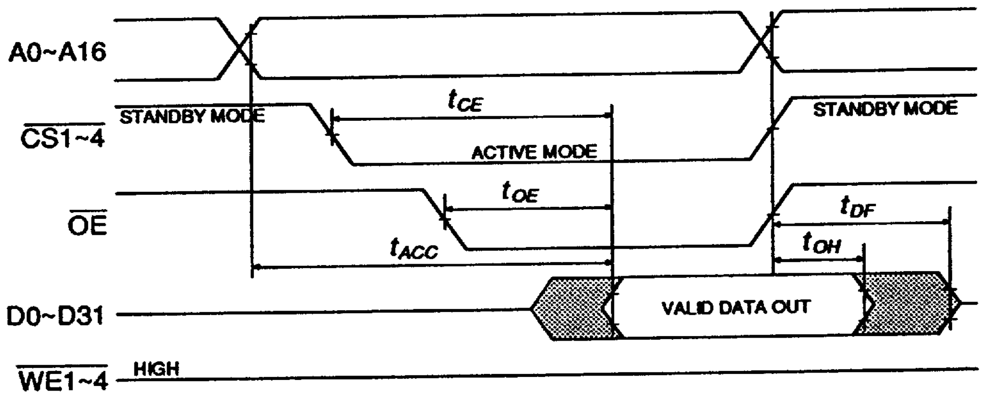


AC Read Characteristics

Parameter	Symbol	-15 min	-15 max	-20 min	-20 max	-25 min	-25 max	Unit
Chip Select Access Time	t_{CS}	-	150	-	200	-	250	ns
Address Access Time	t_{ACC}	-	150	-	200	-	250	ns
Output Enable Access Time	t_{OE}	-	70	-	80	-	90	ns
Output Disable to Output in High Z (1)	t_{DF}	0	50	0	60	0	70	ns
Output Hold Time	t_{OH}	5	-	5	-	5	-	ns

Notes: (1) t_{DF} is defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. This parameter is not 100% tested.

Read Cycle Timing Waveform

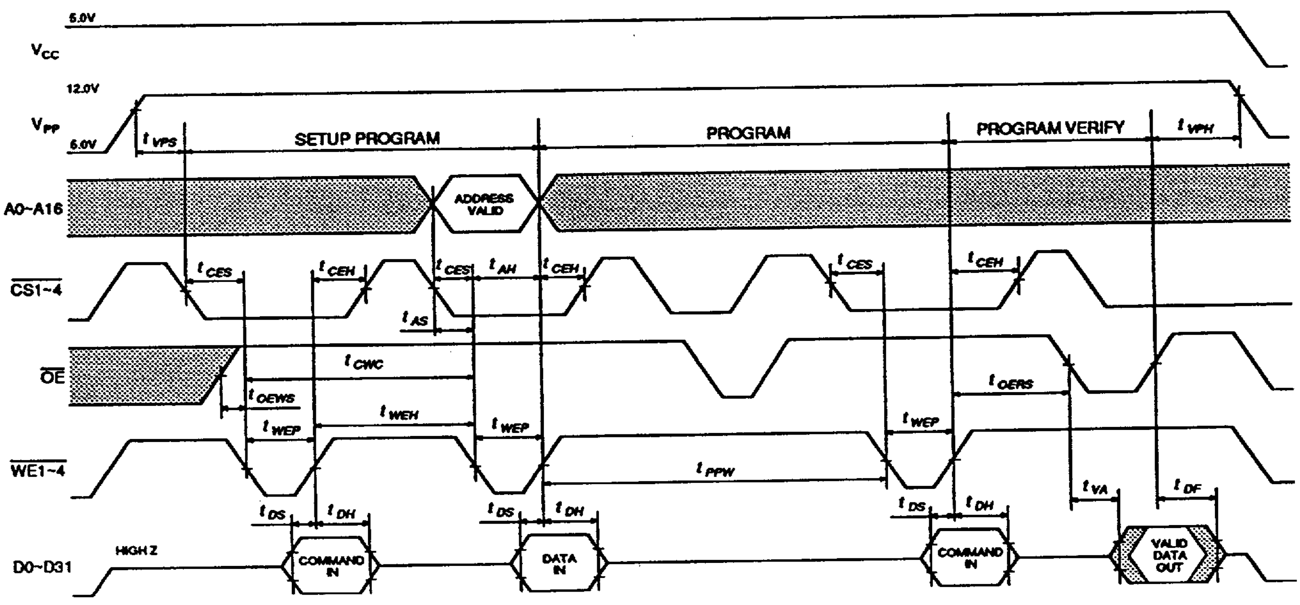


AC Write/Erase/Program Characteristics (V_{CC} = 5V ± 10%)

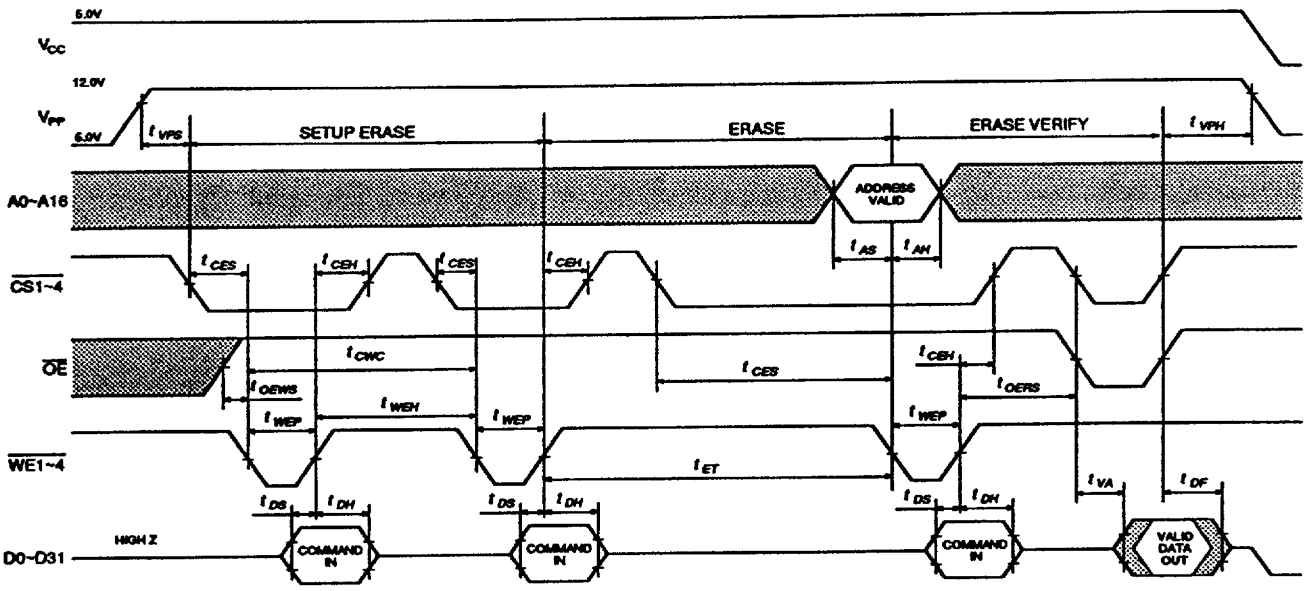
Parameter	Symbol	-15 min	-15 max	-20 min	-20 max	-25 min	-25 max	Unit
Command Programming Cycle Time	t_{CWC}	150	-	200	-	250	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Address Hold Time	t_{AH}	60	-	60	-	60	-	ns
Data Setup Time	t_{DS}	50	-	50	-	50	-	ns
Data Hold Time	t_{DH}	10	-	10	-	10	-	ns
Chip Select Setup Time	t_{CES}	0	-	0	-	0	-	ns
Chip Select Hold Time	t_{CEH}	0	-	0	-	0	-	ns
V_{PP} Setup Time	t_{VPS}	100	-	100	-	100	-	ns
V_{PP} Hold Time	t_{VPH}	100	-	100	-	100	-	ns
Write Programming Pulse Width	t_{WEP}	90	-	90	-	90	-	ns
Write Programming Pulse Width High	t_{WEH}	20	-	20	-	20	-	ns
Output Enable Setup Before Command	t_{OEWS}	0	-	0	-	0	-	ns
Output Enable Setup before Verify	t_{OERS}	6	-	6	-	6	-	µs
Verify Access Time	t_{VA}	-	150	-	200	-	250	ns
Output Enable Setup before Status Polling	t_{OEPS}	20	-	20	-	20	-	ns
Status Polling Access Time	t_{SPA}	-	150	-	200	-	250	ns
Standby Time before Programming	t_{PPW}	25	-	25	-	25	-	µs
Standby Time in Erase	t_{ET}	9	11	9	11	9	11	ms
Output Disable Time (3)	t_{DF}	0	50	0	60	0	70	ns
Automatic Erase Time	t_{AET}	0.5	30	0.5	30	0.5	30	s

Notes (1) $\overline{CS1\text{-}4}$, $\overline{OE}$ and $\overline{WE1\text{-}4}$ must be fixed High during V_{PP} transition from V_{PPL} to V_{PPH} or from V_{PPH} to V_{PPL}.
(2) Refer to Read Operation when V_{PP}=V_{PPL}.
(3) t_{DF} is defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. This parameter is not 100% tested.

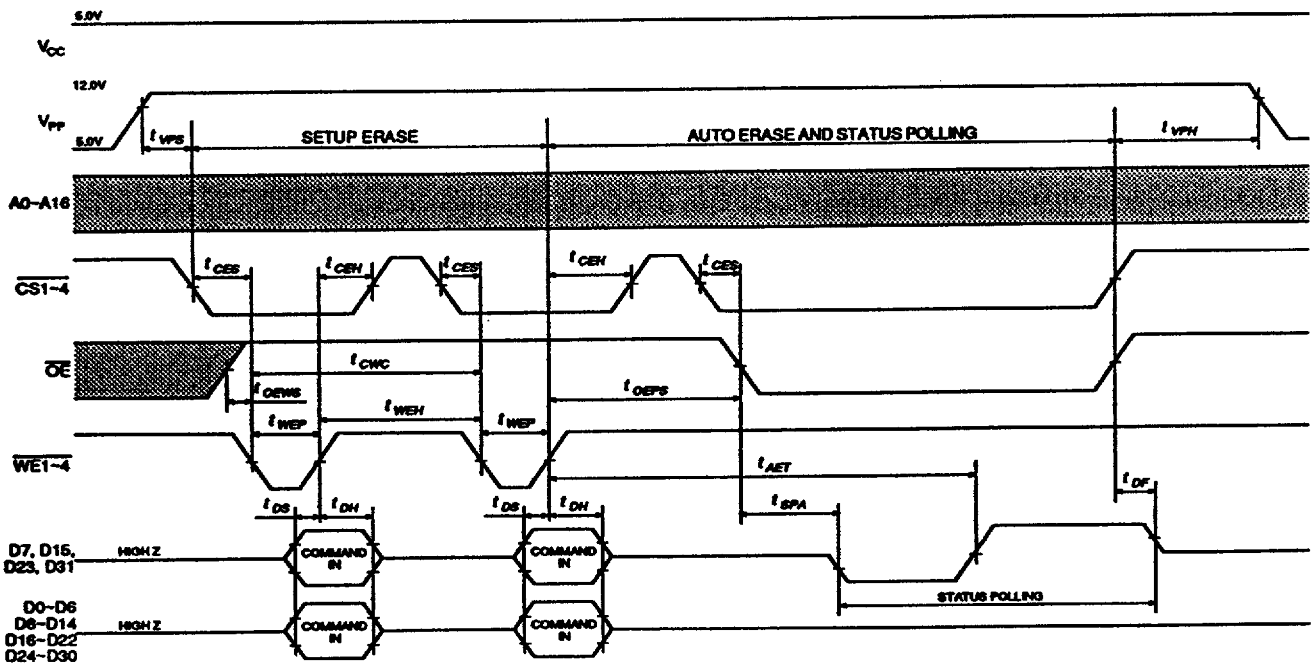
Programming Timing Waveform



Erase Timing Waveform



Automatic Erase Timing Waveform



BUS OPERATIONS

Read Two control functions are provided, both of which must be logically active to obtain data at the outputs. Chip Select selects the module and controls the power, while Output Enable gates data from the output pins - see the Read Cycle Timing Waveform for details.

Write Module Write/Erasure are accessed via the command register while V_{PP} is at V_{PPH}. Note that the register itself does not occupy an addressable memory location, but is simply a latch used to store the command and address/data information required to execute the command.

With Chip Select and Write Enable at V_{IL} the command registers are accessed; addresses are latched on the falling edge of Write Enable and data latched on the rising edge of Write Enable. The three most significant bits of each register (D7- D5) encode the command function while the other bits (D4-D0) must be zero. The exception to this is the Reset command when data FF_H is written to the registers and Identifier mode when 90_H is written to the registers.

Output Disable When Output Enable is at V_{IH} the output pins are placed in a high impedance state and output from the module is disabled.

Standby If Chip Select is held at V_{IH} the power consumption of the PUMA 2F4000 is substantially reduced because most of the on-board circuitry is disabled. The outputs are placed in a high impedance state (independent of Output Enable).

If the PUMA 2F4000 module is deselected and placed in Standby mode during Write/Erase and Verify cycles, the module will continue to draw normal active current until the operation is terminated.

PUMA 2F4000 Operating Modes

OPERATION		*Vpp*	*A0*	*A9*	*$\overline{CS}$*	*$\overline{OE}$*	*$\overline{WE}$*	*D0 - D7*
READ ONLY	Read	V_{PPL}	A0	A9	V_{IL}	V_{IL}	V_{IH}	Data out
	Output Disable	V_{PPL}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby	V_{PPL}	X	X	V_{IH}	X	X	Tri-State
	Manufacturer Identifier[(1)]	V_{PPL}	V_{IL}	V_{ID}[(2)]	V_{IL}	V_{IL}	V_{IH}	Data = 07_H
	Device Identifier[(1)]	V_{PPL}	V_{IH}	V_{ID}[(2)]	V_{IL}	V_{IL}	V_{IH}	Data = 19_H
READ/WRITE	Read[(3)]	V_{PPH}	A0	A9	V_{IL}	V_{IL}	V_{IH}	Data Out[(5)]
	Output Disable	V_{PPH}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby	V_{PPH}	X	X	V_{IH}	X	X	Tri-State
	Write	V_{PPH}	A0	A9	V_{IL}	V_{IH}	V_{IL}	Data In[(4)]

Notes (1) Device Identifier codes can be output in command programming mode. Refer to the Command Definition Table.

(2) $11.4V \leq V_{ID} \leq 12.6V$

(3) Read operations with $V_{PP}=V_{PPH}$ may access array data or identifier codes.

(4) Refer to Command Definition table for valid Data In during a Write operation. Data is Programmed, Erased or Verified after mode setting by command inputs.

(5) Status of AutoErase can be verified in this mode. Status output appears on D7, with D0-D6 in the high impedance state.

(6) X can be V_{IL} or V_{IH}.

(7) If V_{PP} is lowered from 12V to 5V in Erase or Program operation, the erasure or programming will stop.

(8) V_{CC} must be applied before V_{PP} and removed after V_{PP} is removed.

COMMAND DEFINITIONS

With the V_{PP} pin at a low voltage the Command Register contents default to 00_H, enabling Read-only operations. A high voltage on V_{PP} enables Read/Write modes with device operation selected by writing data into the Register - see the Command Definition table for details.

Read While V_{PP} is high the memory contents can be Read by first writing 00_H into the Command Register and thereafter obeying the timings shown on the Read Cycle Waveform. This mode remains enabled until the Command Register contents are altered.

On power up the Register contents will be 00_H, ensuring that the memory contents are not changed during the V_{PP}/V_{CC} power transition. When reading the PUMA67F4000, V_{PP} must be set within V_{SS} to V_{CC} (except during a Command Read).

Intelligent Identifier In order to use the correct programming and erase algorithms on PROM devices, these parts usually have built in codes to identify manufacturer and specific device. However, to access these codes address line A9 normally has to be placed at a high voltage, which is not considered good practice and leads to complications in PCB design.

The PUMA 2F4000 allows the identifiers to be accessed through the Command Register without placing a high voltage on A9. Writing 90_H into the Registers starts this process with a subsequent Read from 00000_H retrieving the manufacturer codes of 07_H and a Read from 00001_H giving the device codes 19_H. To terminate this sequence another valid command must be written to the Register.

PUMA 2F4000 Command Definitions

COMMAND	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Operation (1)	*Addr* (2)	*Data* (3)	*Operation* (1)	*Addr* (2)	*Data* (3)
Read Memory(4)	1	Write	X	00_H	Read	RA	RD
Read Identifier Codes	2	Write	X	90_H	Read	IA	ID
Set-up Erase/Erase(5)	2	Write	X	20_H	Write	X	20_H
Erase Verify (5)	2	Write	EA	$A0_H$	Read	X	EVD
Set-up AutoErase/AutoErase(6)	2	Write	X	30_H	Write	X	30_H
Set-up Program/Program(7)	2	Write	X	40_H	Write	PA	PD
Program Verify (7)	2	Write	X	$C0_H$	Read	X	PVD
Reset	2	Write	X	FF_H	Write	X	FF_H

Notes (1) See Operating Modes Table.

(2) IA = Identifier address. 00000_H for Manufacturers code and 00001_H for device code.
EA = Address of memory location to be read during Erase Verify.
PA = Address of memory location to be programmed.
RA = Address of memory location to be Read.
Addresses are latched on the falling edge of Write Enable pulse.

(3) ID = Data read from location IA during device identification. (Manufacturer = 07_H, Device = 19_H)
EVD = Data read from location EA during Erase Verify.
PD = Data to be programmed at location PA. Data is latched on the rising edge of Write Enable.
RD = Data to be read from location RA during Read operation.
PVD = Data to be read from location PA during Program Verify. PA is latched on the Program command.

(4) Command latch default value when applying 12.0V to V_{PP} is 00_H. Device is in Read mode after VP_P is set to 12.0V.

(5) All data in the chip is erased. Erasure occurs according to the fast High Reliability Erase Flowchart

(6) All data in the chip is erased. The data is erased automatically by the internal logic circuitry, with external verification of the erase not required. Termination of erasure is verified by Status Polling after AutoErase begins.

(7) Data is programmed according to the Fast High Reliability Programming Flowchart. The completion of programming after the program pulse must be verified by Status Polling once programming has begun.

Set-up Program/Program Set-up program is a command only operation which prepares the memories for byte programming, initiated by writing 40_H into the command register.

Once Set-up program has been performed, the next Write Enable pulse causes data to be latched on the rising edge and the address is latched on the falling edge of this pulse. Internal programming begins on the rising edge and is terminated with the next rising edge of Write Enable used to write the program-verify command.

Program-Verify This module is programmed byte by byte, which can occur sequentially or at random, but the byte just written must be verified.

Writing $C0_H$ to the command registers begins this operation, which also terminates the programming operation. The last byte written will be verified; no new address information is required as the previous address is latched. A Read Cycle can now be performed in order to compare the data just written with the byte contents. This process is shown by the Programming Algorithm.

Set-up Erase/Erase Set-up erase is a command only operation which prepares the memory for electrical erasure of all contents, initiated by writing 20_H to the Command Registers.

In order to start erasure 20_H must again be written to the registers; this two-step sequence ensures that accidental erasure will not occur. Additionally, if the V_{PP} pin is not at a high voltage the memory contents are protected against erasure.

Erase-Verify The Erase command erases all the contents of the memory, but after this operation all bytes must be verified. This is accomplished by writing $A0_H$ to the Command Registers, with the address of the byte to be verified supplied as it is latched on the falling edge of the Write-Enable pulse. Reading FF_H from the addressed bytes indicates that they are erased. This command must be issued prior to each byte verification to latch its address.

If the data read is not FF_H another erase operation must be performed. Verification can then continue from the address of the last verified byte, and once all bytes have been verified the erase procedure is complete. This process is shown by the Erase algorithm.

The verify operation is halted by writing another valid command e.g. Set-up Program, into the command register.

Automatic Erase The Erase and Erase Verify processes can be performed automatically by writing 30_H into the Command register, followed by a second write of 30_H to initiate the AutoErase. Once initiated all of the locations in the PUMA 2F4000 will be set to FF_H automatically, without the need to verify each byte. Typically the whole device will be erased in 1 second, with the end of erasure being indicated by Status Polling.

Status Polling Status Polling allows the status of the FLASH memory to be determined. If the PUMA 2F4000 is set to the Status Polling mode during the Erase Cycle, D7 is lowered to V_{OL} to indicate that the PUMA 2F4000 is performing an Erase operation. When the Erase has terminated, D7 is set to V_{OH}. During Status Polling only D7 outputs data. D0 to D6 are in high impedance state (High Z). The Status Polling feature is only active during the automatic erase algorithm.

Reset This command, which consists of two consecutive writes of FF_H, will safely abort either Erase or Program operations after the Set-up commands. Memory contents will not be altered, and a valid command must then be written to place the device in the desired state.

ALGORITHM NOTES

These algorithms **MUST BE FOLLOWED** to ensure correct and reliable device operation.

Fast Pulse Programming Algorithm This programming algorithm uses pulses of 25µs duration in order to improve programming time. Each operation is followed by byte verification in order to check when the specified byte has been successfully programmed. The algorithm allows up to 20 such pulses per byte, even though most bytes will verify on the first or second pulse. Both the Write and Verify sequences take place with $V_{PP} = V_{PPH}$. See the Programming Algorithm for a full description.

Fast Erase Algorithm The Fast Erase algorithm uses a closed loop flow similar to that of the Programming Algorithm to reliably and quickly erase all memory contents.

Uniform and reliable erasure is guaranteed by first writing 00_H to all memory locations. This can be accomplished using the Fast Pulse Programming algorithm. Erase execution then proceeds with an initial Erase operation, after which Erase Verification (data = FF_H) begins at address 00_H. This continues through the devices until the last address is reached or any data other than FF_H is found. With each subsequent Erase operation a greater number of bytes will verify to the erased state.

The erase time may be minimized by storing the address of the last byte verified; after the next Erase operation verification can begin at this address, circumventing the need to re-verify previously erased locations. Erasure occurs typically in 1 second.

Timing Delays Four timing delays are associated with the Program and Erase algorithms described:

(1) When V_{PP} first turns on the capacitors on the V_{PP} line cause an RC ramp, the rise time of which is proportional to the number of devices being erased and the capacitance per device. V_{PP} must reach its final value 100ns before any commands are executed.

(2) The second timing delay is the erase time pulse width of 10ms, which should be timed by a microprocessor routine. This operation is terminated by writing the Erase/Verify Command; if this command is not issued the memory cell will be driven into depletion (no internal times).

(3) Each programming operation lasts 25µs, and since the algorithm is interactive each byte is verified after a Write pulse; the program operation must be terminated at the conclusion of the timing routine.

(4) In order to improve memory cell operation, an internally generated margin voltage is applied to the addressed cell during Write/Erase Verify. It is during this 6µs delay that the internal circuitry is changing voltage levels between the Erase/Write level and those used for Verify and Read operations. Any attempt to Read the device(s) during this period will result in possible false data appearing on the outputs.

DESIGN CONSIDERATIONS

Two Line Control Two Read signals are provided for output control to accommodate large memory arrays, giving the lowest possible memory power dissipation and ensuring bus contention does not occur.

Supply Decoupling Flash memory power-switching characteristics require careful decoupling. Three supply current issues have to be considered - Standby, Active and transient current peaks caused by rising and falling edges of Chip Select.

Two line control and correct decoupling capacitor selection will help to suppress these transient voltage peaks. Each PUMA 2F4000 device should have a 0.1µF ceramic capacitor between V_{CC} and GND and between V_{PP} and GND. These high frequency, low inductance capacitors should be placed as close as possible to the PUMA 2F4000.

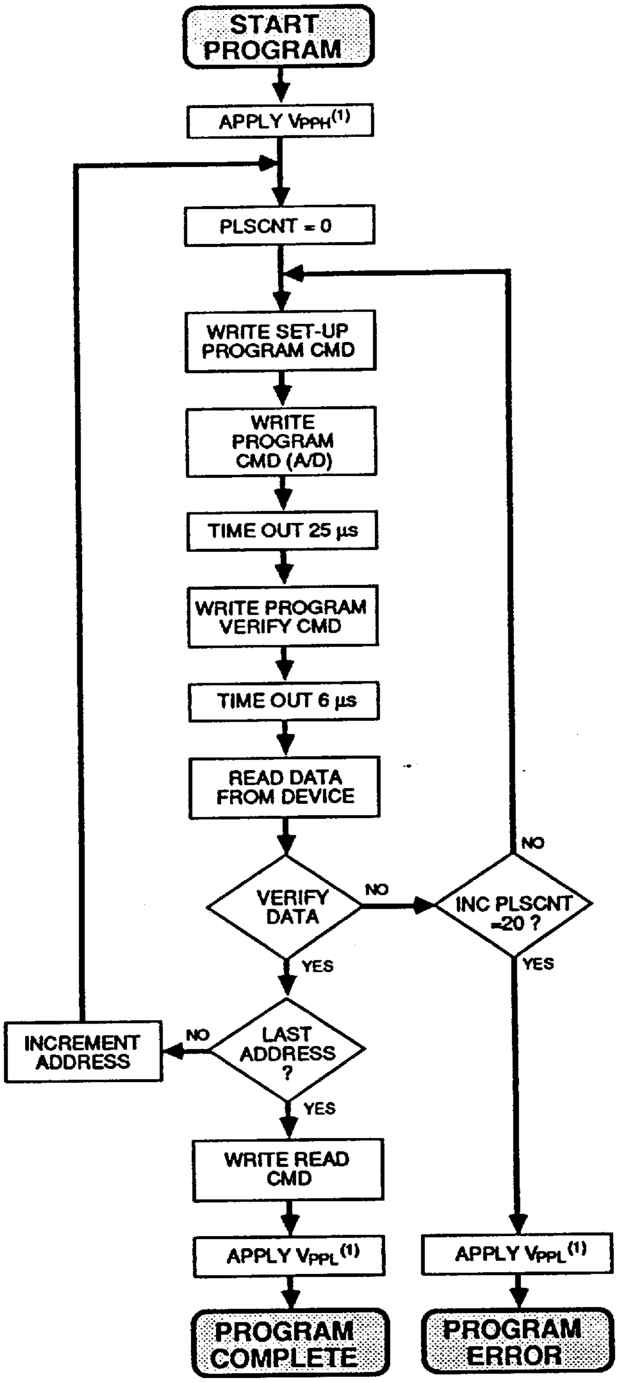
Additionally, it is recommended that a 4.7µF electrolytic capacitor should be placed between V_{CC} and GND every eight PUMA 2F4000 devices. This capacitor will smooth out voltage dips in the supply caused by PCB track inductance and will supply charge to the on-board capacitors as needed.

V_{PP} Trace Because Flash memories are designed to be programmed in situ, the PCB designer must be made aware of the V_{PP} supply trace. This should be made similar to the V_{CC} bus as the V_{PP} pin supplies the memory cell current for Programming and Erase.

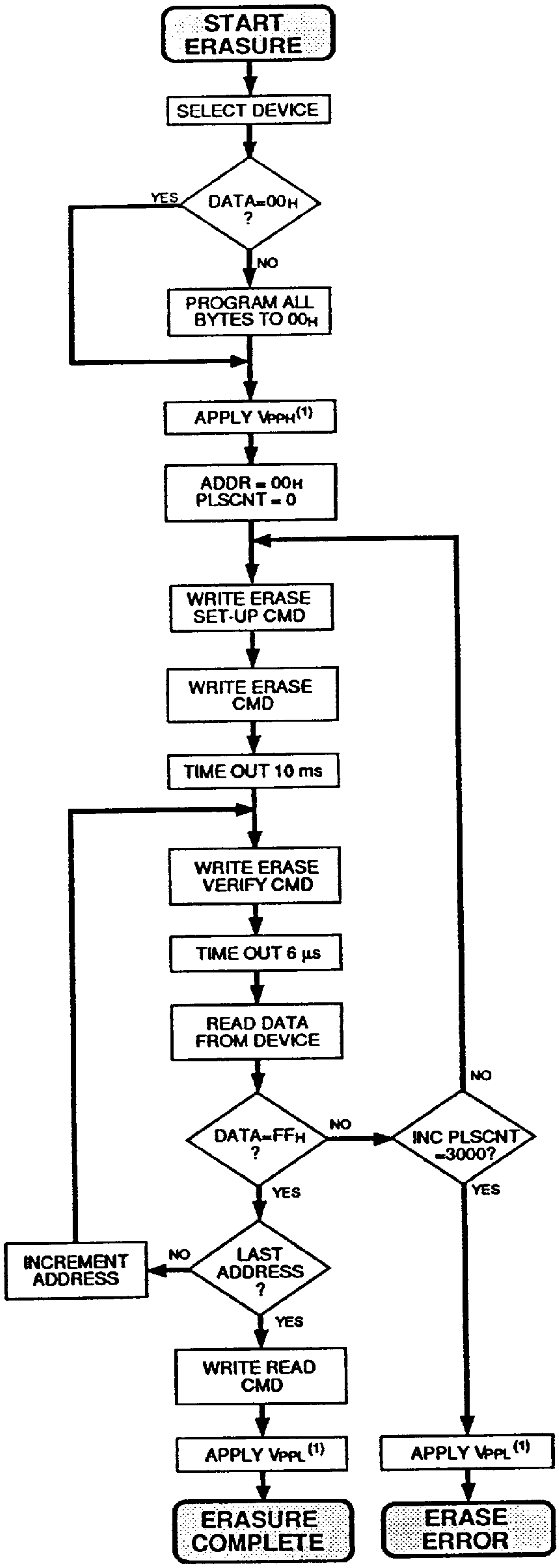
Power Up/Down When lowering V_{PP} to V_{CC} or less, V_{CC} must be set to 5V. V_{CC} must be applied before V_{PP} and removed after V_{PP} is removed.

PROGRAMMING ALGORITHM

These algorithms **MUST BE FOLLOWED** to ensure proper and reliable operation, and are shown for a single device only.



ERASE ALGORITHM



Notes

(1) See DC Characteristics for the value of V_{PPH}. When V_{PP} is switched, V_{PPL} may be GND, NC with a resistor tied to GND or less than V_{CC}+2.0V

Ordering Information

PUMA 67F4000MB-15

Speed	15	= 150 ns
	20	= 200 ns
	25	= 250 ns
Temp. range/screening	Blank	= Commercial Temperature
	I	= Industrial Temperature
	M	= Military Temperature
	MB	= Processed to MIL-STD 883 Method 5004, non-compliant.
Organization	4000	= 4Mbit array, configurable as 128K x 32 , 256K x 16 or 512K x 8 bit
Technology	F	= FLASH MEMORY

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