NEC

MOS INTEGRATED CIRCUIT

μPD42S4260L, 424260L

4 M-BIT DYNAMIC RAM
256 K-WORD BY 16-BIT, FAST PAGE MODE, BYTE READ/WRITE MODE

DESCRIPTION

The μPD42S4260L, 424260L are 262 144 words by 16 bits dynamic CMOS RAMs with optional fast page mode and byte read/write mode.

High performance CMOS sense amplifier, peripheral circuits and one transistor dynamic memory cell technique realize high speed access and low power consumption.

In addition to this, refresh is accomplished by performing $\overline{CAS}$ before $\overline{RAS}$ self refresh on the μPD42S4260L.

The μPD42S4260L and μPD424260L are packaged in 44-pin plastic TSOP, 40-pin plastic SOJ and 40-pin plastic ZIP.

FEATURES

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- 262 144 words by 16 bits organization
- Fast access and cycle time

Part number	Refresh cycle	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μPD42S4260L-A70	512 cycles/128 ms	432.0 mW	70 ns	130 ns	45 ns
μPD424260L-A70	512 cycles/ 8 ms				
μPD42S4260L-A80	512 cycles/128 ms	396.0 mW	80 ns	150 ns	50 ns
μPD424260L-A80	512 cycles/ 8 ms				
μPD42S4260L-A10	512 cycles/128 ms	360.0 mW	100 ns	180 ns	60 ns
μPD424260L-A10	512 cycles/ 8 ms				

- Low power consumption
  Standby (CMOS level input) ..... 0.36 mW MAX. (μPD42S4260L)
  1.8 mW MAX. (μPD424260L)
- Single +3.3 V ± 0.3 V power supply
- Fast page mode and byte read/write mode capability
- The μPD42S4260L has 4 types of refresh
  ..... $\overline{CAS}$ before $\overline{RAS}$ internal address self refresh, $\overline{RAS}$ only refresh, hidden refresh and $\overline{CAS}$ before $\overline{RAS}$ internal address refresh
- The μPD424260L has 3 types of refresh
  ..... $\overline{RAS}$ only refresh, hidden refresh and $\overline{CAS}$ before $\overline{RAS}$ internal address refresh
- Multiplexed address inputs ..... Row address: A0 to A8, Column address: A0 to A8
- On-chip substrate bias generator

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The mark ★ shows revised points.

★ ORDERING INFORMATION

Part number	Access time (MAX.)	Package	Refresh
μPD42S4260LG5-A70-7JF	70 ns	44-pin Plastic TSOP	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{RAS}$ only refresh $\overline{CAS}$ before $\overline{RAS}$ refresh hidden refresh
μPD42S4260LG5-A80-7JF	80 ns		
μPD42S4260LG5-A10-7JF	100 ns		
μPD42S4260LG5-A70-7KF	70 ns	44-pin Plastic TSOP (Reverse bent)	
μPD42S4260LG5-A80-7KF	80 ns		
μPD42S4260LG5-A10-7KF	100 ns		
μPD42S4260LLE-A70	70 ns	40-pin Plastic SOJ	
μPD42S4260LLE-A80	80 ns		
μPD42S4260LLE-A10	100 ns		
~~μPD42S4260LV-A70~~	70 ns	~~40-pin Plastic ZIP~~	
~~μPD42S4260LV-A80~~	~~80 ns~~		
~~μPD42S4260LV-A10~~	100 ns		
μPD424260LG5-A70-7JF	70 ns	44-pin Plastic TSOP	$\overline{RAS}$ only refresh $\overline{CAS}$ before $\overline{RAS}$ refresh hidden refresh
μPD424260LG5-A80-7JF	80 ns		
μPD424260LG5-A10-7JF	100 ns		
μPD424260LG5-A70-7KF	70 ns	44-pin Plastic TSOP (Reverse bent)	
μPD424260LG5-A80-7KF	80 ns		
μPD424260LG5-A10-7KF	100 ns		
μPD424260LLE-A70	70 ns	40-pin Plastic SOJ	
μPD424260LLE-A80	80 ns		
μPD424260LLE-A10	100 ns		
~~μPD424260LV-A70~~	70 ns	~~40-pin Plastic ZIP~~	
~~μPD424260LV-A80~~	~~80 ns~~		
~~μPD424260LV-A10~~	100 ns		

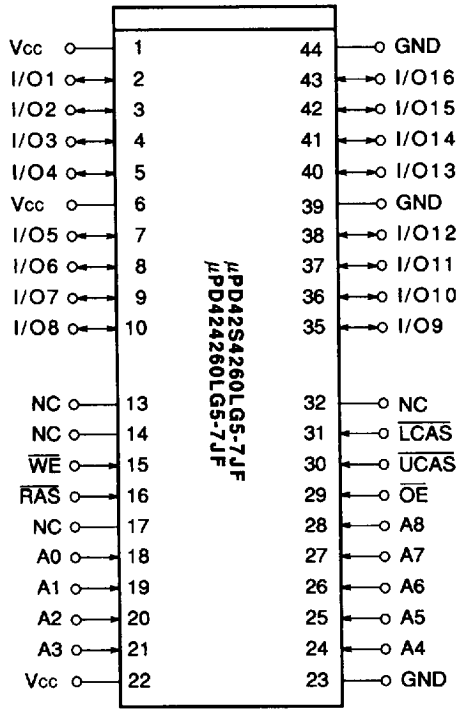
QUALITY GRADE

STANDARD

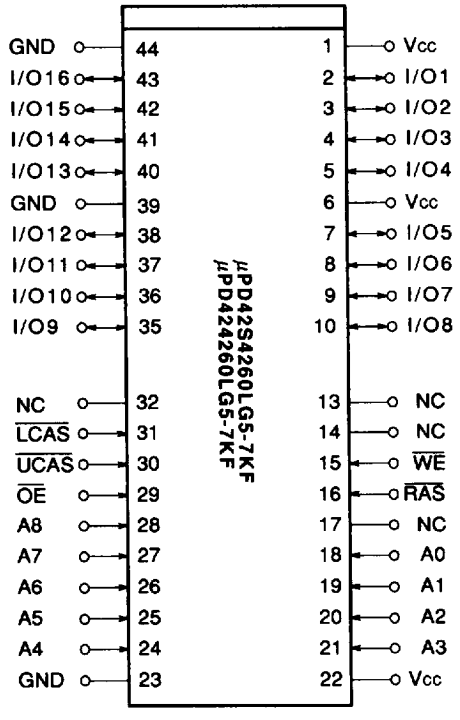
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

PIN CONFIGURATIONS ★

44-pin Plastic TSOP
(Marking Side)

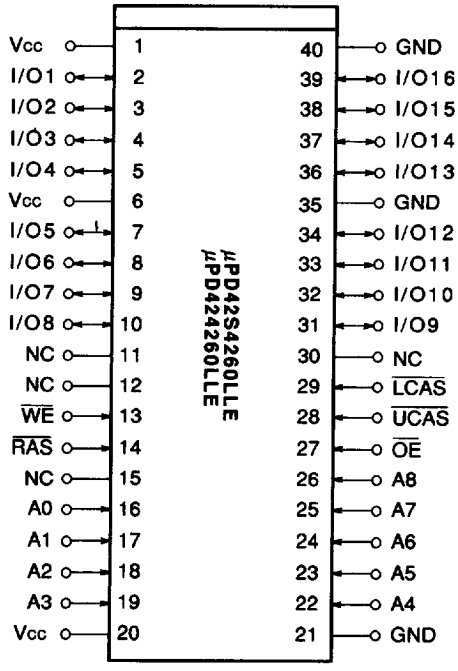


44-pin Plastic TSOP (Reverse bent)
(Marking Side)

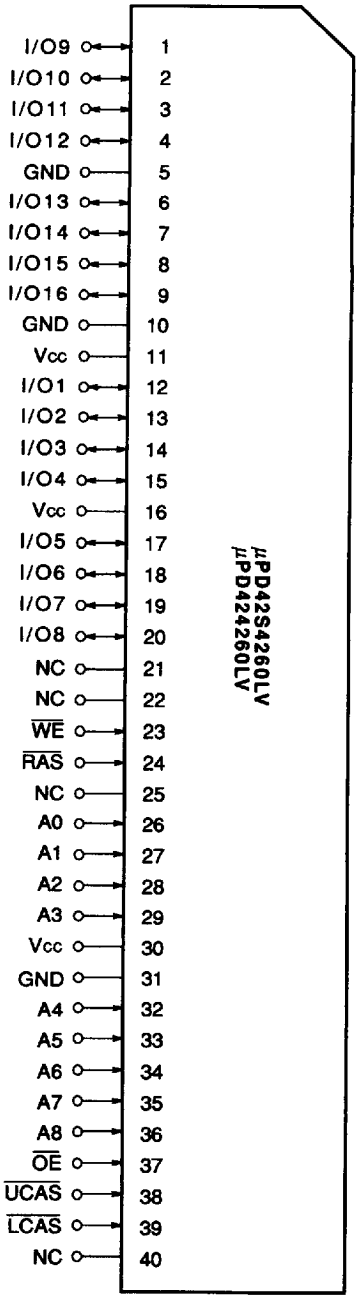


A0 to A8	: Address Inputs
I/O1 to I/O16	: Data Inputs/Outputs
$\overline{RAS}$	: Row Address Strobe
$\overline{UCAS}$	: Column Address Strobe (upper)
$\overline{LCAS}$	: Column Address Strobe (lower)
$\overline{WE}$	: Write Enable
$\overline{OE}$	: Output Enable
Vcc	: Power Supply (+3.3 V ± 0.3 V)
GND	: Ground
NC	: No Connection

40-pin Plastic SOJ
(Top View)



40-pin Plastic ZIP
(Front View)



A0 to A8	: Address Inputs
I/O1 to I/O16	: Data Inputs/Outputs
$\overline{RAS}$	: Row Address Strobe
$\overline{UCAS}$	: Column Address Strobe (upper)
$\overline{LCAS}$	: Column Address Strobe (lower)
$\overline{WE}$	: Write Enable
$\overline{OE}$	: Output Enable
Vcc	: Power Supply (+3.3 V ± 0.3 V)
GND	: Ground
NC	: No Connection

ELECTRICAL SPECIFICATIONS NOTE 1 ★

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	RATING	UNIT
Voltage on Any Pin Relative to GND	V_T		−0.5 to +4.6	V
Supply Voltage	V_{CC}		−0.5 to +4.6	V
Output Current	I_O		20	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		−55 to +125	°C

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS NOTE 2, 3

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
High Level Input Voltage	V_{IH}		2.0		V_{CC} +0.3	V
Low Level Input Voltage	V_{IL}		−0.3		0.8	V
Ambient Temperature	T_a		0		70	°C

CAPACITANCE (T_a = +25 °C, f = 1 MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Capacitance	C_{I1}	A0 to A8			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	pF
Data Input/Output Capacitance	C_D	I/O1 to I/O16			7	pF

★ DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER		SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT	NOTE
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN)}$, I_O = 0 mA	t_{RAC} = 70 ns		120	mA	4, 5
				t_{RAC} = 80 ns		110		
				t_{RAC} = 100 ns		100		
Standby current	μPD42S4260L	I_{CC2}	$V_{IH(MIN)} \leqq \overline{RAS}$, $\overline{CAS}$	I_O = 0 mA		0.5	mA	
			V_{CC}–0.2 V $\leqq \overline{RAS}$, $\overline{CAS}$	I_O = 0 mA		0.1		
	μPD424260L		$V_{IH(MIN)} \leqq \overline{RAS}$, $\overline{CAS}$	I_O = 0 mA		2		
			V_{CC}–0.2 V $\leqq \overline{RAS}$, $\overline{CAS}$	I_O = 0 mA		0.5		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ Cycling, $V_{IH(MIN)} \leqq \overline{CAS}$ $t_{RC} = t_{RC(MIN)}$, I_O = 0 mA	t_{RAC} = 70 ns		120	mA	4, 5
				t_{RAC} = 80 ns		110		
				t_{RAC} = 100 ns		100		
Operating current (Fast page mode)		I_{CC4}	$\overline{RAS} \leqq V_{IL(MAX)}$ $\overline{CAS}$ Cycling, $t_{PC} = t_{PC(MIN)}$, I_O = 0 mA	t_{RAC} = 70 ns		80	mA	4, 5
				t_{RAC} = 80 ns		70		
				t_{RAC} = 100 ns		60		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC6}	$\overline{RAS}$ Cycling, $t_{RC} = t_{RC(MIN)}$, I_O = 0 mA	t_{RAC} = 70 ns		120	mA	4, 5
				t_{RAC} = 80 ns		110		
				t_{RAC} = 100 ns		100		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (512 cycles/128 ms, only for μPD42S4260L)		I_{CC6}	Standby : V_{CC}–0.2 V $\leqq \overline{RAS}$ V_{CC}–0.2 V $\leqq \overline{CAS}$ or $\overline{CAS} \leqq$ 0.2 V $\overline{CAS}$ before $\overline{RAS}$ refresh : 512 cycles/128 ms $\overline{RAS}$, $\overline{CAS}$: 0 V $\leqq V_{IL} \leqq$ 0.2 V V_{CC}–0.2 V $\leqq V_{IH} \leqq V_{IH(MAX)}$ $\overline{OE}$: V_{IH} Address input, $\overline{WE}$: V_{IH} or V_{IL} Output : Don't care	$t_{RAS} \leqq$ 200 ns		100	μA	4, 5
				$t_{RAS} \leqq$ 1 μs		150		
Self refresh current ($\overline{CAS}$ before $\overline{RAS}$ self refresh, only for μPD42S4260L)		I_{CC7}	I_O = 0 mA $\overline{RAS}$, $\overline{CAS}$: 0 V $\leqq V_{IL} \leqq$ 0.2 V V_{CC}–0.2 V $\leqq V_{IH} \leqq V_{IH(MAX)}$			100	μA	
Input leakage current		$I_{I(L)}$	V_I = 0 to 3.3 V all other pins except for testing pin = 0 V		–5	+5	μA	
Output leakage current		$I_{O(L)}$	D_{OUT} is disabled (Hi-Z) V_O = 0 to 3.3 V		–5	+5	μA	
Output high voltage		V_{OH}	I_O = –2.0 mA		2.4		V	
Output low voltage		V_{OL}	I_O = 2.0 mA			0.4	V	

AC CHARACTERISTICS ★

(Recommended Operating Conditions unless otherwise noted) NOTE 6, 7 (1/2)

PARAMETER	SYMBOL	tRAC = 70 ns		tRAC = 80 ns		tRAC = 100 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	tRC	130		150		180		ns	8
Read Modify Write Cycle Time	tRWC	175		200		245		ns	8
Fast Page Mode Cycle Time	tPC	45		50		60		ns	8
Read Modify Write Cycle Time (Fast Page Mode)	tPRWC	90		100		120		ns	8
Access Time from $\overline{RAS}$	tRAC		70		80		100	ns	9, 10
Access Time from $\overline{CAS}$	tCAC		20		20		25	ns	9, 10
Access Time from Column Address	tAA		35		40		50	ns	9, 10
Access Time from $\overline{CAS}$ Precharge	tACP		40		45		55	ns	10
$\overline{CAS}$-Output Data Setup Time	tCLZ	0		0		0		ns	10
Output Buffer Turn-off Delay ($\overline{CAS}$)	tOFF	0	15	0	15	0	20	ns	11
Transition Time (rise and fall)	tT	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	tRP	50		60		70		ns	
$\overline{RAS}$ Pulse Width	tRAS	70	10 000	80	10 000	100	10 000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	tRASP	70	125 000	80	125 000	100	125 000	ns	
$\overline{RAS}$ Hold Time	tRSH	20		20		25		ns	
$\overline{CAS}$ Hold Time	tCSH	70		80		100		ns	
$\overline{CAS}$ Pulse Width	tCAS	20	10 000	20	10 000	25	10 000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	20	50	20	60	25	75	ns	9
$\overline{RAS}$ to Column Address Delay Time	tRAD	15	35	15	40	17	50	ns	9
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	10		10		10		ns	12
$\overline{CAS}$ Precharge Time (Fast Page Mode)	tCP	10		10		10		ns	
Row Address Setup Time	tASR	0		0		0		ns	
Row Address Hold Time	tRAH	10		10		12		ns	
Column Address Setup Time	tASC	0		0		0		ns	
Column Address Hold Time	tCAH	15		15		20		ns	
$\overline{CAS}$ Precharge Time	tCPN	10		10		10		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	tRAL	35		40		50		ns	
Read Command Setup Time	tRCS	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{CAS}$	tRCH	0		0		0		ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	tRRH	0		0		0		ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	tWCH	10		15		20		ns	14
Write Command Pulse Width	tWP	10		15		20		ns	14
Write Command Lead Time Referenced to $\overline{RAS}$	tRWL	20		20		25		ns	
Write Command Lead Time Referenced to $\overline{CAS}$	tCWL	15		15		20		ns	
Data-in Setup Time	tDS	0		0		0		ns	15
Data-in Hold Time	tDH	15		15		20		ns	15

(2/2)

PARAMETER		SYMBOL	tRAC = 70 ns		tRAC = 80 ns		tRAC = 100 ns		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Refresh Time	μPD42S4260L	tREF		128		128		128	ms	17
	μPD424260L			8		8		8	ms	
Write Command Setup Time		tWCS	0		0		0		ns	16
$\overline{CAS}$ to $\overline{WE}$ Delay Time		tCWD	40		45		55		ns	16
$\overline{RAS}$ to $\overline{WE}$ Delay Time		tRWD	90		105		130		ns	16
$\overline{CAS}$ Precharge Delay Time Referenced to $\overline{WE}$ (Fast Page Mode)		tCPWD	60		70		85		ns	16
Column Address Delay Time Referenced to $\overline{WE}$		tAWD	55		65		80		ns	16
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		tCSR	5		5		5		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		tCHR	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time		tRPC	10		10		10		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive Setup Time		tOES	0		0		0		ns	
Access Time from $\overline{OE}$		tOEA		20		20		25	ns	
$\overline{OE}$ Data Delay Time		tOED	15		15		20		ns	
Output Buffer Turn-off Delay ($\overline{OE}$)		tOEZ	0	15	0	15	0	20	ns	11
$\overline{OE}$ Output Data Setup Time		tOLZ	0		0		0		ns	
$\overline{OE}$ Hold Time		tOEH	0		0		0		ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{CAS}$ Precharge		tRHCP	40		45		55		ns	
Masked Write Hold Time referenced to $\overline{RAS}$		tMRH	0		0		0		ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)		tRASS	100		100		100		μs	17
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)		tRPS	130		150		180		ns	17
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)		tCHS	–50		–50		–50		ns	17

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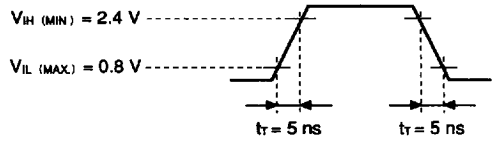
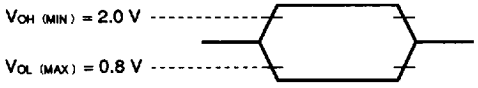
NOTE

1. $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
2. All voltages are referenced to GND.
3. An initial pause of 100 μs is required after power up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal address refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
4. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on t_{RC} and t_{PC}. Specified values are obtained with outputs open.
5. Address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
6. AC measurements assume t_T = 5 ns.
7. AC Characteristics test condition
   (1) Input timing specification



   (2) Output timing specification

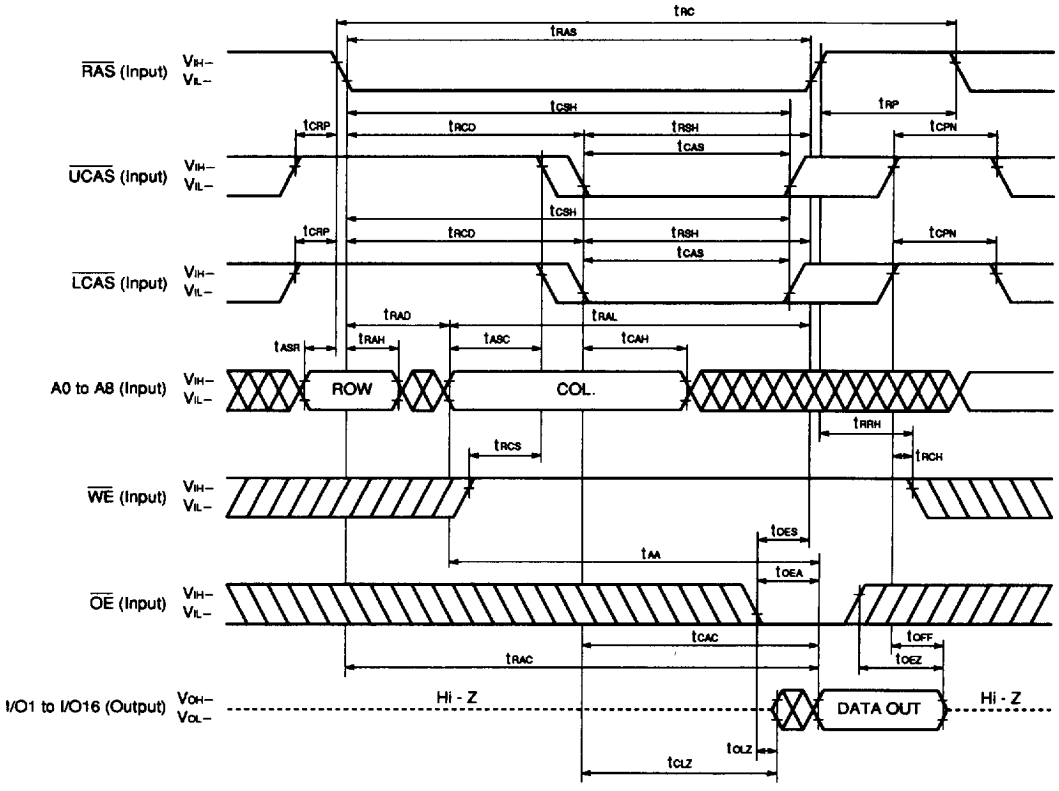


8. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (T_a = 0 to 70 °C) is assured.
9. In random read cycle, the access time is changed by the conditions of t_{RAD} and t_{RCD} as follows.

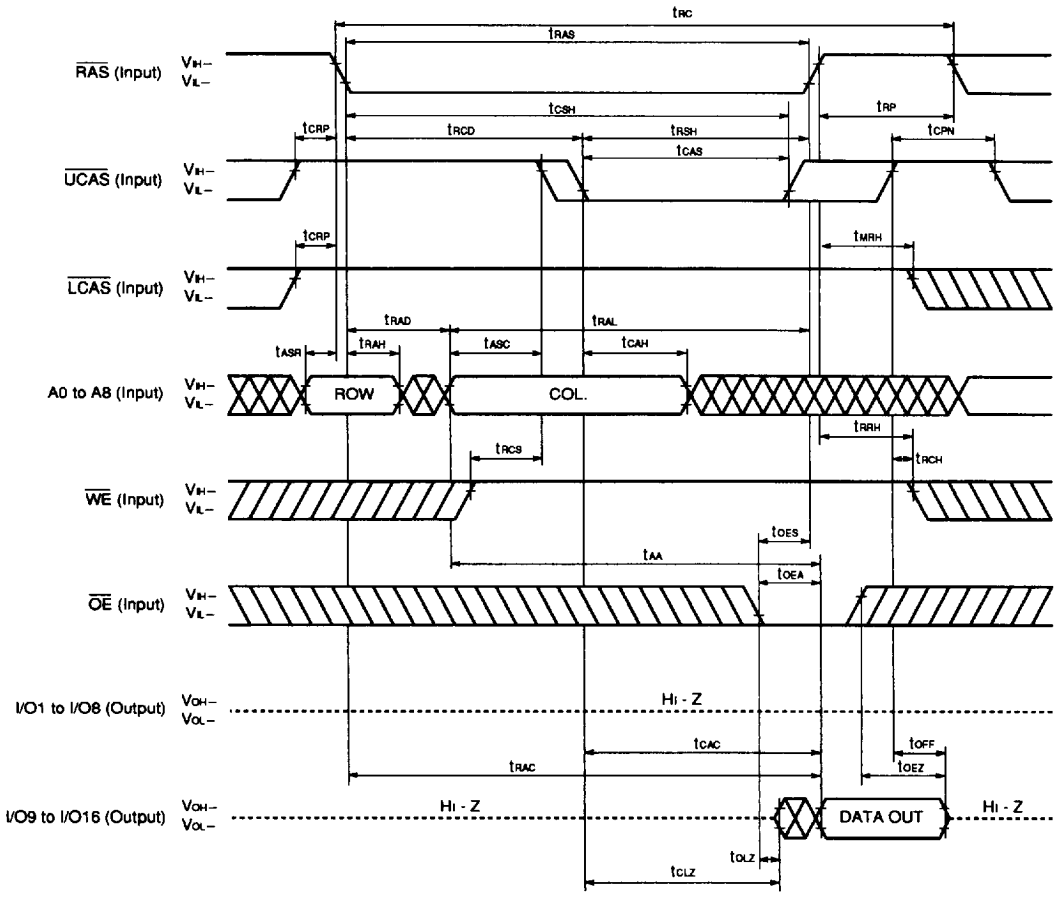
CONDITION	ACCESS TIME
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD\ (MAX.)} \leq t_{RAD}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$
$t_{RCD\ (MAX.)} \leq t_{RCD}$	$t_{CAC\ (MAX.)}$

   $t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ indicate the point which the access time changes and are not the limits of operation.
10. Loading conditions are 1TTL and 100 pF.
11. $t_{OFF\ (MAX.)}$ and $t_{OEZ\ (MAX.)}$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.
12. $t_{CRP\ (MIN.)}$ requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycles.
13. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ must be satisfied for a read cycle.
14. $t_{WP\ (MIN.)}$ is applicable for late write cycle or read modify write cycle. In early write cycles, $t_{WCH\ (MIN.)}$ should be satisfied.
15. This specification is referenced to $\overline{CAS}$ falling edge in early write cycles and to $\overline{WE}$ falling edge in late write or read modify write cycles.
16. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS\ (MIN.)} \leq t_{WCS}$, the cycle is an early write cycle and the data out pins will remain Hi-Z through the entire cycle. If $t_{RWD\ (MIN.)} \leq t_{RWD}$, $t_{CWD\ (MIN.)} \leq t_{CWD}$, $t_{AWD\ (MIN.)} \leq t_{AWD}$, $t_{CPWD\ (MIN.)} \leq t_{CPWD}$, the cycle is a read modify write cycle and condition of the data out (at access time) is indeterminate.
17. This specification is applicable only for μPD42S4260L.

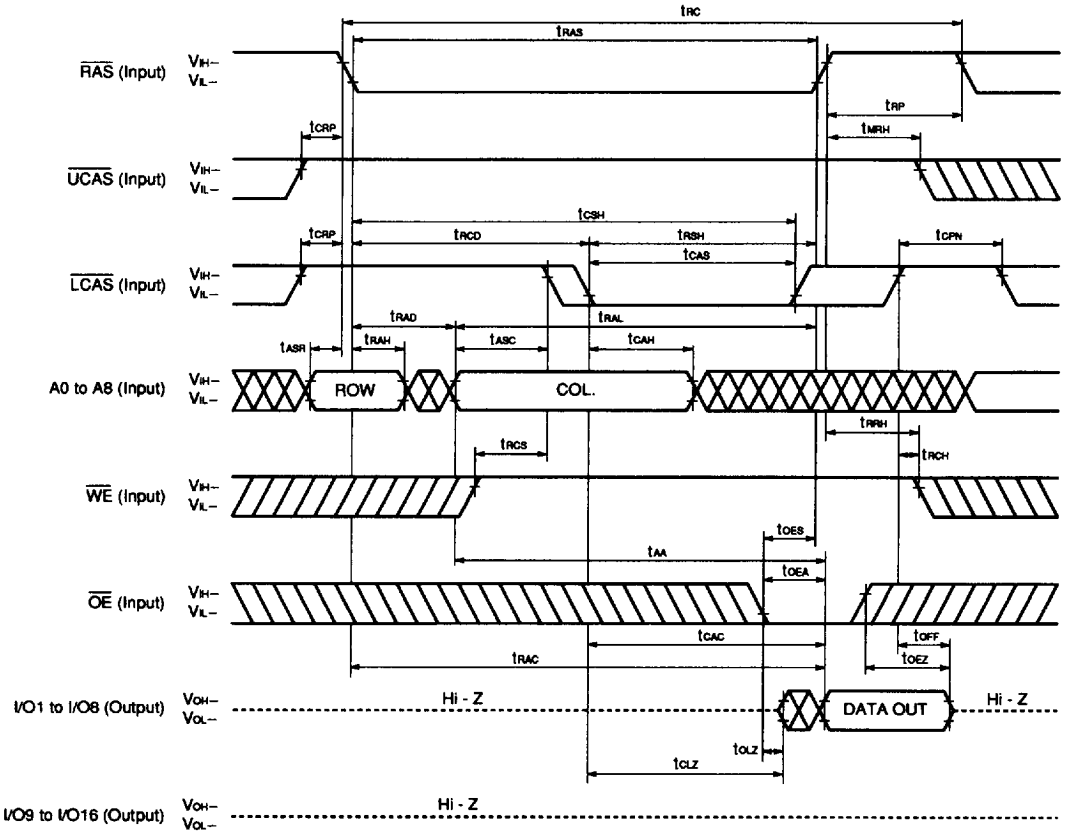
READ CYCLE



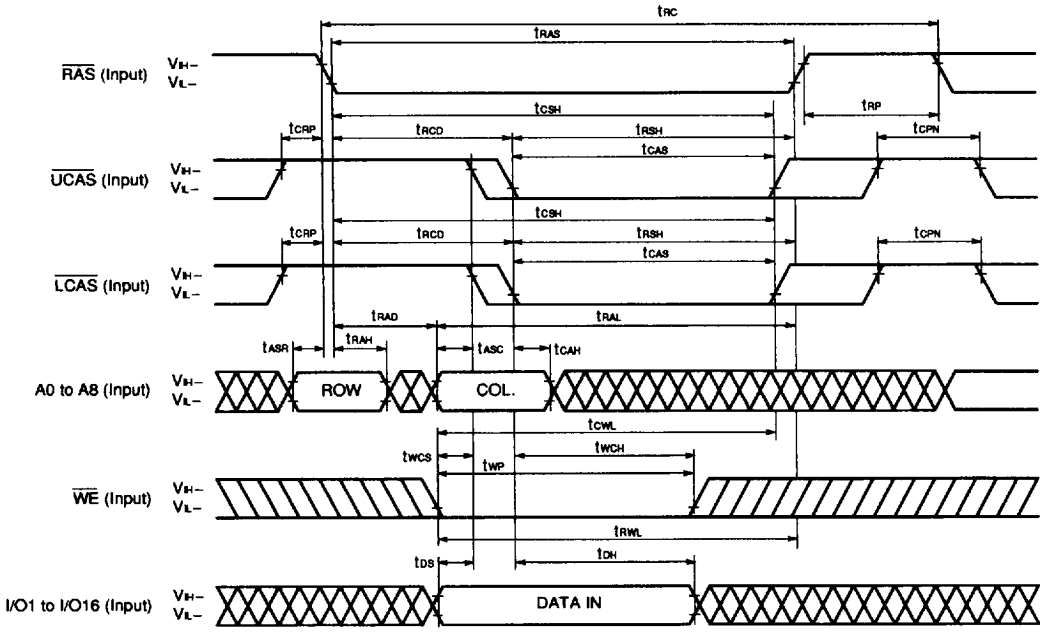
UPPER BYTE READ CYCLE



LOWER BYTE READ CYCLE

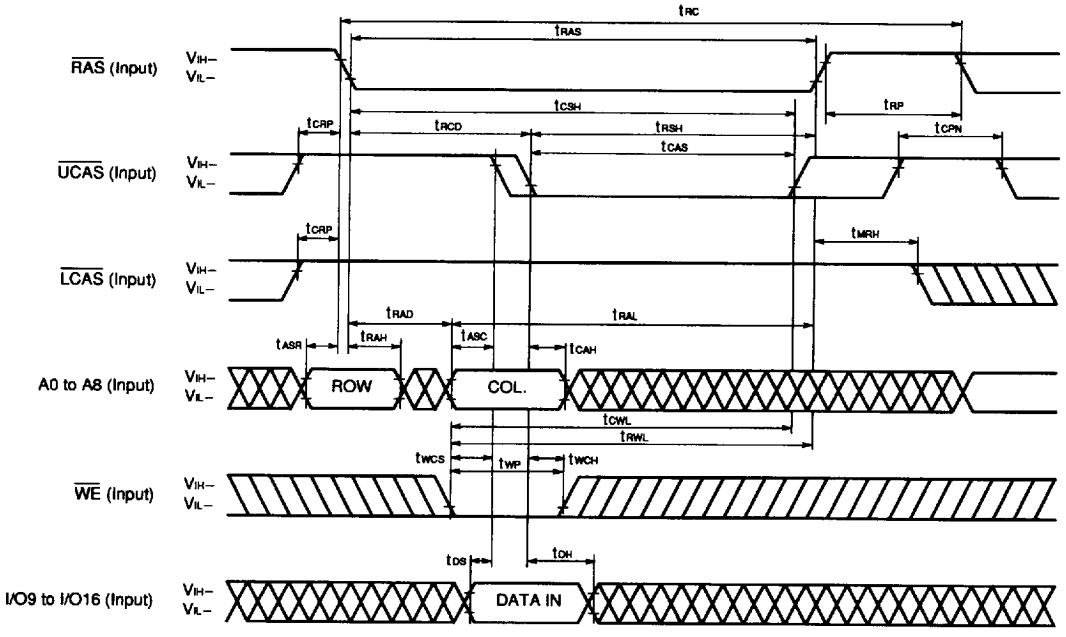


EARLY WRITE CYCLE



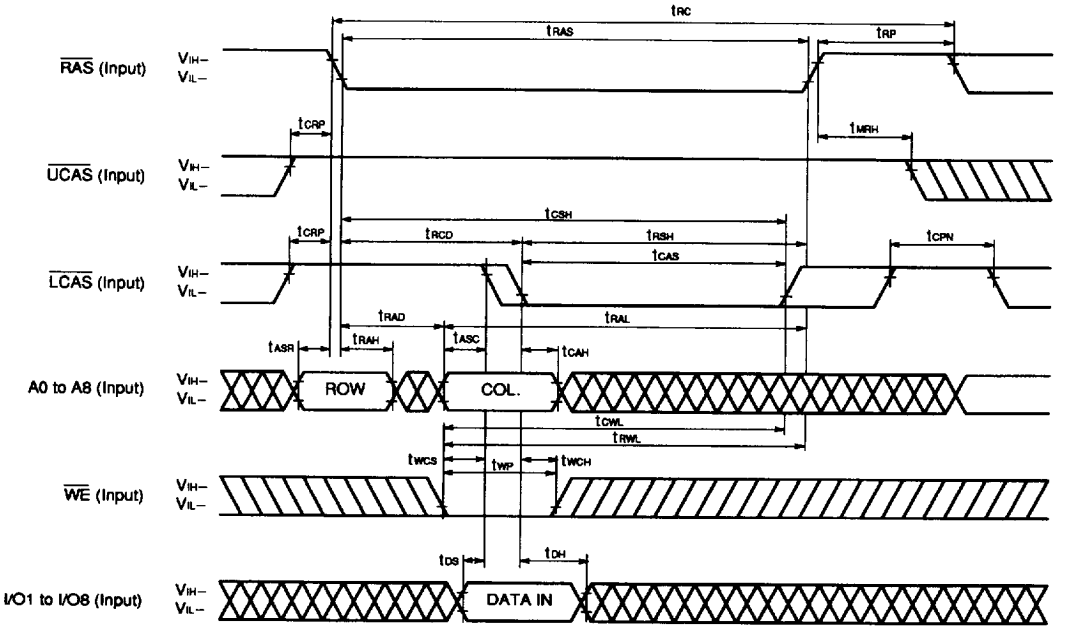
Remark $\overline{OE}$ = Don't care

UPPER BYTE EARLY WRITE CYCLE



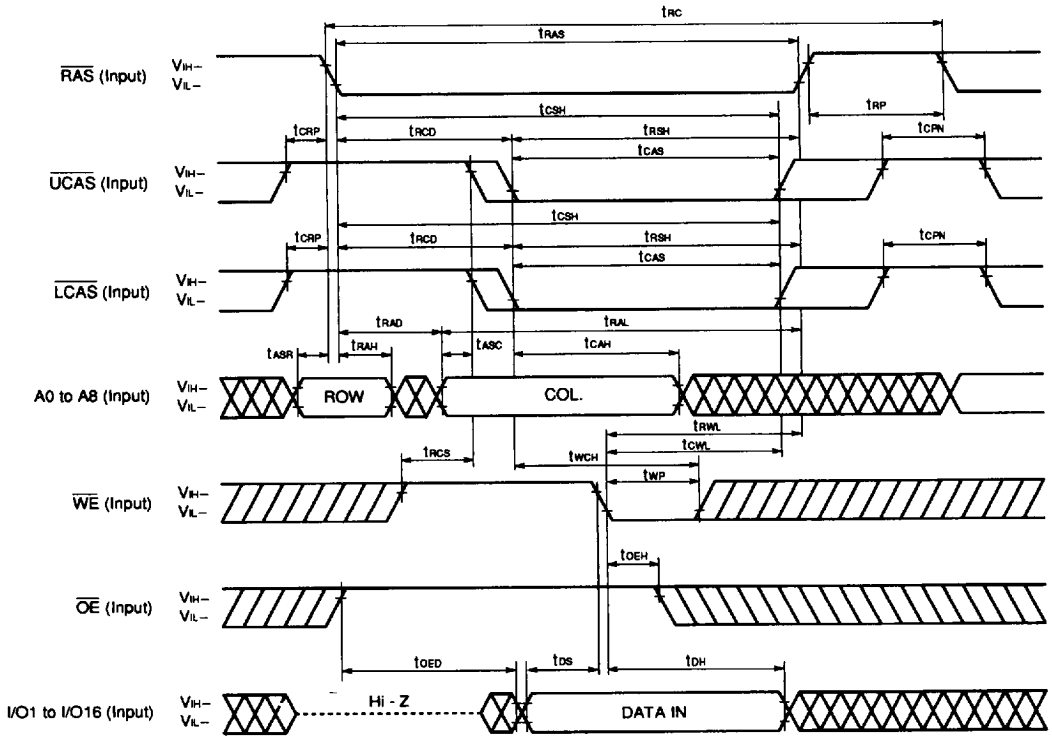
Remark $\overline{OE}$, I/O1 to I/O8 = Don't care

LOWER BYTE EARLY WRITE CYCLE

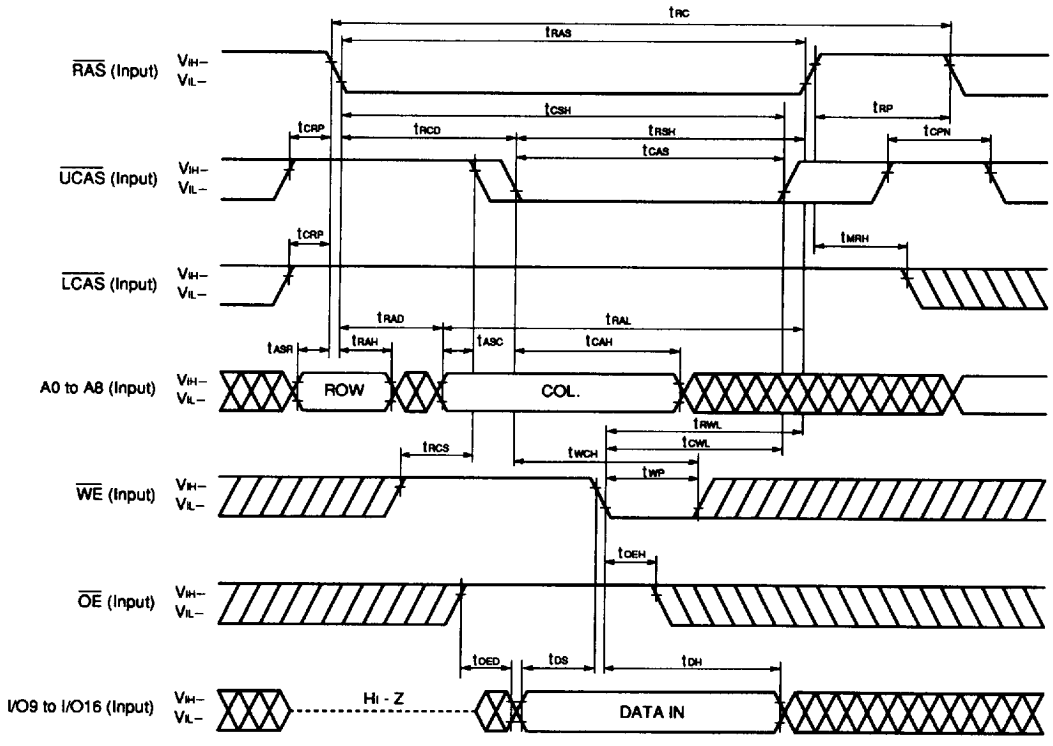


Remark $\overline{OE}$, I/O9 to I/O16 = Don't care

LATE WRITE CYCLE

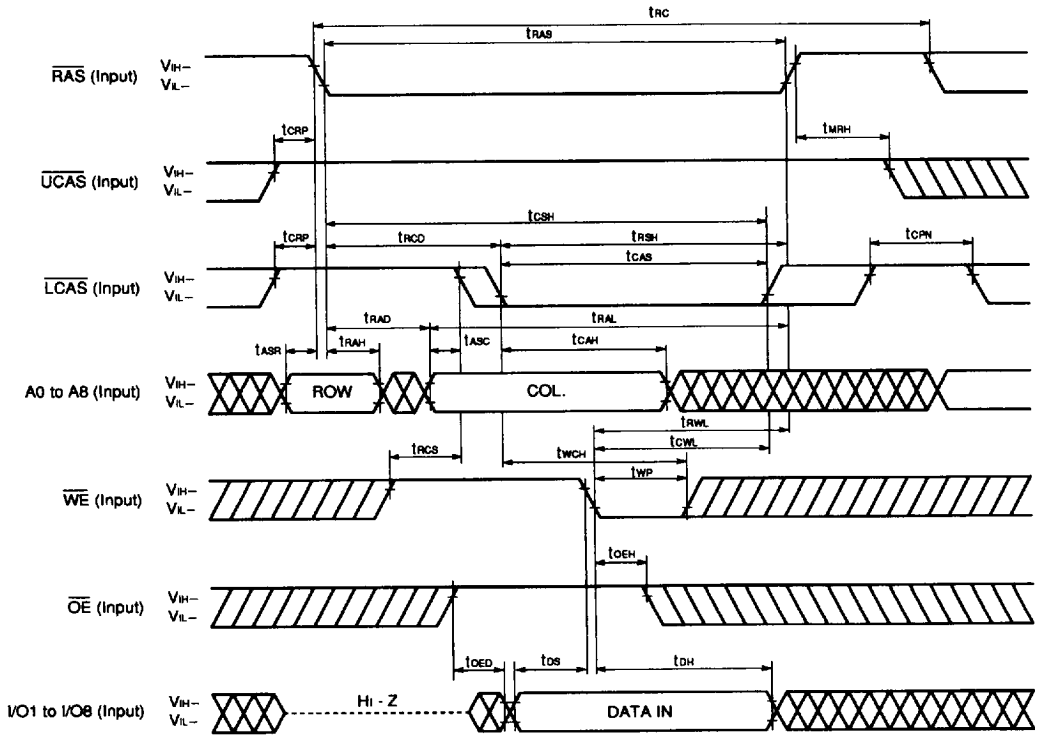


UPPER BYTE LATE WRITE CYCLE



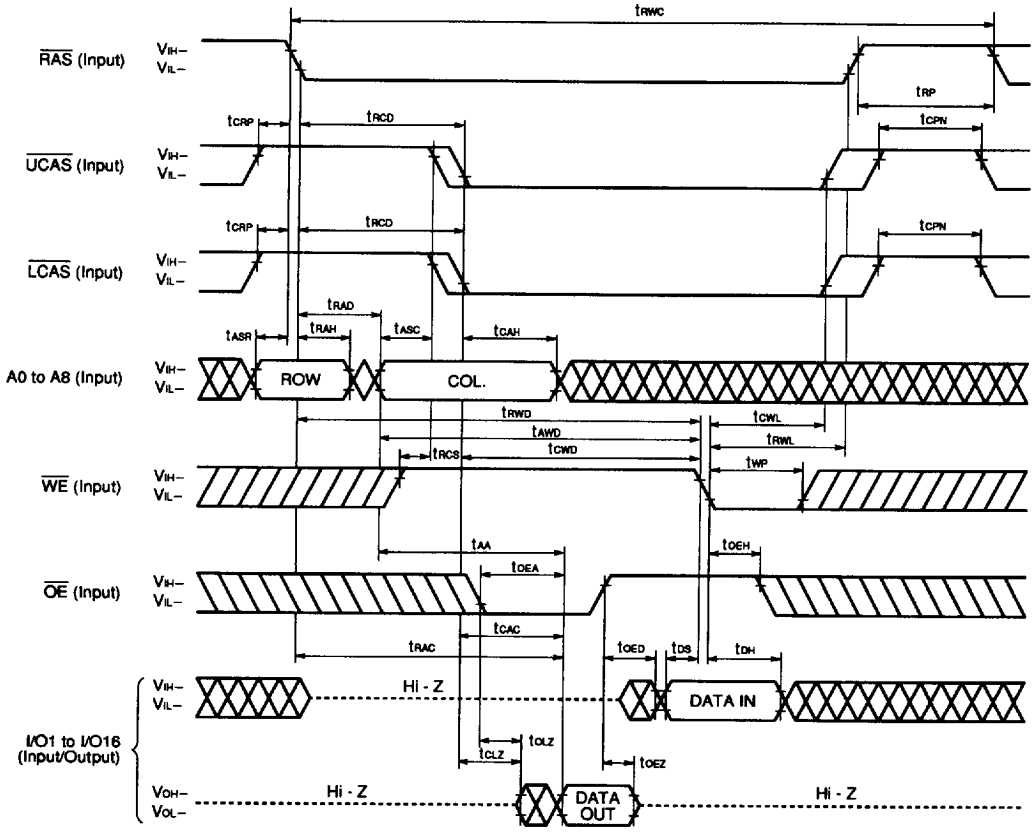
Remark I/O1 to I/O8 = Don't care

LOWER BYTE LATE WRITE CYCLE

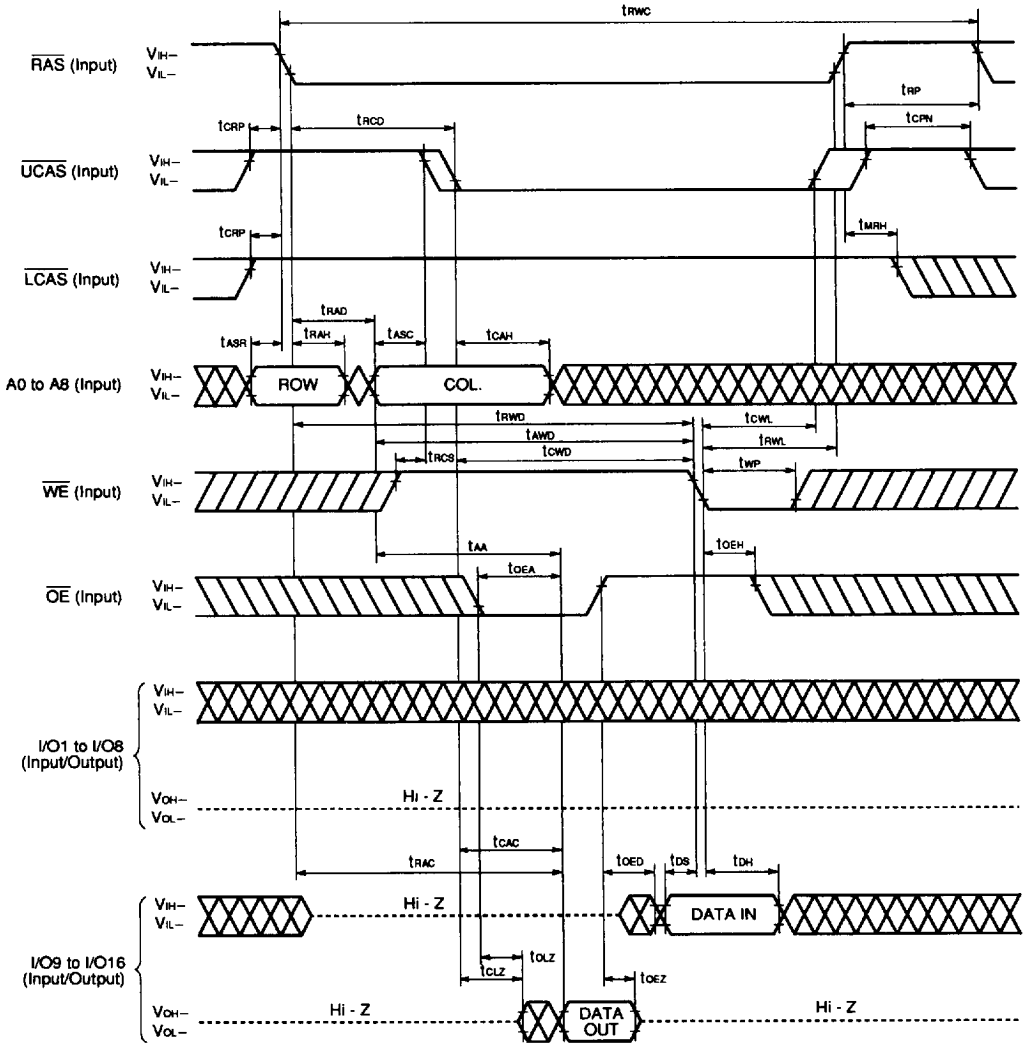


Remark I/O9 to I/O16 = Don't care

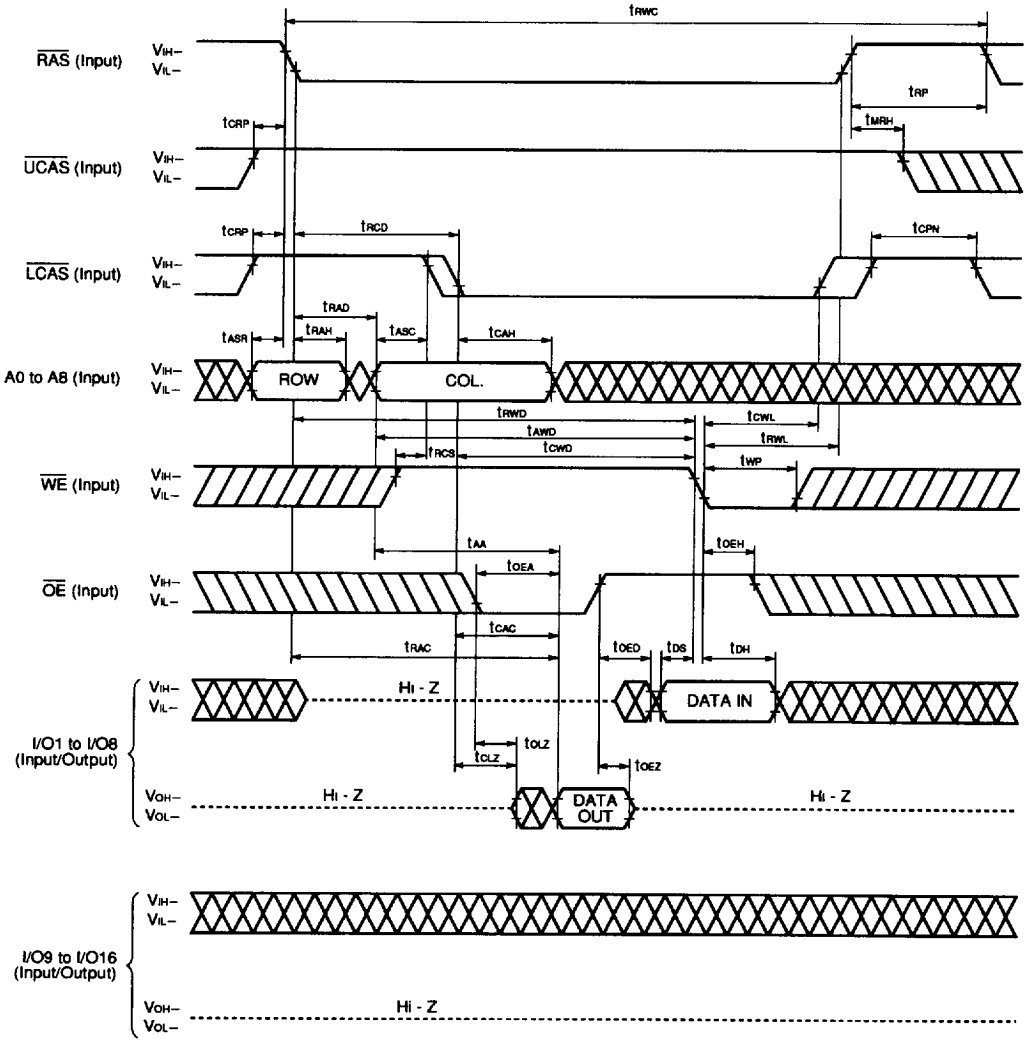
READ MODIFY WRITE CYCLE



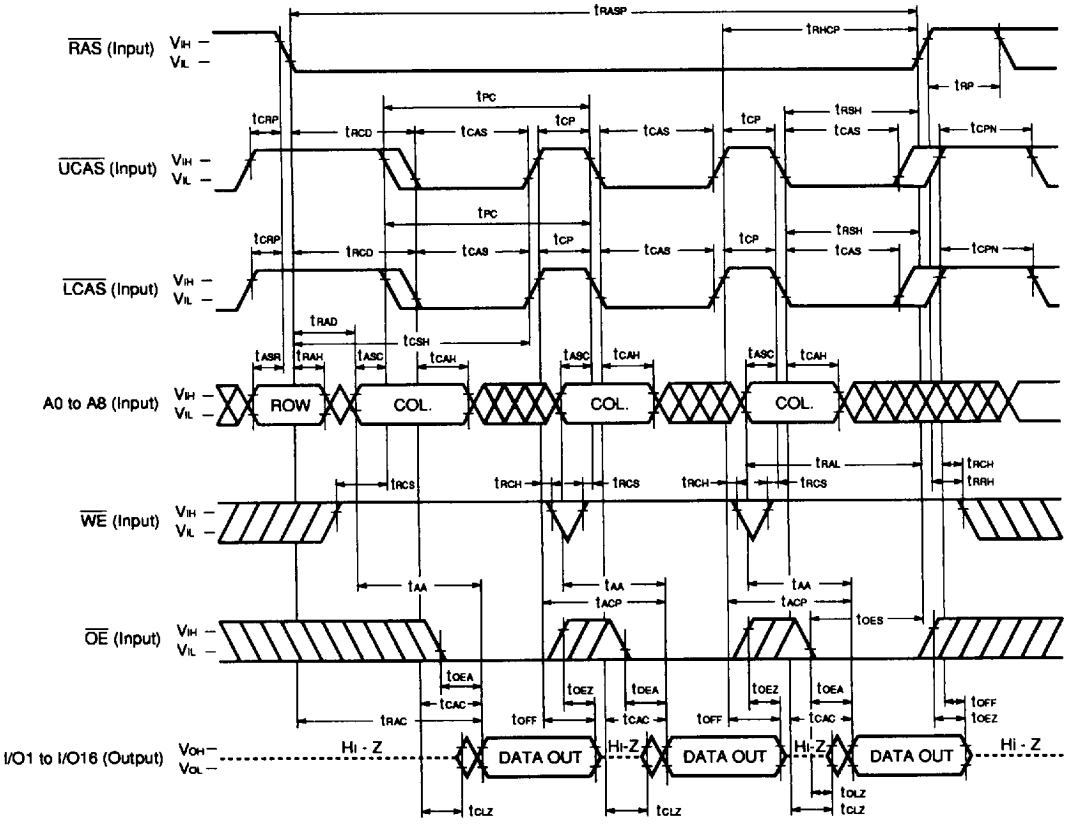
UPPER BYTE READ MODIFY WRITE CYCLE



LOWER BYTE READ MODIFY WRITE CYCLE

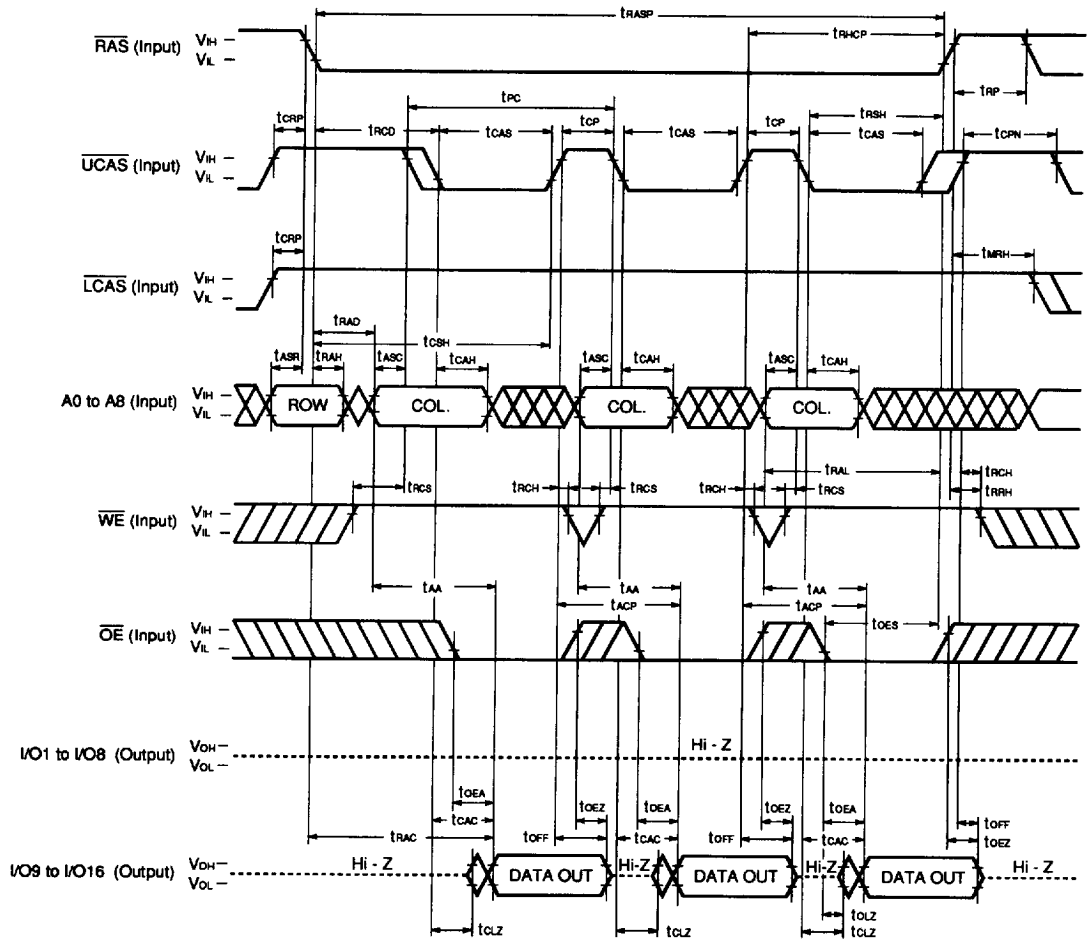


FAST PAGE MODE READ CYCLE



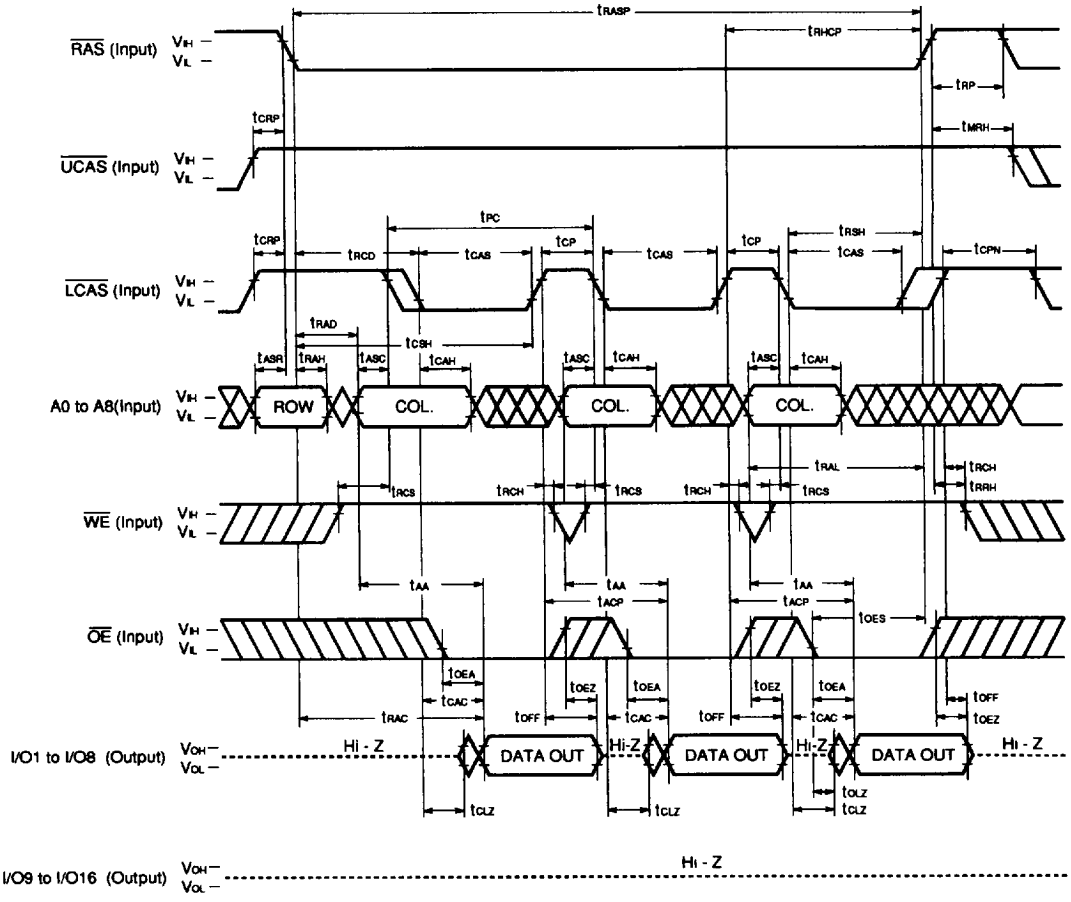
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE UPPER BYTE READ CYCLE



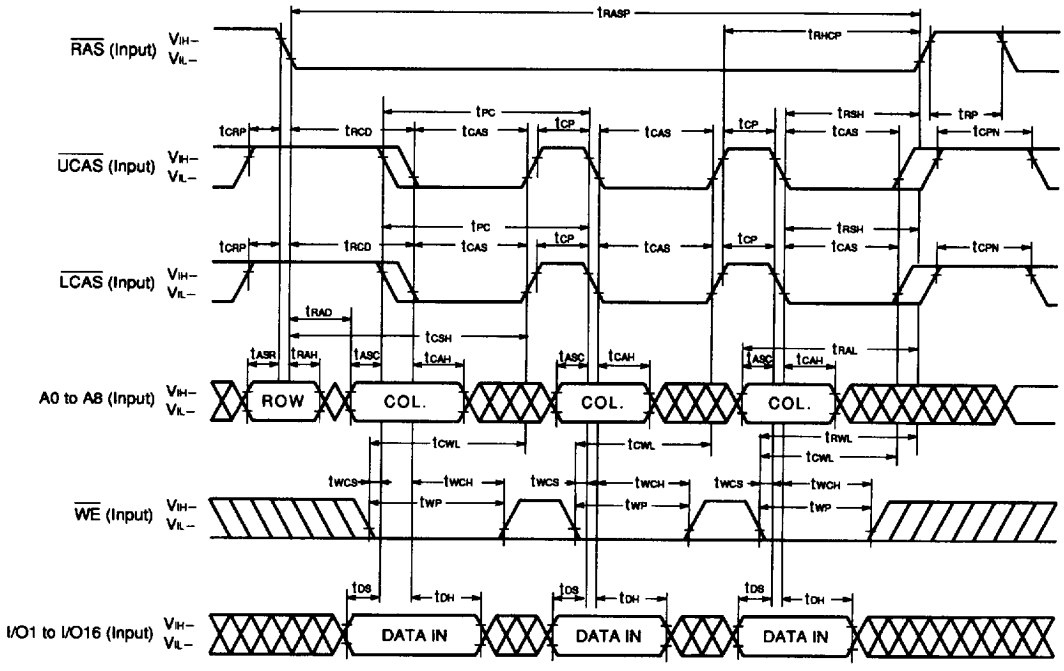
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE LOWER BYTE READ CYCLE



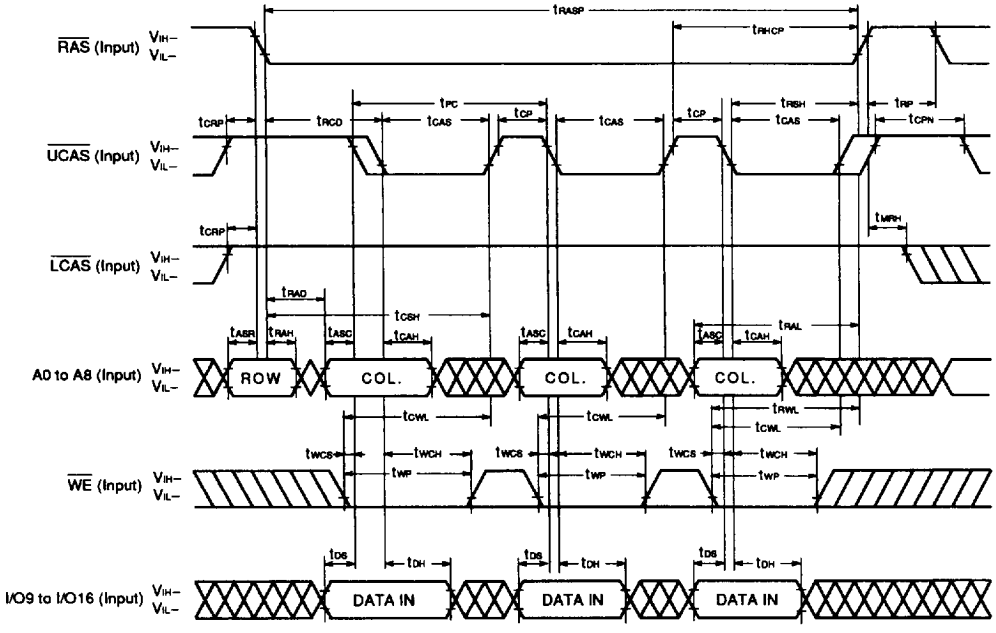
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE EARLY WRITE CYCLE



Remark $\overline{OE}$ = Don't care
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

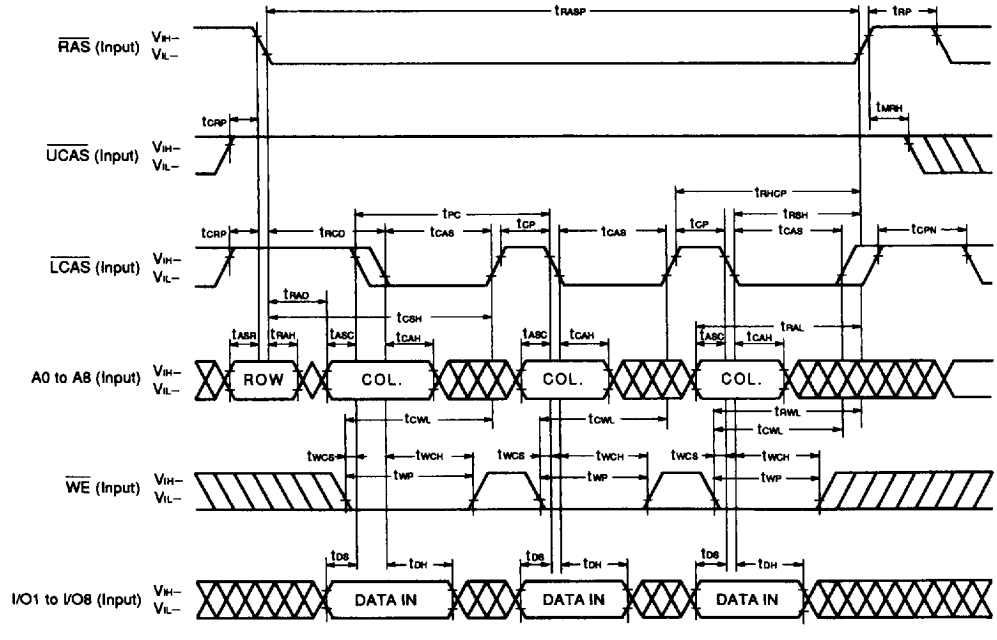
FAST PAGE MODE UPPER BYTE EARLY WRITE CYCLE



Remark I/O1 to I/O8, $\overline{OE}$ = Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

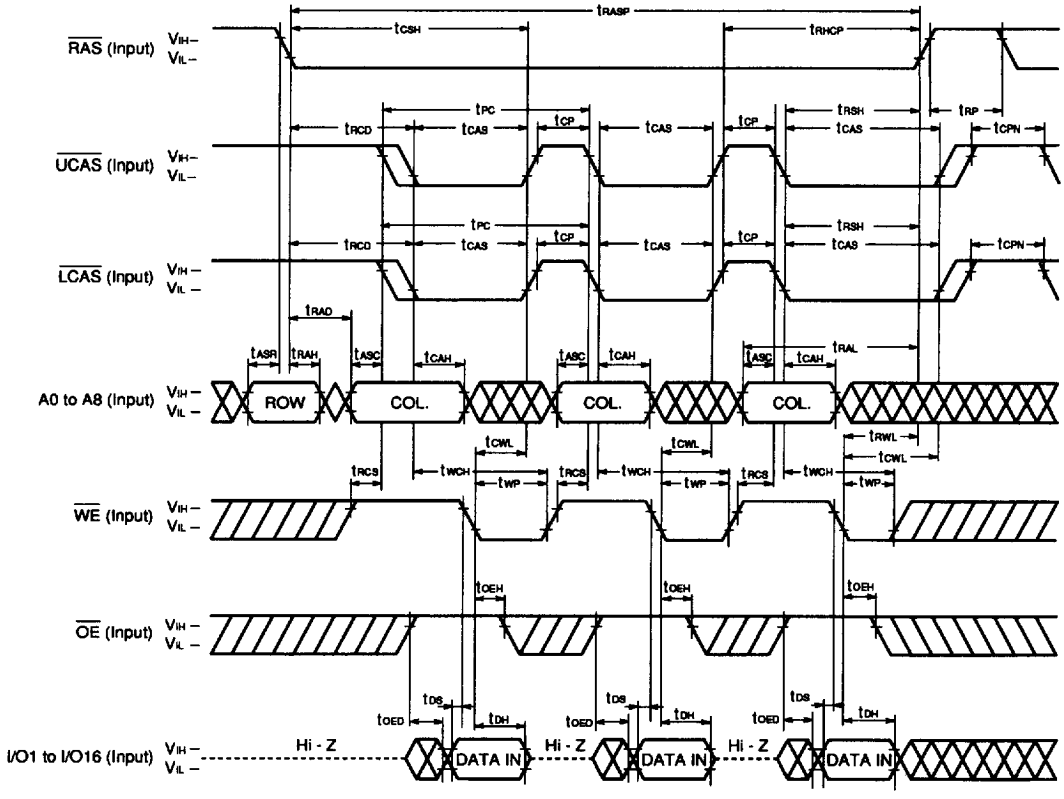
FAST PAGE MODE LOWER BYTE EARLY WRITE CYCLE



Remark I/O9 to I/O16, $\overline{OE}$ = Don't care

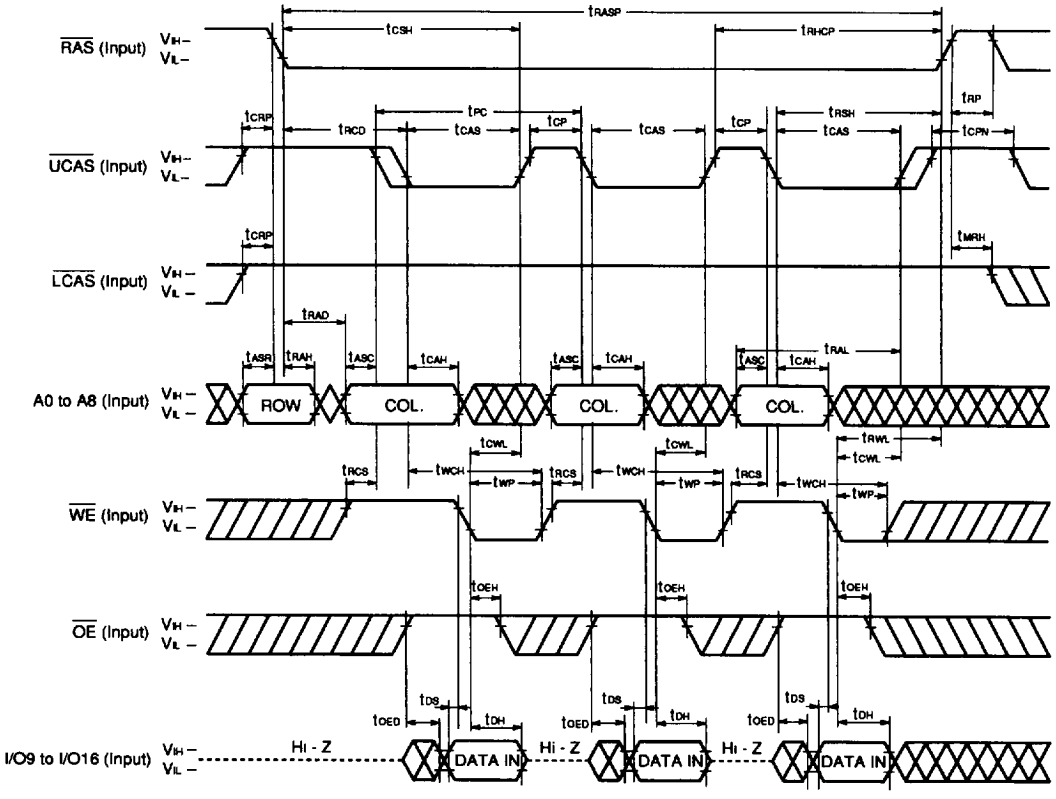
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE LATE WRITE CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

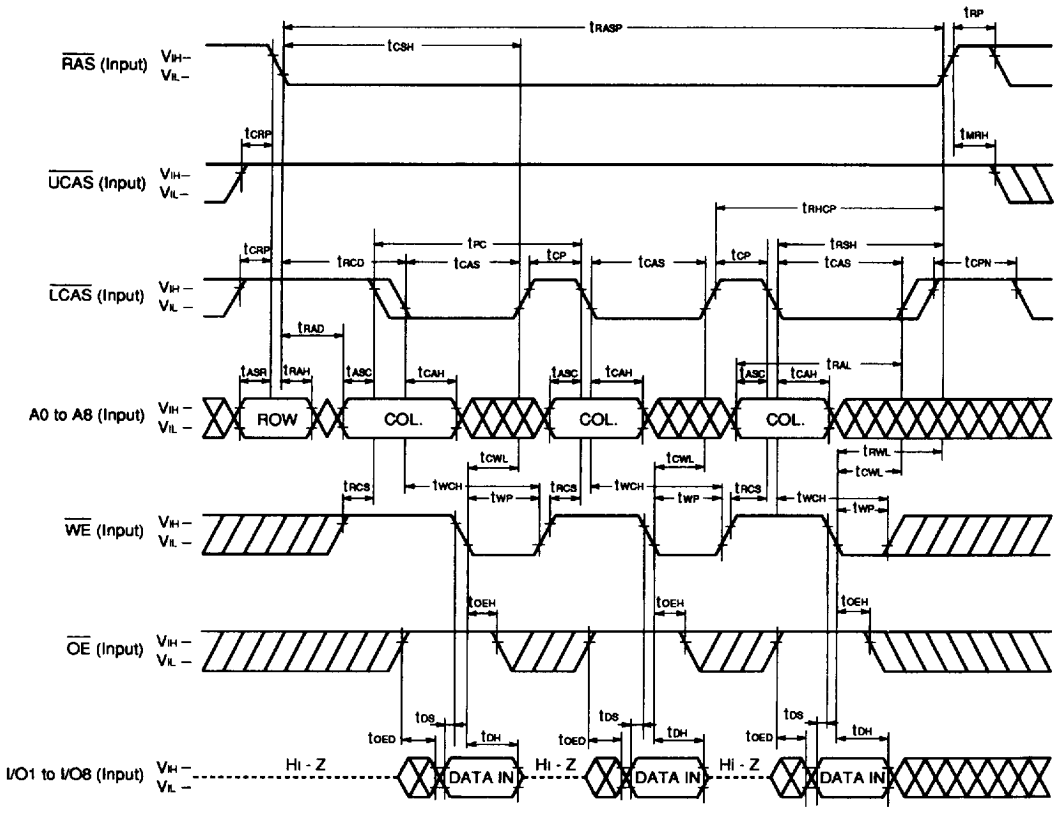
FAST PAGE MODE UPPER BYTE LATE WRITE CYCLE



Remark I/O1 to I/O8 = Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

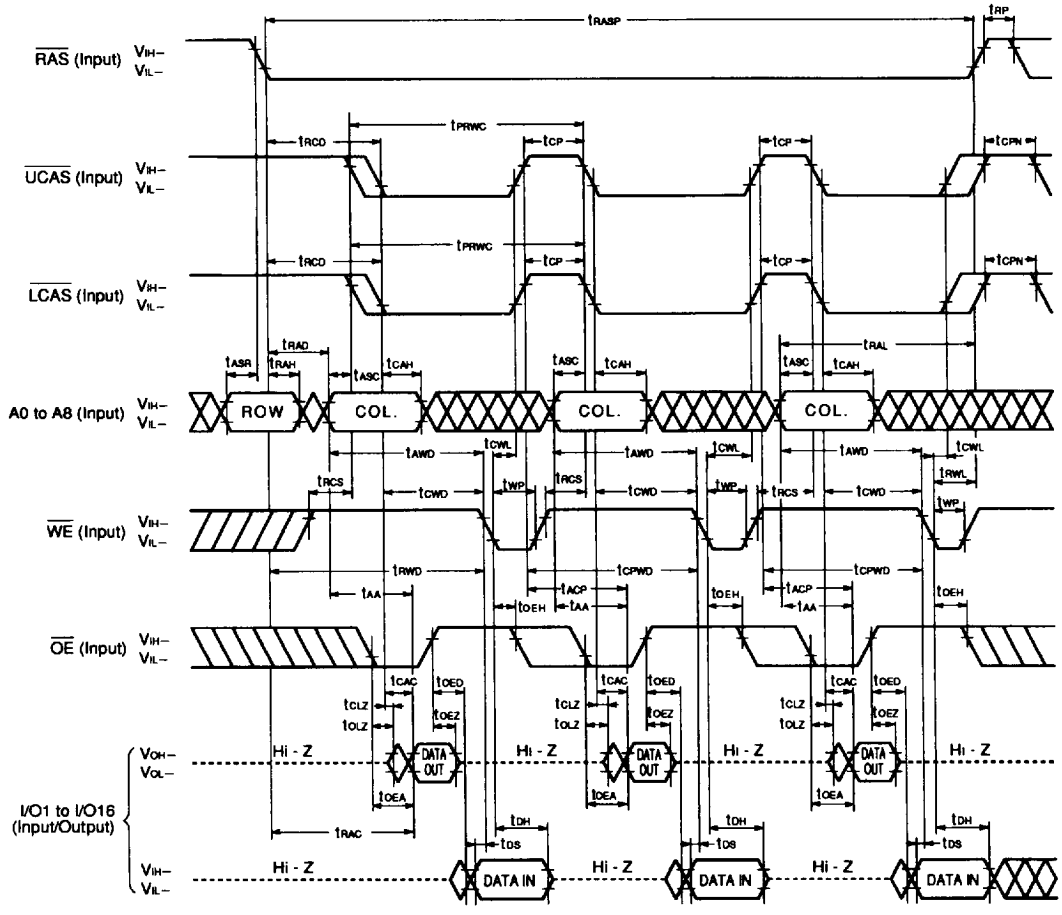
FAST PAGE MODE LOWER BYTE LATE WRITE CYCLE



Remark I/O9 to I/O16 = Don't care

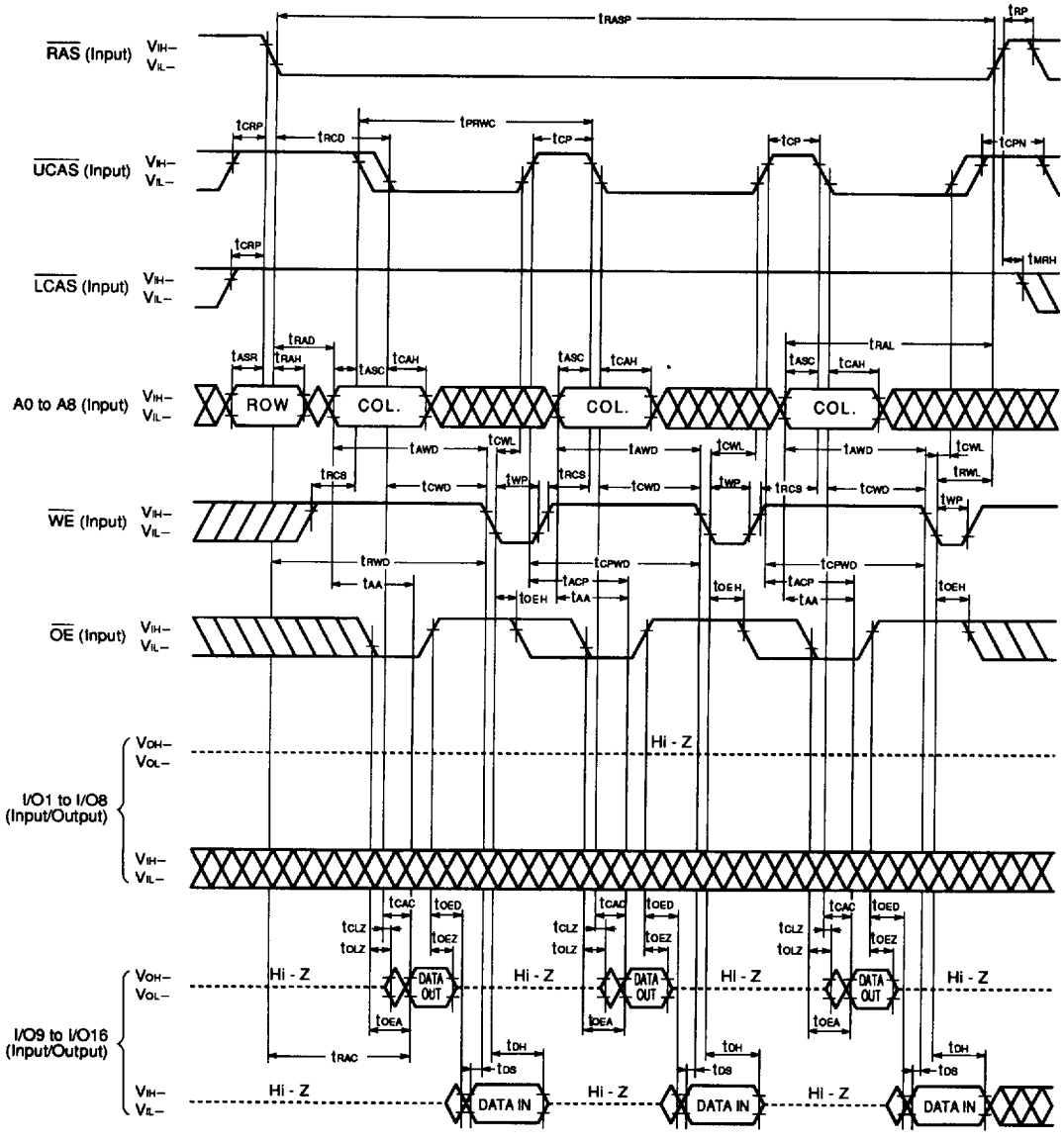
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

FAST PAGE MODE READ MODIFY WRITE CYCLE



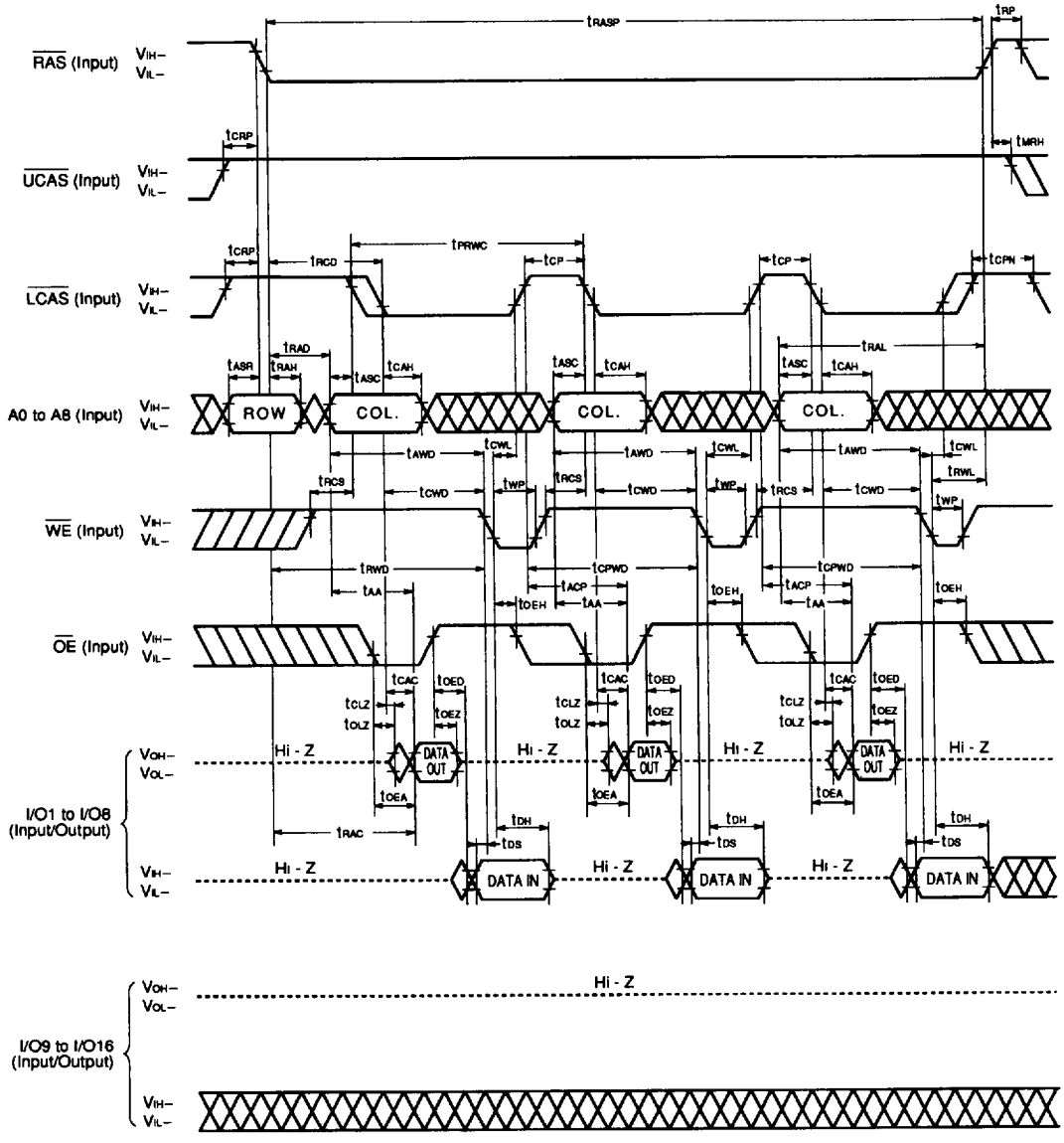
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE UPPER BYTE READ MODIFY WRITE CYCLE



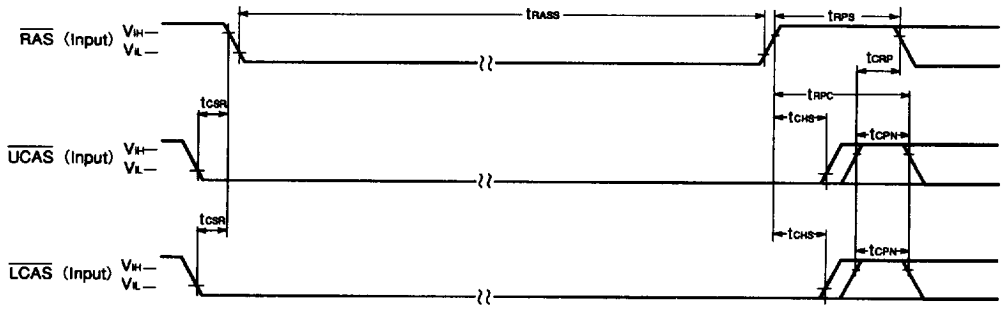
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE LOWER BYTE READ MODIFY WRITE CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

★ $\overline{CAS}$ BEFORE $\overline{RAS}$ SELF REFRESH CYCLE (Only for μPD42S4260L)



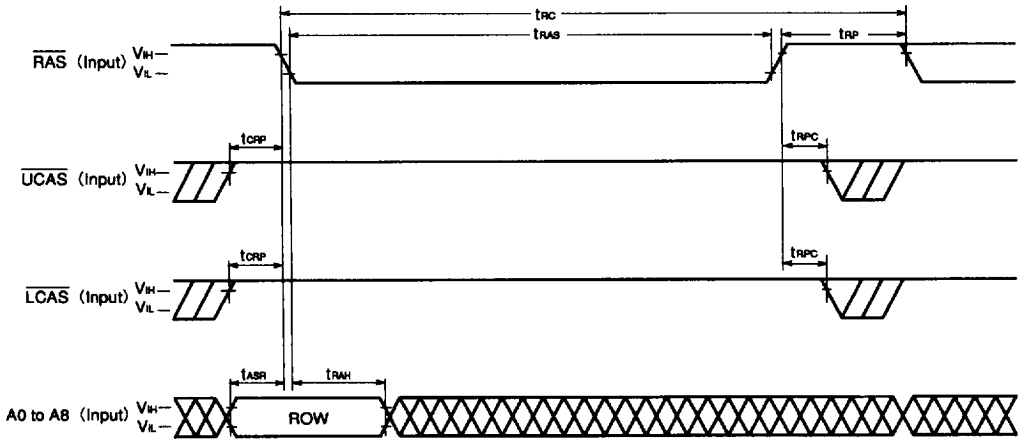
Remark Address, $\overline{WE}$, $\overline{OE}$ = Don't care I/O1 to I/O16 = Hi - Z

How to use $\overline{CAS}$ before $\overline{RAS}$ self refresh mode.

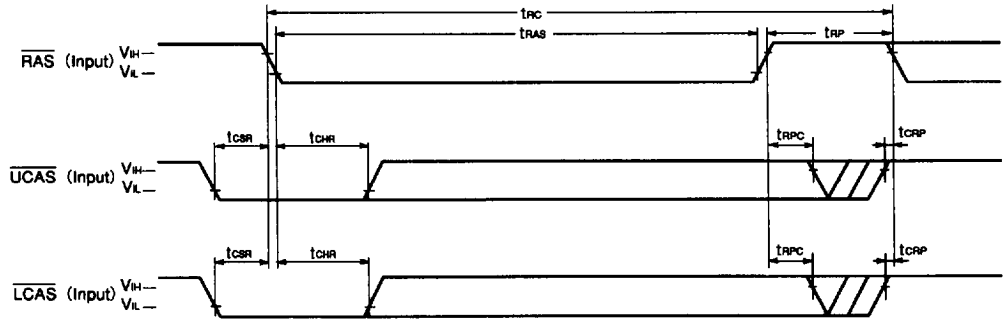
$\overline{CAS}$ before $\overline{RAS}$ self refresh mode can't be used by itself. It must be used with performing one of 3 refreshes below.

- **In case of using distributed $\overline{CAS}$ before $\overline{RAS}$ refresh**
  Refresh 512 times during 128 ms before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode and after reset.
- **In case of using burst $\overline{CAS}$ before $\overline{RAS}$ refresh**
  Refresh 512 times during 8 ms before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode and after reset.
- **In case of using $\overline{RAS}$ only refresh**
  Refresh all refresh addresses during 8 ms before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode and after reset.

$\overline{RAS}$ ONLY REFRESH CYCLE

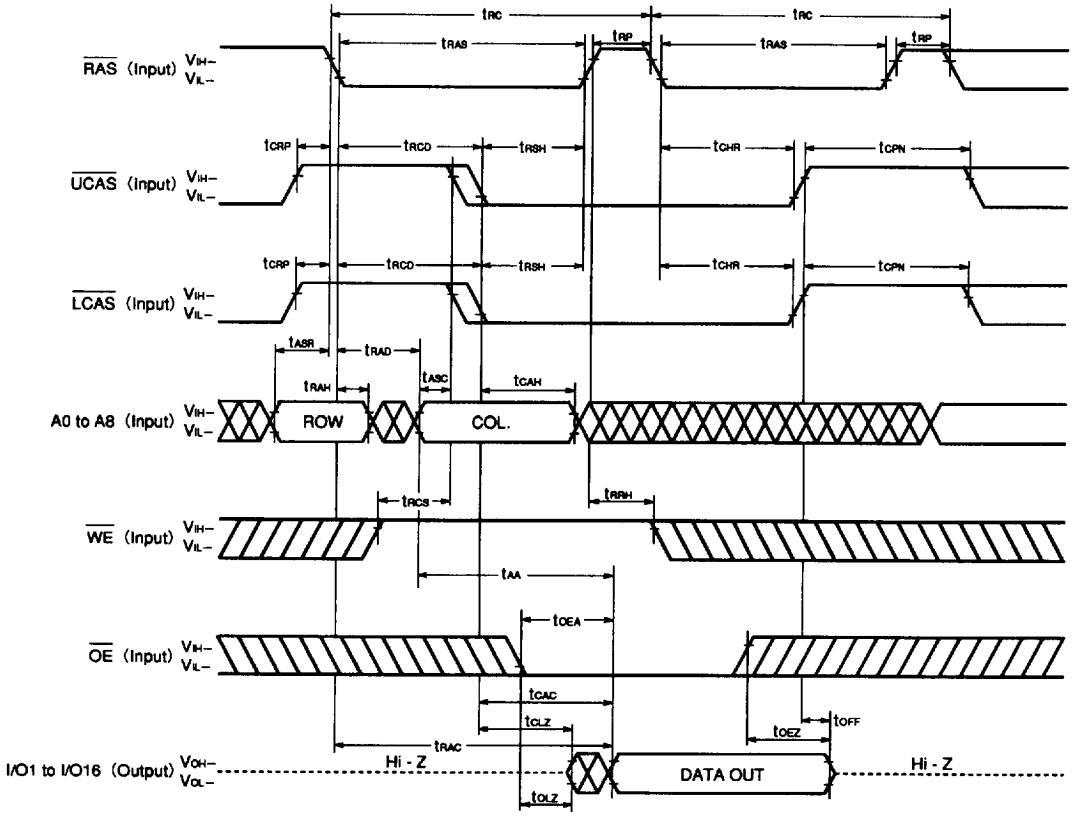


$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

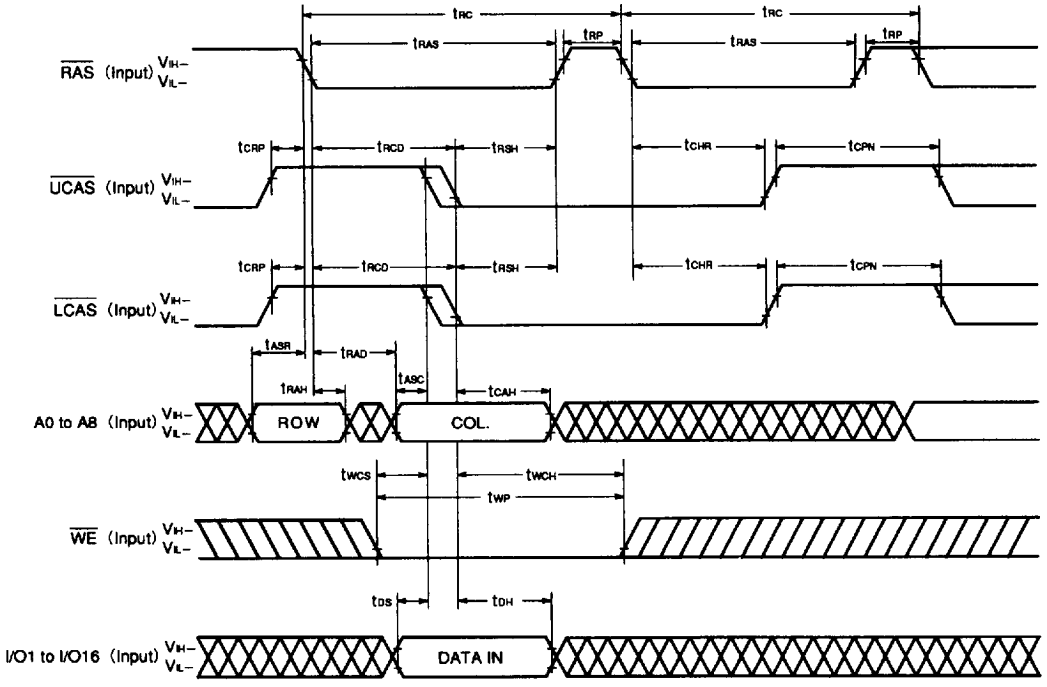


Remark A0 to A8, $\overline{WE}$, $\overline{OE}$ = Don't care I/O1 to I/O16 = Hi - Z

$\overline{CAS}$ BEFORE $\overline{RAS}$ HIDDEN REFRESH CYCLE (READ)

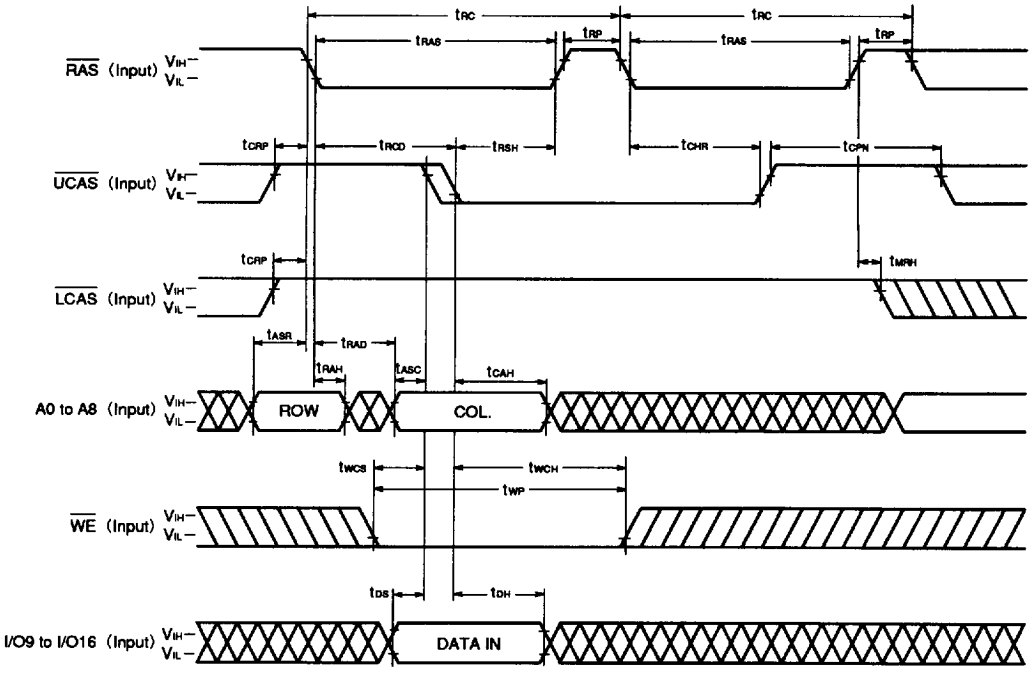


$\overline{CAS}$ BEFORE $\overline{RAS}$ HIDDEN REFRESH CYCLE (WRITE)



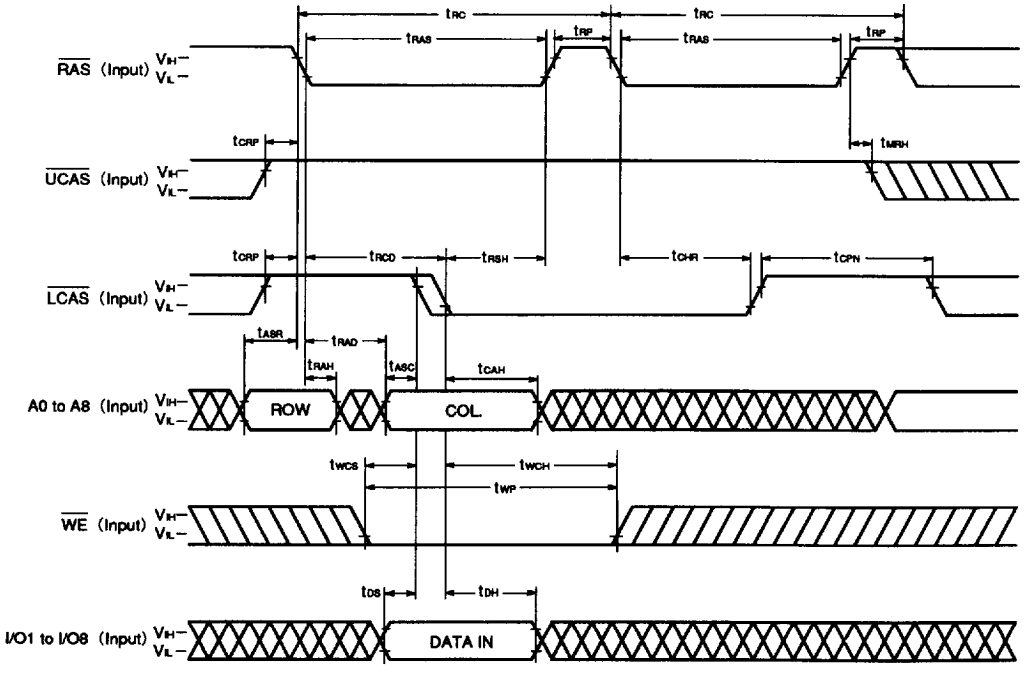
Remark $\overline{OE}$ = Don't care

$\overline{CAS}$ BEFORE $\overline{RAS}$ HIDDEN REFRESH CYCLE (UPPER BYTE WRITE)



Remark $\overline{OE}$, I/O1 to I/O8 = Don't care

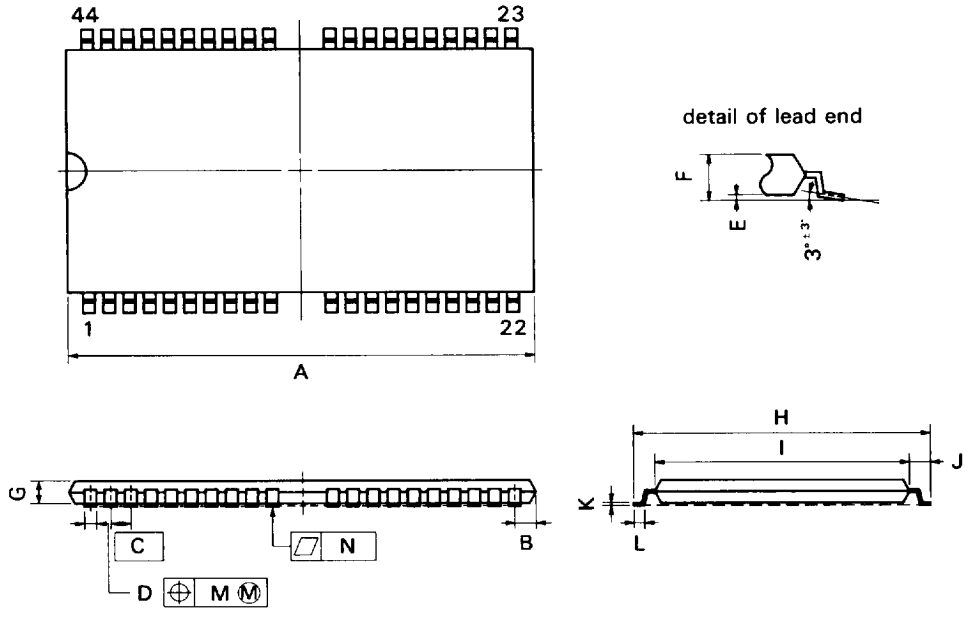
$\overline{CAS}$ BEFORE $\overline{RAS}$ HIDDEN REFRESH CYCLE (LOWER BYTE WRITE)



Remark $\overline{OE}$, I/O9 to I/O16 = Don't care

PACKAGE INFORMATION

44 PIN PLASTIC TSOP (400mil)



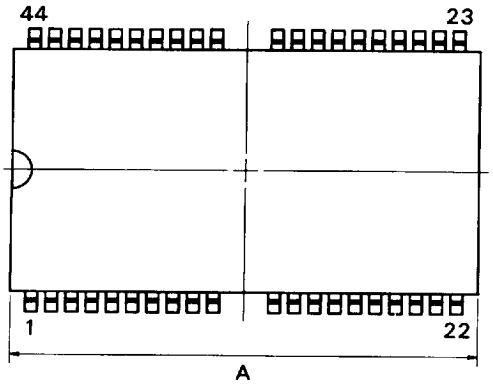
S44G5-80-7JF

NOTE

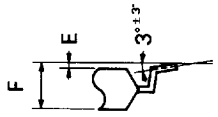
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

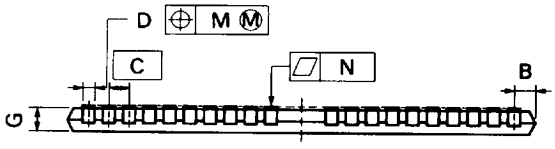
ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.0 MAX	0 040 MAX.
C	0.8 (T.P)	0 031 (T P.)
D	$0.30^{\pm 0\ 10}$	$0.012^{+0\ 004}_{-0\ 005}$
E	$0\ 05^{\pm 0\ 05}$	$0\ 002^{\pm 0\ 002}$
F	1 1 MAX.	0.044 MAX.
G	0.97	0.038
H	$11\ 76^{\pm 0\ 2}$	$0.463^{\pm 0\ 008}$
I	$10.16^{\pm 0\ 1}$	$0.400^{\pm 0\ 004}$
J	$0\ 8^{\pm 0\ 2}$	$0\ 031^{+0\ 009}_{-0\ 008}$
K	$0\ 125^{+0\ 10}_{-0\ 05}$	$0\ 005^{+0\ 004}_{-0\ 002}$
L	$0\ 5^{\pm 0\ 1}$	$0.020^{+0\ 004}_{-0\ 005}$
M	0 13	0.005
N	0.10	0.004

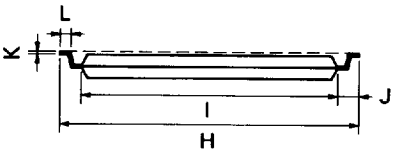
44 PIN PLASTIC TSOP (400mil)



detail of lead end







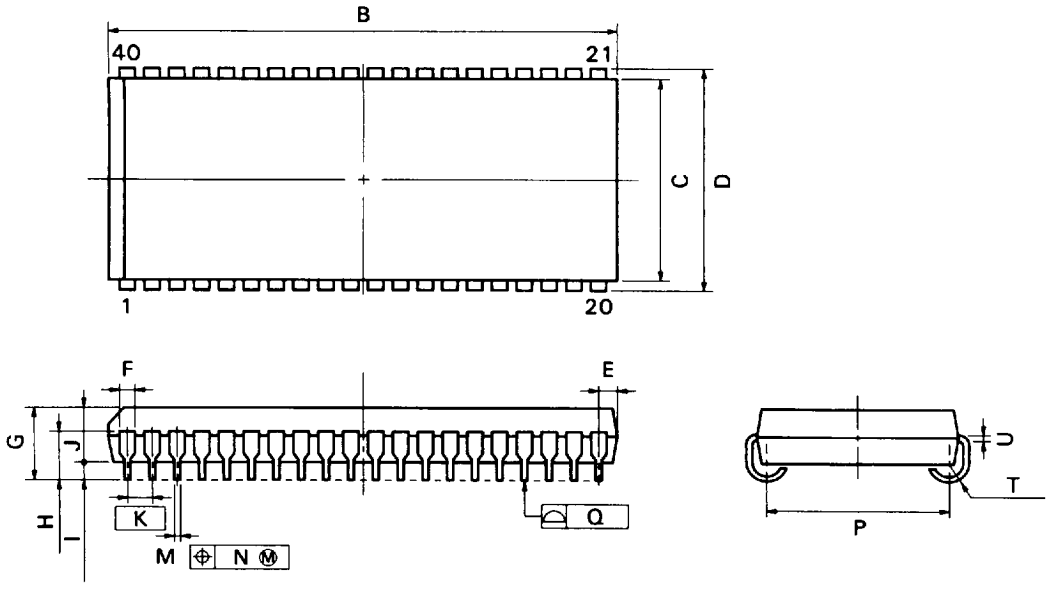
S44G5-80-7KF

NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.0 MAX.	0.040 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.30^{\pm 0.10}$	$0.012^{+0.004}_{-0.005}$
E	$0.05^{\pm 0.05}$	$0.002^{\pm 0.002}$
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	$11.76^{\pm 0.2}$	$0.463^{\pm 0.008}$
I	$10.16^{\pm 0.1}$	$0.400^{\pm 0.004}$
J	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	$0.5^{\pm 0.1}$	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004

40PIN PLASTIC SOJ (400 mil)



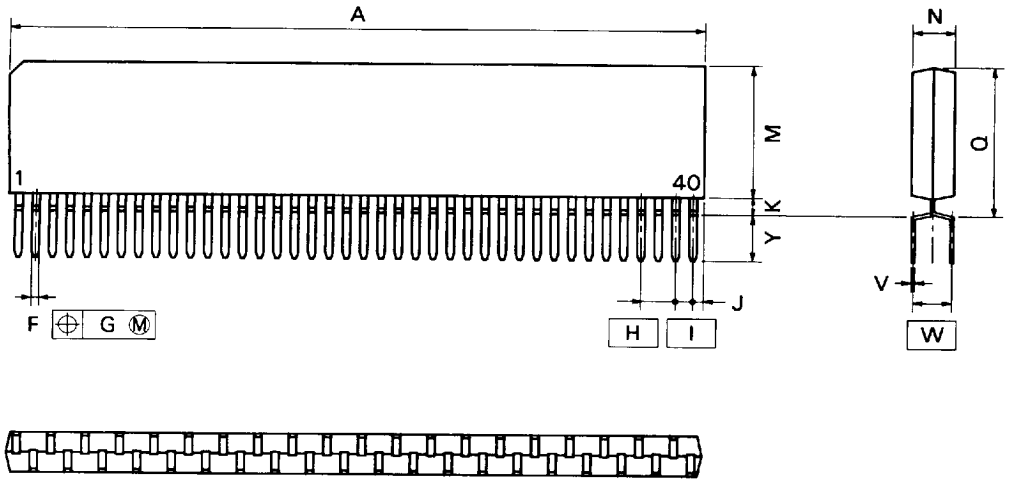
P40LE-400A-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$26.29^{+0.2}_{-0.35}$	$1.035^{+0.008}_{-0.014}$
C	10.16	0.400
D	$11.18^{\pm 0.2}$	$0.440^{\pm 0.008}$
E	$1.08^{\pm 0.15}$	$0.043^{+0.006}_{-0.007}$
F	0.7	0.028
G	$3.5^{\pm 0.2}$	$0.138^{\pm 0.008}$
H	$2.4^{\pm 0.2}$	$0.094^{+0.009}_{-0.008}$
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	$9.4^{\pm 0.20}$	$0.370^{\pm 0.008}$
Q	0.15	0.006
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

40 PIN PLASTIC ZIP(475mil)



P40V-100-475A

NOTE
Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	51.23 MAX.	2.017 MAX.
F	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
G	0.25	0.010
H	2.54 (T.P.)	0.100 (T.P.)
I	1.27 (T.P.)	0.050 (T.P.)
J	0.85 MAX	0.034 MAX.
K	0.9 MIN.	0.035 MIN.
M	10.5 MAX.	0.414 MAX.
N	$2.8^{\pm 0.2}$	$0.110^{+0.009}_{-0.008}$
Q	12.07 MAX.	0.476 MAX.
V	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
W	2.54 (T.P.)	0.100 (T.P.)
Y	$3.25^{\pm 0.2}$	$0.128^{\pm 0.008}$

RECOMMENDED SOLDERING CONDITIONS

Please consult with our sales offices when soldering μPD42S4260L, 424260L.

TYPES OF SURFACE MOUNT DEVICE

μPD42S4260LG5, 424260LG5 (44-pin Plastic TSOP)
μPD42S4260LLE, 424260LLE (40-pin Plastic SOJ)

TYPE OF THROUGH HOLE MOUNT DEVICE

μPD42S4260LV, 424260LV (40-pin Plastic ZIP)