FLASH MODULE

AVAILABLE AS MILITARY SPECIFICATIONS

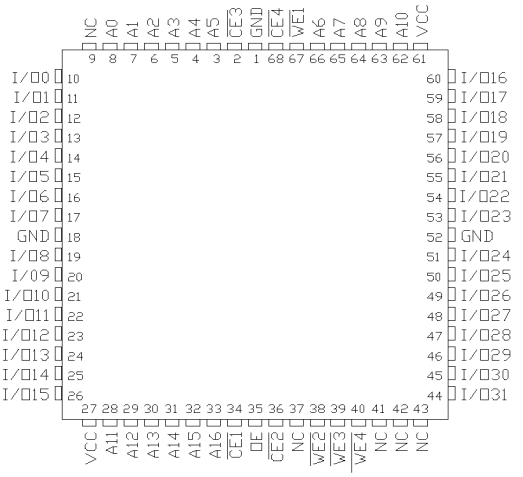
•SMD 5962-94716
•MIL-STD-883

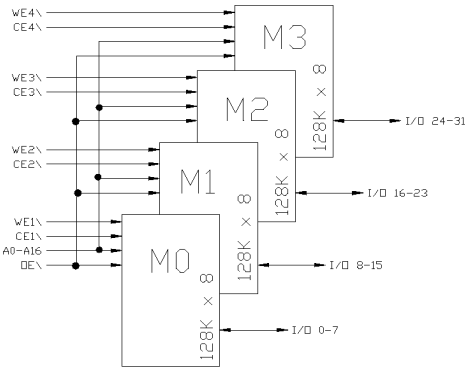
FEATURES

- SMD 5962-94716 Pending
- Fast Access Time 60, 70, 90, 120, and 150ns
- Eight Equal Sectors of 16k Bytes for each 128kx8
- Compatible with JEDEC EEPROM command set
- Any Combination of Sectors can be Erased
- Supports Full Chip Erase
- Embedded Erase and Program Algorithms
- Data Polling and Toggle Bit feature for detection of program or erase cycles completion
- Operation with single 5 volt supply
- TTL Compatible Inputs and CMOS Outputs
- Low Power CMOS (typical)
- Built in decoupling caps for low noise operation
- Sector Protection
  Hardware method disables any combination of sectors from program or erase operations
- Minimum 10,000 Write/Erase Cycles
- Packaging
  68 lead CQFP

PIN ASSIGNMENT (Top View)

68 Lead CQFP





GENERAL DESCRIPTION

The AS8F128K32 is a nonvolatile, electrically sector-erasable (Flash), programmable read-only memory. The AS8F128K32 is a 4 Mbit, 5.0 V Flash memory organized as 128K bytes of bits each. This device is offered in a 68-pin CQFP package. The AS8F128K32 is designed to be programmed or erased in system with the standard system 5.0 V V_{CC} supply. A 12.0 V V_{PP} is not required for program or erase operations. The device can also be reprogrammed in standard EEPROM programmers.

The AS8F128K32 offers access times between 60ns to 150ns allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enables ($\overline{CE}$), write enables ($\overline{WE}$), and output enable ($\overline{OE}$) controls.

The AS8F128K32 is entirely pin and command set compatible with JEDEC standard EEPROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an Internal State Machine

PIN DESCRIPTION	
I/O 0-31	Data Inputs/Outputs
A 0-16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{cc}	Power Supply
GND	Ground
NC	Not Connected

(ISM) which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from EEPROM devices.

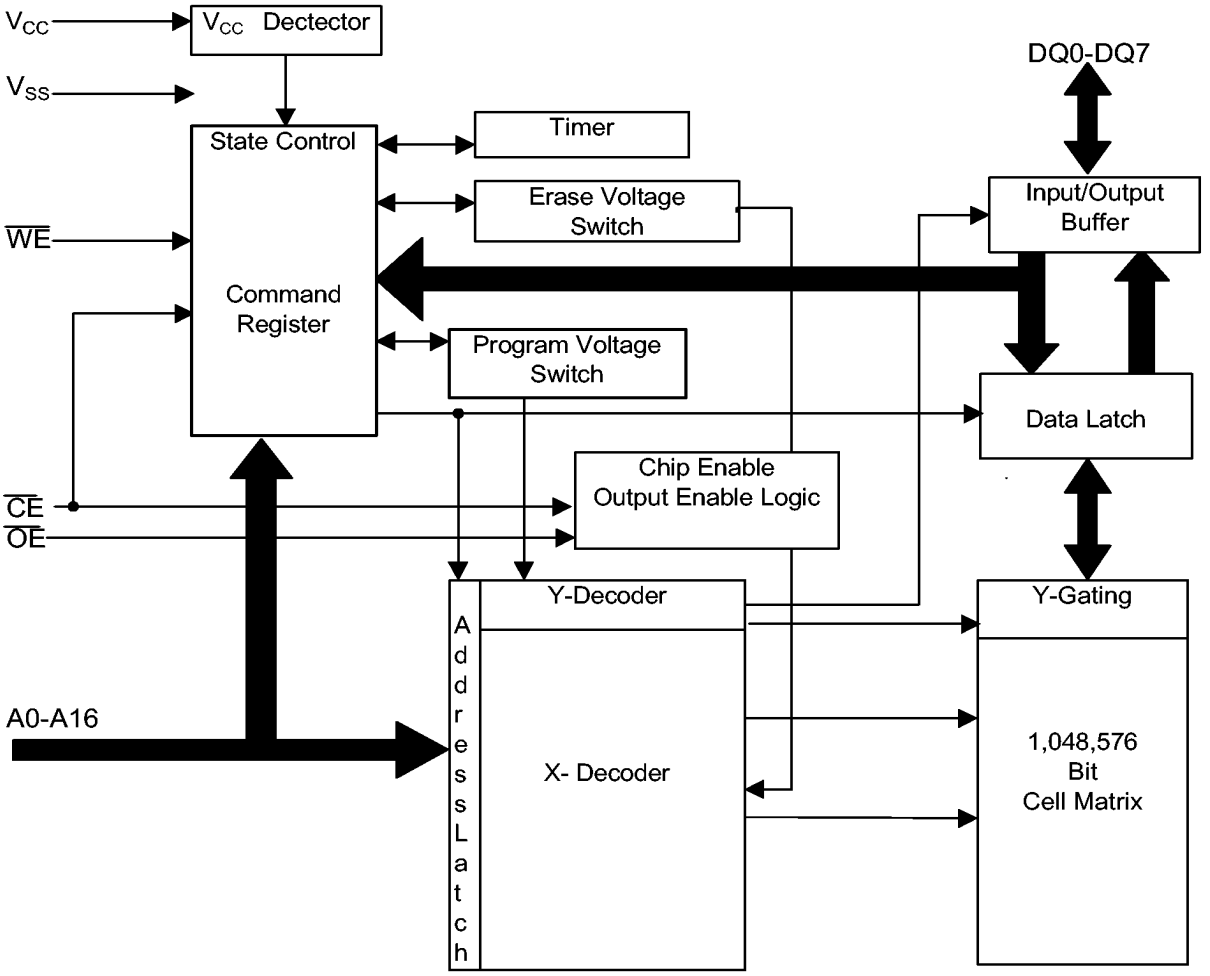
Executing the program command sequence programs the AS8F128K32. This will invoke the Embedded Program algorithm, which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in less than 0.3 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase algorithm, which is an internal algorithm that automatically preprogram the array if it is not already programmed before executing the erase operations. During erase, the device automatically times the erase pulse widths and verifies the proper cell margin. The entire memory is typically erased and verifies in three second (including preprogramming).

Any individual sector is typically erased and verified in 1.3 seconds (including preprogramming).

This device also features sector erase architecture. The sector mode allows for 16k byte blocks of memory to be erased and reprogrammed without affecting other blocks. The AS8F128K32 is erased when shipped from factory.

These device features single 5.0V power supply operations for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A very low V_{CC} detector automatically inhibits write operations during power transitions. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ7 or by the Toggle Bit feature on DQ6. Once the program or erase cycle has been completed, the device internally resets to the read mode.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss
Vcc (Note 1) .....-2.0V to +7.0V
A9 (Note 2)..... -2.0V to +12.5V
All Other Pins (Note 1).....-2.0V to +7.0V
Operating Temperature, T_A (Ambient).....55°C to +125°C
Storage Temperature .....-65°C to +125°C
Power Dissipation.....1.5W
Short Circuit Output Current (Note 3).....200mA
Lead Temperature (soldering 10 seconds).....+300°C
Junction Temperature.....+165°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied, Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Notes:

1. Minmum DC voltage on input or I/O pins is -0.5V. During Vaoltage transitions, inputs may overshoot Vss to -2.0V for periods of up to 20 ns. See Figure 1. Maximum DC voltage on input or I/O pins isVcc +0.5V. During Voltage transitions, inputs may overshoot Vcc to +2.0V for periods of up to 20 ns. See Figure 2.

2. Minmum DC input voltage on A9 pin is -0.5V. During voltage transitions, A9 pins may overshoot Vss to-2.0V for periods of up to 20 ns. See Figure 1. Maximum DC inpuy voltage on A9 is +12.5V inputs which may overshoot to

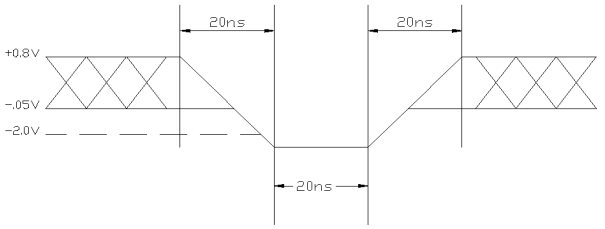


Figure 1.
Maximum Negative Overshoot Waveform

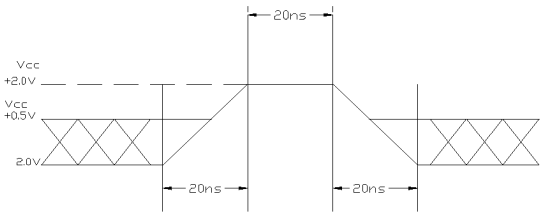


Figure 2.
Maximum Positive Overshoot Waveform

Capacitance Table[Note 1, 2]

V_{IN} = 0V, f = 1MHz, TA = 25°C

Symbol	Parameter	Maximum	Units
C_{ADD}	A0 - A16 Capacitance	50	pF
C_{OE}	OE\ Capacitance	50	pF
C_{WE} ,C_{CE}	WE\ 1-4 Capacitance CE\ 1-4 Capacitance	20	pF
C_{IO}	I/O0 - I/O 31 Capacitance	20	pF

Notes:
1. This parameter is sampled.
2. 32 bit configuration.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C < TA < 125°C; V_{CC} = 5V +/- 10%)

Erase and Program Operations

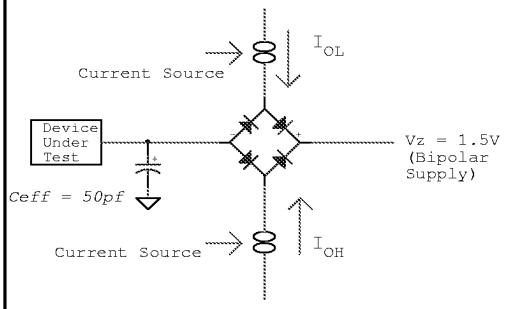
Alternate CE# Controlled Writes

Parameter Symbol		Parameter Description		Speed Options					Units
JEDEC	Std.			-60	-70	-90	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	60	70	90	120	150	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0					ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	55	55	55	60	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	30	30	40	55	60	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0					ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write	Min	0					ns
t_{WLEL}	t_{WS}	Write Enable Setup Time	Min	0					ns
t_{EHWH}	t_{WH}	Write Enable Hold Time	Min	0					ns
t_{ELEH}	t_{CP}	Chip Enable Pule Width	Min	35	40	45	55	60	ns
t_{EHELH}	t_{CPH}	Chip Enable Pule Width High	Min	20					ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation (Note 1,2)	Typ	14					mA
t_{WHWH2}	t_{WHWH2}	Chip/Sector Erase Operation (Note 1,2)	Typ	28					sec
		Chip Programming Time	Max	12.5					sec

Notes:

1. The Icc current listed is typically less than 2mA/MHz, with $\overline{OE}$ at V_{IH}.
2. Icc active while Embedded Program or Embedded Erase Algorithm is in progress.
3. Guaranteed but not tested.

AC TEST CONDITONS



AC Test Setup

PARAMETER	TYP	UNITS
Input Pulse Level	V_{IL}=0, V_{IH}=3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V
I_{OL} and I_{OH} programmable from 0 to 16mA.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.

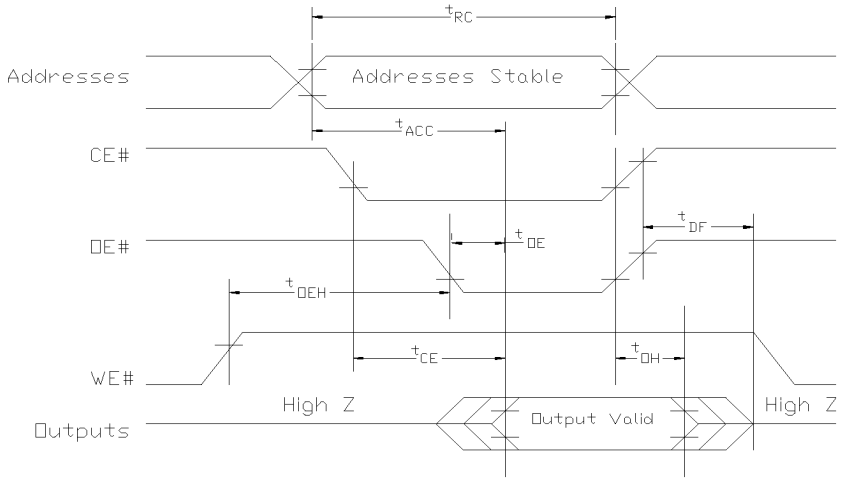
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(-55°C < TA < 125°C; V_{CC} = 5V +/- 10%)

Parameter Symbol	Parameter Description	Test Description	Min	Max	Unit
I_{LI}	Input Load Current	V_{IN} = V_{SS} to V_{CC}, V_{CC}=V_{CC} Max		10	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}, V_{CC}=V_{CC} Max		10	µA
I_{CC1}	V_{cc} Active Current (Note 1)	CE\ = V_{IL}, OE\ = V_{IH}, V_{CC} = V_{CC} Max		140	mA
I_{CC2}	V_{cc} Active Current (Note 2,3)	CE\ = V_{IL}, OE\ = V_{IH}, V_{CC} = V_{CC} Max		200	mA
I_{CC3}	V_{cc} Standby Current	V_{CC} = V_{CC} Max, CE\ = V_{IH}, f=5MHz		6.5	mA
V_{IL}	Input Low Voltage		-.05	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} +0.3	V
V_{ID}	A9 Voltage for Sector Protect	V_{CC} = 5.0 V	11.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12mA, V_{CC} = V_{CC} Min		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -2.5mA, V_{CC} = V_{CC} Min	0.85xV_{CC}		V
V_{OH2}		I_{OH} = -100µA, V_{CC} = V_{CC} Min	V_{CC}-0.4		V
V_{LKO}	Low V_{cc} Lock-out Voltage		3.2	4.2	V

Notes:
1 Guaranteed but not tested.
2. Output Driver Disable Time.
3. See AC Test Conditions for test Specification.

Read Operations Timings



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(-55°C < TA < 125°C; V_{CC} = 5V +/- 10%)

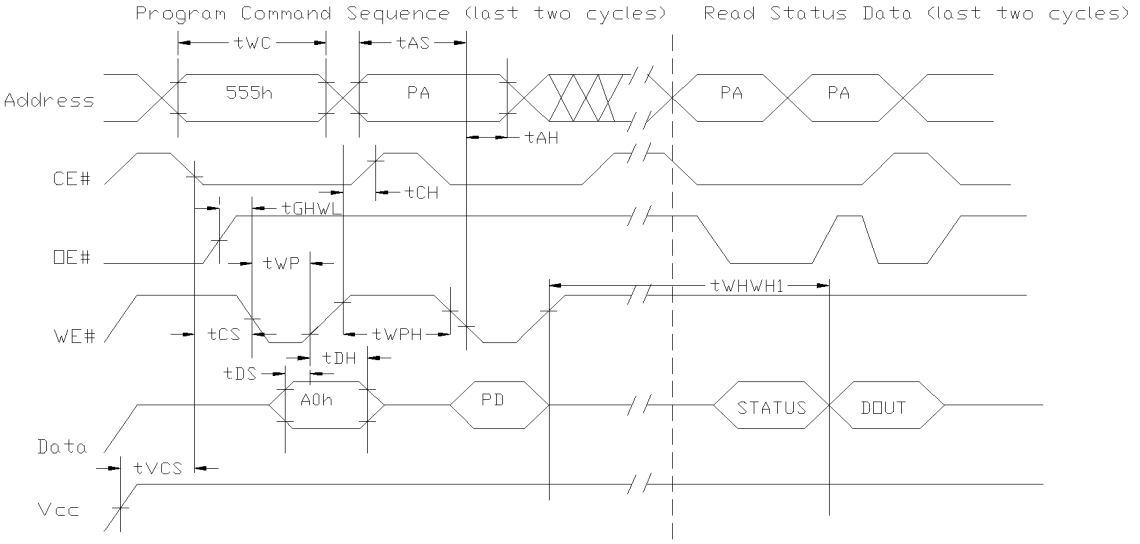
Erase and Program Operations Characteristics

Parameter Symbol		Parameter Description		Speed Options					Units
JEDEC	Std.			-60	-70	-90	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	60	70	90	120	150	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0					ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	55	55	55	60	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	30	30	40	55	60	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0					ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write (OE\ High to WE\ Low)	Min	0					ns
t_{ELWL}	t_{CS}	Chip Enable Setup Time	Min	0					ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min	0					ns
t_{WLWH}	t_{WP}	Write Pule Width	Min	35	40	45	55	60	ns
t_{WHWL}	t_{WHP}	Write Pule Width High	Min	20					ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation (Note 1,2)	Typ	24					mA
t_{WHWH2}	t_{WHWH2}	Sector Erase Operations (Note 1,2)	Typ	28					sec
	t_{VCS}	VCC Setup Time	Min	60					mA
		Chip Programming Time	Max	12.5					sec
	t_{OES}	Output Enable Setup Time	Min	0					ns
	t_{OEH}	Output Enable Hold Time (1)	Min	10					ns

Notes:

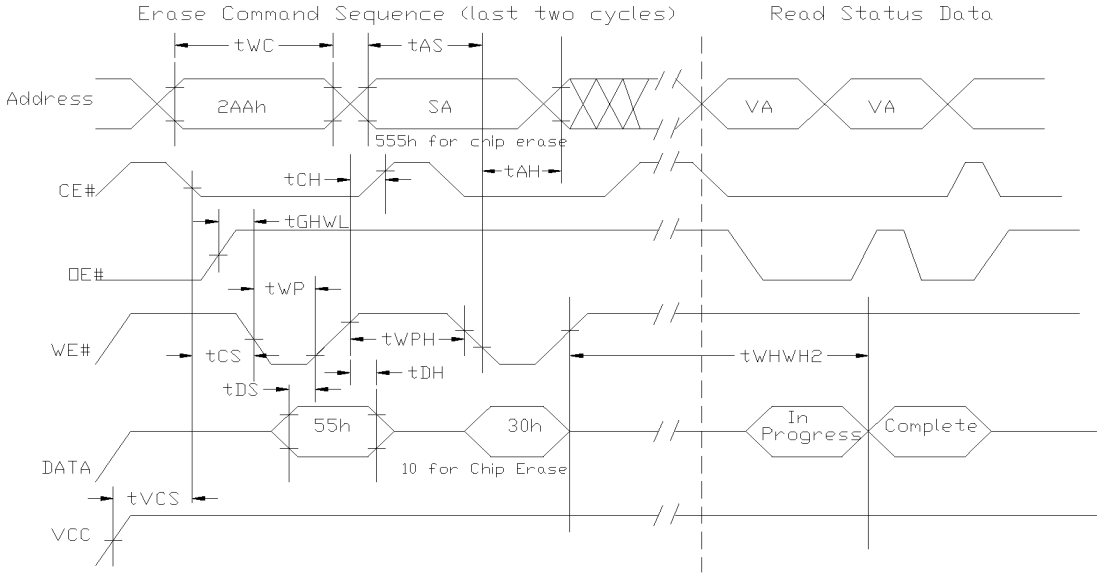
1. Guaranteed but not tested.
2. See the "Erase and Programming Performance" section for more details.

Program Operations Timings



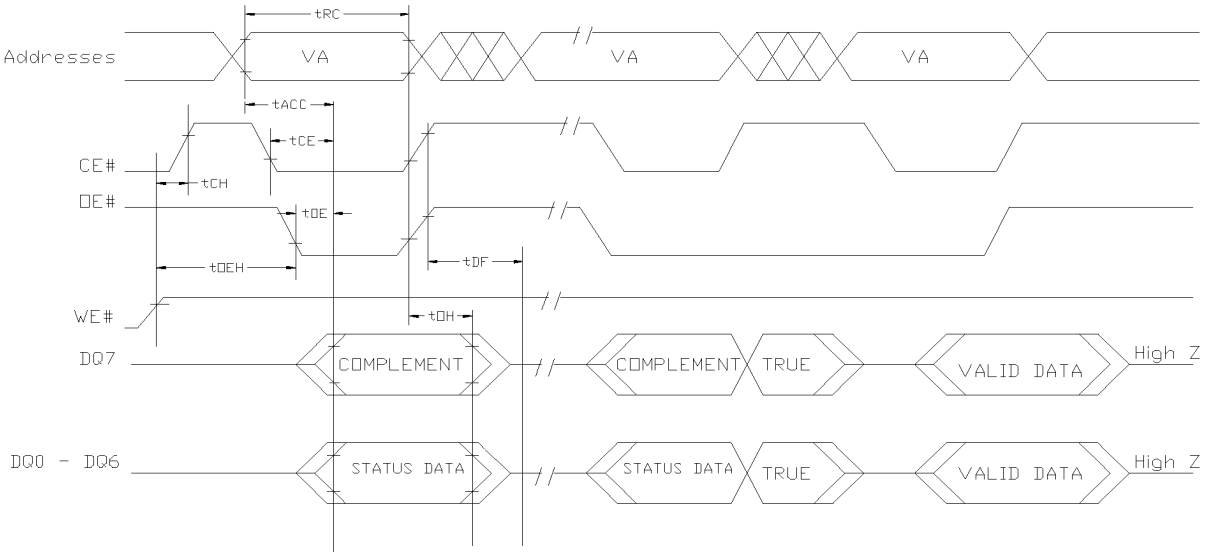
Note: PA= program address, PD= program data, D_{OUT} is the true data at the program address.

Chip/Sector Erase Operations Timings



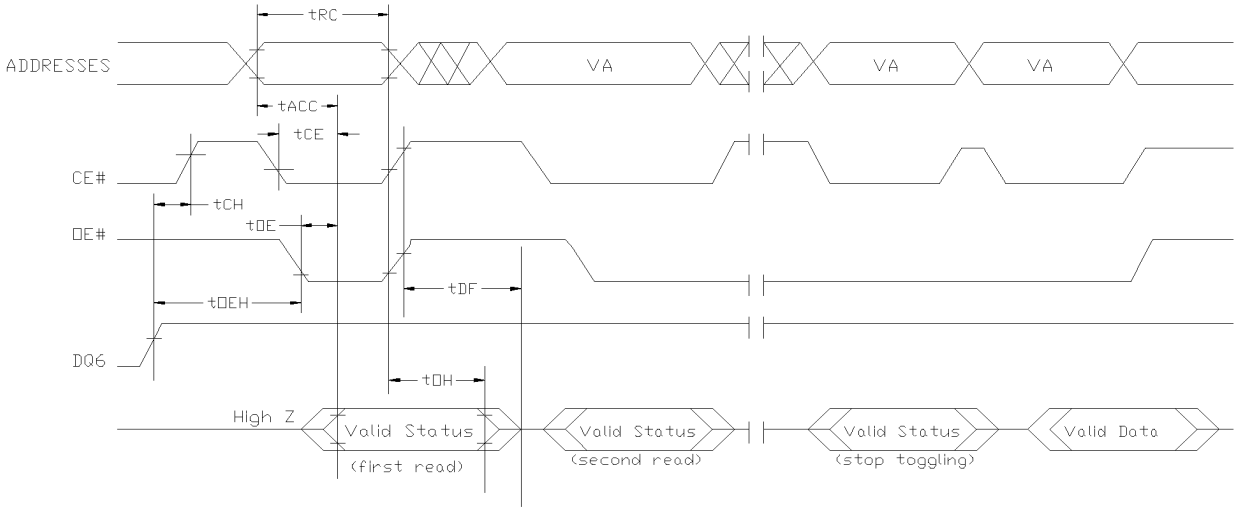
Note: SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status").

Data Polling Timings (During Embedded Algorithms)



Note: VA = Valid address. Illustration show first status cycle after command sequence, last status read cycle, and array data read cycle.

Toggle Bit Timings (During Embedded Algorithms)



Note: VA = Valid address; not required for DQ6. Illustration show first two status cycle after command sequence, last status read cycle, and array data read cycle.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(-55°C < TA < 125°C; V_{CC} = 5V +/- 10%)

Erase and Program Operations

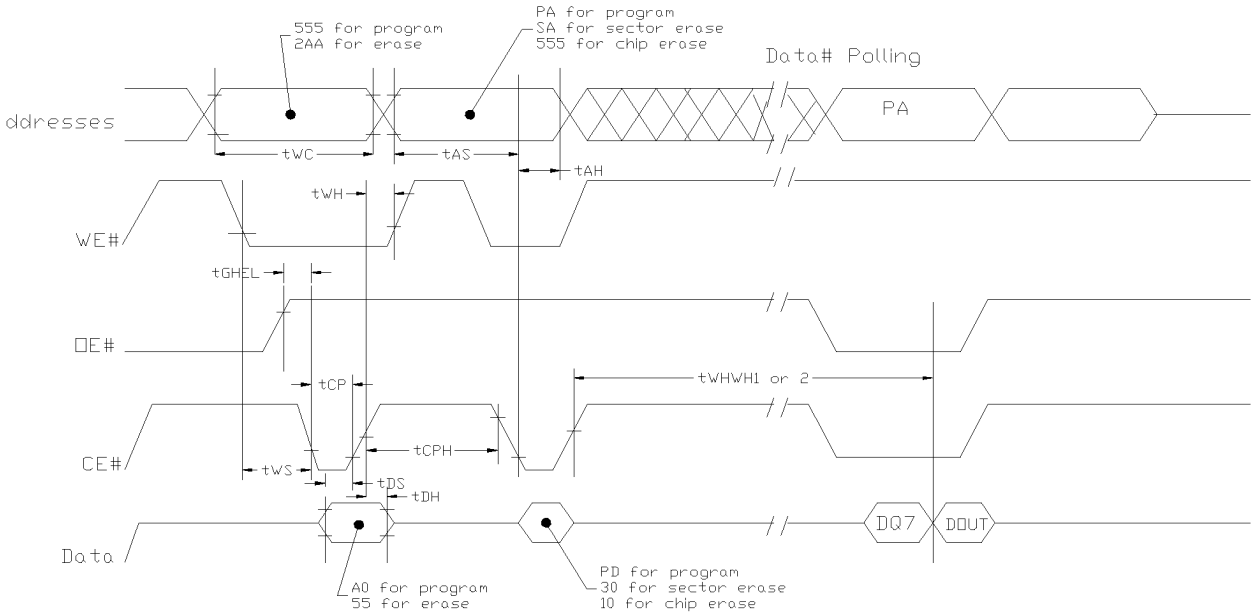
Alternate CE# Controlled Writes

Parameter Symbol		Parameter Description		Speed Options					Units
JEDEC	Std.			-60	-70	-90	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	60	70	90	120	150	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0					ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	55	55	55	60	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	30	30	40	55	60	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0					ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write	Min	0					ns
t_{WLEL}	t_{WS}	Write Enable Setup Time	Min	0					ns
t_{EHWH}	t_{WH}	Write Enable Hold Time	Min	0					ns
t_{ELEH}	t_{CP}	Chip Enable Pule Width	Min	35	40	45	55	60	ns
t_{EHELH}	t_{CPH}	Chip Enable Pule Width High	Min	20					ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation (Note 1,2)	Typ	14					mA
t_{WHWH2}	t_{WHWH2}	Chip/Sector Erase Operation (Note 1,2)	Typ	28					sec
		Chip Programming Time	Max	12.5					sec

Notes:

1. Guaranteed but not tested.
2. See the "Erase and Programming Performance" section for more details.

Alternate CE# Controlled Write Operation Timings



Notes:

1. PA = Program Address, PD = Program Data, SA = Sector Address, DQ7 = Complement of Data Input, D_{OUT} = Array Data.
2. Figure indicates the last two bus cycles of the command sequence.

MECHANICAL DEFINITION

for the AS8F128K32Q Ceramic Quad Flat Pack